CPE 631 Advanced Computer Systems Architecture: Homework #1

Question #1 (10 points).
Your team has been considering two different architectural improvements A1 and A2 (both have roughly the same complexity) to a base system (Base). Your collaborator responsible for evaluation handed you the following table showing speedups relative to the base system for each improvement for a set of 5 benchmarks (B1-B5). Your task is to make decision which one A1 or A2 should be pursued further. Can you make a decision, and if yes, what is your choice? Show your analytical work.
Hint: use the total execution time of all benchmarks as a metric for determining performance of the base system and systems with the improvements A1 and A2. Find the ratios (ET.Base/ET.A1 and ET.Base/ET.A2).

Speedup	B1	B2	B3	B4	B5
A1	2	4	3	5	7
A2	3	3	4	4	8

Question #2 (10 points). In this exercise, assume that we are considering enhancing a machine by adding vector hardware to it. When a computation is run in vector mode on the vector hardware, it is 10 times faster than the normal mode of execution. We call the percentage of time that could be spent using vector mode the percentage of vectorization.
2.A. Draw a graph that plots the speedup as a percentage of the computation performed in vector mode. Label the y-axis "Net speedup" and label the x-axis "Percent vectorization."
2.B. What percentage of vectorization is needed to achieve a speedup of 2?
2.C. What percentage of the computation run time is spent in vector mode if a speedup of 2 is achieved?
2.D. What percentage of vectorization is needed to achieve one-half the maximum speedup attainable from using vector mode?
2.E. Suppose you have measured the percentage of vectorization of the program to be 70%. The hardware design group estimates it can speed up the vector hardware even more with significant additional investment. You wonder whether the compiler crew could increase the percentage of vectorization, instead. What percentage of vectorization would the compiler team need to achieve in order to equal an addition 2× speedup in the vector unit (beyond the initial 10×)?

Question #3 (10 points).
Four enhancements E1, E2, E3 and E4 with the following speedups are proposed for a new architecture:
Speedup1 = 10; Speedup2 = 20; Speedup3 = 5; Speedup4 = 50, respectively.
The enhancements are non-overlapping and orthogonal to each other. We are considering two approaches in maximizing performance (A1 and A2) where A2 requires slightly more complex hardware support.
A1: Enhancements E1 and E2 are in use; the distribution of enhancement usage is 30% (E1) and 40% (E2).
A2: Enhancements E3 and E4 are in use; the distribution of enhancement usage is 20% (E3) and 50% (E4).
Which of these 2 approaches (A1 or A2) is better?

Question #4 (10 points)
Consider two different implementations, M1 and M2, of the same instruction set. M1 has a clock rate of 400MHz, and M2 has a clock rate of 200MHz. The average number of clock cycles for each instruction class on M1 and M2 is given in the following table:

Instruction class	CPI (M1)	CPI (M2)	C1 usage	C2 usage	C3 usage
A	4	2	30%	30%	50%
B	6	4	50%	20%	30%
C	8	3	20%	50%	20%

The table also contains a summary of three different compilers using the instruction set.
C1 is a compiler produced by the makers of M1, C2 is a compiler produced by the makers of M2, and the other compiler C3 is a third-party product. Assume that each compiler uses the same number of instructions for a given program but that the instruction mix is as described in the table.
Answer the following questions:

4.A (2 points) Using C1 on both M1 and M2, how much faster can the makers of M1 claim that M1 is compared to M2?
4.B (2 points) Using C2 on both M2 and M1, how much faster can the makers of M2 claim that M2 is compared to M1?
4.C (2 points) If you purchase M1, which compiler would you use?
4.D (2 points) If you purchase M2, which compiler would you use?
4.E (2 points) Which machine would you purchase given the choice of compiler, if we assume that all other criteria are identical, including costs?

Question #5 (10 points) Read the paper "Amdahl's Law in the Multicore Era." Assume that the number of BCE (base core equivalent) is n=64. Consider two fractions of parallelism f1=0.99 and f2=0.90. Using the models described in the paper determine the Speedup for the following multicore configurations.

(a) Symmetric multicore chip with 64 one BCE cores (assume perf(1)=1).
(b) Symmetric multicore chip with 16 four-BCE cores (assume performance of r-core equivalents is $perf(r)=(r)^{2/3}$).
(c) Asymmetric multicore chip with one sixteen-BCE core and 48 single BCE cores.
(d) Dynamic multicore chip with one sixteen-BCE core and 48 single BCE cores.

Which configuration does it give the highest speed for f=0.99 and which one for f=0.90?