

COMPUTER ORGANIZATION 2

Intel 8255 PPI chip

Submitted by:

Abdulrahman Hatem Metwally

Abdullah Ahmed Fathy

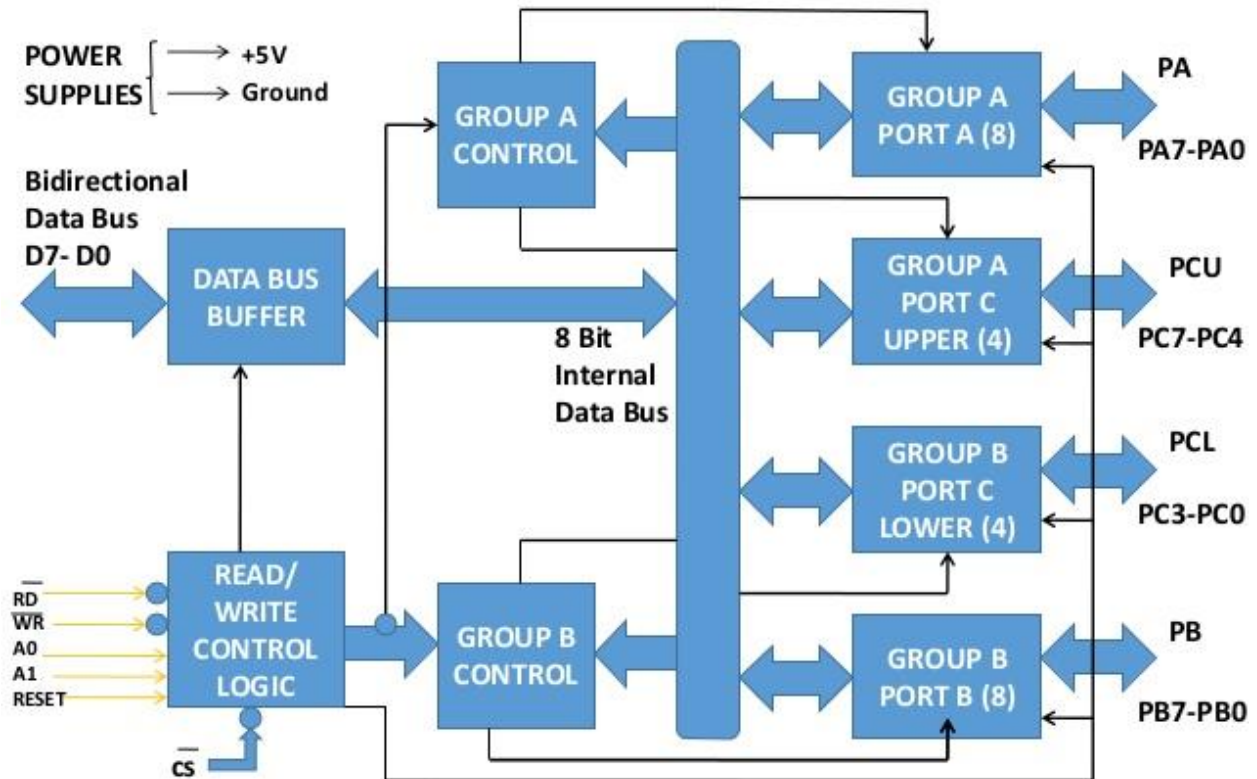
Section: 2

Peripheral interference:

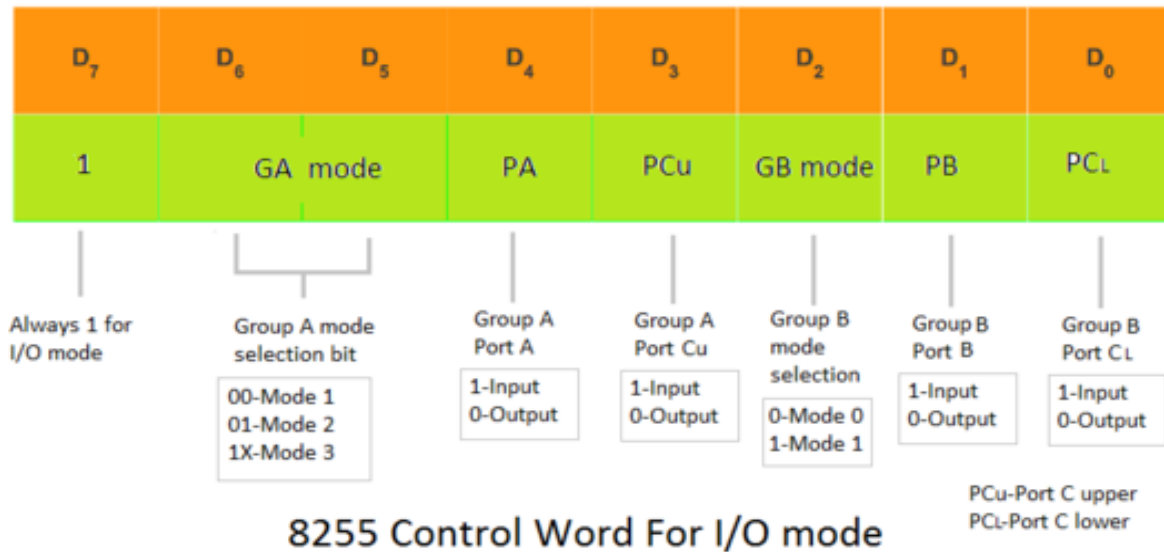
PA3	1	8255	40	PA4
PA2	2		39	PA5
PA1	3		38	PA6
PA0	4		37	PA7
RD	5		36	WR
CS	6		35	RESET
GND	7		34	DO
A1	8		33	D1
A0	9		32	D2
PC7	10		31	D3
PC6	11		30	D4
PC5	12		29	D5
PC4	13		28	D6
PC0	14		27	D7
PC1	15		26	VCC
PC2	16		25	PB7
PC3	17		24	PB6
PB0	18		23	PB5
PB1	19		22	PB4
PB2	20		21	PB3

Block diagram:

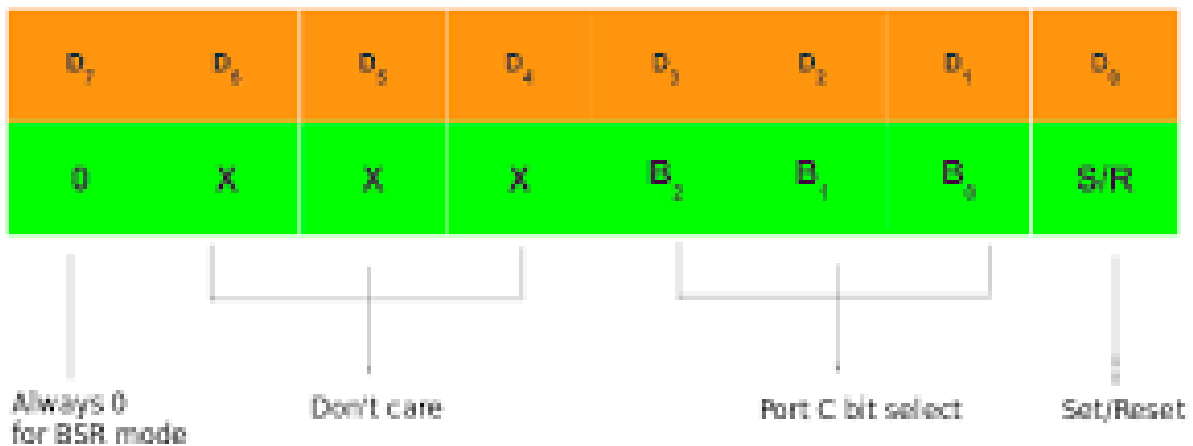
Block Diagram of 8255 PPI



Control word for I/O mode :



Control word for BSR mode:

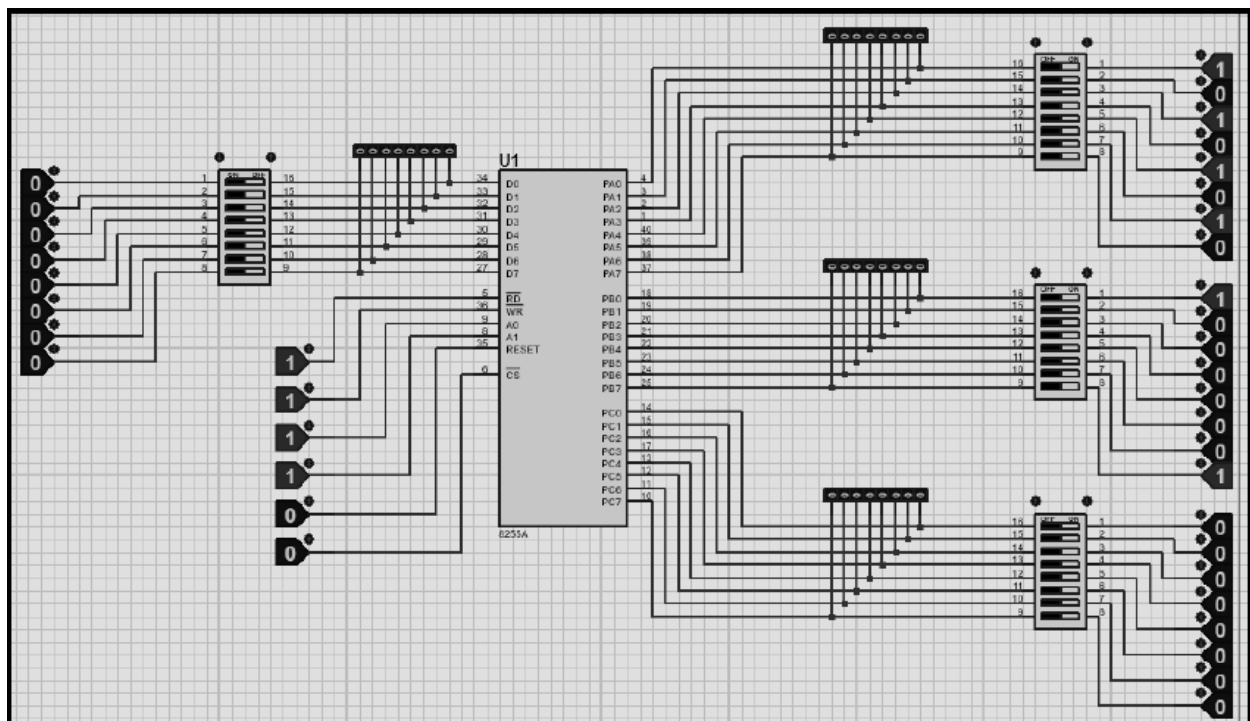


8255 Control Register format for BSR Mode

Cases of input/output operations:

A1	A0	RD_bar	WR_bar	CS	Input
0	0	0	1	0	Port A to Data Bus
0	1	0	1	0	Port B to Data Bus
1	0	0	1	0	Port C to Data Bus
1	1	0	1	0	Control Register to Data Bus
Output					
0	0	1	0	0	Data Bus to Port A
0	1	1	0	0	Data Bus to Port B
1	0	1	0	0	Data Bus to Port C
1	1	1	0	0	Data Bus to Control Register

Schematic



Final desgined chip :

