COMPUTER ORGANIZATION 2

Intel 8255 PPI chip

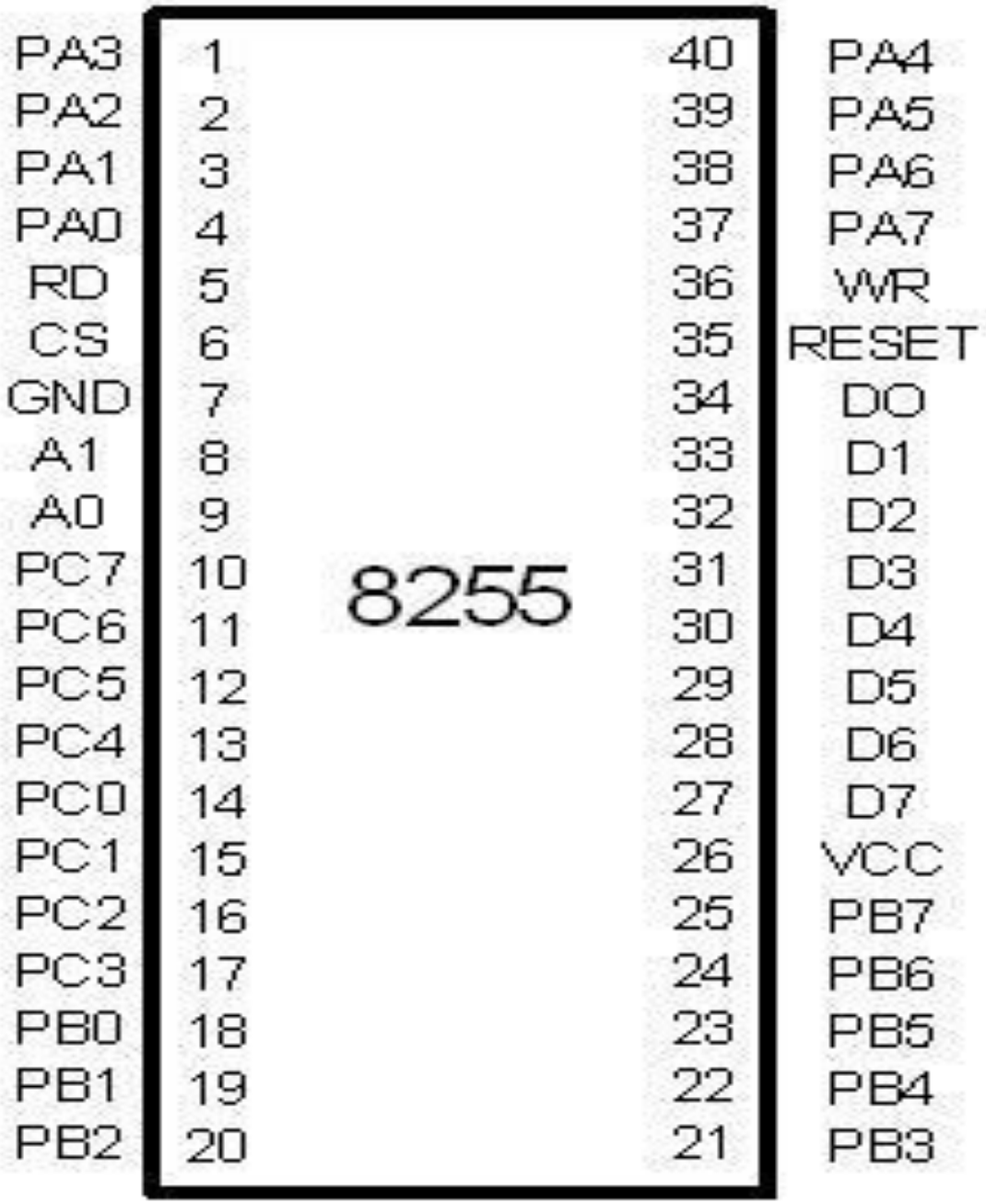
Submitted by:

Abdulrahman Hatem Metwally

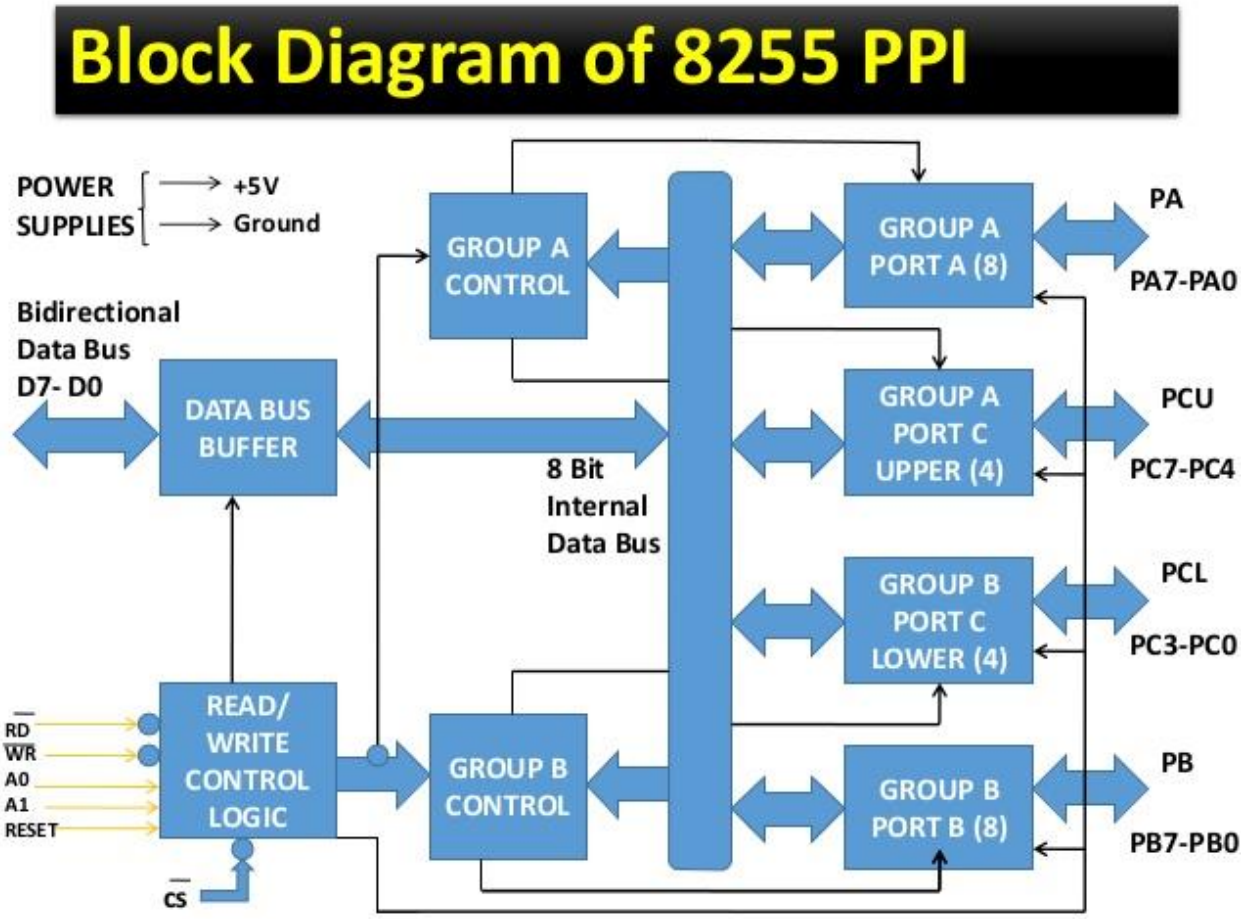
Abdullah Ahmed Fathy

Section: 2

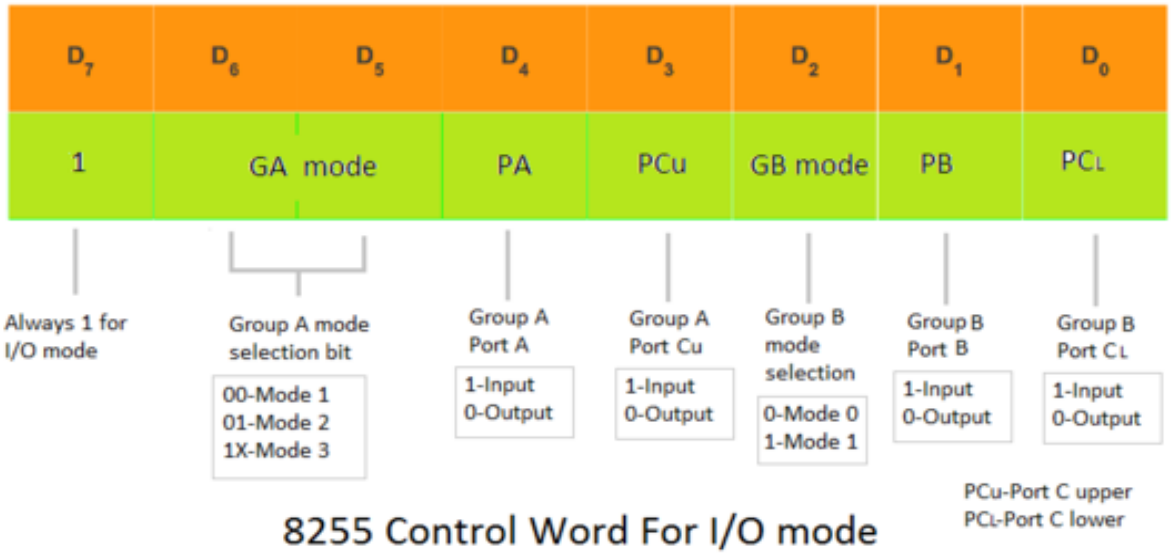
Peripheral interference:



Block diagram:

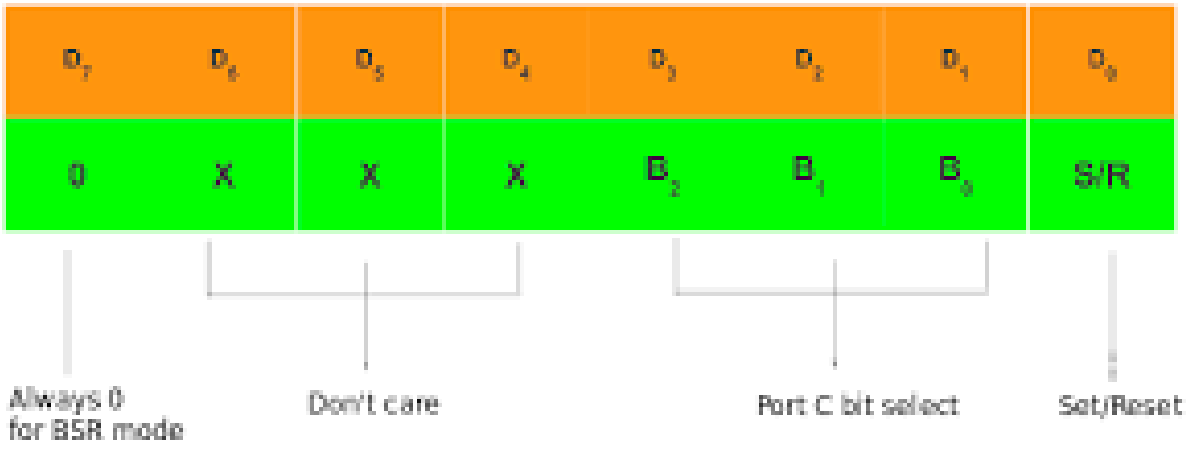


Control word for I/O mode :



8255 Control Word For I/O mode

Control word for BSR mode:

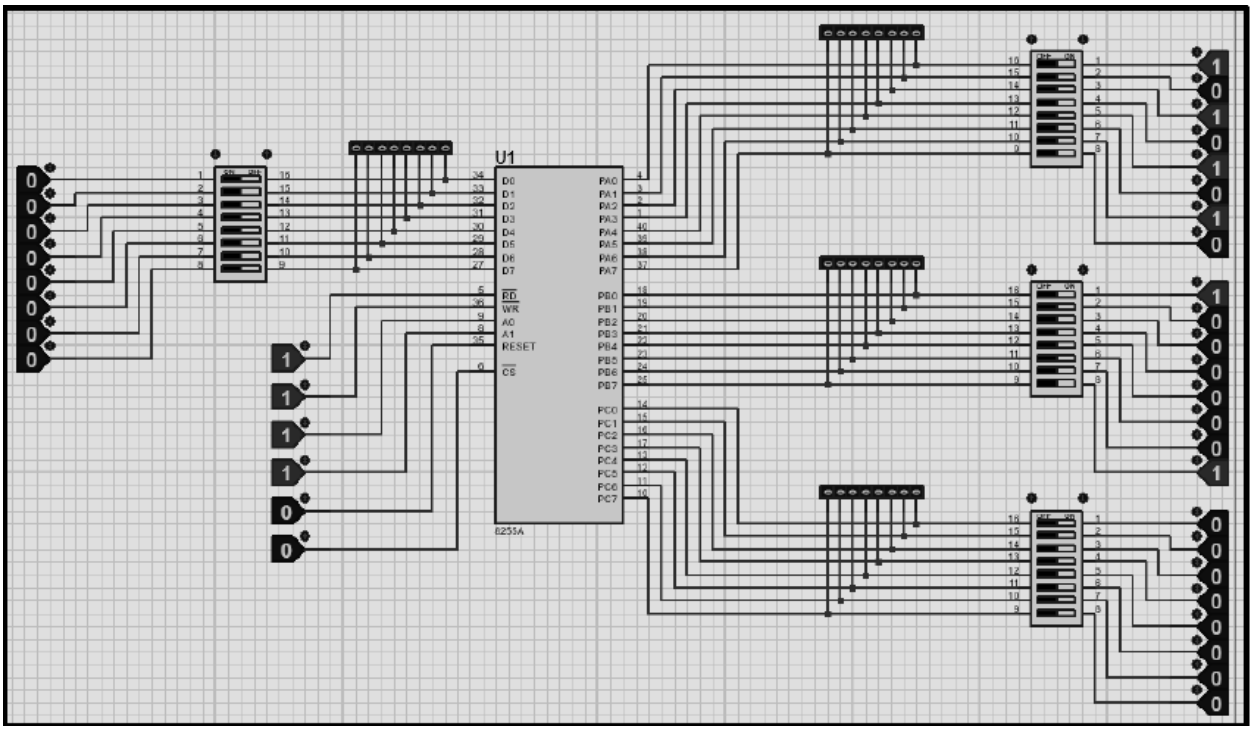


8255 Control Register format for BSR Mode

Cases of input/output operations:

A1	A0	RD_bar	WR_bar	CS	Input
0	0	0	1	0	Port A to Data Bus
0	1	0	1	0	Port B to Data Bus
1	0	0	1	0	Port C to Data Bus
1	1	0	1	0	Control Register to Data Bus
					Output
0	0	1	0	0	Data Bus to Port A
0	1	1	0	0	Data Bus to Port B
1	0	1	0	0	Data Bus to Port C
1	1	1	0	0	Data Bus to Control Register

Schematic



Final desgined chip :