2019
COMPUTER ORGANIZATION & ARCHITECTURE
IT401

TIME ALLOTTED: 3HRS **FULL MARKS: 70**

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP – A
(Multiple Choice Type Questions)

1. Answer any ***ten*** from the following, choosing the correct alternative of each question: **10×1=10**

CO No.

1. (i) The number of cycles required to complete n tasks in a k stage pipeline is — IT401.3
   a) k
   b) n + k – 1
   c) nk + 1
   d) n – k + 1

   ii) The address of next instruction to be executed is stored in — IT401.1
   a) Stack pointer
   b) General purpose register
   c) Program counter
   d) Address Latch

   iii) The situation where in the data of operands are not available is called _____. — IT401.3
   a) Data hazard
   b) Stock
   c) Deadlock
   d) Structural hazard

   iv) Which of the following architectures practically does not exist? — IT401.1
   a) MISD b) MIMD c) SISD d) SIMD

   v) Which of the following is not the cause of possible data hazard? — IT401.3
   a) RAR b) RAW c) WAR d) WAW

   vi) The CISC stands for — IT401.2
   a) Computer Instruction Set Compliment
   b) Complete Instruction Set Compliment
   c) Computer Indexed Set Components
   d) Complex Instruction set Computer

vii) Each stage in pipelining should be completed within ____ cycle. IT401.3
a) 1 b) 2 c) 3 d) 4

viii) Associative memory is a IT401.2
a) Pointer addressable memory
b) Very cheap memo
c) Content addressable memory
d) Slow memory

ix) In DMA transfers, the required signals and addresses are given by the IT401.3
a) Processor
b) Device drivers
c)DMA controllers
d) The program itself

x) Cache memory works on the principle of IT401.2
a) Locality of data.
b) Locality of reference
c) Locality of memory
d) Locality of reference & memory

xi) The number failed attempts to access memory, stated in the form of fraction are called as -------. IT401.3
a) Hit rate
b) Miss rate
c) Failure rate
d) Delay rate

xii) Which is not the property of a memory module? IT401.2
a) Inclusion
b) Consistency
c) Capability
d) Locality.

GROUP – B
(Short Answer Type Questions)

(Answer any *three* of the following)**3 x 5 = 15**

		CO No.
2.	Differentiate RISC and CISC architecture.	IT401.2
3.	Explain Arithmetic Pipeline with an example.	IT401.3
4.	Discuss working principle of carry look ahead adder.	IT401.1

5.		Explain Flyyn's Classification with Diagrammatic representation		IT401.4
6.		Differentiate memory mapped I/O and I/O mapped I/O		IT401.3

GROUP – C
(Long Answer Type Questions)

(Answer any *three* of the following) **3 x 15 = 45**

				CO No.
7.	a)	Given the following, determine size of the sub-fields (in bits) in the addresses for direct mapping, associative mapping and set associative mapping schemes: we have 256 MB main memory and 1MB cache memory. The address space of this processor is 256 MB. The block size is 128 bytes. There are 8 blocks in a cache set.		IT401.4
	b)	State different addressing modes.	**8+7**	IT401.2
8.	a)	What is paging? Discuss different Page Replacement policies.		IT401.3
	b)	Explain Different types of Interrupt.	**(2+6)+7**	IT401.2
9.	a)	Apply the Booth's Multiplication algorithm to multiply -23 and 9.		IT401.2
	b)	Design a common Bus transfer unit using Multiplexer.		IT401.4
	c)	Distinguish between Static RAM & Dynamic RAM	**8+5+2**	IT401.1
10.	a)	What is Pipeline Hazards?		IT401.3
	b)	Illustrate different types of Control Hazards and their overcome process		IT401.1
	c)	Design Memory Hierarchy with suitable diagram	**2+8+5**	IT401.4
11.	a)	Explain Handshaking Data Transfer technique		IT401.2
	b)	Design an 8x4 memory chip using 2x1 memory chips.		IT401.4

c) Consider the following Reservation Table. IT401.3

What are the forbidden latencies?

What are the Permissible latencies?

What is Collision Vector?

Find out Latency Cycles.

	1	2	3	4	5	6	7	8
S 1	X					X		X
S 2		X		X				
S 3			X		X		X	

5+5+5

12. Write Short Notes on *any three* **3 X 5 = 15**

i) Memory interleaving IT401.2

ii) Ripple carry adder IT401.1

iii) Cache Coherence IT401.3

iv) Dataflow Architecture IT401.4

v) Hardwired Controlled unit IT401.2