NARULAINSTITUTEOFTECHNOLOGY
An Autonomous Institute under MAKAUT

B. TECH/IT/EVEN/4th SEM/R_18/IT401/2021-2022
YEAR: 2022

COMPUTER ORGANIZATION & ARCHITECTURE

IT401

TIME ALLOTTED: 3 HOURS FULL MARKS: 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP – A
(Multiple Choice Type Questions)

1. Answer any ***ten*** from the following, choosing the correct alternative for each question:
10×1=10

SL. NO.	Question	Marks	CO
(i)	Which Register is used to storing the address of the next instruction to be executed a) Program Counter b) Stack Pointer c) Address Register d) Instruction Register	1	CO3
(ii)	What will be the maximum capacity of a memory, which uses an address bus of size 12 bit a) 2048 words b) 4096 words c) 512 words d) 246words	1	CO1
(iii)	Associative memory is a a) very cheap memory b) slow memory c) content addressable memory d) pointer addressable memory	1	CO3
(iv)	The offset used in the conditional branching is___ bit a) 24 b) 16 c) 24 d) 8	1	CO2
(v)	What is the formula for Hit Ratio? a) Hit/(Hit + Miss) b) Miss/(Hit + Miss) c) (Hit + Miss)/Miss d) (Hit + Miss)/Hit	1	CO4
(vi)	The users view of memory is supported by a) Paging b) Segmentation c) Both d) None of these	1	CO5

(vii)	Instruction cycle is a) Fetch-decode-execution b) Decode-fetch-execution c) Fetch-execution-decode d) None of these	1	CO3
(viii)	A certain processor supports only the immediate and the direct addressing modes. Which of the following programming language features cannot be implemented on this processor? a) Pointers b) Arrays c) Records d) All of these	1	CO4
(ix)	What will be the speed up for a 4 segment linear pipeline when the number of instruction n=64 a) 4.5 b) 3.82 c) 8.16 d) 2.95	1	CO1
(x)	In which of the following modes is the immediate operand included in the instruction? a) Register operand mode b) Register and immediate operand mode c) Immediate operand mode d) None of the mentioned	1	CO4
(xi)	What is the 2's complement representation of 24 in a 16-bit microprocessor a) 0000 0000 0001 1000 b) 1111 1111 1110 1000 c) 1111 1111 1110 0111 d) 0001 0001 1111 0011	1	CO1
(xii)	The Von-Neuman bottleneck is a problem, which occurs due to a) Small size main memory b)Speed disparity between CPU and Main Memory c) high speed CPU d) Malfunctioning of any unit in CPU	1	CO4

GROUP – B
(Short Answer Type Questions)

Answer any ***three*** from the following: **3×5=15**

SL.NO.			Marks	CO
2.	(a)	Compare RISC and CISC.	2	CO3
	(b)	Two 1024X4 bits RAM chips are given. Design a memory of size 2048X8 bits.	3	CO4
3	(a)	Write the assembly language procedures using 0,1,2, and 3 address instructions to implement the instruction: X=(A + B) * (C +D).	5	CO2
4.	(a)	Explain Von-Neumann architecture.	3	CO1
	(b)	What is pipelining? Give an example.	2	CO5
5.	(a)	What is cache memory? Explain memory write operation.	3	CO4
	(b)	Explain memory read operation?	2	CO3
6.	(a)	Briefly explain the IEEE 754 standard format for floating-point number representation.	2	CO4
	(b)	Represent the decimal value (-7.5) in IEEE single-precision format.	3	CO4

GROUP – C
(Long Answer Type Questions)

Answer any ***three*** from the following: **3×15=45**

SL. NO.			Marks	CO No.
7.	(a)	Explain the advantages of Carry's look ahead adder over Carry Propagator adder.	6	CO4
	(b)	Explain "NINE" property of cache memory?	4	CO5
	(c)	A Computer has 512 KB cache memory and 2 MB main memory. If the block size is 64 bytes, then find out the subfield for a) Direct Mapped Cache b) Associative Cache c) 8-way set associative Cache	5	CO5
8.	(a)	Briefly describe the following addressing modes with example: a)implied b)immediate c)register indirect	6	CO3
	(b)	Discuss the advantage of interrupt-initiated I/O over programmed I/O.	4	CO4
	(c)	Suppose the time delays of the four stages of a pipeline are t1=60 ns, t2=70ns, t3=90ns and t4=80ns respectively and the	5	CO4

		interface latch has a delay t=10ns. Calculate a) Maximum clock frequency of the above pipeline b) Maximum speed-up of this pipeline over its equivalent non-pipeline counterpart.		
9.	(a)	Perform (-7) * (3) using Booth's algorithm.	8	CO2
	(b)	Write the Booth's flowchart.	4	CO5
	(c)	Compare and contrast SRAM and DRAM	3	CO1
10.	(a)	Consider page reference string 1, 3, 0, 3, 5, 6, 3 with 3 page frames. Find the number of page faults for LRU page replacement algorithm.	5	CO5
	(b)	You are required to write a program segment that can perform the operation C ← A+B (a) A machine with one-address instructions (b) A machine with one-and-half instructions (c) A machine with two-address instructions (d) A machine with three-address instructions (e) A machine with zero-address instructions	10	CO3
11.		Write down the short notes on any three of the followings;	3*5=15	
	(a)	Direct Memory Access	5	CO2
	(b)	Addressing Modes	5	CO3
	(c)	Flynn's classification	5	CO1
	(d)	Cache Coherence	5	CO4
	(e)	VLIW Architecture	5	CO4