NARULA INSTITUTE OF TECHNOLOGY
An Autonomous Institute under MAKAUT

B.TECH./IT/EVEN/4TH/R-18/ IT402/2022-2023
YEAR: 2023

Computer Organization and Architecture
IT402

TIME ALLOTTED: 3 HOURS FULL MARKS: 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP – A
(Multiple Choice Type Questions)

1. Answer any ***ten*** from the following, choosing the correct alternative of each question: **10×1=10**

SL	Question	Marks	Co	Blooms Taxonomy Level
(i)	Cache memory works on the principle of a) Locality of data. b) Locality of reference c) Locality of memory d) Locality of reference & memory	1	2	1
(ii)	Which Register is used to storing the address of the next instruction to be executed a) Program Counter b) Stack Pointer c) Address Register d) Instruction Register	1	1	1
(iii)	CPU does not perform the operation …… a) data transfer b) logic operation c) arithmetic operation d) all of the above	1	2	1
(iv)	What is the 2's complement representation of 48 in a 16-bit microprocessor a) 0000 0000 0001 1000 b) 1111 1111 1110 1000 c) 1111 1111 1101 0000 d) 0001 0001 1111 0011	1	3	1
(v)	Micro instructions are kept in a) main memory b) control store c) cache d) none of these.	1	3	1
(vi)	The fastest data access is provided using …… a) Caches b) DRAM's c) SRAM's d) Registers	1	5	1
(vii)	In DMA transfers, the required signals and addresses are given by the a) Processor b) Device drivers c)DMA controllers d) The program itself	1	4	1

(viii)	. ___ is the logical structure of a computer's Random-Access Memory (RAM). a) Memory addressing b)Operation field c) Address field d) Addressing mode	1	3	1
(ix)	Each stage in pipelining should be completed within ____ cycle. a) 1 b) 2 c) 3 d) 4	1	1	1
(x)	Which of the following is not the cause of possible data hazard? a) RAR b) RAW c) WAR d) WAW	1	3	1
(xi)	The principle of locality of reference justifies the use of a) Interrupt b) Polling c) DMA d) Cache memory	1	1	1
(xii)	Basic difference between vector and array processor is a) Pipeline b) Interconnection network c) Register d) None of these	1	2	1

GROUP – B
(Short Answer Type Questions)
(Answer any three of the following) 3 x 5 = 15

SL	Question	Marks	Co	Blooms Taxonomy Level
2.	Differentiate RISC and CISC architecture.	5	4	2
3.	Explain Flynn's Classification with Diagrammatic representation	5	2	2
4.	A system uses 4 page frames for storing process pages in main memory. It uses the Optimal page replacement policy. Assume that all the page frames are initially empty. What is the total number of page faults that will occur while processing the page reference string given below- 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7, 0, 1	5	3	3
5.	A microprocessor has a data bus with 64 lines and an address bus with 32 lines. What is the maximum number of bits that	5	4	3

		can be stored in memory?			
6.		Briefly describe programmed i/o and interrupt driven i/o.	5	3	1

GROUP – C
(Long Answer Type Questions)

(Answer any three of the following) 3 x 15 = 45

SL		Question	Marks	Co	Blooms Taxonomy Level
7.	(i)	Differentiate direct, associative and set associative mapping.	5	2	2
	(ii)	A Computer has 512 KB cache memory and 2 MB main memory. If the block size is 64 bytes, then find out the tag bits for a) Direct Mapped Cache b) Associative Cache c) 8-way set associative Cache	10	5	3
8.		Consider a disk pack with the following specifications- 16 surfaces, 128 tracks per surface, 256 sectors per track and 512 bytes per sector. Answer the following questions- 1. What is the number of bits required to address the sector? 2. If the format overhead is 32 bytes per sector, what is the formatted disk space? 3. If the diameter of innermost track is 21 cm, what is the maximum recording density? 4. If the disk is rotating at 3600 RPM, what is the data transfer rate? 5. If the disk system has rotational speed of 3000 RPM, what is the average access time with a seek time of 11.5 msec?	15	2	3
9.	(i)	What is Pipeline Hazards? Illustrate different types of Pipeline Hazards.	10	2	2
	(ii)	A five-stage pipeline has the stage delays as 150, 120, 160,130 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate, what will be the total time taken to process 1000 data items on the pipeline?	5	5	3
10.	(i)	Differentiate direct, associative and set associative mapping.	5	4	2

(ii)	Consider a 2-way set associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find- I. Number of bits in tag II. Tag directory size	10	1	3
11.	Write down the short notes on any three of the followings:	5*3		
	a) DMA		3	2
	b) Memory Hierarchy		4	2
	c) IEEE 754 format		2	2
	d) Locality of reference		3	2
	e) Von Neumann architecture		1	2