NARULA INSTITUTE OF TECHNOLOGY
An Autonomous Institute under MAKAUT

B.TECH/IT/EVEN/4/IT401/2020-2021
PAPER TYPE: REGULAR/SUPPLE(R18)
YEAR: 2021

COMPUTER ORGANISATION AND ARCHITECTURE
IT401

TIME ALLOTTED: 3 HOURS FULL MARKS: 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP – A
(Multiple Choice Type Questions)

1. Answer any ***ten*** from the following, choosing the correct alternative of each question: **10×1=10**

SL. NO.	Question	CO No.	Marks
(i)	CPU does not perform the operation …… a) data transfer b) logic operation c) arithmetic operation d) all of the above	3	1
(ii)	The main difference between the VLIW and the other approaches to improve performance is a) Cost effectiveness. b) Increase in performance c) Lack of complex hardware design d) All of the above	5	1
(iii)	The contention for the usage of a hardware device is called as _____. **a)** Structural hazard b) Stalk c) Deadlock d) None of the mentioned	1	1
(iv)	The basic principle of Von-Neumann computer is a) storing program and data in separate memory b) using pipeline concept c) storing program and data in same memory d) using a large number of registers	1	1
(v)	The fastest data access is provided using …… a) Caches b) DRAM's c) SRAM's d) Registers	4	1
(vi)	What is the advantage of write through cache a) memory bandwidth is high b) retains consistent image of program activity in memory c) dirty bit is set d) none of these.	5	1
(vii)	The effectiveness of the cache memory is based on	4	1

	the property of _____. a) Locality of reference b) Memory localisation c) Memory size d) None of the above		
(viii)	_____is used to implement virtual memory organisation. a) Page table b) Frame table c) MMU d) None of the above	1	1
(ix)	The bit used to signify that the cache location is updated is _____. a)Dirtybit b)Updatebit c)Referencebit d) Flag bit	4	1
(x)	To increase the speed of memory access in pipelining, we make use of _____. a) Special memory locations b) Special purpose registers c) Cache d) Buffers	3	1
(xi)	Micro instructions are kept in a) main memory b) control store c) cache d) none of these.	4	1
(xii)	In a microprocessor the address of the next instruction to be executed is stored in a) stack pointer b) address latch c) program counter d) general purpose register	2	1

GROUP – B*
(Short Answer Type Questions)

Answer any ***three*** from the following: **3×5=15**

SL. NO.		CO No.	Marks
2.	Explain data hazards and how to overcome it.	4	5
3.	Give the flowchart for multiplication of two binary numbers and explain.	2	5
4.	Briefly discuss SIMD and MISD architecture.	3	5
5.	Explain the working principle of a static RAM cell with proper diagram.	4	5
6.	What are the advantages of microprogramming	5	3+2

control over hardwired control? What is the role of an operating system here?

GROUP – C*
(Long Answer Type Questions)

Answer any ***three*** from the following: **3×15=45**

SL. NO.			CO No.	Marks
7.		Apply Booth's algorithm to multiply the two numbers (+14) and (-12). Assume the multiplier and multiplicand to be of 5 bits each.	1	15
8	(a)	Explain Von Neumann architecture.	3	8
	(b)	What is vector processor?	3	4
	(c)	Write the different types of vector instructions.	1	3
9	(a)	Explained loosely coupled and tightly coupled multiprocessor system.	2	**5**
	(b)	Explain immediate, direct, implied, register indirect and relative addressing modes with example	1	10
10	(a)	Explain DMA working principle.	3	10
	(b)	Explain the difference between instruction and arithmetic pipeline.	4	5
11		Write short notes on the following (Any three)		
	(a)	CISC and RISC	2	**5**
	(b)	Cache coherence problem	1	**5**
	(c)	Memory Hierarchy	5	**5**
	(d)	VLIW Architecture	2	**5**
	(e)	Flynn's classification	3	**5**