NARULA INSTITUTE OF TECHNOLOGY

An Autonomous Institute under MAKAUT

B.Tech./IT/ODD/3rd SEM/R_21/ IT303 /2022-2023 YEAR: 2022

ANALOG AND DIGITAL ELECTRONICS IT303

TIME ALLOTTED: 3 HOURS FULL MARKS: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable

GROUP – A (Multiple Choice Type Questions)

1	Answer any ten from the following, choosing the correct alternative		e of each question: 10×1=10		
SL	Question	Marks	СО	Blooms Taxonomy Level	
(i)	The circuit overcomes the problem of switching caused by jitter on the inputs.	01	IT303.1	Understanding	
	 a) Astable Multivibrator b) Monostable Multivibrator c) Bistable Multivibrator d) Schmitt Trigger 				
(ii)	The output of an exclusive-NOR gate is 1. Which input combination is correct?	01	IT303.2	Analyzing	
	 a) A = 1, B = 0 b) A = 0, B = 1 c) A = 0, B = 0 d) none of the above 				
(iii)	How many AND gates are required to implement the Boolean expression? AB'+A'B'	01	IT303.2	Applying	
	a) 1 b) 2 c) 3 d) 4				
(iv)	What is another name for a bistable multivibrator? a) an on-off switch b) an oscillator	01	IT303.1	Understanding	
	c) a flip-flopd) none of the above				
(v)	An astable 555 timer has the following number of stable states: a) 0 b) 1 c) 2 d) 3	01	IT303.1	Applying	
(vi)	The binary numbers $A = 1100$ and $B = 1001$ are applied to the inputs of a comparator. What are the output levels? a) $A > B = 1$, $A < B = 0$, $A < B = 1$	01	IT303.2	Analyzing	

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		A > B = 0, A < B = 1, A = B = 0 A > B = 1, A < B = 0, A = B = 0 A > B = 0, A < B = 1, A = B = 1			
(vii)	How is	a J-K flip-flop made to toggle?	01	IT303.3	Understanding
		J = 0, K = 0			
		J = 1, K = 0 J = 0, K = 1			
		J = 1, K = 1			
(viii)		tive-HIGH S-R latch has a 0 on the S input and a 1 on aput and then the R input goes to 0, the latch will be	01	IT303.3	Analyzing
	a)	SET			
	b) c)	RESET CLEAR			
	d)	INVALID			
(ix)	On a J-	K flip-flop, when is the flip-flop in a hold condition?	01	IT303.3	Applying
		J = 0, K = 0			
	,	J = 1, K = 0 J = 1, K = 1			
	d)	J = 1, K = 1 J = 0, K = 1			
(x)	Which gates?	of these sets of logic gates are designated as universal	01	IT303.2	Understanding
	a)	NOR, NAND.			
	b) c)	XOR, NOR, NAND. OR, NOT, AND.			
	d)	NOR, NAND, XNOR			
(xi)	Registe	r is a?	01	IT303.3	Applying
	a)	Set of capacitor used to register input instructions in a digital computer			
	b)	Set of paper tapes and cards put in a file			
	c)	Temporary storage unit within the CPU having dedicated or general-purpose use			
	d)	Part of the auxiliary memory			
(xii)	An SR	flip flop cannot accept the following input entry	01	IT303.3	Analyzing
	a)	Both input zero			
	b) c)	zero at R and one at S zero at S and one at R			
	d)	Both inputs one			

$GROUP-B \\ (Short Answer Type Questions) \\ (Answer any three of the following) 3 x 5 = 15$

SL	Question	Marks	CO	Blooms
				Taxonomy
				Level
2.	Design a Full Subtractor Circuit using logic gates.	05	IT303.3	Understanding

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3.	(i)	Prove the following Boolean identity- $(A+B)(A+B')(A'+C)=AC$.	03	IT303.2	Understanding	
	(ii)	Convert Hexa decimal to binary number: (2E5A) ₁₆ .	02	IT303.2	Applying	
4.		Explain 1-to-8 De-multiplexer by using logic gates.	05	IT303.3	Understanding	
5.		Solve the function using K map method- F = \sum m (1,2,4,6,7) + \sum d (11,14)	05	IT303.2	Applying	
6.		Describe the operation of a 555 timer in a table mode.	05	IT303.1	Analyzing	
	GROUP – C (Long Answer Type Questions)					
		(Answer any three of the following)	$3 \times 15 = 45$			
	SL	Question	Marks	CO	Blooms Taxonomy Level	
7.		What is Shift register? What are the different types of shift register? Explain the working of Serial in parallel out shift register with logic diagram.	02+ 04 + 09	IT303.3	Analyzing	
8.		Represent the following in both SOP and POS using Karnaugh map- (A'+B'+D') (A+B'+C') (A'+B+D') (B+C'+D)	08+ 07	IT303.2	Understanding	
9.		What is multi-vibrator? Draw and explain the working Principle of CMOS. In a monostable multivibrator R= 100KQ, and the time delay T= 100ms, Calculate the value of C.	15	IT303.1	Understanding	
10.	(i)	Design a 2-bit Magnitude Comparator Circuit.	07	IT303.2	Applying	
	(ii)	Explain 4-bit R-2R ladder type D/A converter.	08	IT303.4	Applying	
11.		Define Followings any three:				
	(i)	4-bit R-2R ladder type D/A converter	05	IT303.4	Applying	
	(ii)	Parity Generator	05	IT303.2	Analyzing	
	(iii)	Successive approximation type A/D Converter	05	IT303.4	Understanding	
	(iv)	Class AB Amplifier	05	IT303.1	Analyzing	
	(v)	Encoder	05	IT303.2	Understanding	