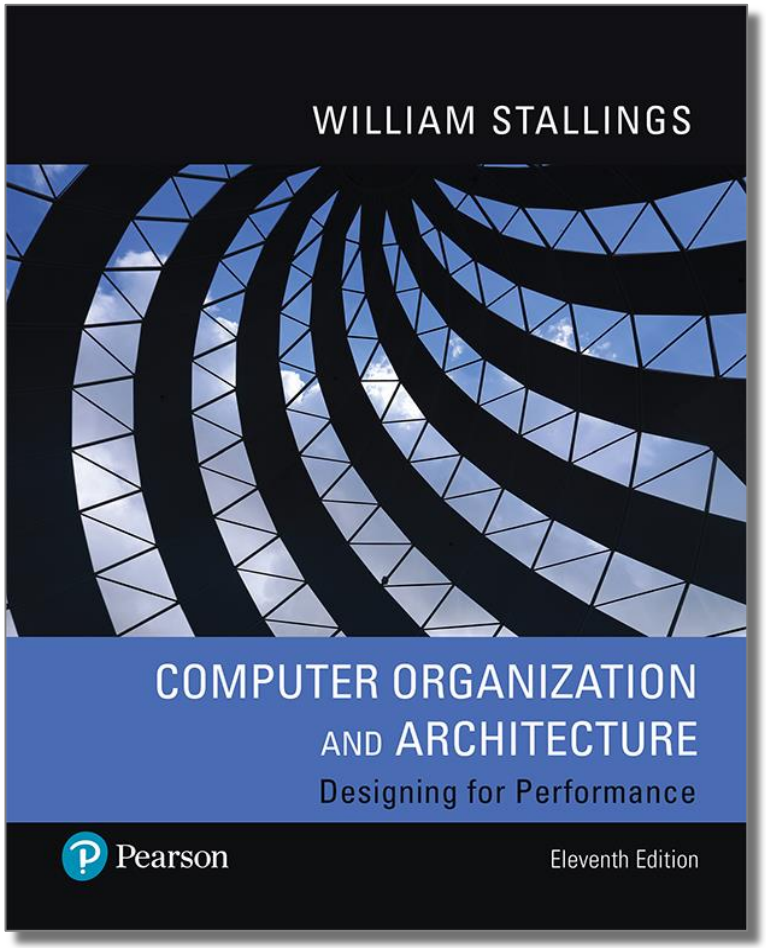
# Computer Organization and Architecture

## Designing for Performance

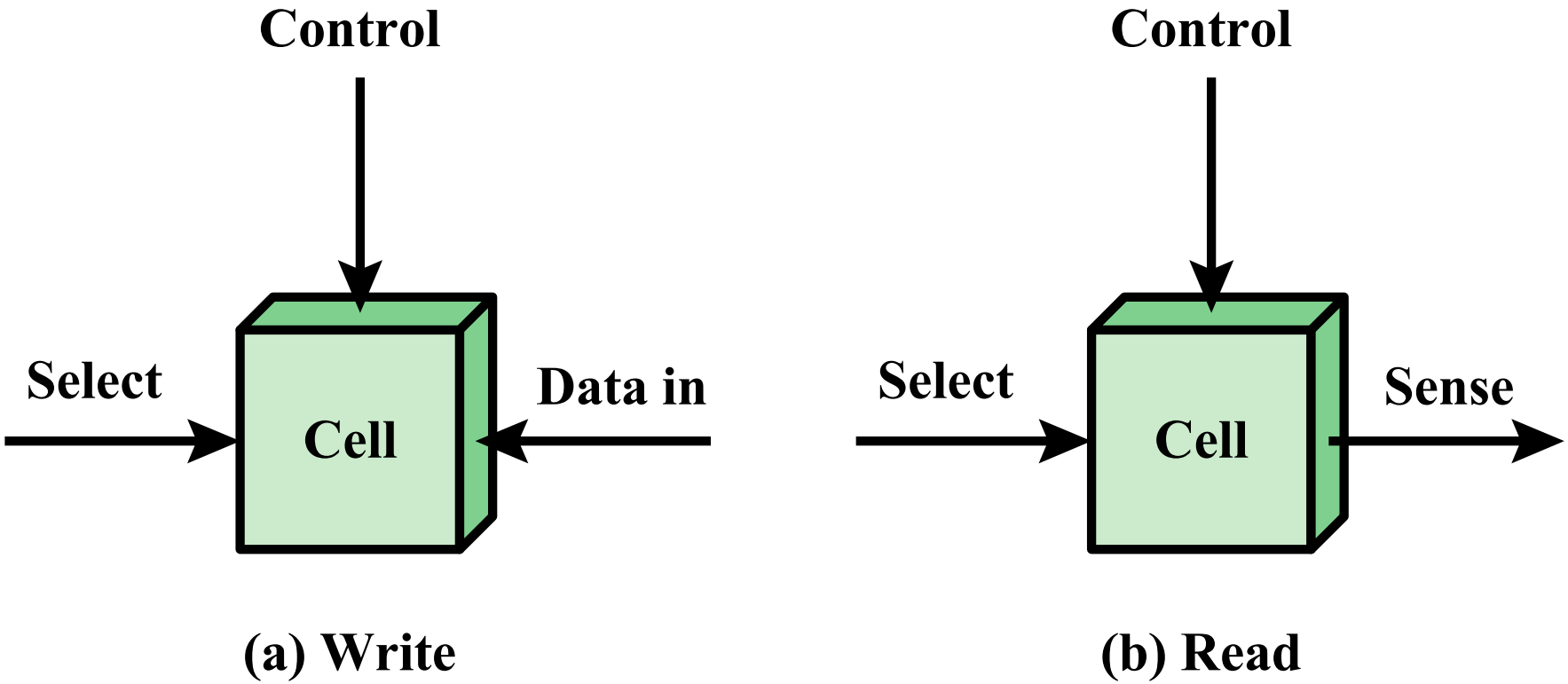
11th Edition




## Chapter 6

Internal Memory

# Figure 6.1
# Memory Cell Operation



# Memory Cell Operation

- The basic element of a semiconductor memory is the memory cell. Although a variety of electronic technologies are used, all semiconductor memory cells share certain properties:
  - They exhibit two stable (or semi-stable) states, which can be used to represent binary 1 and 0.
  - They are capable of being written into (at least once), to set the state.
  - They are capable of being read to sense the state.

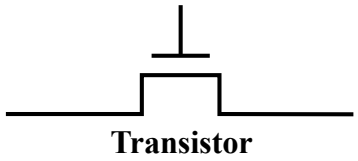
# Table 6.1
# Semiconductor Memory Types

| Memory Type | Category | Erasure | Write Mechanism | Volatility |
|---|---|---|---|---|
| Random-access memory (RAM) | Read-write memory | Electrically, byte-level | Electrically | Volatile |
| Read-only memory (ROM) | Read-only memory | Not possible | Masks | Nonvolatile |
| Programmable ROM (PROM) | | | Electrically | |
| Erasable PROM (EPROM) | Read-mostly memory | UV light, chip-level | | |
| Electrically Erasable PROM (EEPROM) | | Electrically, byte-level | | |
| Flash memory | | Electrically, block-level | | |

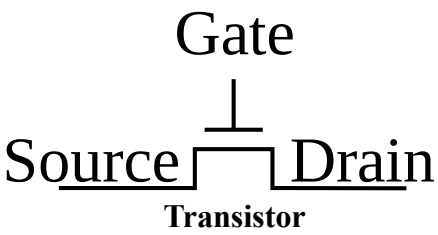
# Dynamic RAM (DRAM)

- RAM technology is divided into two technologies:
  - Dynamic RAM (DRAM)
  - Static RAM (SRAM)
- DRAM
  - Made with cells that store data as charge on capacitors
  - Presence or absence of charge in a capacitor is interpreted as a binary 1 or 0
  - Requires periodic charge refreshing to maintain data storage
  - The term *dynamic* refers to tendency of the stored charge to leak away, even with power continuously applied

# Figure 6.2
# Typical Memory Cell Structures



# Figure 6.2
# Typical Memory Cell Structures



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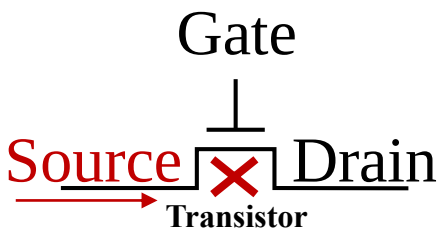
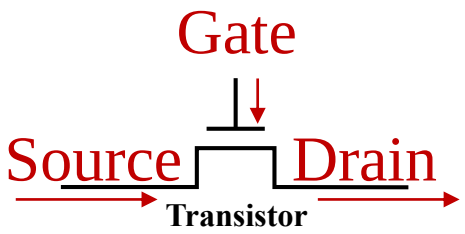
# Typical Memory Cell Structures



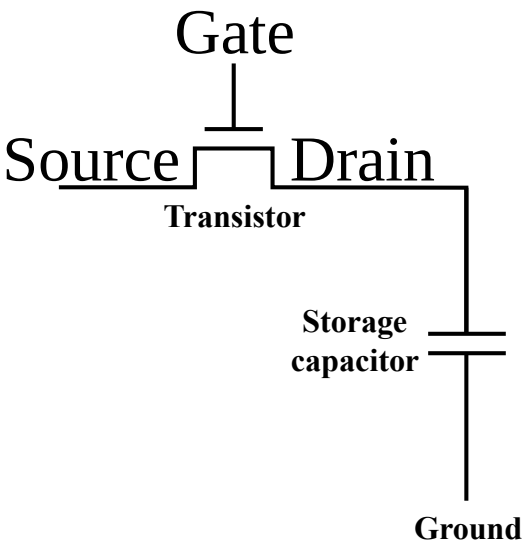

- When a voltage is applied to the source, current is blocked from flowing through the transistor.

# Figure 6.2
# Typical Memory Cell Structures



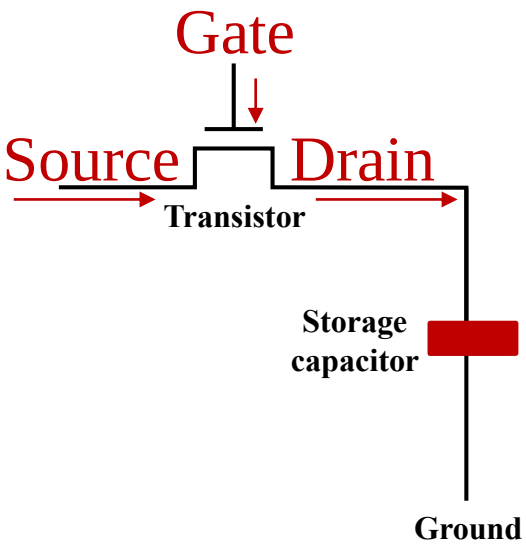

- When a voltage is applied to the source, current is blocked from flowing through the transistor.
- BUT when a voltage is applied to both the gate and the source, current is allowed to flow through the transistor.
- This makes the transistor work as switch.

# Figure 6.2
# Typical Memory Cell Structures



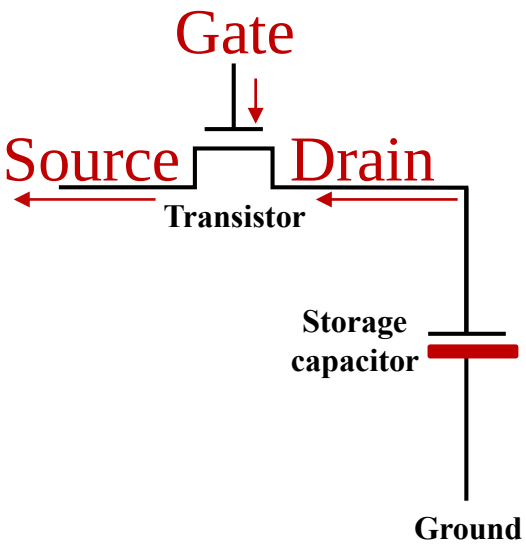

- To create a memory cell, the transistor is connected to a capacitor.
- A capacitor stores an electric charge, a high charge means a ‘1’ and a low charge means a ‘0’ (based on threshold)
- Capacitors are analog devices not digital.

# Figure 6.2
# Typical Memory Cell Structures



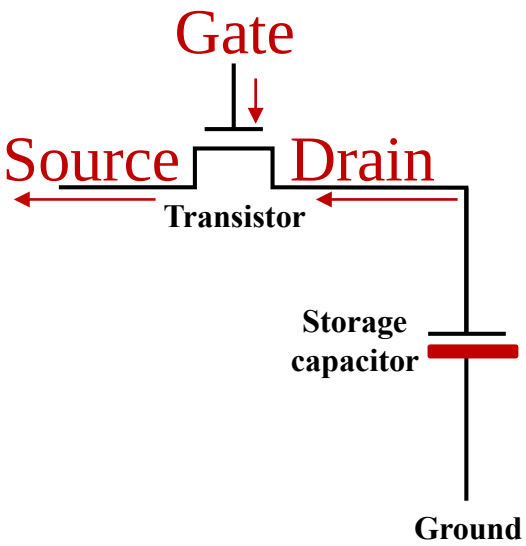

- Writing ‘1’ to this cell: Apply voltage to the gate and source. This will allow current flow that will charge the capacitor.

# Figure 6.2
# Typical Memory Cell Structures



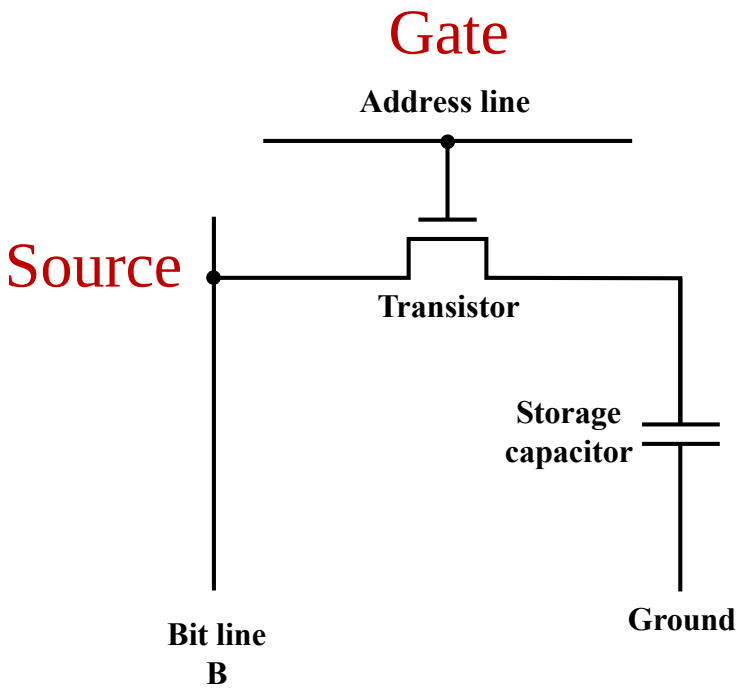

- Writing ‘0’ to this cell: Apply voltage to the gate ONLY.
- This will allow current flow in reverse from the drain to the source, which means discharging the capacitor.

# Figure 6.2
# Typical Memory Cell Structures



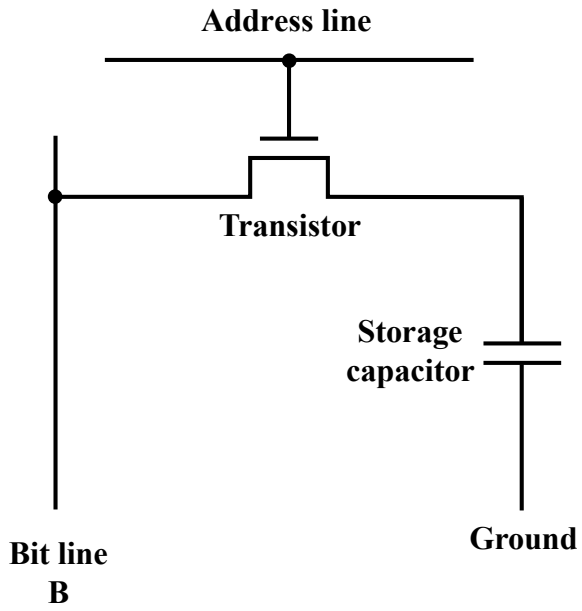

- It could also means reading data from this cell!
- This means, a read operation destroys the data and requires a write operator immediately after that to restore the data.
- Also, a capacitor is discharged slowly over time. It requires a refresh mechanism to renew its charge.

# Figure 6.2
# Typical Memory Cell Structures

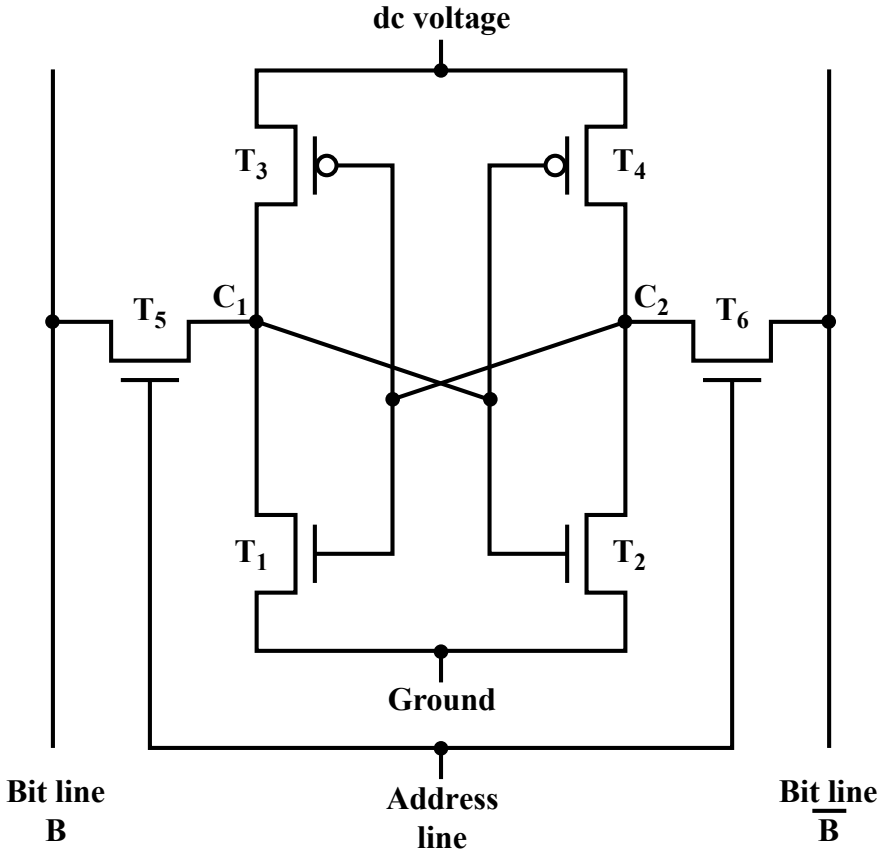



(a) Dynamic RAM (DRAM) cell

# Figure 6.2
# Typical Memory Cell Structures




(a) Dynamic RAM (DRAM) cell




(b) Static RAM (SRAM) cell

# Static RAM (SRAM)

- Digital device that uses the same logic elements used in the processor
- Binary values are stored using traditional flip-flop logic gate configurations
- Will hold its data as long as power is supplied to it

# SRAM versus DRAM

SRAM

- Both volatile
  - Power must be continuously supplied to the memory to preserve the bit values
- Dynamic cell
  - Simpler to build, smaller
  - More dense (smaller cells = more cells per unit area)
  - Less expensive
  - Requires the supporting refresh circuitry
  - Tend to be favored for large memory requirements
  - Used for main memory
- Static
  - Faster
  - Used for cache memory (both on and off chip)

DRAM

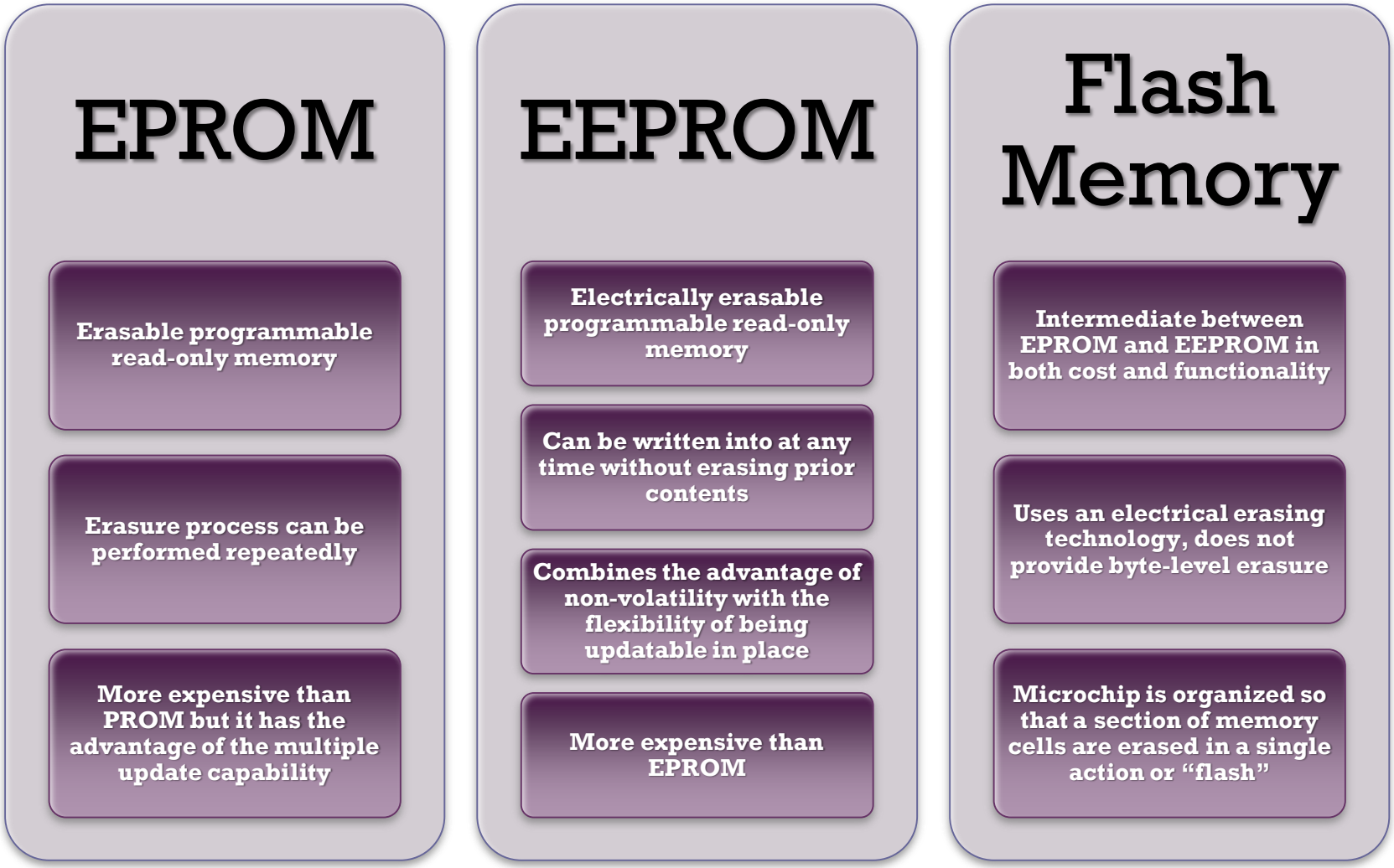
# Read Only Memory (ROM)

- Contains a permanent pattern of data that cannot be changed or added to
- No power source is required to maintain the bit values in memory
- Data or program is permanently in main memory and never needs to be loaded from a secondary storage device
- Data is actually wired into the chip as part of the fabrication process
  - Disadvantages of this:
    - No room for error, if one bit is wrong the whole batch of ROMs must be thrown out
    - Data insertion step includes a relatively large fixed cost

# Programmable ROM (PROM)

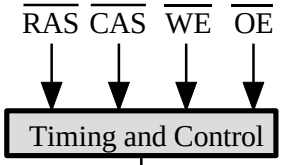
- Less expensive alternative
- Nonvolatile and may be written into only once
- Writing process is performed electrically and may be performed by supplier or customer at a time later than the original chip fabrication
- Special equipment is required for the writing process
- Provides flexibility and convenience
- Attractive for high volume production runs

# Read-Mostly Memory

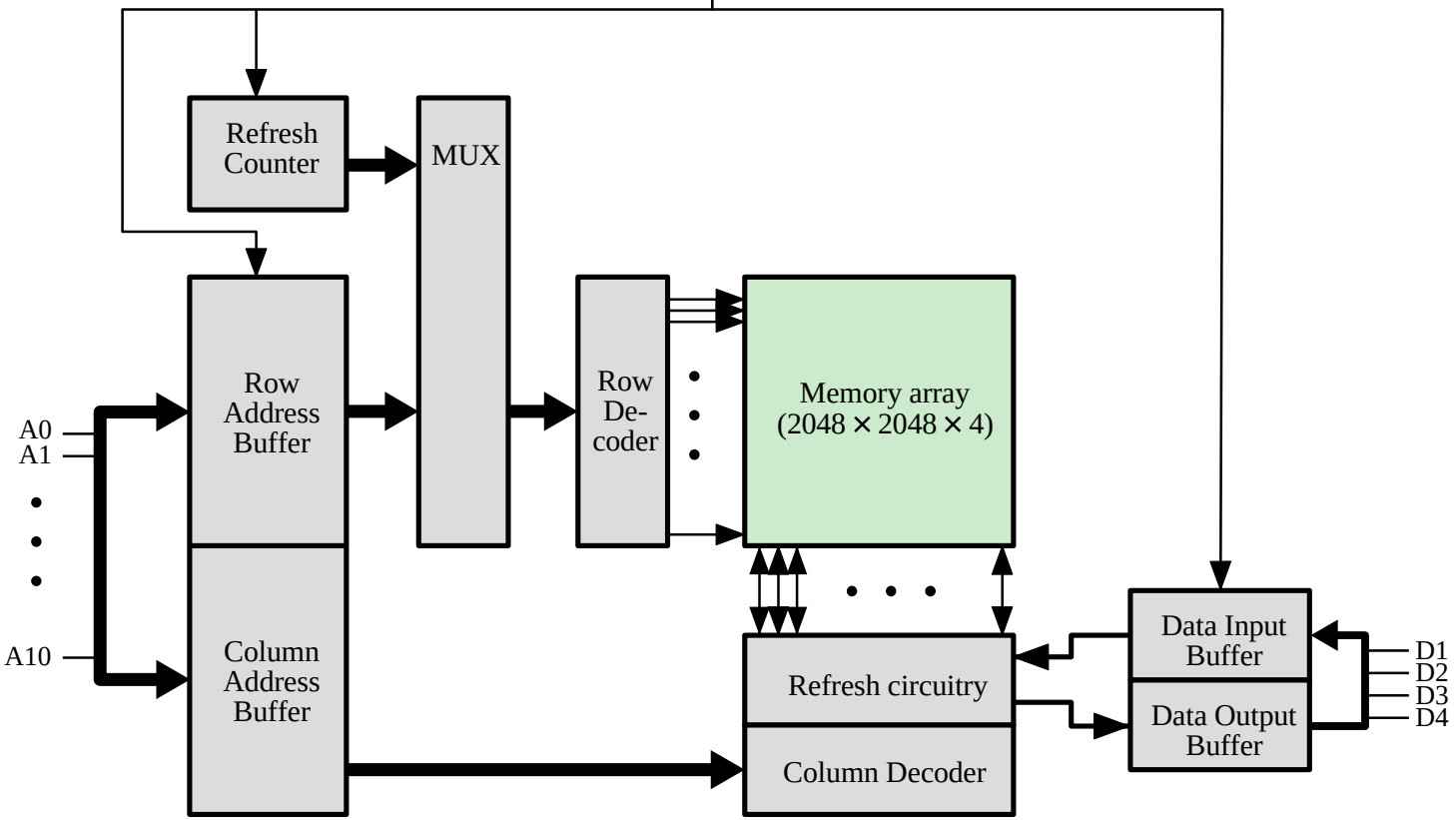


# Figure 6.3
# Typical 16-Mbit DRAM (4M × 4)

RAS: Row Address Select
CAS: Column Address Select




WE: Write Enable
OE: Output Enable



# Chip Logic

- Logically, the memory array is organized as four square arrays of 2048 by 2048 elements. Various physical arrangements are possible.
- The elements of the array are connected by both horizontal (row) and vertical (column) lines. Each horizontal line connects to the Select terminal of each cell in its row; each vertical line connects to the Data-In/Sense terminal of each cell in its column.

# Chip Logic

- Address lines supply the address of the word to be selected. In our example, 11 address lines are needed to select one of 2048 rows. These 11 lines are fed into a row decoder, which has 11 lines of input and 2048 lines for output.
- The logic of the decoder activates a single one of the 2048 outputs depending on the bit pattern on the 11 input lines ($2^{11} = 2048$).
- An additional 11 address lines select one of 2048 columns of 4 bits per column. Four data lines are used for the input and output of 4 bits to and from a data buffer.

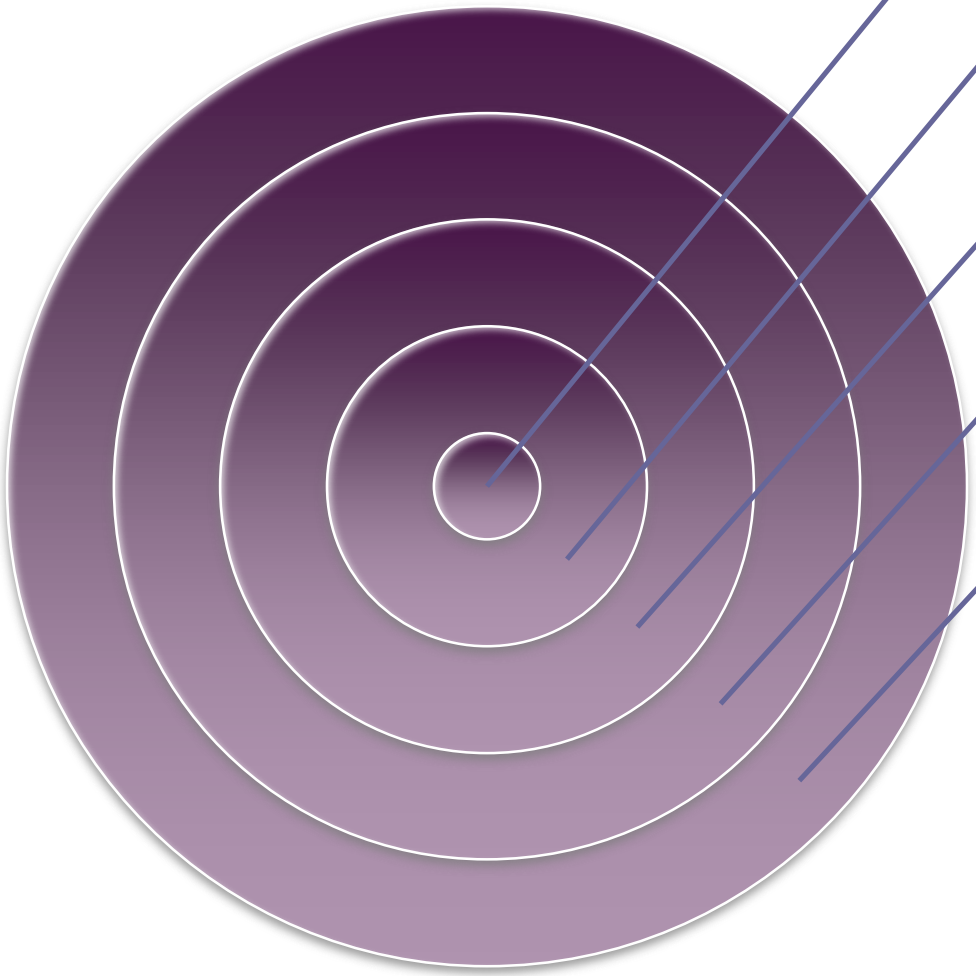
# Chip Logic

- Note that there are only 11 address lines (A0–A10), half the number you would expect for a 2048 * 2048 array. This is done to save on the number of pins.
- The 22 required address lines are passed through select logic external to the chip and multiplexed onto the 11 address lines.
- First, 11 address signals are passed to the chip to define the row address of the array, and then the other 11 address signals are presented for the column address.

# Chip Logic

- The refresh counter steps through all of the row values. For each row, the output lines from the refresh counter are supplied to the row decoder and the RAS line is activated.
- The data are read out and written back into the same location. This causes each cell in the row to be refreshed.

# Interleaved Memory



Composed of a collection of DRAM chips

Grouped together to form a *memory bank*

Each bank is independently able to service a memory read or write request

*K* banks can service *K* requests simultaneously, increasing memory read or write rates by a factor of *K*

If consecutive words of memory are stored in different banks, the transfer of a block of memory is speeded up

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