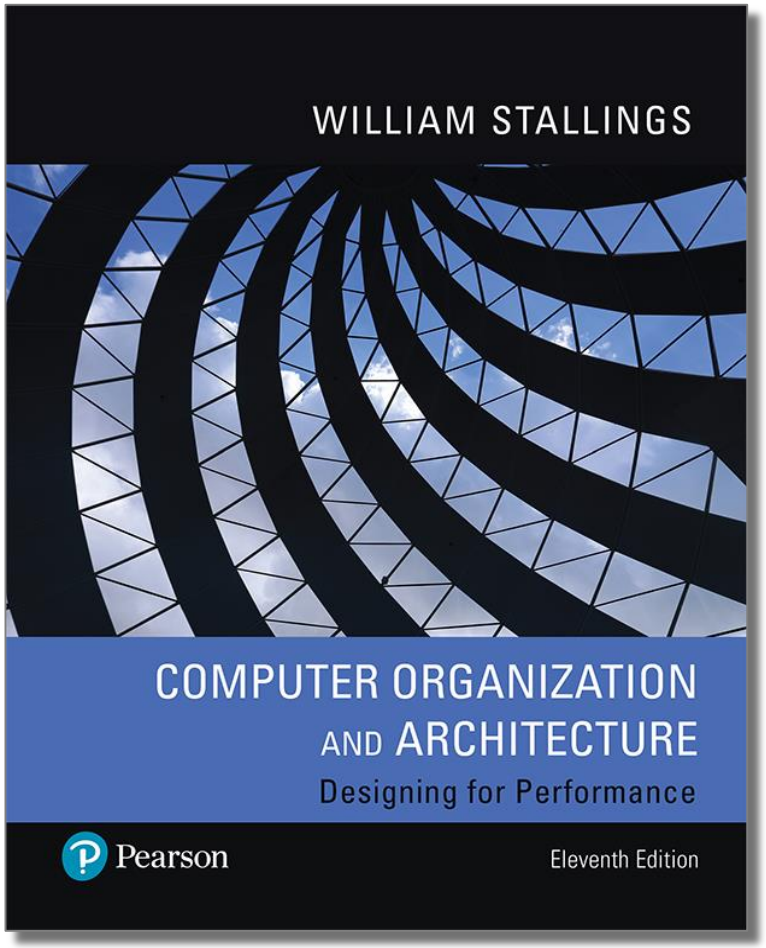
Computer Organization and Architecture

Designing for Performance

11th Edition



Chapter 3

A Top-Level View of Computer Function and Interconnection

Figure 3.15

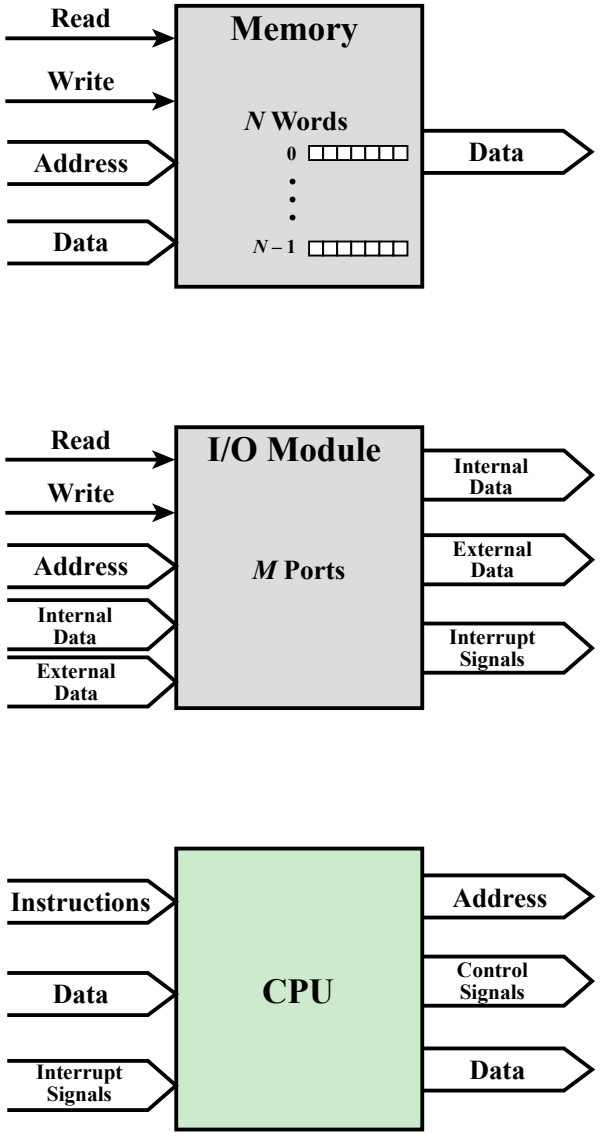


Figure 3.15 Computer Modules

Memory Module

- A memory module will consist of N words of equal length
- Each word is assigned a unique numerical address (0,1,...,N1)
- A word of data can be read from or written into the memory
- The nature of the operation is indicated by read and write control signals
- The location for the operation is specified by an address

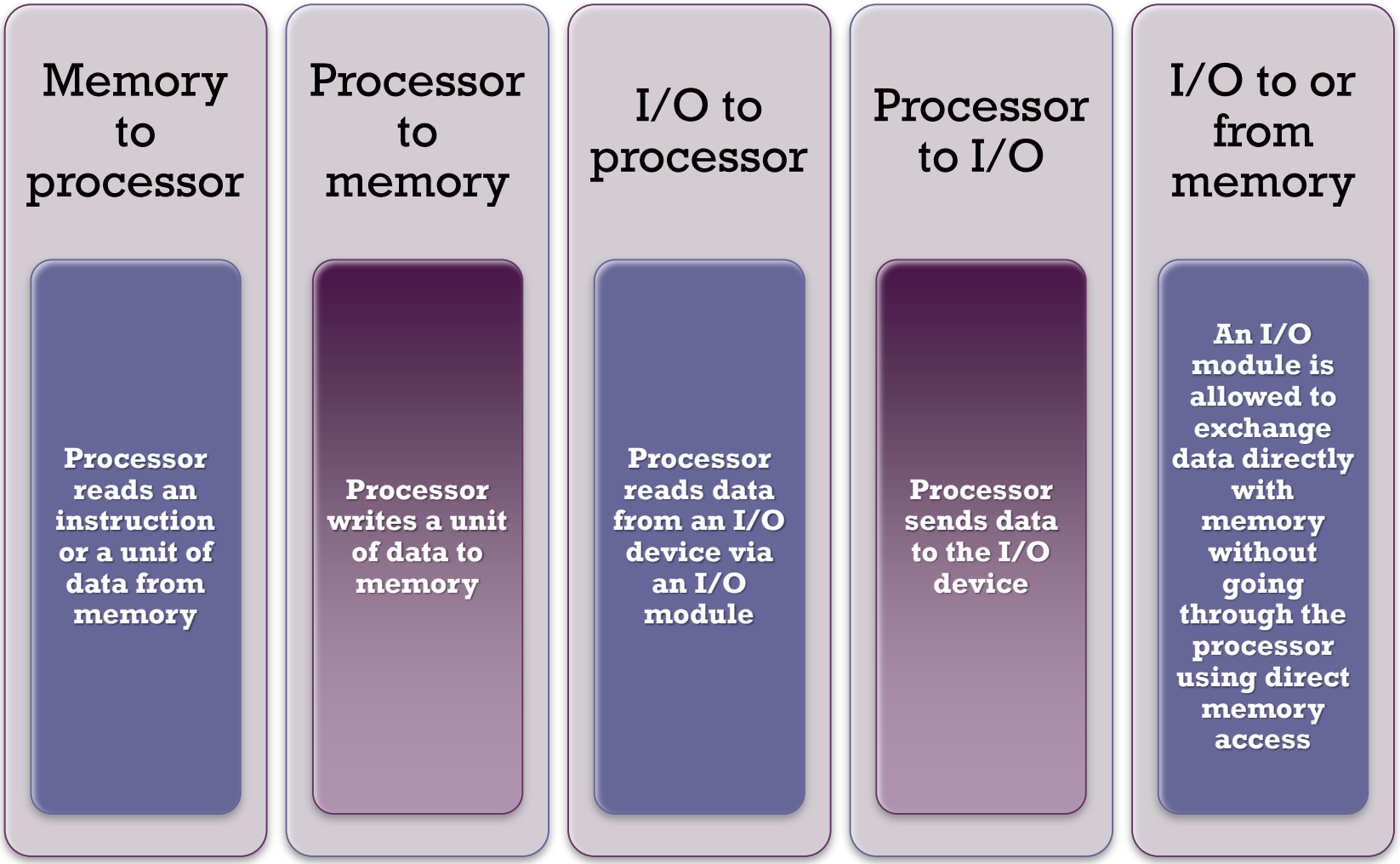
I/O Module

- I/O is functionally similar to memory.
- There are two operations, read and write for the data
- It controls more than one external device.
- We can refer to each of the interfaces to an external device as a port and give each a unique address (e.g., 0,1,...,M-1)
- Also, there are external data paths for the input and output of data with an external device
- It is able to send interrupt signals to the processor

Processor

- The processor reads in instructions and data, writes out data after processing, and uses control signals to control the overall operation of the system
- It also receives interrupt signals

The interconnection structure must support the following types of transfers:



Interconnection Structure

- There is a number of interconnection structures that have been used over the years.

- The most common interconnection structures are:

  1. The bus (various bus structures)
  2. Point-to-point (packetized data transfer)
     - Now the dominant.

Bus Interconnection

Bus is a communication pathway connecting two or more devices

- Key characteristic is that it is a shared transmission medium

Signals transmitted by any one device are available for reception by all other devices attached to the bus

- If two devices transmit during the same time period their signals will overlap and become garbled.

Typically consists of multiple communication lines

- Each line is capable of transmitting signals representing binary 1 and binary 0

Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy

System bus

- A bus that connects major computer components (processor, memory, I/O)

The most common computer interconnection structures are based on the use of one or more system buses

Data Bus

- Data lines that provide a path for moving data among system modules
- May consist of 32, 64, 128, or more separate lines
- The number of lines is referred to as the *width* of the data bus
- The number of lines determines how many bits can be transferred at a time
- The width of the data bus is a key factor in determining overall system performance
- For example, if the data bus is 32 bits wide and each instruction is 64 bits long, then the processor must access the memory module twice during each instruction cycle.

Address Bus

- Used to designate the source or destination of the data on the data bus
  - If the processor wishes to read a word of data from memory it puts the address of the desired word on the address lines
- Width determines the maximum possible memory capacity of the system
- Also used to address I/O ports
  - The higher order bits are used to select a particular module on the bus and the lower order bits select a memory location or I/O port within the module

Control Bus

- Used to control the access and the use of the data and address lines
- Because the data and address lines are shared by all components there must be a means of controlling their use
- Control signals transmit both command and timing information among system modules
- Timing signals indicate the validity of data and address information
- Command signals specify operations to be performed

Control Lines Examples

- **Memory write:** causes data on the bus to be written into the addressed location
- **Memory read:** causes data from the addressed location to be placed on the bus
- **I/O write:** causes data on the bus to be output to the addressed I/O port
- **I/O read:** causes data from the addressed I/O port to be placed on the bus
- **Transfer ACK:** indicates that data have been accepted from or placed on the bus
- **Bus request:** indicates that a module needs to gain control of the bus
- **Bus grant:** indicates that a requesting module has been granted control of the bus
- **Interrupt request:** indicates that an interrupt is pending
- **Interrupt ACK:** acknowledges that the pending interrupt has been recognized
- **Clock:** is used to synchronize operations
- **Reset:** initializes all modules

Figure 3.16

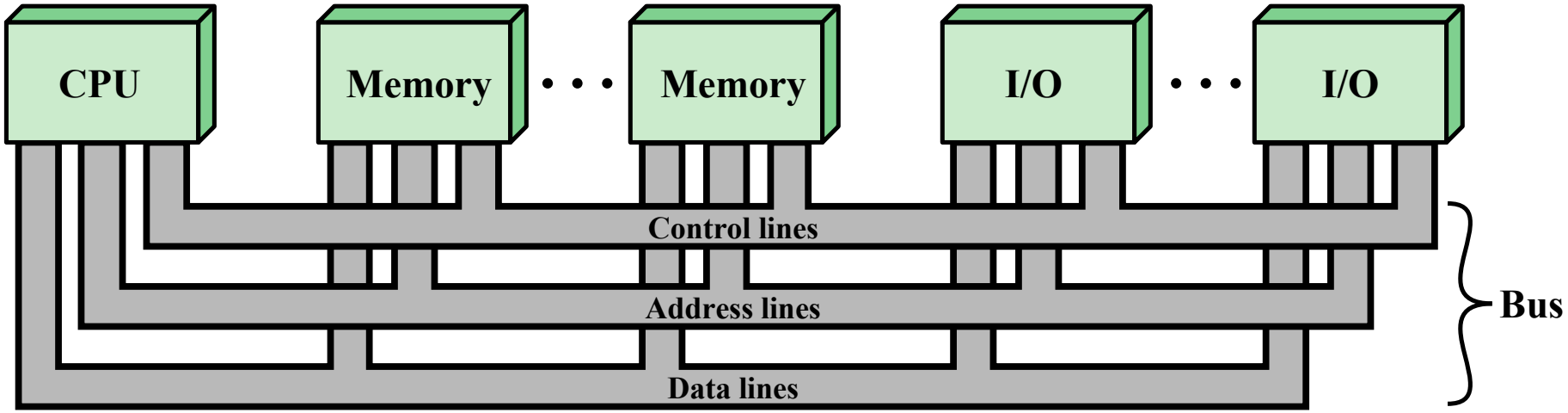
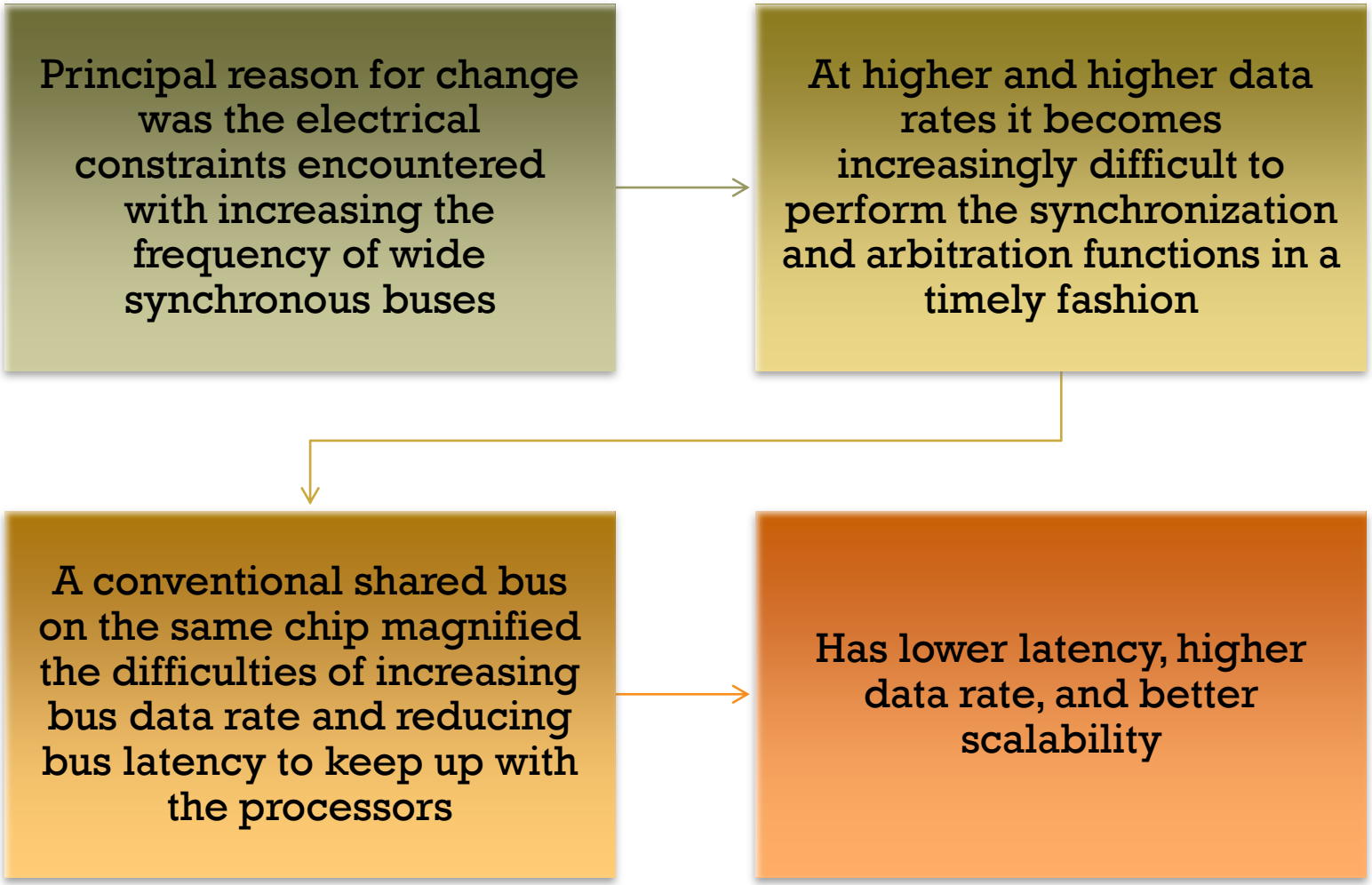


Figure 3.16 Bus Interconnection Scheme

Point-to-Point Interconnect



Quick Path Interconnect

QPI

- Introduced in 2008
- Multiple direct connections
  - Direct pairwise connections to other components eliminating the need for arbitration found in shared transmission systems
- Layered protocol architecture
  - These processor level interconnects use a layered protocol architecture rather than the simple use of control signals found in shared bus arrangements
- Packetized data transfer
  - Data are sent as a sequence of packets each of which includes control headers and error control codes

Figure 3.17

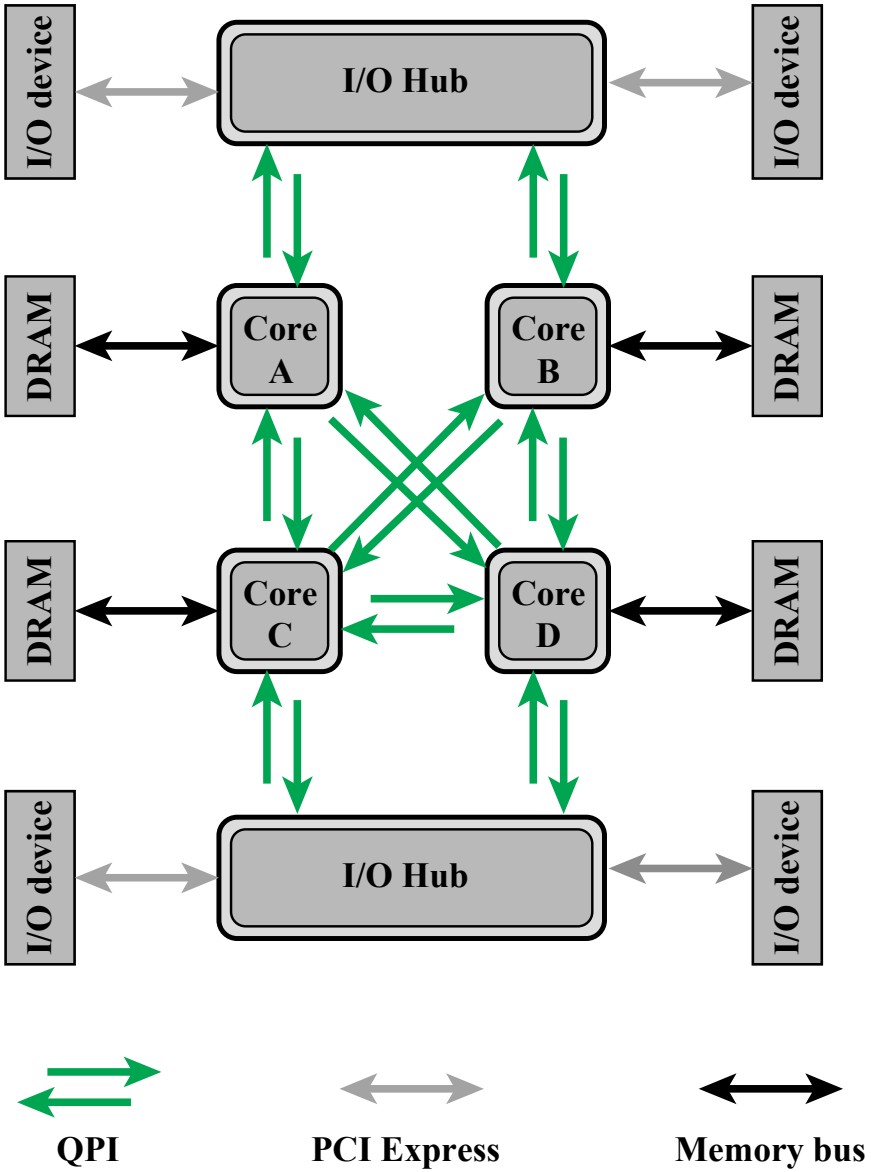


Figure 3.17 Multicore Configuration Using QPI

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