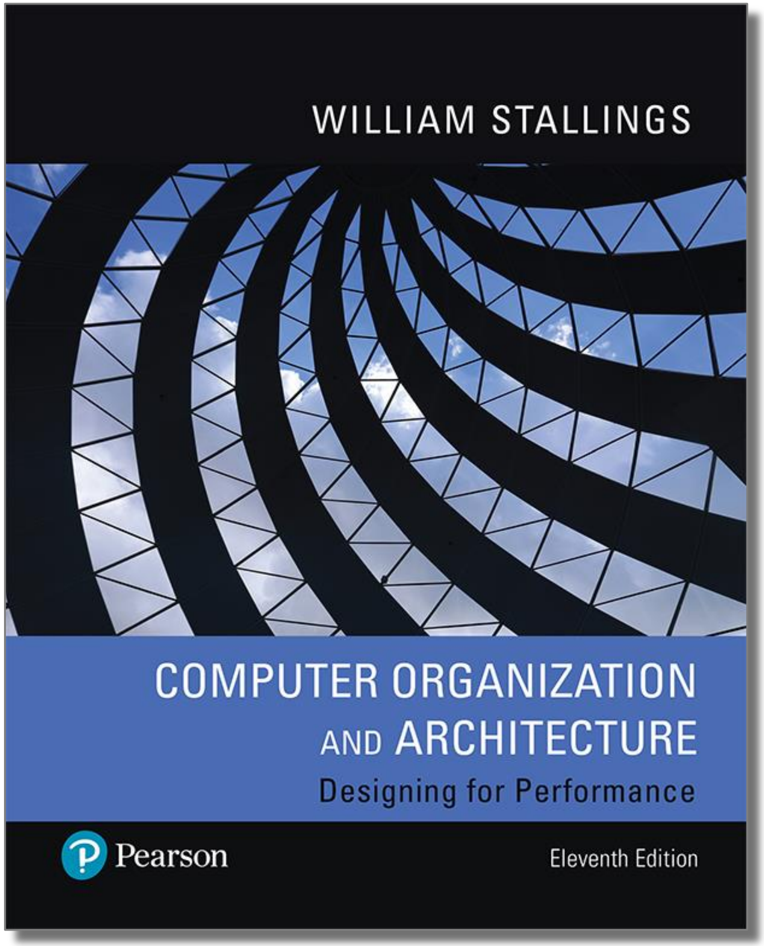
Computer Organization and Architecture

Designing for Performance

11th Edition


WILLIAM STALLINGS
COMPUTER ORGANIZATION AND ARCHITECTURE
Designing for Performance
Pearson
Eleventh Edition

Chapter 14

Instruction Sets: Addressing Modes and Formats

Copyright © 2019, 2016, 2013 Pearson Education, Inc. All Rights Reserved

Instruction Formats

Define the layout of the bits of an instruction, in terms of its constituent fields

Must include an opcode and, implicitly or explicitly, indicate the addressing mode for each operand

For most instruction sets more than one instruction format is used

Pearson

Copyright © 2019, 2016, 2013 Pearson Education, Inc. All Rights Reserved

Instruction Length

- Most basic design issue
- Affects, and is affected by:
  - Memory size
  - Memory organization
  - Bus structure
  - Processor complexity
  - Processor speed
- Should be equal to the memory-transfer length or one should be a multiple of the other
- Should be a multiple of the character length, which is usually 8 bits, and of the length of fixed-point numbers

Pearson

Copyright © 2019, 2016, 2013 Pearson Education, Inc. All Rights Reserved

Allocation of Bits

- Number of addressing modes
- Number of operands
- Register versus memory
- Number of register sets
- Address range
- Address granularity

Pearson

Copyright © 2019, 2016, 2013 Pearson Education, Inc. All Rights Reserved

Allocation of bits

- **Number of addressing modes:** Sometimes an addressing mode can be indicated implicitly. For example, certain opcodes might always call for indexing. In other cases, the addressing modes must be explicit, and one or more mode bits will be needed.
- **Number of operands:** We have seen that fewer addresses can make for longer, more awkward programs. Typical instruction formats on today's machines include two operands. Each operand address in the instruction might require its own mode indicator, or the use of a mode indicator could be limited to just one of the address fields.

Pearson

Copyright © 2019, 2016, 2013 Pearson Education, Inc. All Rights Reserved

Allocation of bits

- **Register versus memory:** The more that registers can be used for operand references, the fewer bits are needed.
- **Number of register sets:** Most contemporary machines have one set of general- purpose registers, with typically 32 or more registers in the set. These registers can be used to store data and can be used to store addresses for displacement addressing.
- **Address range:** Because this imposes a severe limitation, direct addressing is rarely used. With displacement addressing, the range is opened up to the length of the address register

Copyright © 2019, 2016, 2013 Pearson Education, Inc. All Rights Reserved

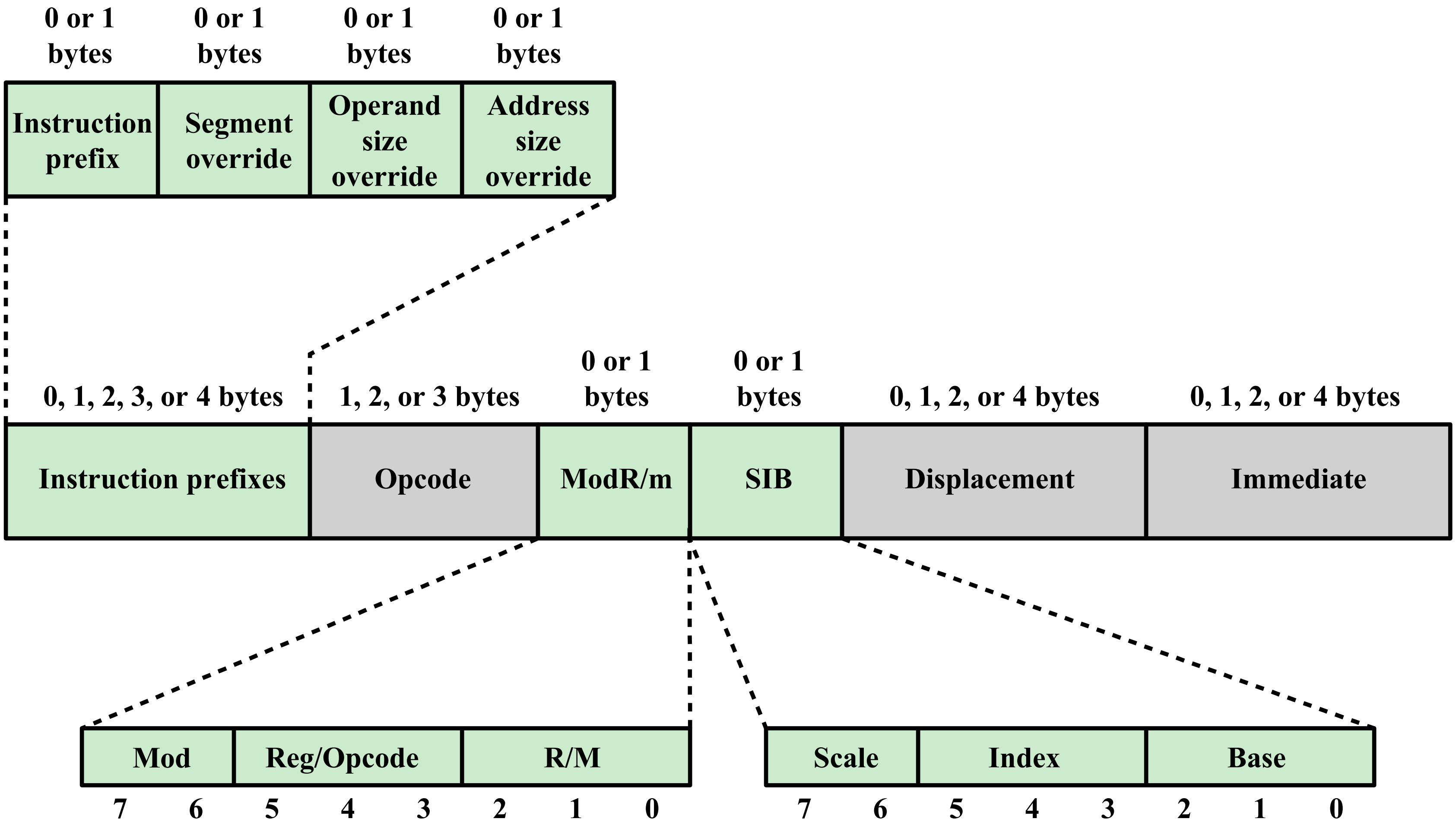
Allocation of bits

- **Address granularity:** In a system with 16- or 32-bit words, an address can reference a word or a byte at the designer’s choice. Byte addressing is convenient for character manipulation but requires, for a fixed-size memory, more address bits.

Pearson

Copyright © 2019, 2016, 2013 Pearson Education, Inc. All Rights Reserved

Figure 14.9
x86 Instruction Format



Copyright © 2019, 2016, 2013 Pearson Education, Inc. All Rights Reserved

x86 Instruction Format

- **Instruction prefixes:** The instruction prefix, if present, consists of the LOCK prefix or one of the repeat prefixes.
  - The LOCK prefix is used to ensure exclusive use of shared memory in multiprocessor environments.
  - The repeat prefixes specify repeated operation of a string, which enables the x86 to process strings much faster than with a regular software loop.
- **Segment override:** Explicitly specifies which segment register an instruction should use, overriding the default segment-register selection generated by the x86 for that instruction.

Pearson

Copyright © 2019, 2016, 2013 Pearson Education, Inc. All Rights Reserved

x86 Instruction Format

- **Operand size:** An instruction has a default operand size of 16 or 32 bits, and the operand prefix switches between 32-bit and 16-bit operands.

- **Address size:** The processor can address memory using either 16- or 32-bit addresses.

Copyright © 2019, 2016, 2013 Pearson Education, Inc. All Rights Reserved

x86 Instruction Format

- **Opcode:** The opcode field is 1, 2, or 3 bytes in length.
- **ModR/M:** This byte, and the next, provide addressing information.
- The ModR/M byte specifies whether an operand is in a register or in memory; if it is in memory, then fields within the byte specify the addressing mode to be used.
- The ModR/M byte consists of three fields:
  - The Mod field (2 bits) combines with the R/M field to form 32 possible values: 8 registers and 24 indexing modes;
  - the Reg/Opcode field (3 bits) specifies either a register number or three more bits of opcode information; the R/M field (3 bits) can specify a register as the location of an operand.

Pearson

Copyright © 2019, 2016, 2013 Pearson Education, Inc. All Rights Reserved

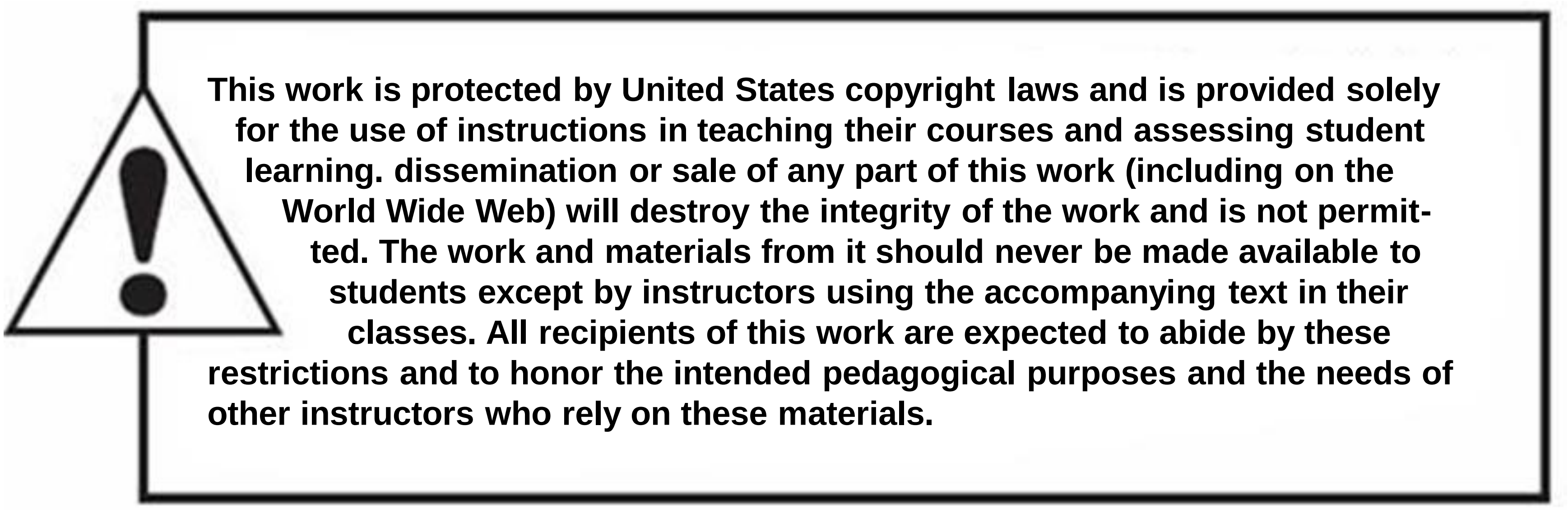
x86 Instruction Format

- **SIB:** Certain encoding of the ModR/M byte specifies the inclusion of the SIB byte to specify fully the addressing mode. The SIB byte consists of three fields:
  - The Scale field (2 bits) specifies the scale factor for scaled indexing;
  - the Index field (3 bits) specifies the index register;
  - the Base field (3 bits) specifies the base register.
- **Displacement:** When the addressing-mode specifier indicates that a displacement is used, an 8-, 16-, or 32-bit signed integer displacement field is added.
- **Immediate:** Provides the value of an 8-, 16-, or 32-bit operand.

Pearson

Copyright © 2019, 2016, 2013 Pearson Education, Inc. All Rights Reserved

Copyright



This work is protected by United States copyright laws and is provided solely for the use of instructions in teaching their courses and assessing student learning. dissemination or sale of any part of this work (including on the World Wide Web) will destroy the integrity of the work and is not permitted. The work and materials from it should never be made available to students except by instructors using the accompanying text in their classes. All recipients of this work are expected to abide by these restrictions and to honor the intended pedagogical purposes and the needs of other instructors who rely on these materials.