שפת תכנון חומרה
ורילוג - Verilog

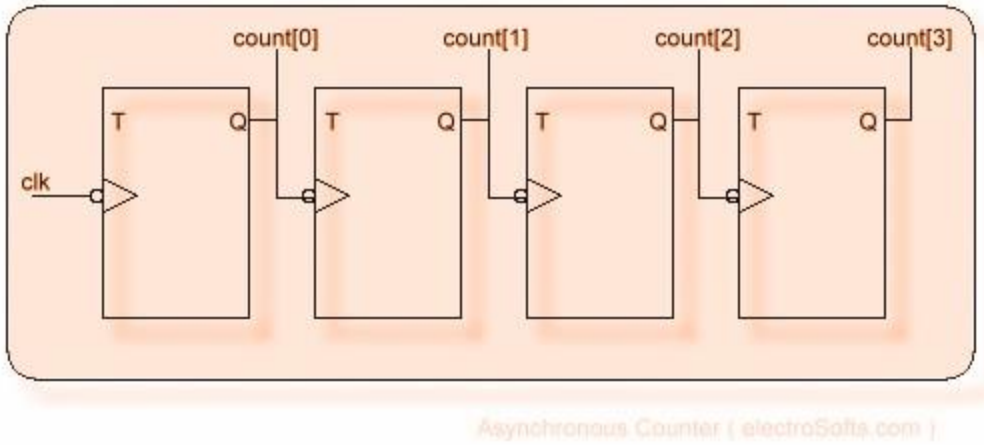
Verilog – Asynchronous Modules

Dr. Avihai Aharon

Asynchronous Counter

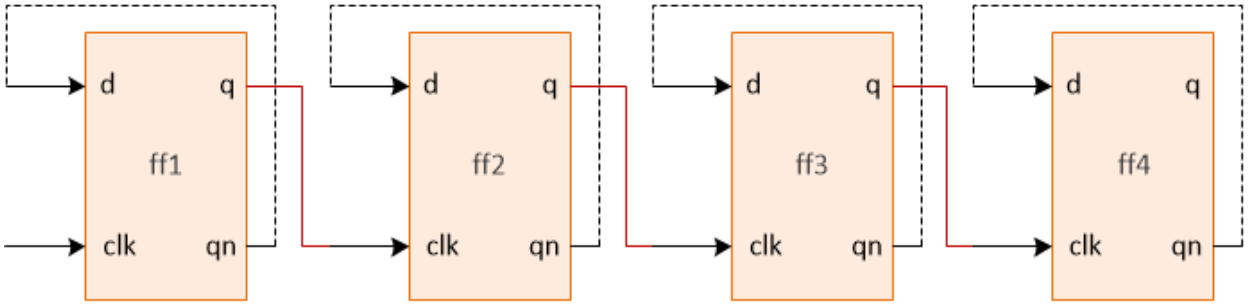
- 4-bit asynchronous counter; Ripple counter. This is a simple counter without reset or load options.

```
module counter( clk, count );
input clk;
output[3:0] count;

reg[3:0] count;
wire clk;
initial
        count = 4'b0;

always @( negedge clk )
        count[0] <= ~count[0];

always @( negedge count[0] )
        count[1] <= ~count[1];

always @( negedge count[1] )
        count[2] <= ~count[2];

always @( negedge count[2] )
        count[3] <= ~count[3];
endmodule
```



Asynchronous Counter

```
module ripple ( input clk,
                input rstn,
                output [3:0] out);
   wire  q0;
   wire  qn0;
   wire  q1;
   wire  qn1;
   wire  q2;
   wire  qn2;
   wire  q3;
   wire  qn3;

   dff   dff0 ( .d (qn0),
                .clk (clk),
                .rstn (rstn),
                .q (q0),
                .qn (qn0));

   dff   dff1 ( .d (qn1),
                .clk (q0),
                .rstn (rstn),
                .q (q1),
                .qn (qn1));
   dff   dff2 ( .d (qn2),
                .clk (q1),
                .rstn (rstn),
                .q (q2),
                .qn (qn2));
   dff   dff3 ( .d (qn3),
                .clk (q2),
                .rstn (rstn),
                .q (q3),
                .qn (qn3));
   assign out = {qn3, qn2, qn1, qn0};
endmodule
```

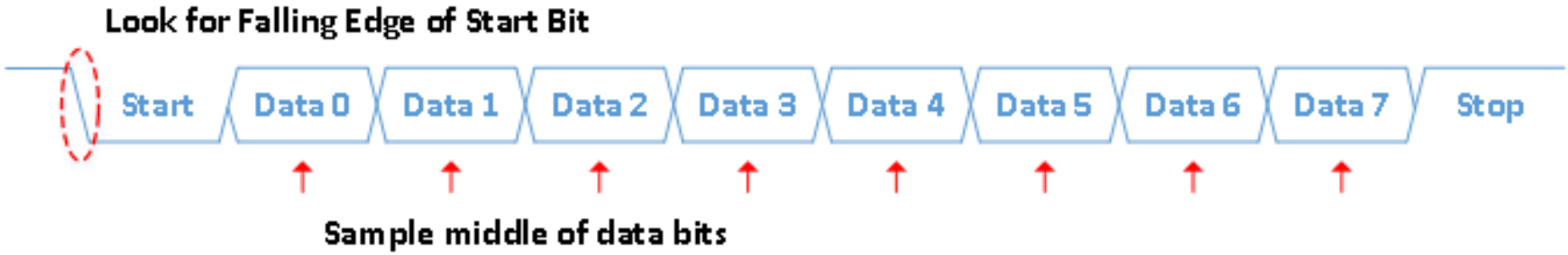



```
module dff (input d,
                input clk,
                input rstn,
                output reg q,
                output qn);
   always @ (posedge clk or negedge rstn)
      if (!rstn)
         q <= 0;
      else
         q <= d;

   assign qn = ~q;
endmodule
```

UART (Universal Asynchronous Receiver Transmitter)

UART, Serial Port, RS-232 Interface

UART Serial Data Stream:



The baud rate is the rate at which the data is transmitted. For example, 9600 baud means 9600 bits per second.

UART parameters:

```
Baud Rate            (9600, 19200, 115200, others)
Number of Data Bits  (7, 8)
Parity Bit           (On, Off)
Stop Bits            (0, 1, 2)
```