CS-683 Project checkpoint II

Improving IPCP with Irregular Access Support using ISB

Sm Arif Ali, Soumik Dutta
Team Gandiva
23m0822@iitb.ac.in, 23m0826@iitb.ac.in

Problem statement

- Instruction Pointer Classifier-based Prefetcher (IPCP) handles regular patterns but falls short for irregular memory accesses.
- Need for efficient handling of irregular access patterns for applications like graph processing.
- An example access pattern involving *temporal locality* can be seen below:

A B C X Y X Y X Y A B C X Y ..

Where these are memory address accesses

Prior Works

- Bouquet of Instruction Pointers (ISCA ‘20): Established IPCP, categorizing regular memory access patterns.

- Linearizing Irregular Accesses (MICRO ‘13): Introduced Irregular Stream Buffer (ISB) to address irregular accesses.

First IP prefetcher: Constant stride

Second IP prefetcher: Complex stride

Third IP prefetcher: Global stream

Fourth prefetcher: Next-line

Temporal Stream:

A B C X Y X Y X Y *A* B C

GHB
A
B
C
X
Y
X
Y
X
Y
A

(a) GHB

Physical Address	Structural Address
A	19
B	20
C	21
X	22
Y	23

(b) ISB

Figure 1: Metadata for GHB (left) and ISB (right).

Image ref- fig1: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8980330;
fig2: https://dpc3.compas.cs.stonybrook.edu/slides/bouquet.pdf

Goal of the Project

- Integrate ISB into IPCP framework to create a new Irregular Access (IA) class.
- Improve prefetching for workloads with irregular memory access patterns.

First IP prefetcher: Constant stride

Second IP prefetcher: Complex stride

Third IP prefetcher: Global stream

ISB prefetcher: temporal stream

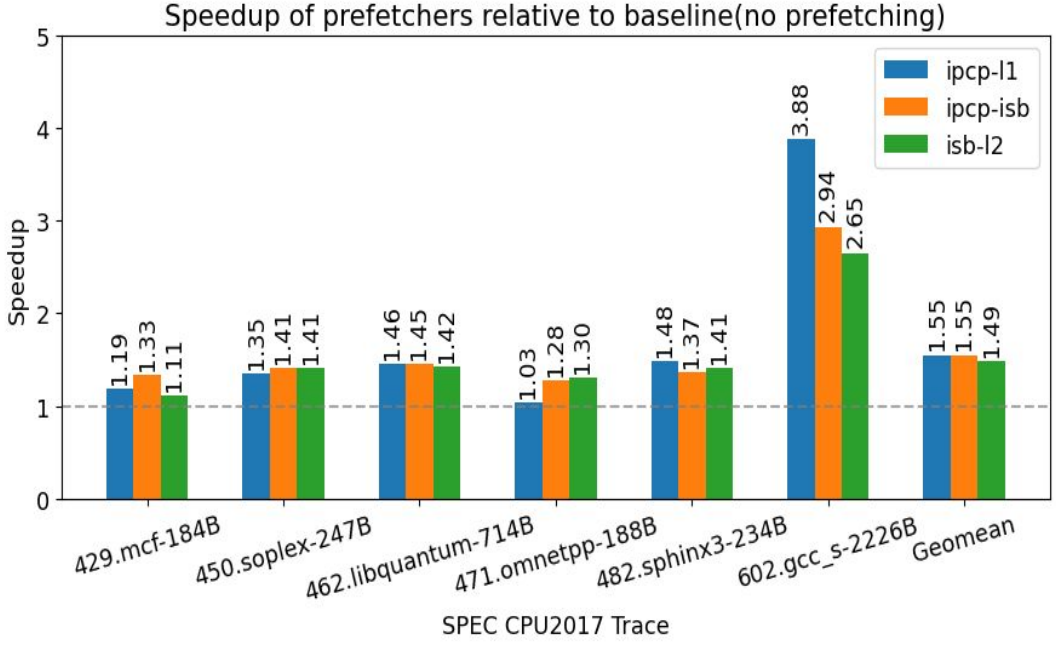
Fourth prefetcher: Next-line

Work done @checkpoint I

- Integrated IPCP and ISB separately in ChampSim.
- Configured and executed GAP and SPEC-CPU benchmarks separately.
- Initial integration of ISB within the IPCP framework completed, with early tests results.

Initial Test Results with SPEC-CPU17 @checkpoint I

- Combined IPCP-ISB shows comparable performance to individual IPCP and ISB.
- No significant performance gain observed, but no degradation either.



Plan for checkpoint-II

- Use confidence counter to influence prefetch decision in ISB - Soumik
- Adapt prefetch degree in ISB based on accuracy. - Soumik
- Share the IPCP IP-Table with ISB - Arif
- Adjust ISB parameters: lookahead distance, buffer size, and stream length - Arif
- Refine classification logic for the new Irregular Access(IA) class - brainstorming together

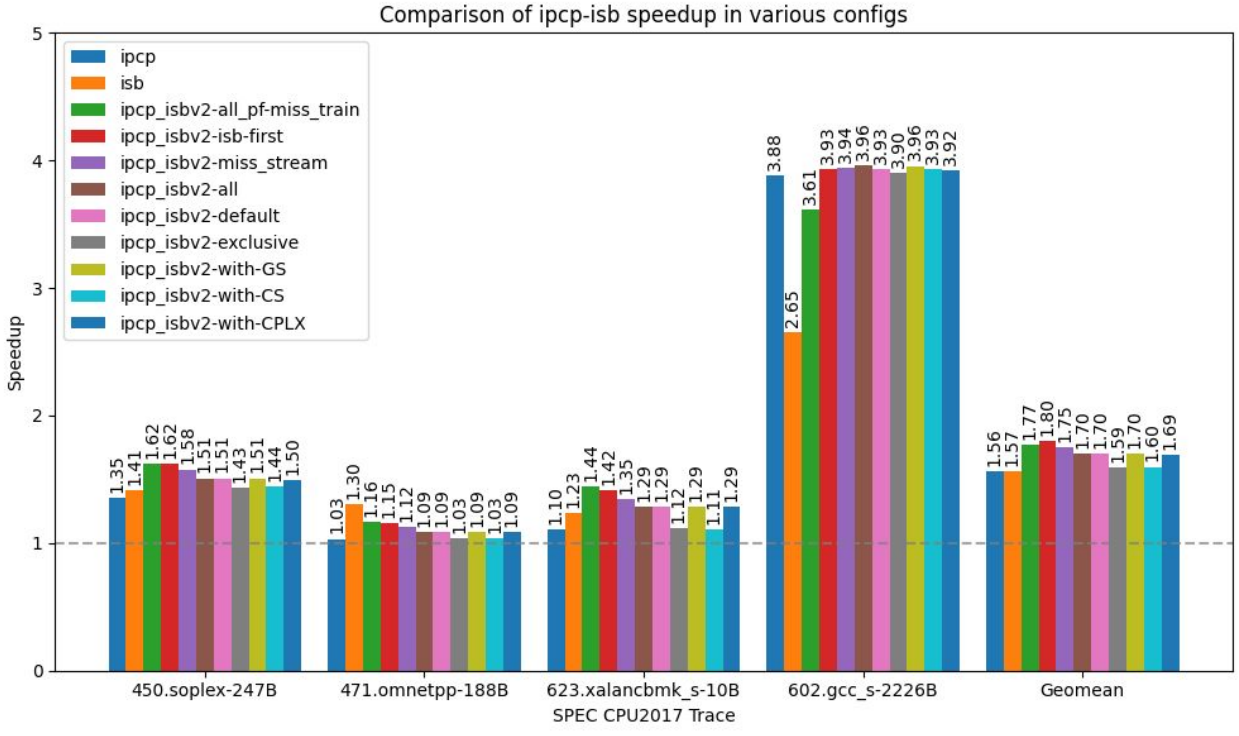
Work done @checkpoint-II

- Tested with implementation of Confidence counter to influence prefetch decision in ISB - found not beneficial.
- Integrated accuracy based prefetch degree adaption technique into ISB
- Tested by sharing the IPCP IP-Table with ISB to keep metadata - found not beneficial
- Refined classification logic for Irregular Access(IA) class

Simulator and configuration @checkpoint-II

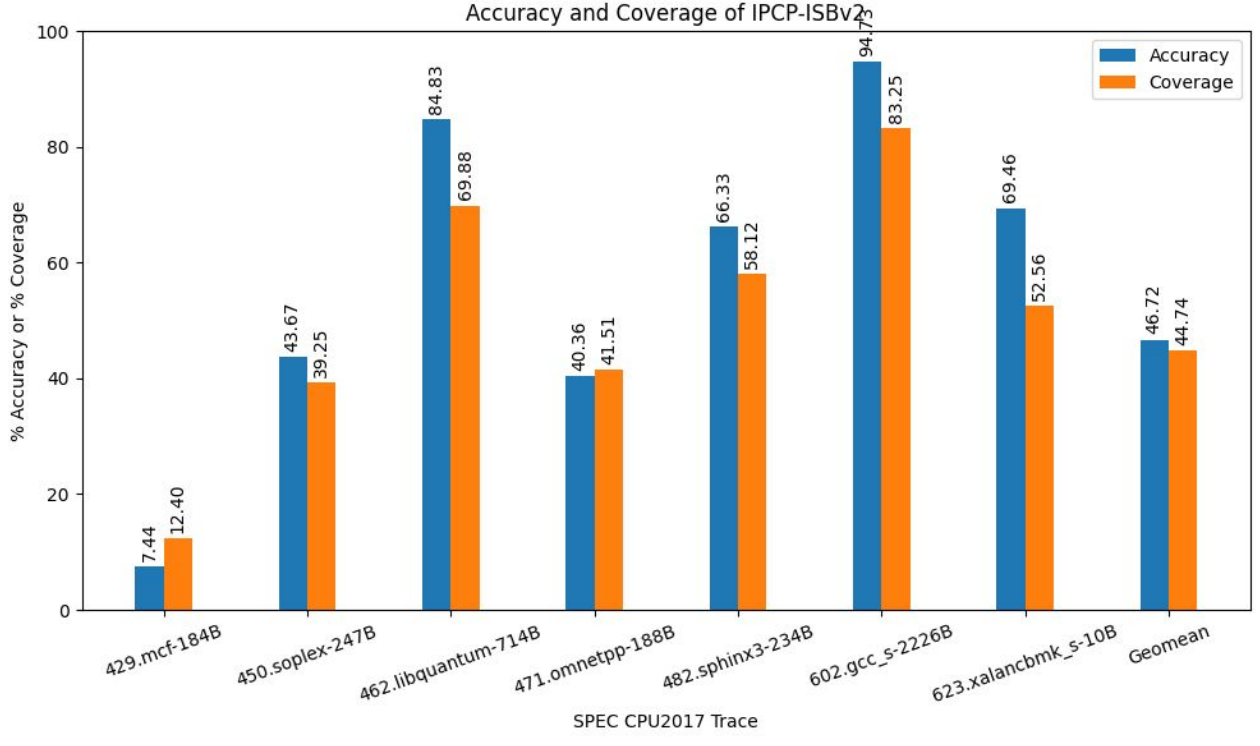
- Core Configuration
  - 1 core
  - 4 GHz
  - 4-wide 256-entry ROB
- TLBs
  - ITLB: 64 entries
  - DTLB: 64 entries
  - Shared L2 TLB: 1536 entries
- DRAM
  - 4GB
  - 1 channel/core
  - 6400 MT/sec
- Cache Hierarchy
  - L1 I: 32KB, 8-way, 3 cycles, PQ: 8, MSHR: 8
  - L1 D: 48KB, 12-way, 5 cycles, PQ: 8, MSHR: 16
  - L2: 512KB, 8-way, 10 cycles, PQ: 16, MSHR: 32
  - LLC: 2MB/core, 16-way, 20 cycles, PQ: 32/cores, MSHR: 64 /core
- Simulation details
  - Simulation Instructions: 50M
  - Warmup Instructions: 50M

Benchmark: SPEC-CPU17 @checkpoint-II



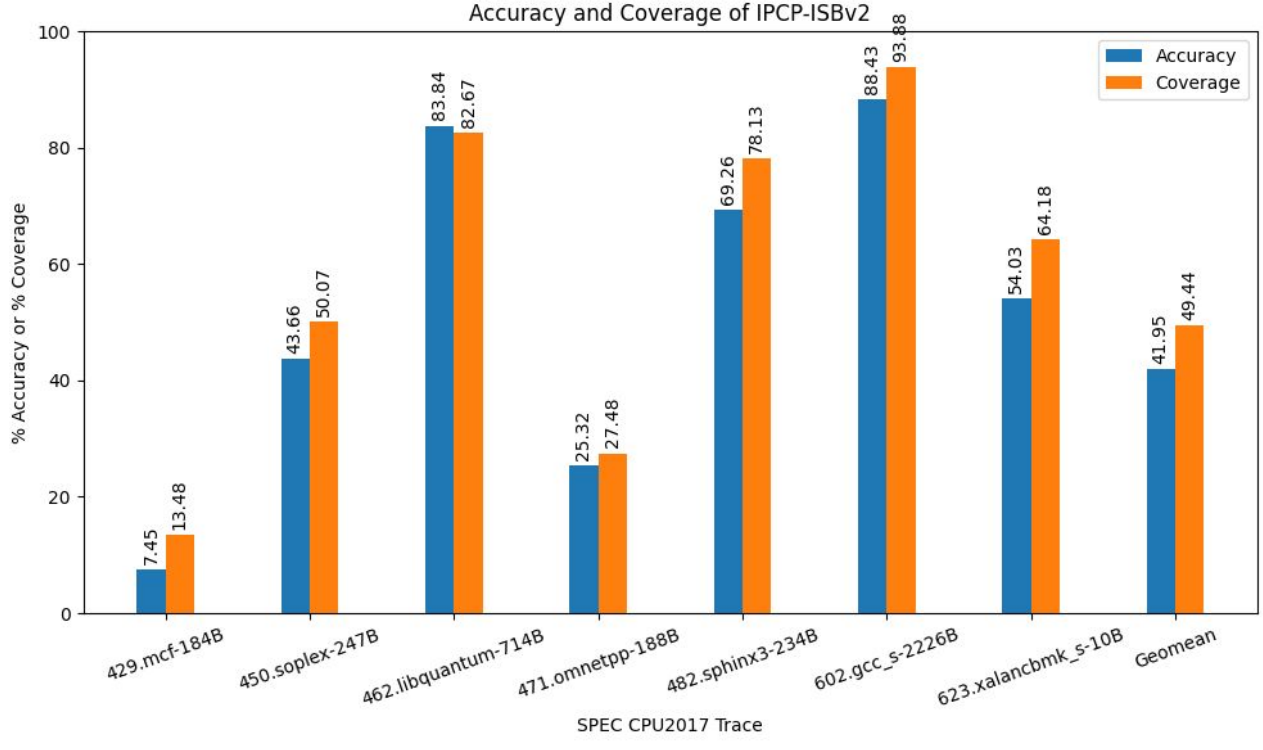
- Evaluated multiple configurations for combining ISB .
- ISB-first configuration is the best found so far.

Benchmark: SPEC-CPU17 @checkpoint-II



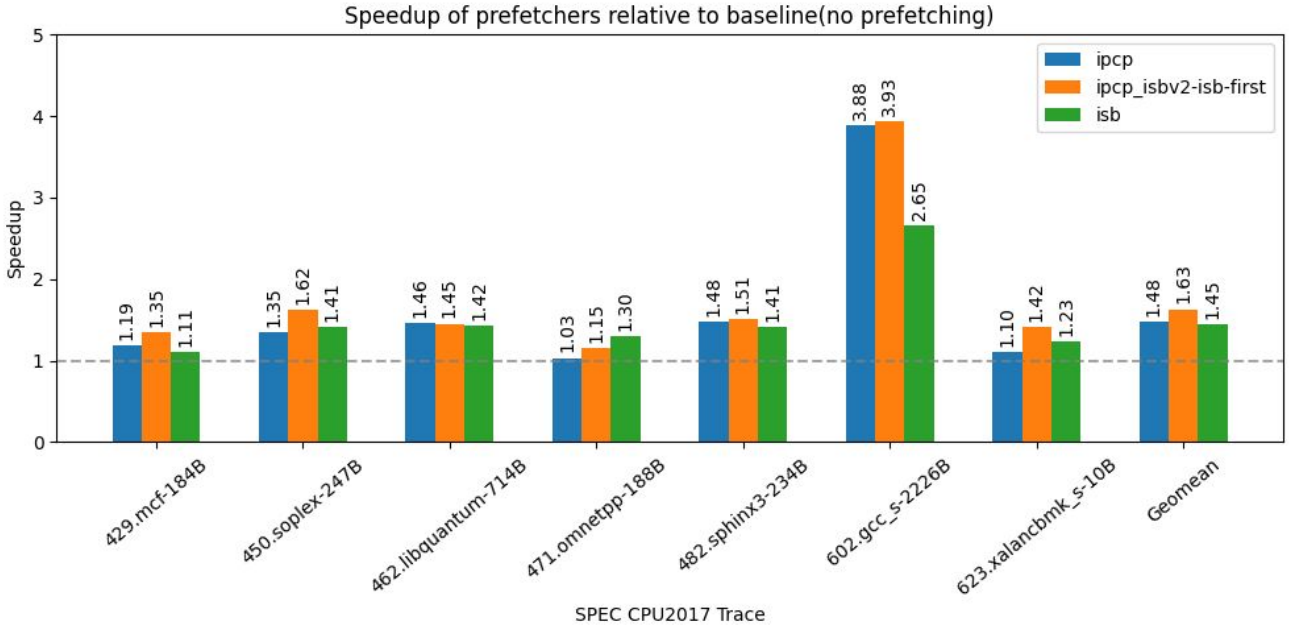
- Evaluated accuracy and coverage of the existing combined prefetcher(v1)

Benchmark: SPEC-CPU17 @checkpoint-II



- Evaluated accuracy and coverage of the improved combined prefetcher(v2)

Benchmark: SPEC-CPU17 @checkpoint-II



- Performance on gcc is improved, but omnetpp is reduced.
- Gained 15% and 18% more speedup over IPCP and ISB on average.

Plan for Final submission

- Adjust ISB parameters: lookahead distance, buffer size, and stream length - Soumik
- Evaluate per class contribution in the combined prefetcher- Arif
- Further refine classification logic by evaluating more configurations - together
- Performing benchmarks on more spec-cpu traces - together
- Final take on optimal IPCP class design with ISB - together

Insights and results

- Performance on gcc is increased due to proper incorporation of both prefetchers
- On Omnetpp combined prefetcher isn’t able to reach ISB’s performance due to modified training in combined prefetcher.

Github link

- https://github.com/ArifAli-0/CS683-Project.git

Video link

- Checkpoint1: https://youtu.be/JrZYAXMjjzY
- Checkpoint2: https://youtu.be/AmGMXzYUihc