Project 2, ECE 521 – Digital ASIC Design

Name: Arijit Sengupta, ID: 001441748

PART A & B

Truth Table of 8:3 Priority Encoder:

Input								Output			
I7	**I6**	**I5**	**I4**	**I3**	**I2**	**I1**	**I0**	**P2**	**P1**	**P0**	**V**
0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	1	X	0	0	1	1
0	0	0	0	0	1	X	X	0	1	0	1
0	0	0	0	1	X	X	X	0	1	1	1
0	0	0	1	X	X	X	X	1	0	0	1
0	0	1	X	X	X	X	X	1	0	1	1
0	1	X	X	X	X	X	X	1	1	0	1
1	X	X	X	X	X	X	X	1	1	1	1

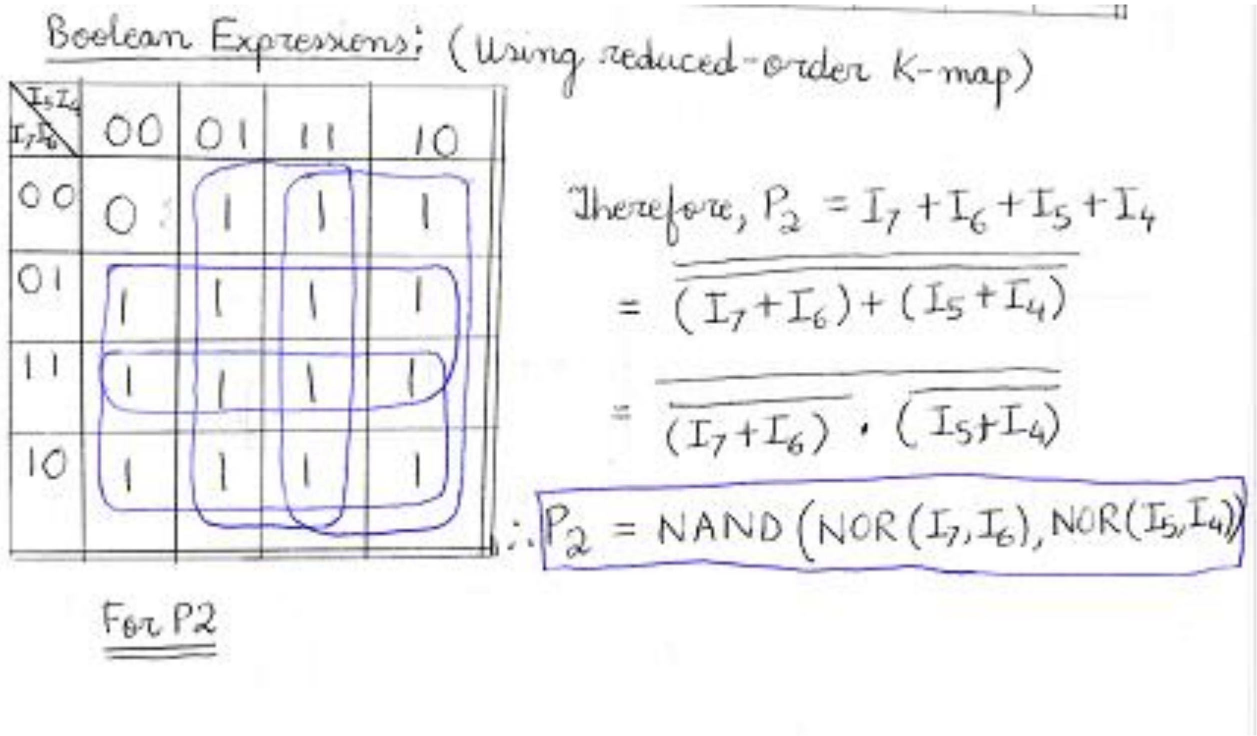
Boolean Expressions:

P0 = I7 + I7’I6’I5 + I6’I5’I4’I3 + I6’I5’I4’I3’I2’I1

P1 = I7 + I6 + I6’I5’I4’I3 + I6’I5’I4’I2

P2 = I7 + I6 + I5 + I4

Simplified Boolean Expressions for P0, P1 and P2:



Boolean Expressions: (Using reduced-order K-map)

I_7I_6 \ I_5I_4	00	01	11	10
00	0	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

For P2

Therefore, $P_2 = I_7 + I_6 + I_5 + I_4$

$$= \overline{\overline{(I_7+I_6)+(I_5+I_4)}}$$

$$= \overline{\overline{(I_7+I_6)} \cdot \overline{(I_5+I_4)}}$$

$$\therefore \boxed{P_2 = NAND(NOR(I_7,I_6), NOR(I_5,I_4))}$$

For P1:

$I_7I_6I_5$ \ $I_4I_3I_2$	000	001	011	010	110	111	110	100
000	0	1	1	1	0	0	0	0
001	0	0	0	0	0	0	0	0
011	1	1	1	1	1	1	1	1
010	1	1	1	1	1	1	1	1
110	1	1	1	1	1	1	1	1
111	1	1	1	1	1	1	1	1
101	1	1	1	1	1	1	1	1
100	1	1	1	1	1	1	1	1

Therefore, $P_1 = I_7 + I_6 + I_6' I_5' I_4' I_3 + I_6' I_5' I_4' I_2$

$$= (I_7 + I_6) + I_6' I_5' I_4' (I_3 + I_2)$$

~~= NOT (AOI (I_7+I_6)~~

$$= \overline{I_7' \cdot I_6'} + \overline{(I_6 + I_5 + I_4)} \cdot \overline{I_3' \cdot I_2'}$$

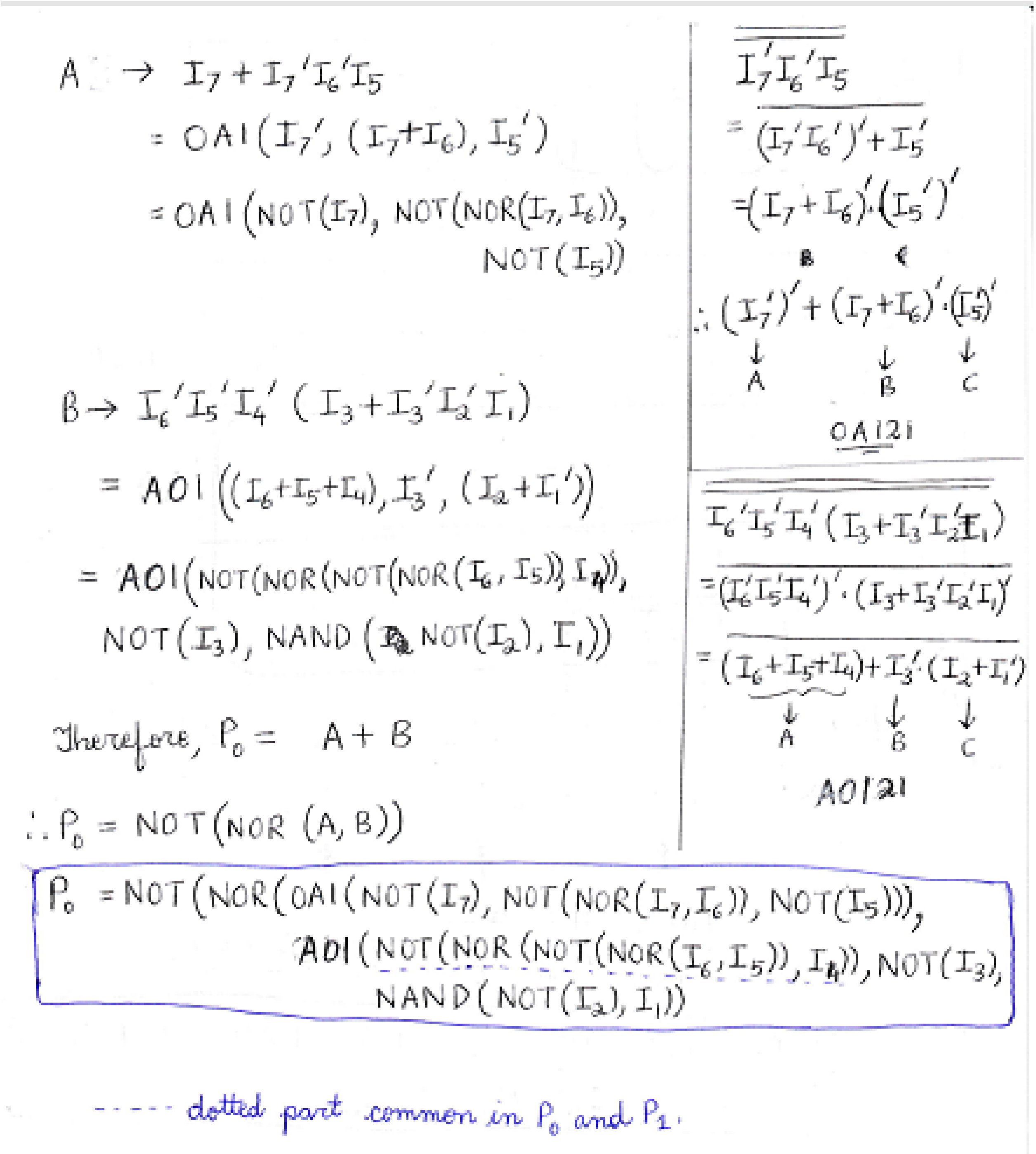
$$\therefore \boxed{P_1 = \text{OAI}\left(\text{NOR}(I_7, I_6), \text{NOT}(\text{NOR}(\text{NOT}(\text{NOR}(I_6, I_5)), I_4)), \text{NOR}(I_3, I_2)\right)}$$

For P0:

$I_7I_6I_5I_4$ \ $I_3I_2I_1$	000	001	011	010	110	111	101	100
0000	0	1	0	0	1	1	1	1
0001	0	0	0	0	0	0	0	0
0011	1	1	1	1	1	1	1	1
0010	1	1	1	1	1	1	1	1
0110	0	0	0	0	0	0	0	0
0111	0	0	0	0	0	0	0	0
0101	0	0	0	0	0	0	0	0
0100	0	0	0	0	0	0	0	0
1100	1	1	1	1	1	1	1	1
1101	1	1	1	1	1	1	1	1
1111	1	1	1	1	1	1	1	1
1110	1	1	1	1	1	1	1	1
1010	1	1	1	1	1	1	1	1
1011	1	1	1	1	1	1	1	1
1001	1	1	1	1	1	1	1	1
1000	1	1	1	1	1	1	1	1

Therefore, $P_0 = I_7 + I_7'I_6'I_5 + I_6'I_5'I_4'I_3 + I_6'I_5'I_4'I_3'I_2'I_1$

$$= \underbrace{I_7 + I_7'I_6'I_5}_{A} + \underbrace{I_6'I_5'I_4'\,(I_3 + I_3'I_2'I_1)}_{B}$$



$A \rightarrow I_7 + I_7' I_6' I_5$

$= OAI(I_7', (I_7+I_6), I_5')$

$= OAI(NOT(I_7), NOT(NOR(I_7, I_6)),$
$NOT(I_5))$

$\overline{\overline{I_7' I_6' I_5}}$

$= \overline{(I_7' I_6')' + I_5'}$

$= (I_7 + I_6)' \cdot (I_5')'$

B C

$\therefore \underset{\substack{\downarrow \\ A}}{(I_7')'} + \underset{\substack{\downarrow \\ B}}{(I_7+I_6)'} \cdot \underset{\substack{\downarrow \\ C}}{(I_5)'}$

OAI21

$B \rightarrow I_6' I_5' I_4' (I_3 + I_3' I_2' I_1)$

$= AOI((I_6+I_5+I_4), I_3', (I_2+I_1'))$

$= AOI(NOT(NOR(NOT(NOR(I_6, I_5)), I_4)),$
$NOT(I_3), NAND(NOT(I_2), I_1))$

$\overline{\overline{I_6' I_5' I_4' (I_3 + I_3' I_2' I_1)}}$

$= \overline{(I_6' I_5' I_4')' \cdot (I_3 + I_3' I_2' I_1)'}$

$= \overline{\underset{\substack{\downarrow \\ A}}{\underbrace{(I_6+I_5+I_4)}} + \underset{\substack{\downarrow \\ B}}{I_3'} \cdot \underset{\substack{\downarrow \\ C}}{(I_2+I_1')}}$

AOI21

Therefore, $P_0 = A + B$

$\therefore P_0 = NOT(NOR(A, B))$

$$\boxed{\begin{aligned} P_0 = NOT(NOR(&OAI(NOT(I_7), NOT(NOR(I_7, I_6)), NOT(I_5))), \\ &AOI(NOT(NOR(NOT(NOR(I_6, I_5)), I_4)), NOT(I_3), \\ &NAND(NOT(I_2), I_1)) \end{aligned}}$$

- - - - dotted part common in P_0 and P_1.

Bill of Materials (BOM):

INVX2 - 8

NAND2X1 – 2

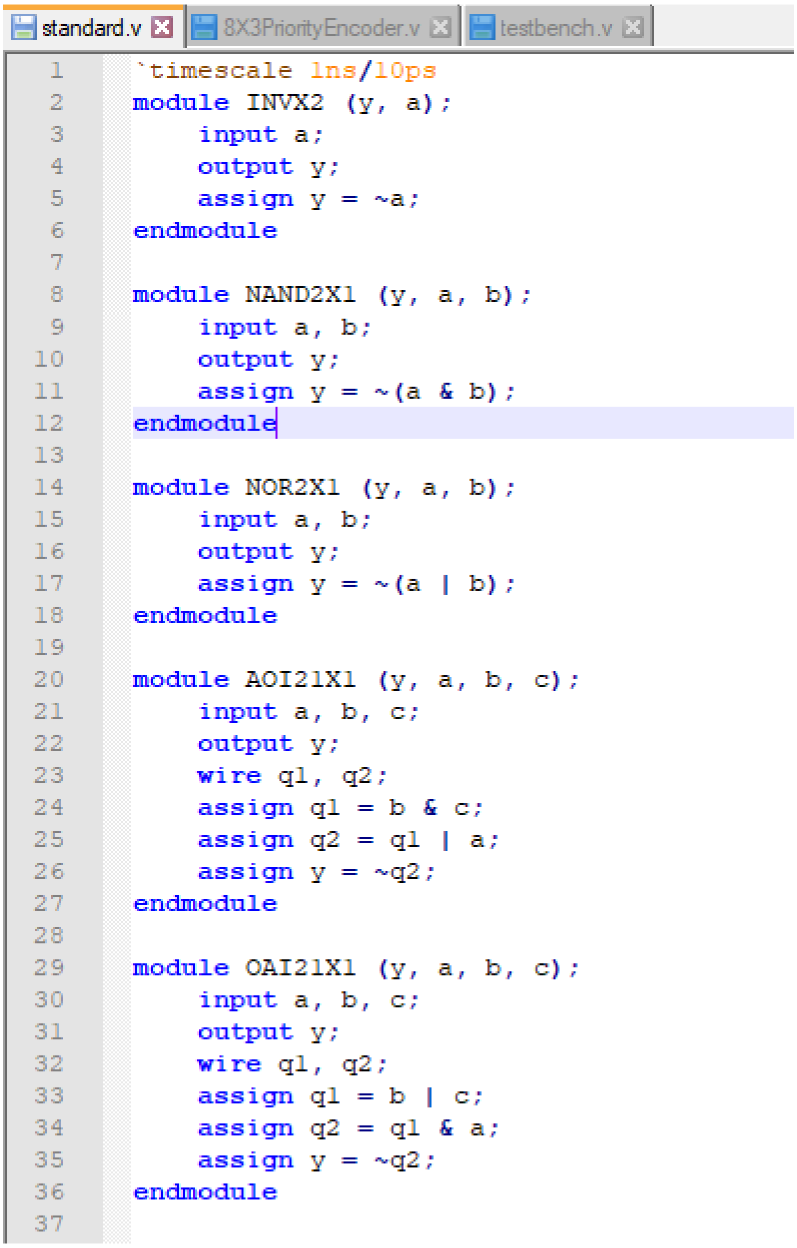
NOR2X1 – 6

AOI21X1 - 1

OAI21X1 – 2

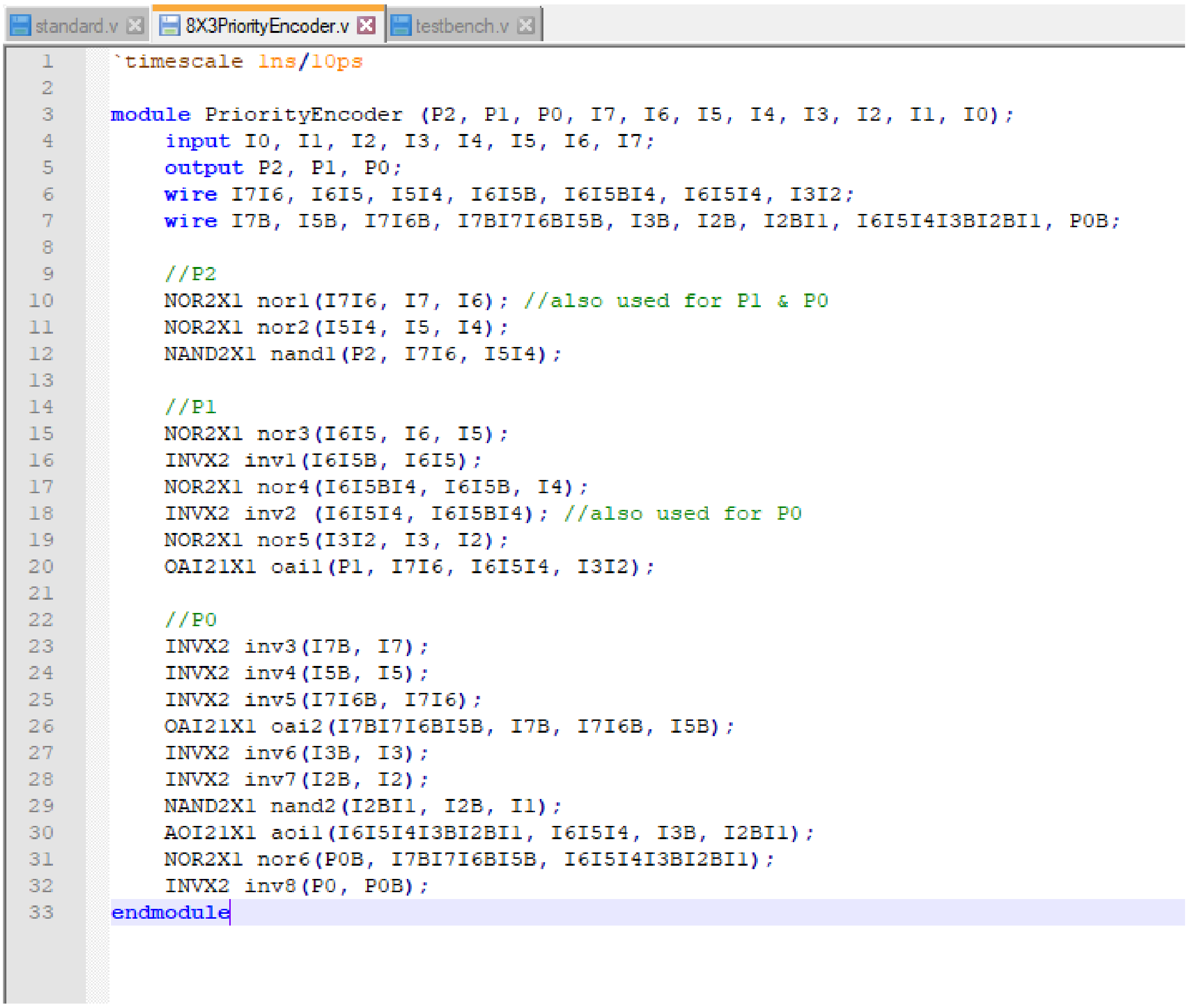
PART C

Verilog Codes:



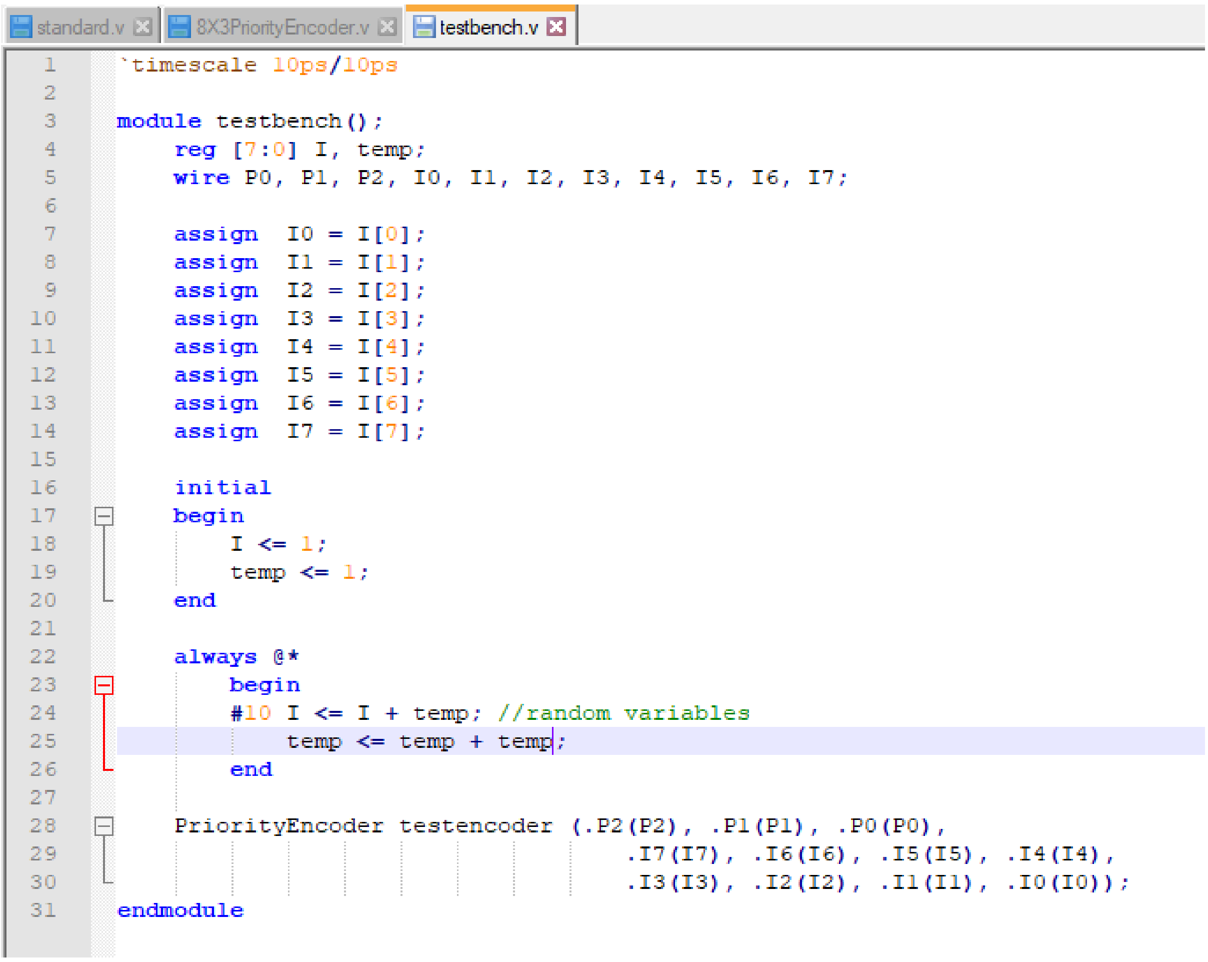
```
`timescale 1ns/10ps
module INVX2 (y, a);
    input a;
    output y;
    assign y = ~a;
endmodule

module NAND2X1 (y, a, b);
    input a, b;
    output y;
    assign y = ~(a & b);
endmodule

module NOR2X1 (y, a, b);
    input a, b;
    output y;
    assign y = ~(a | b);
endmodule

module AOI21X1 (y, a, b, c);
    input a, b, c;
    output y;
    wire q1, q2;
    assign q1 = b & c;
    assign q2 = q1 | a;
    assign y = ~q2;
endmodule

module OAI21X1 (y, a, b, c);
    input a, b, c;
    output y;
    wire q1, q2;
    assign q1 = b | c;
    assign q2 = q1 & a;
    assign y = ~q2;
endmodule
```

standard.v



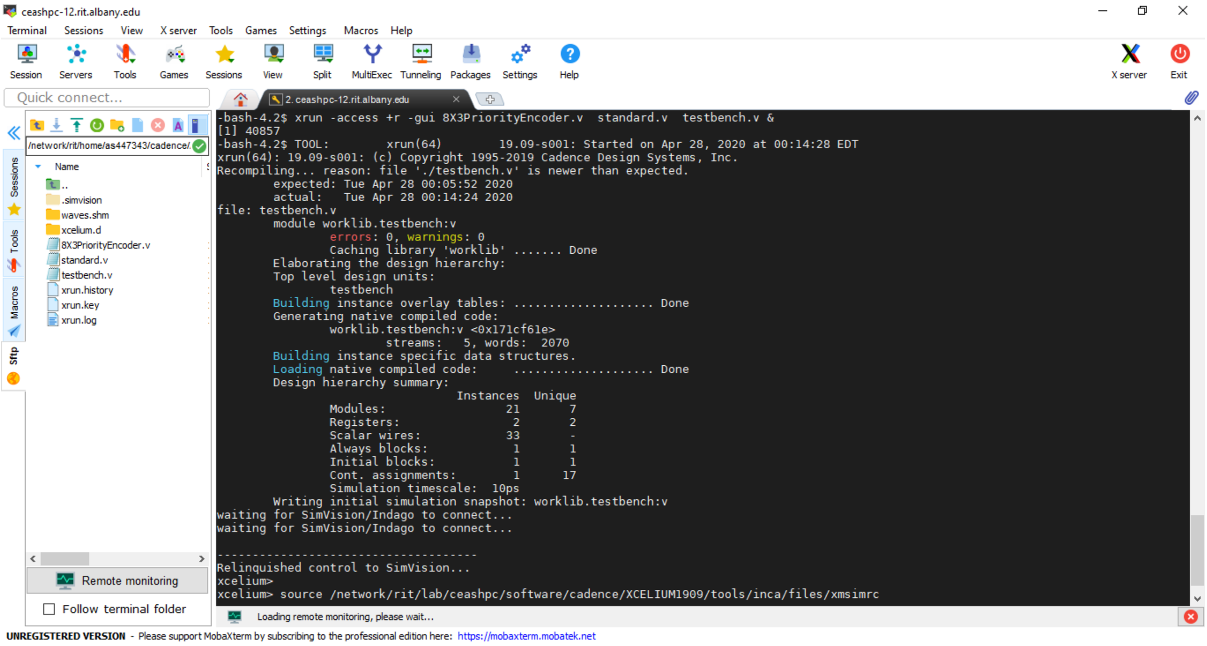
```verilog
`timescale 1ns/10ps

module PriorityEncoder (P2, P1, P0, I7, I6, I5, I4, I3, I2, I1, I0);
    input I0, I1, I2, I3, I4, I5, I6, I7;
    output P2, P1, P0;
    wire I7I6, I6I5, I5I4, I6I5B, I6I5BI4, I6I5I4, I3I2;
    wire I7B, I5B, I7I6B, I7BI7I6BI5B, I3B, I2B, I2BI1, I6I5I4I3BI2BI1, P0B;

    //P2
    NOR2X1 nor1(I7I6, I7, I6); //also used for P1 & P0
    NOR2X1 nor2(I5I4, I5, I4);
    NAND2X1 nand1(P2, I7I6, I5I4);

    //P1
    NOR2X1 nor3(I6I5, I6, I5);
    INVX2 inv1(I6I5B, I6I5);
    NOR2X1 nor4(I6I5BI4, I6I5B, I4);
    INVX2 inv2 (I6I5I4, I6I5BI4); //also used for P0
    NOR2X1 nor5(I3I2, I3, I2);
    OAI21X1 oai1(P1, I7I6, I6I5I4, I3I2);

    //P0
    INVX2 inv3(I7B, I7);
    INVX2 inv4(I5B, I5);
    INVX2 inv5(I7I6B, I7I6);
    OAI21X1 oai2(I7BI7I6BI5B, I7B, I7I6B, I5B);
    INVX2 inv6(I3B, I3);
    INVX2 inv7(I2B, I2);
    NAND2X1 nand2(I2BI1, I2B, I1);
    AOI21X1 aoi1(I6I5I4I3BI2BI1, I6I5I4, I3B, I2BI1);
    NOR2X1 nor6(P0B, I7BI7I6BI5B, I6I5I4I3BI2BI1);
    INVX2 inv8(P0, P0B);
endmodule
```

8X3PriorityEncoder.v



```verilog
`timescale 10ps/10ps

module testbench();
    reg [7:0] I, temp;
    wire P0, P1, P2, I0, I1, I2, I3, I4, I5, I6, I7;

    assign  I0 = I[0];
    assign  I1 = I[1];
    assign  I2 = I[2];
    assign  I3 = I[3];
    assign  I4 = I[4];
    assign  I5 = I[5];
    assign  I6 = I[6];
    assign  I7 = I[7];

    initial
    begin
        I <= 1;
        temp <= 1;
    end

    always @*
        begin
        #10 I <= I + temp; //random variables
            temp <= temp + temp;
        end

    PriorityEncoder testencoder (.P2(P2), .P1(P1), .P0(P0),
                                    .I7(I7), .I6(I6), .I5(I5), .I4(I4),
                                    .I3(I3), .I2(I2), .I1(I1), .I0(I0));
endmodule
```

testbench.v

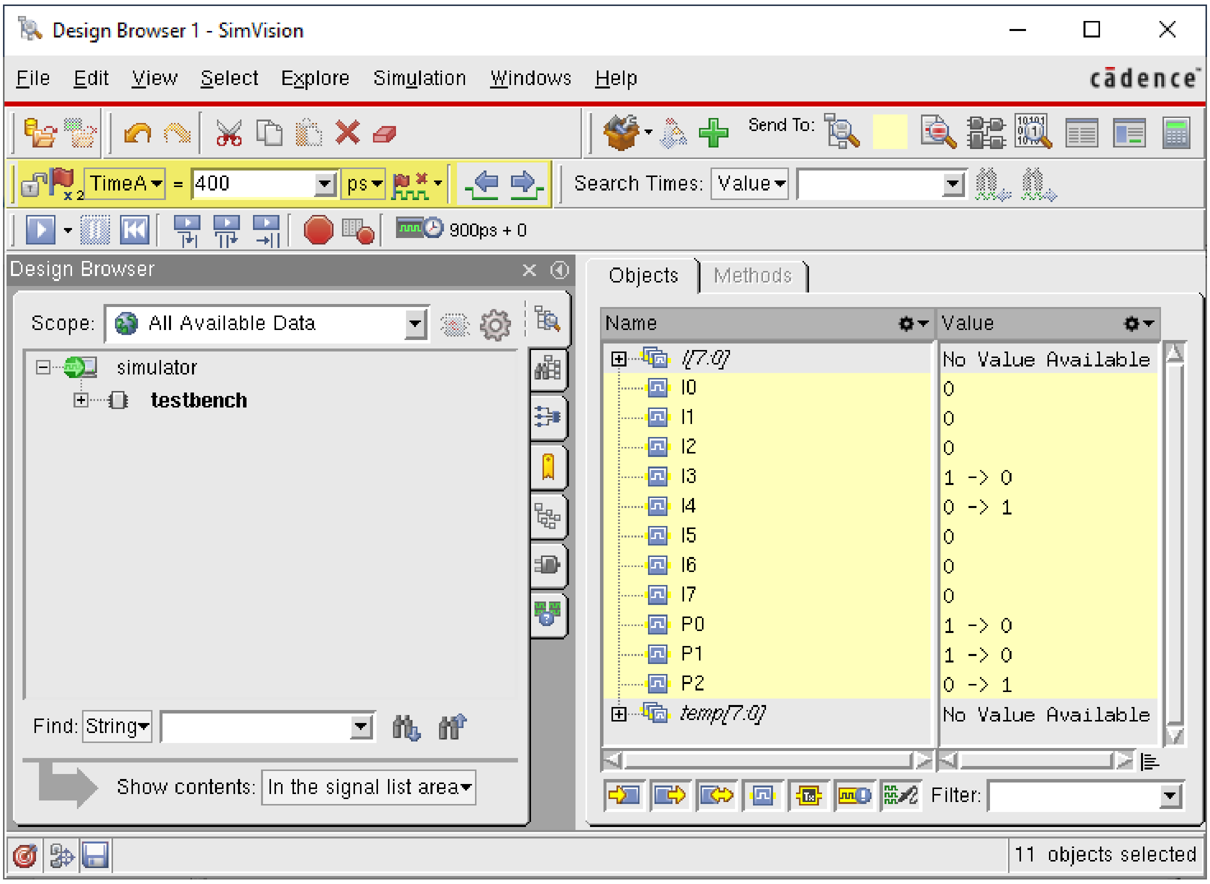


```
-bash-4.2$ xrun -access +r -gui 8X3PriorityEncoder.v  standard.v  testbench.v &
[1] 40857
-bash-4.2$ TOOL:        xrun(64)        19.09-s001: Started on Apr 28, 2020 at 00:14:28 EDT
xrun(64): 19.09-s001: (c) Copyright 1995-2019 Cadence Design Systems, Inc.
Recompiling... reason: file './testbench.v' is newer than expected.
        expected: Tue Apr 28 00:05:52 2020
        actual:   Tue Apr 28 00:14:24 2020
file: testbench.v
        module worklib.testbench:v
                errors: 0, warnings: 0
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Top level design units:
                testbench
        Building instance overlay tables: .................... Done
        Generating native compiled code:
                worklib.testbench:v <0x171cf61e>
                        streams:   5, words:  2070
        Building instance specific data structures.
        Loading native compiled code:     .................... Done
        Design hierarchy summary:
                                  Instances  Unique
                Modules:                 21       7
                Registers:                2       2
                Scalar wires:            33       -
                Always blocks:            1       1
                Initial blocks:           1       1
                Cont. assignments:        1      17
                Simulation timescale:  10ps
        Writing initial simulation snapshot: worklib.testbench:v
waiting for SimVision/Indago to connect...
waiting for SimVision/Indago to connect...

-------------------------------------
Relinquished control to SimVision...
xcelium>
xcelium> source /network/rit/lab/ceashpc/software/cadence/XCELIUM1909/tools/inca/files/xmsimrc
```

Loading remote monitoring, please wait...

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net

SSH terminal message


Design Browser 1 - SimVision
File Edit View Select Explore Simulation Windows Help
cadence
Send To:
Search Times:
Design Browser
Objects
Methods
Find:
Show contents:

TimeA = 400 ps

900ps + 0

Scope: All Available Data

simulator
testbench

Find: String

Show contents: In the signal list area

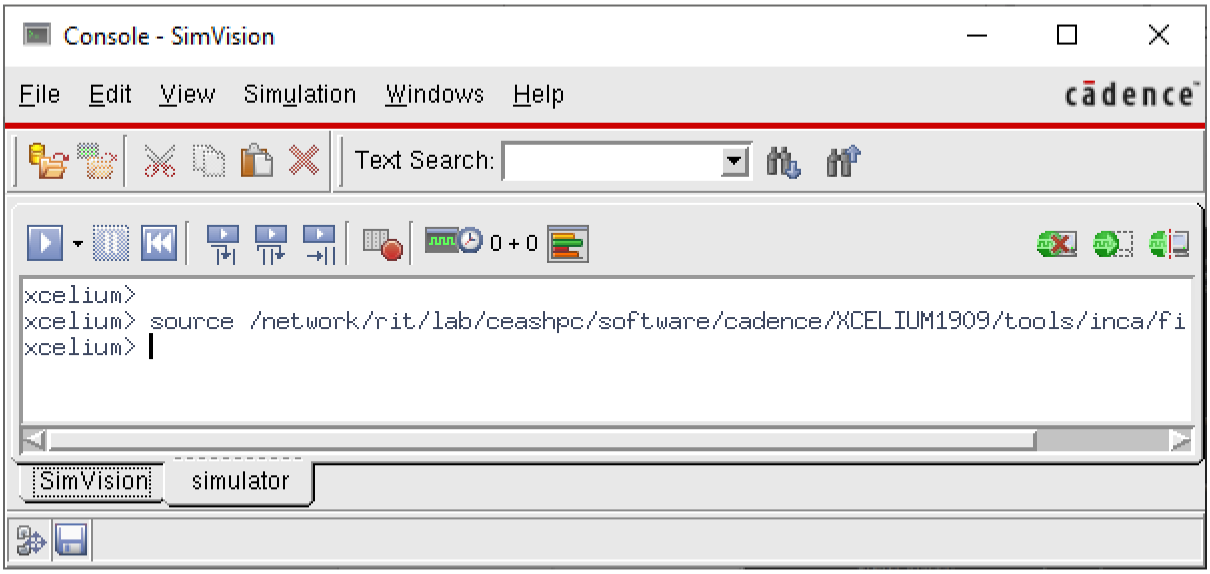
Search Times: Value

Name	Value
I[7:0]	No Value Available
I0	0
I1	0
I2	0
I3	1 -> 0
I4	0 -> 1
I5	0
I6	0
I7	0
P0	1 -> 0
P1	1 -> 0
P2	0 -> 1
temp[7:0]	No Value Available

Filter:

11 objects selected

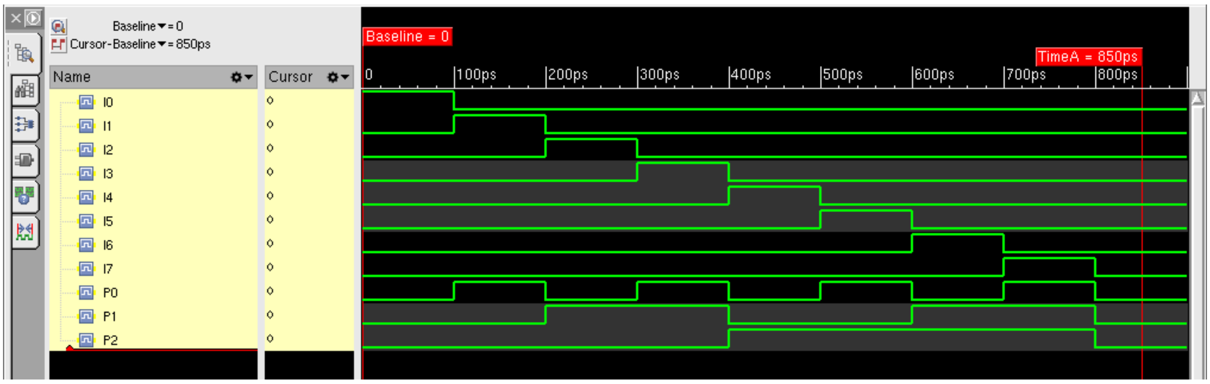
SimVision Design Browser



0 + 0

```
xcelium>
xcelium> source /network/rit/lab/ceashpc/software/cadence/XCELIUM1909/tools/inca/fi
xcelium>
```

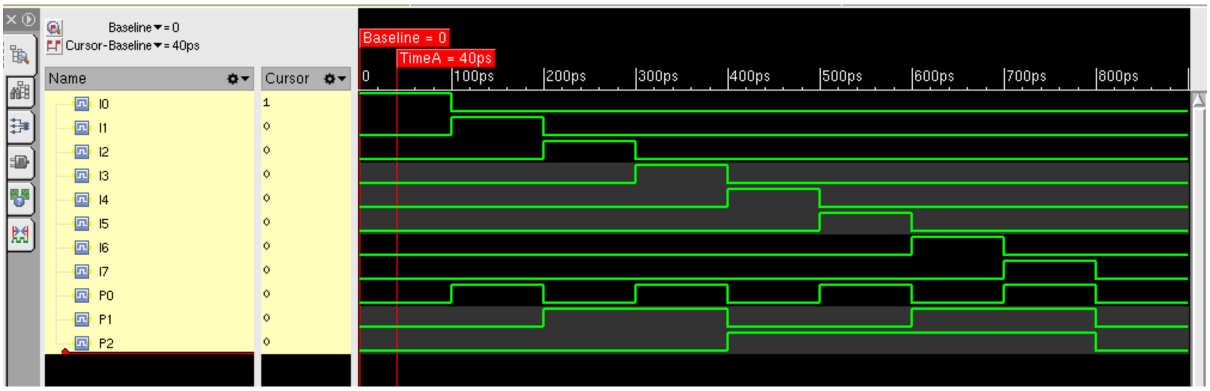
SimVision Console



Baseline = 0
Cursor-Baseline = 850ps

Name	Cursor
I0	0
I1	0
I2	0
I3	0
I4	0
I5	0
I6	0
I7	0
P0	0
P1	0
P2	0

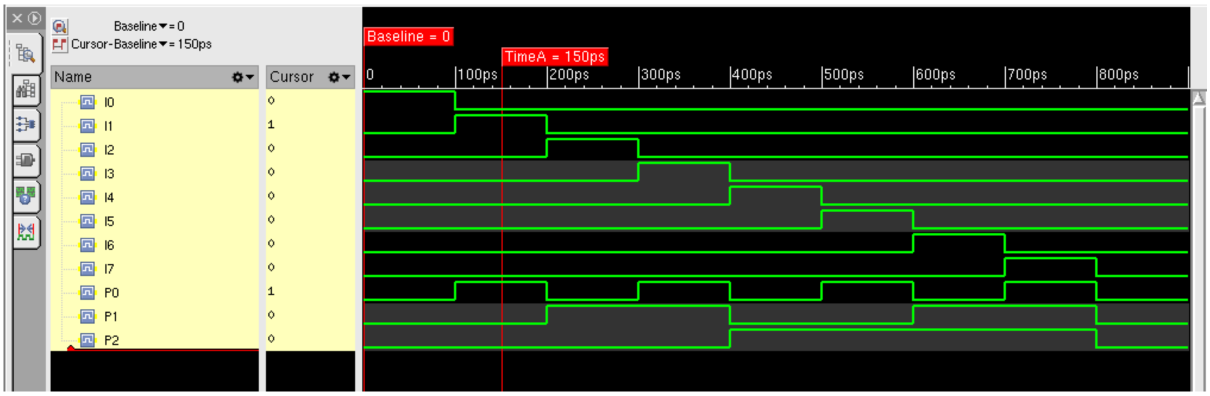
All Zeros



Baseline = 0
Cursor-Baseline = 40ps

Name	Cursor
I0	1
I1	0
I2	0
I3	0
I4	0
I5	0
I6	0
I7	0
P0	0
P1	0
P2	0

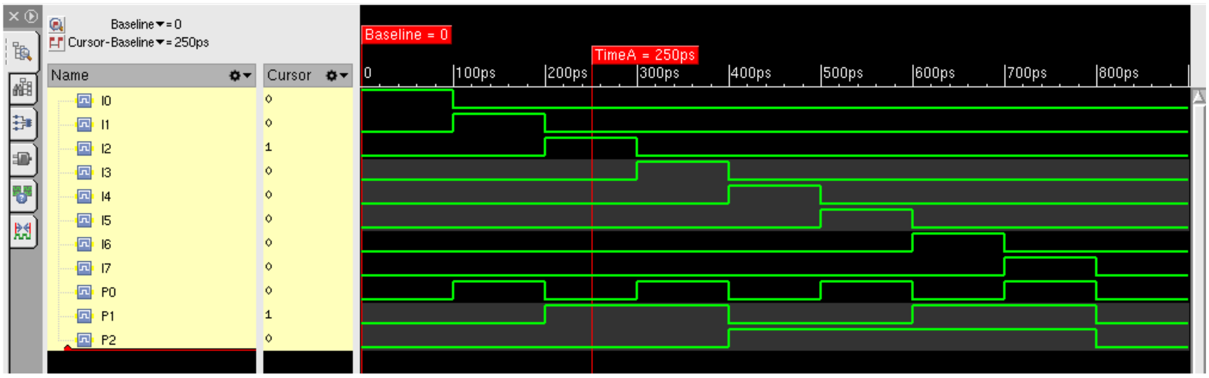
I0 = 1



Baseline = 0
Cursor-Baseline = 150ps

Name	Cursor
I0	0
I1	1
I2	0
I3	0
I4	0
I5	0
I6	0
I7	0
P0	1
P1	0
P2	0

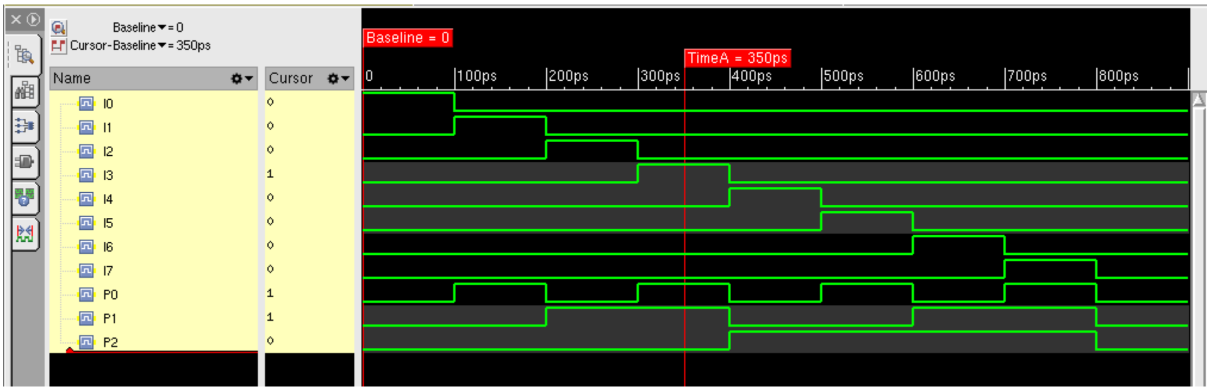
I1 = 1



Baseline = 0
Cursor-Baseline = 250ps

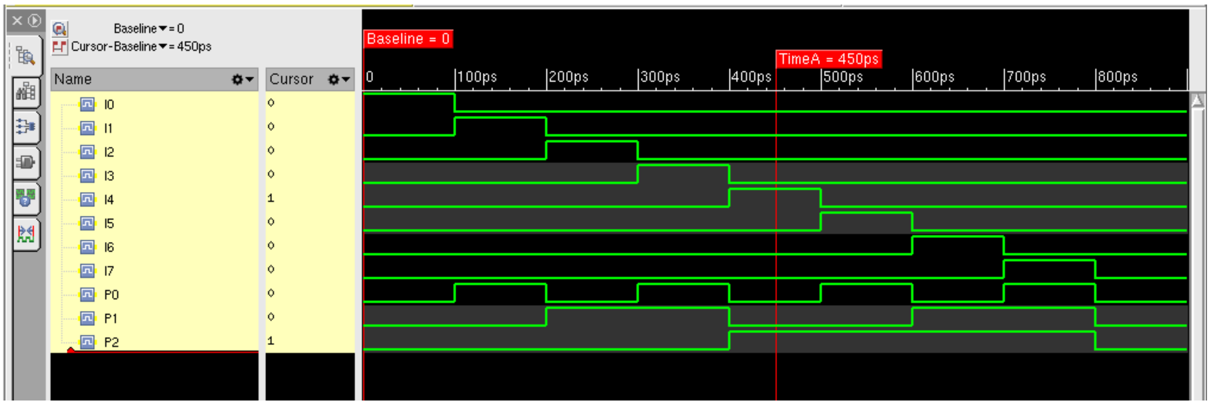
Name	Cursor
I0	0
I1	0
I2	1
I3	0
I4	0
I5	0
I6	0
I7	0
P0	0
P1	1
P2	0

I2 = 1


Baseline = 0
Cursor-Baseline = 350ps

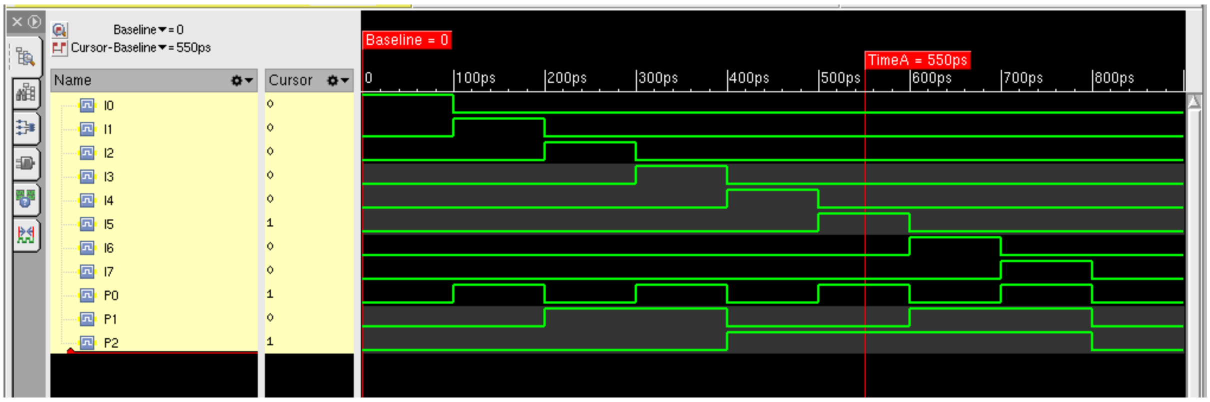
Name	Cursor
I0	0
I1	0
I2	0
I3	1
I4	0
I5	0
I6	0
I7	0
P0	1
P1	1
P2	0

I3 = 1


Baseline = 0
Cursor-Baseline = 450ps

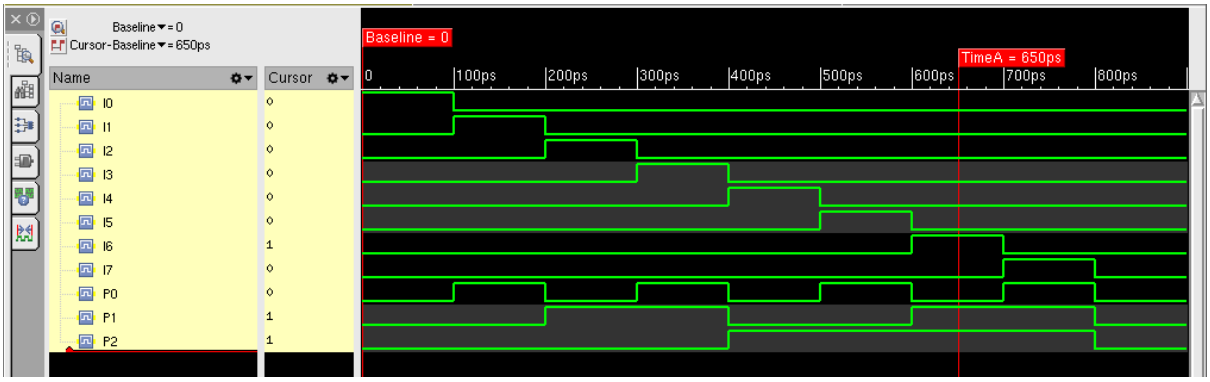
Name	Cursor
I0	0
I1	0
I2	0
I3	0
I4	1
I5	0
I6	0
I7	0
P0	0
P1	0
P2	1

I4 = 1


Baseline = 0
Cursor-Baseline = 550ps

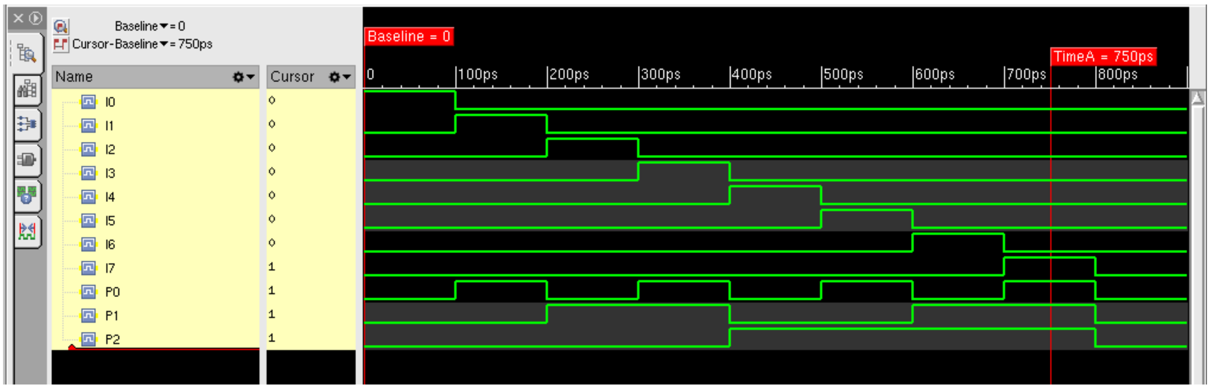
Name	Cursor
I0	0
I1	0
I2	0
I3	0
I4	0
I5	1
I6	0
I7	0
P0	1
P1	0
P2	1

I5 =1


Baseline = 0
Cursor-Baseline = 650ps

Name	Cursor
I0	0
I1	0
I2	0
I3	0
I4	0
I5	0
I6	1
I7	0
P0	0
P1	1
P2	1

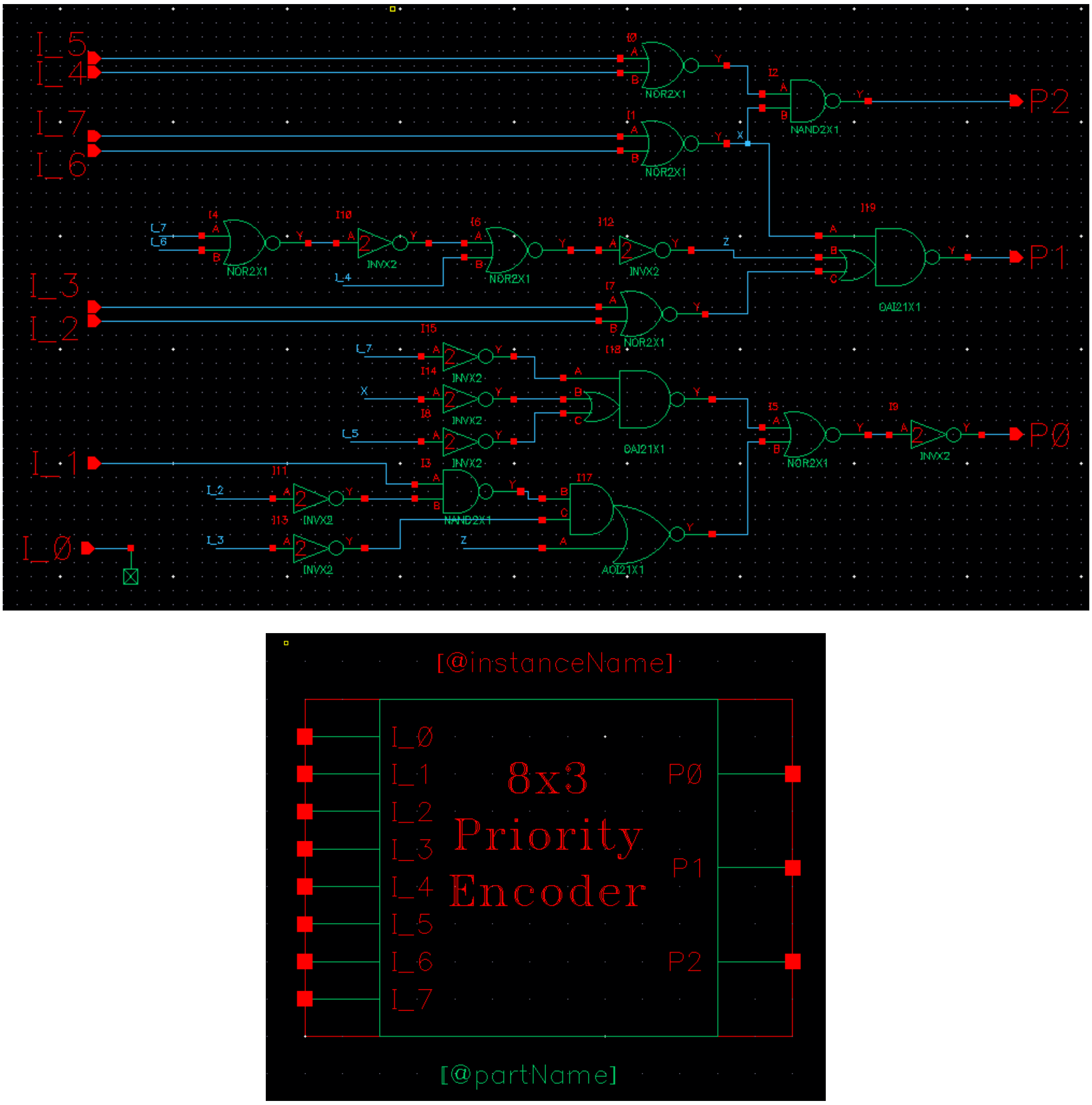
I6 = 1



I7 = 1

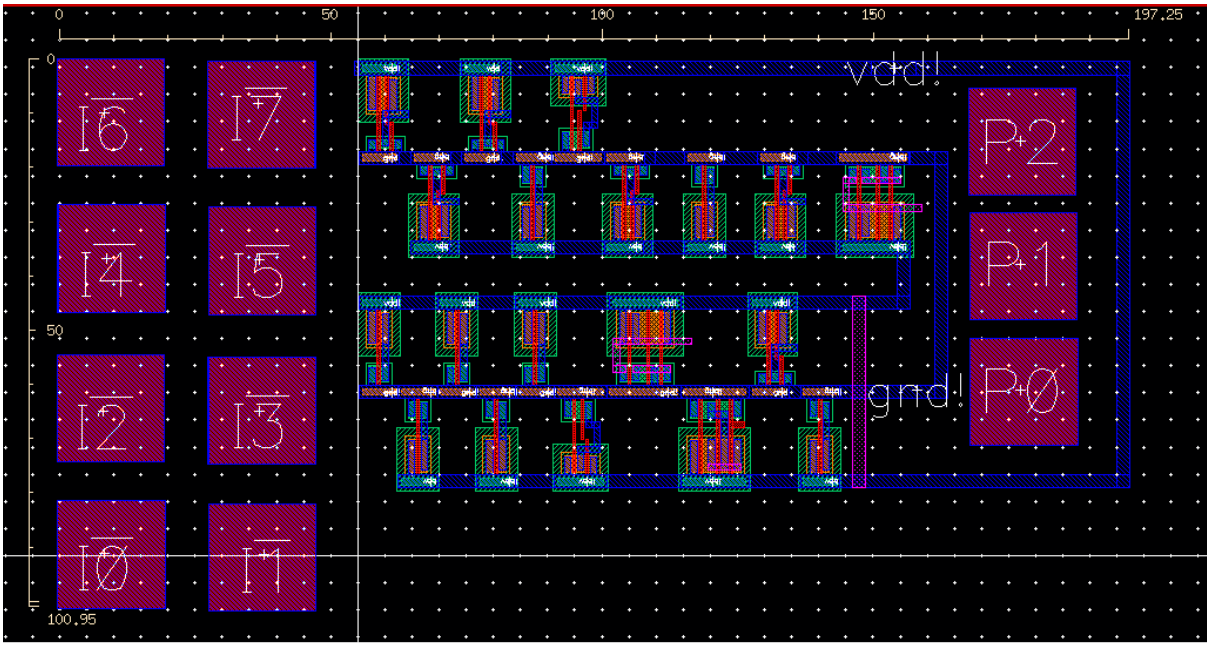
The output from Xcelium follows the truth table, hence the circuit is working perfectly.

PARTS D, E & F



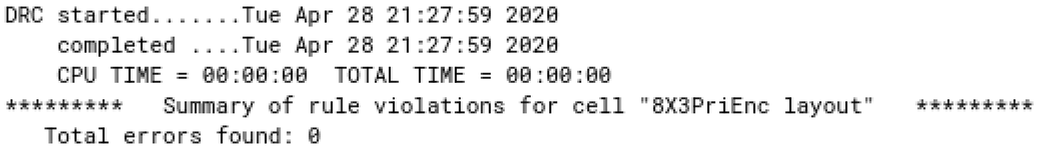
8x3 Priority Encoder Schematic and Symbol

PLACE:



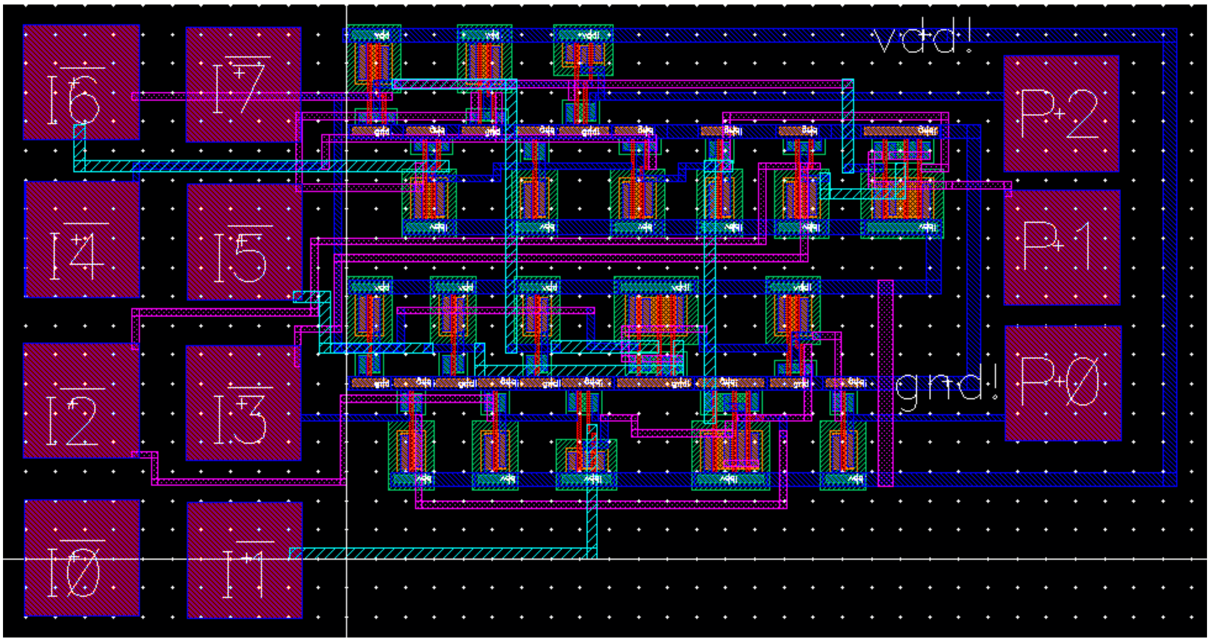
All the elements of the layout placed, along with pads for the inputs, outputs, vdd! and gnd!. The cross-sectional measurements shown above is **100.95µm x 197.25µm**, which is far within the given range of 250µm x 250µm.

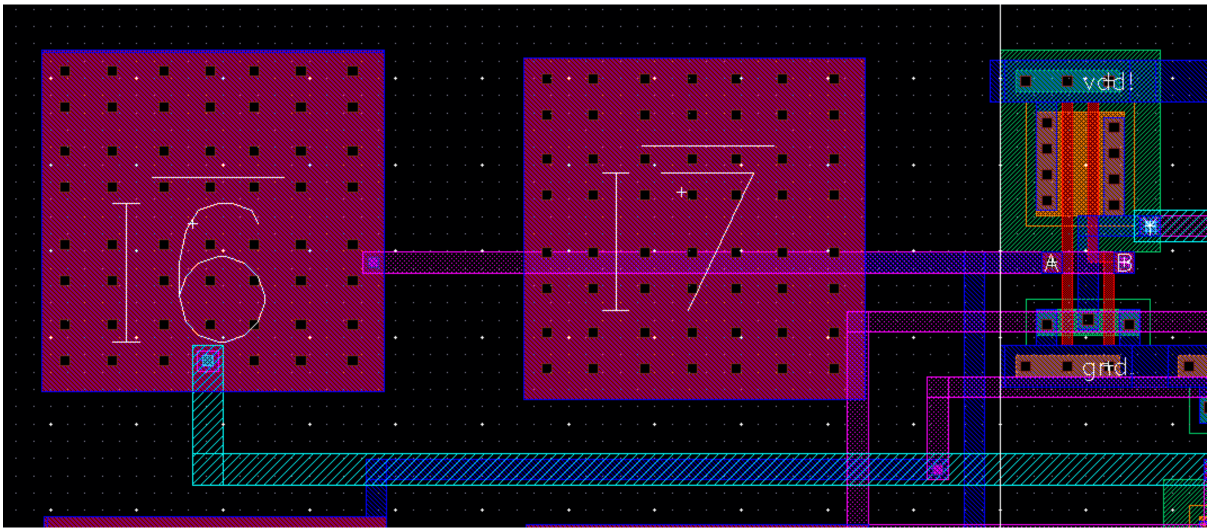
Before routing the wires for the next step, we check DRC to ensure the placements are perfect.



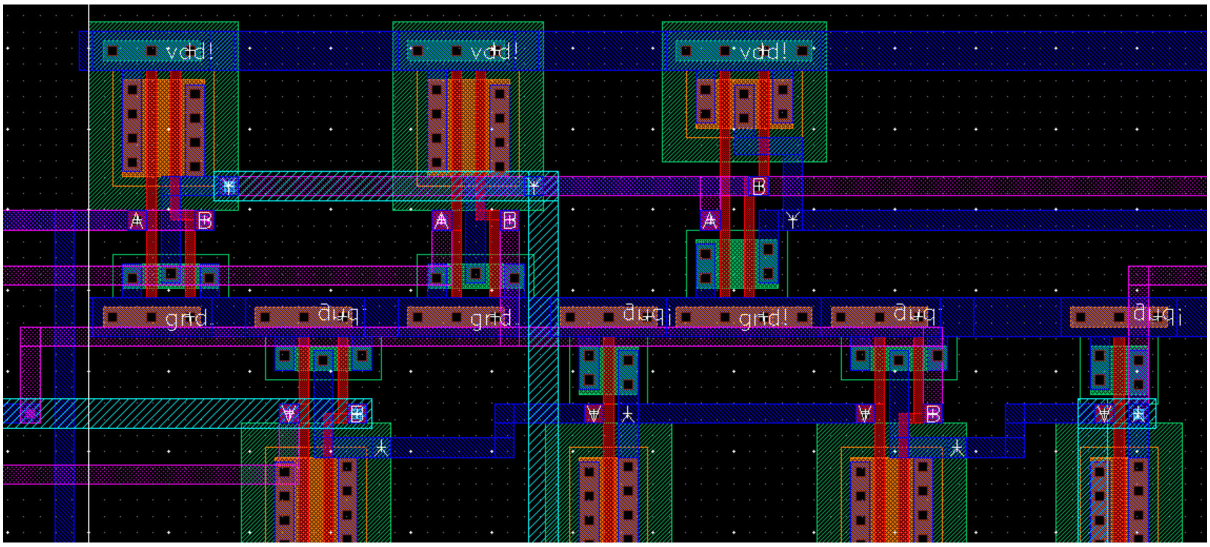
```
DRC started.......Tue Apr 28 21:27:59 2020
    completed ....Tue Apr 28 21:27:59 2020
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "8X3PriEnc layout"   *********
   Total errors found: 0
```

ROUTE:

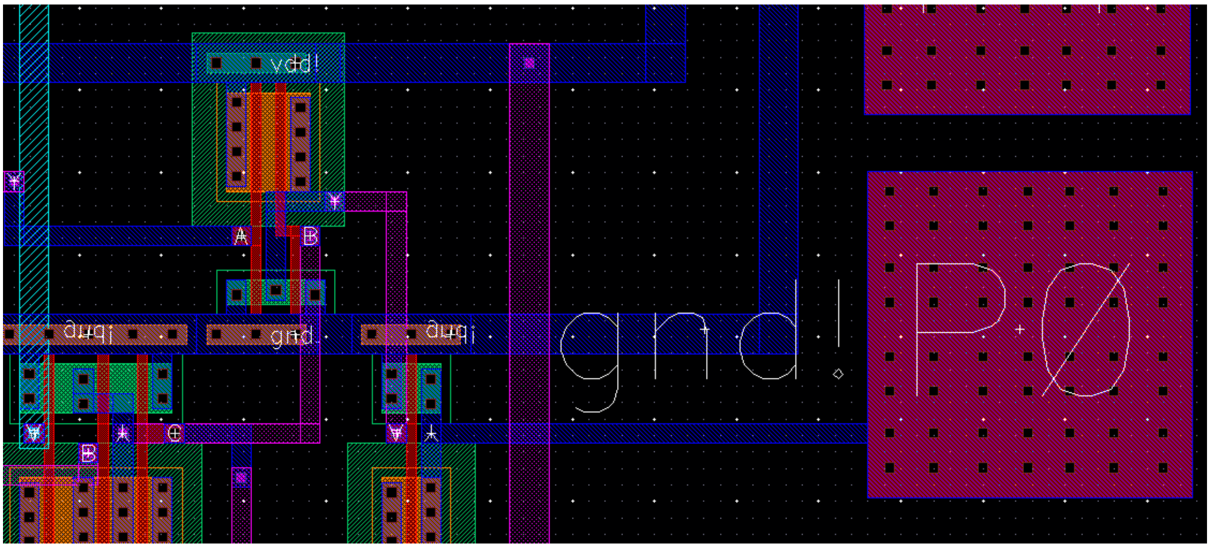




Input pads, zoomed in, each pad 19.95µm x 19.95µm

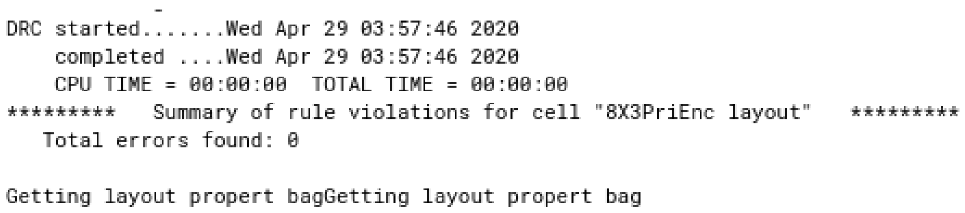


Inner routing of the cells, zoomed in



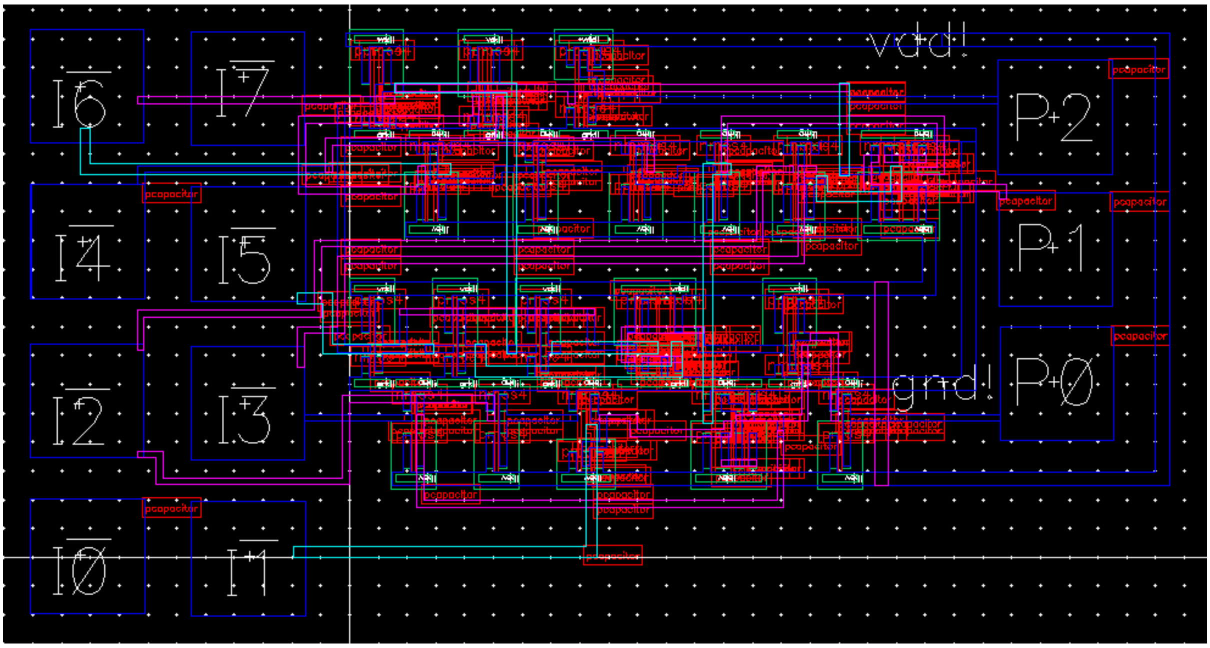
Gnd! and output pads, zoomed in, each pad 19.95µm x 19.95µm

The completed layout is shown above. We run DRC.

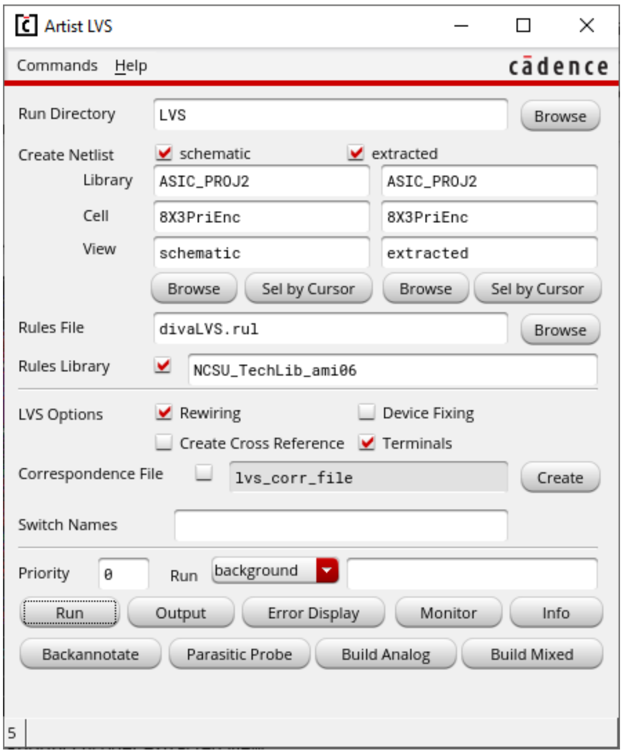


```
DRC started.......Wed Apr 29 03:57:46 2020
    completed ....Wed Apr 29 03:57:46 2020
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "8X3PriEnc layout"   *********
   Total errors found: 0

Getting layout propert bagGetting layout propert bag
```

Now we create the extracted view and check LVS.



8x3 Priority Encoder extracted view



Run Directory: LVS

Create Netlist: ☑ schematic ☑ extracted

	schematic	extracted
Library	ASIC_PROJ2	ASIC_PROJ2
Cell	8X3PriEnc	8X3PriEnc
View	schematic	extracted

Rules File: divaLVS.rul

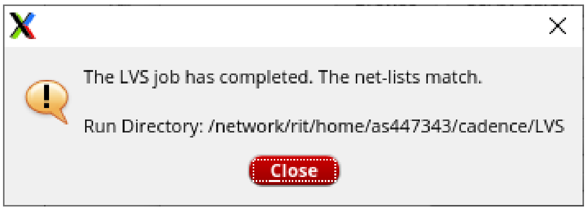
Rules Library: ☑ NCSU_TechLib_ami06

LVS Options: ☑ Rewiring □ Device Fixing □ Create Cross Reference ☑ Terminals

Correspondence File: □ lvs_corr_file

Switch Names:

Priority: 0 Run: background

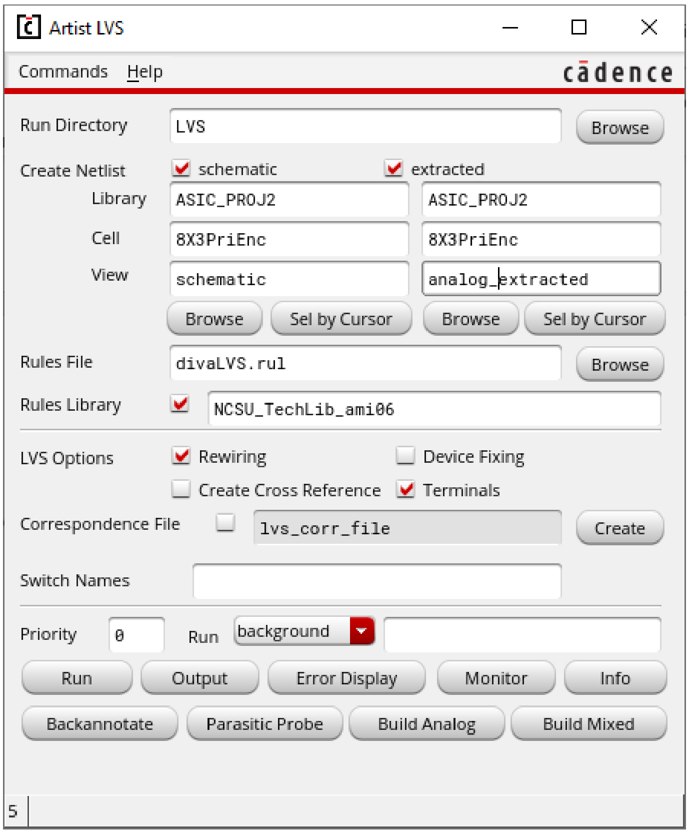


The LVS job has completed. The net-lists match.

Run Directory: /network/rit/home/as447343/cadence/LVS

The net-lists match!

Now, it is time to create the analog_extracted view to be used in the testbench.



Artist LVS

Commands Help

Run Directory: LVS

Create Netlist: ☑ schematic ☑ extracted

	schematic	extracted
Library	ASIC_PROJ2	ASIC_PROJ2
Cell	8X3PriEnc	8X3PriEnc
View	schematic	analog_extracted

Rules File: divaLVS.rul

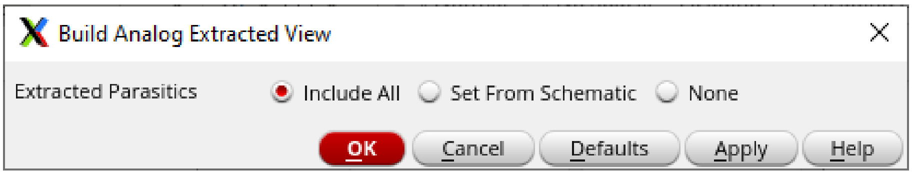
Rules Library: ☑ NCSU_TechLib_ami06

LVS Options: ☑ Rewiring □ Device Fixing □ Create Cross Reference ☑ Terminals

Correspondence File: □ lvs_corr_file

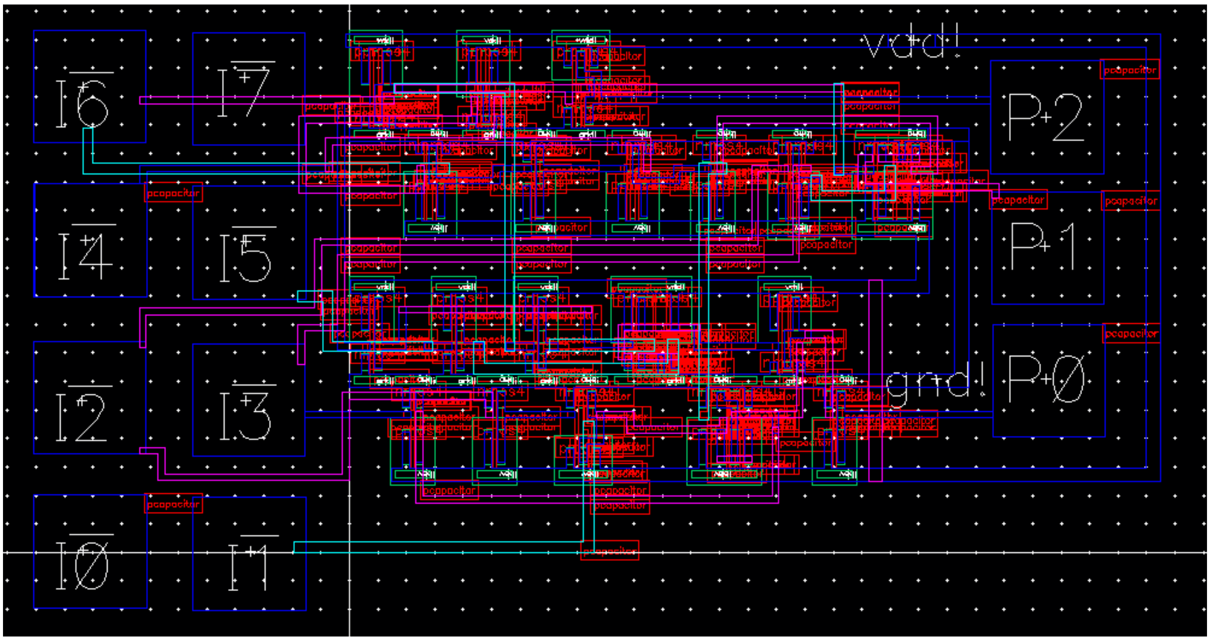
Switch Names:

Priority: 0 Run: background



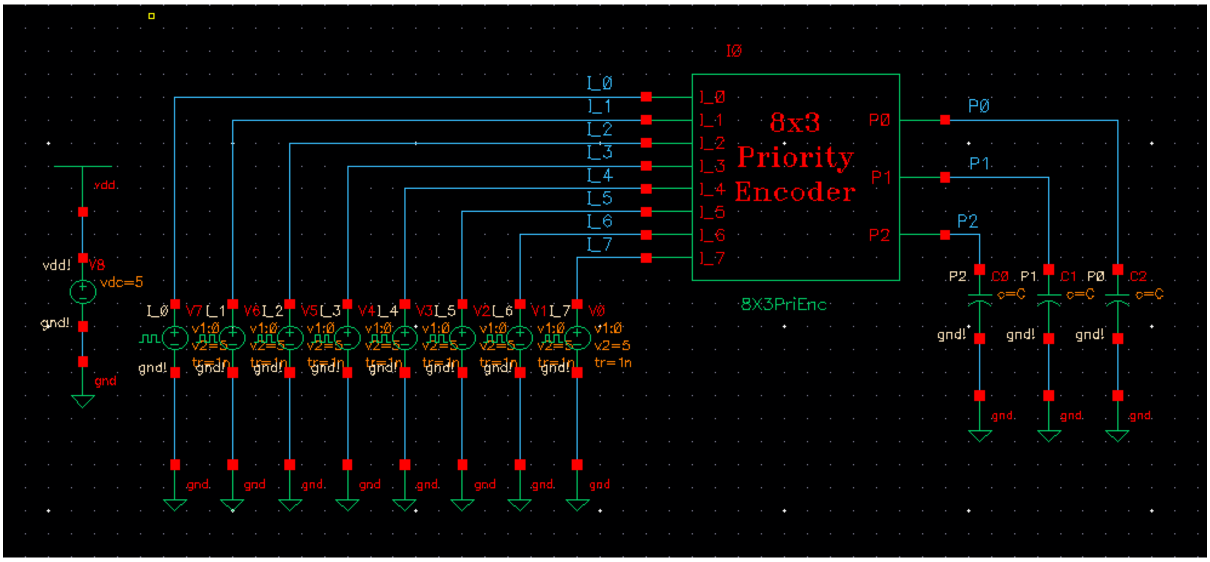
Build Analog Extracted View

Extracted Parasitics: ● Include All ○ Set From Schematic ○ None

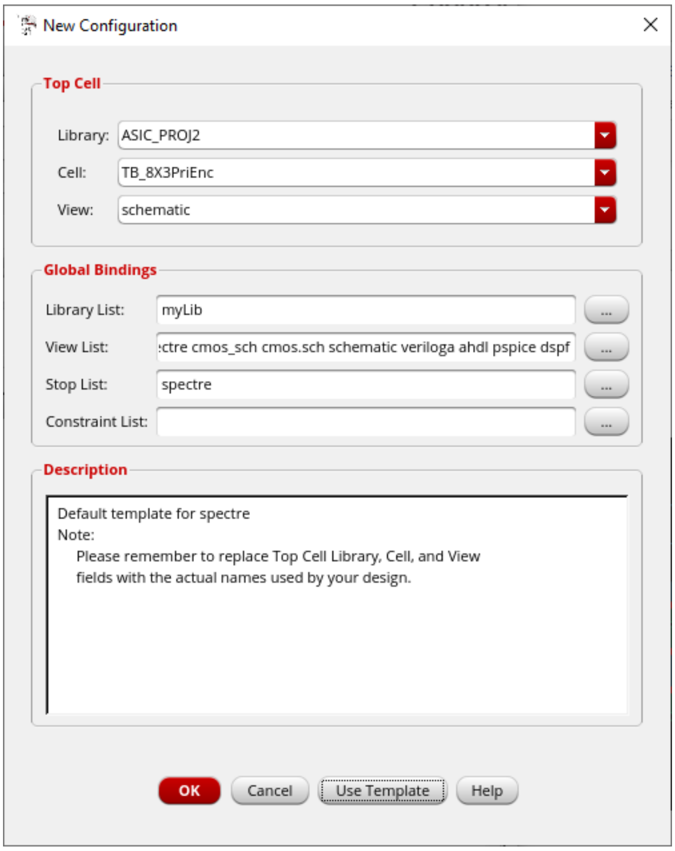


8x3 Priority Encoder analog_extracted view

TEST/VERIFY:



TB_8x3PriEnc Schematic view



Top Cell

Library: ASIC_PROJ2

Cell: TB_8X3PriEnc

View: schematic

Global Bindings

Library List: myLib

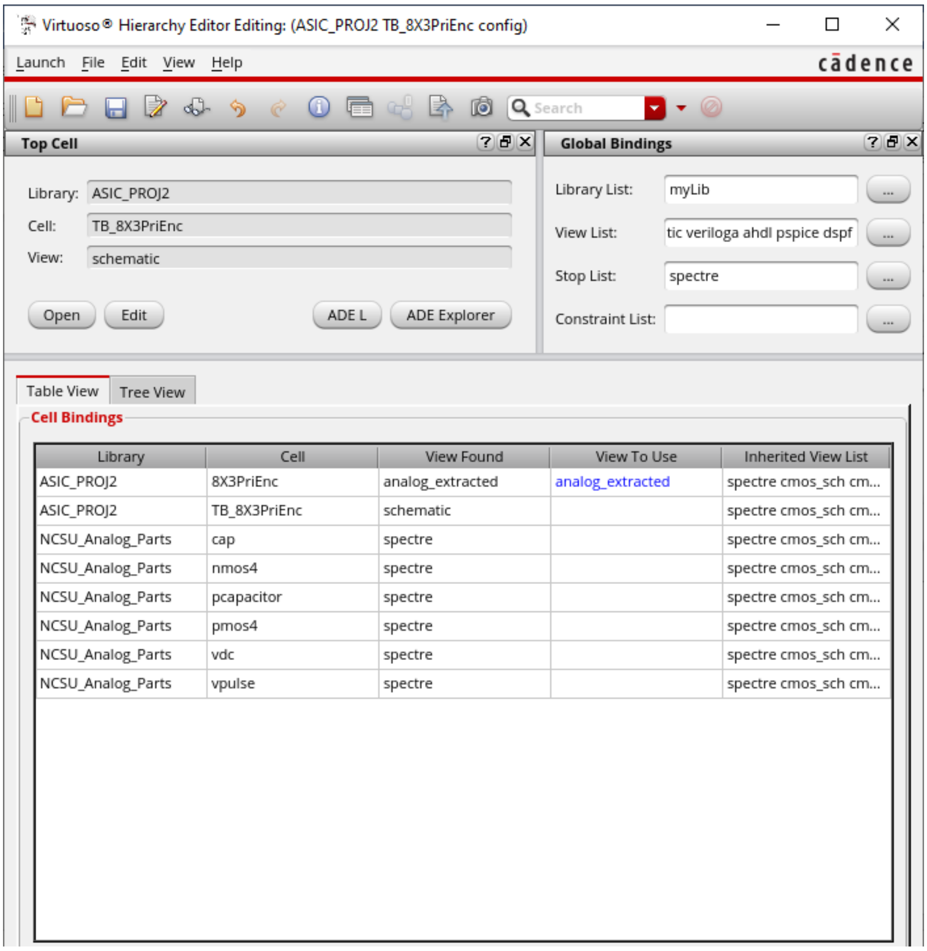
View List: :ctre cmos_sch cmos.sch schematic veriloga ahdl pspice dspf

Stop List: spectre

Constraint List:

Description

Default template for spectre
Note:
Please remember to replace Top Cell Library, Cell, and View
fields with the actual names used by your design.



Virtuoso® Hierarchy Editor Editing: (ASIC_PROJ2 TB_8X3PriEnc config)

Top Cell

Library: ASIC_PROJ2

Cell: TB_8X3PriEnc

View: schematic

Global Bindings

Library List: myLib

View List: tic verilog ahdl pspice dspf

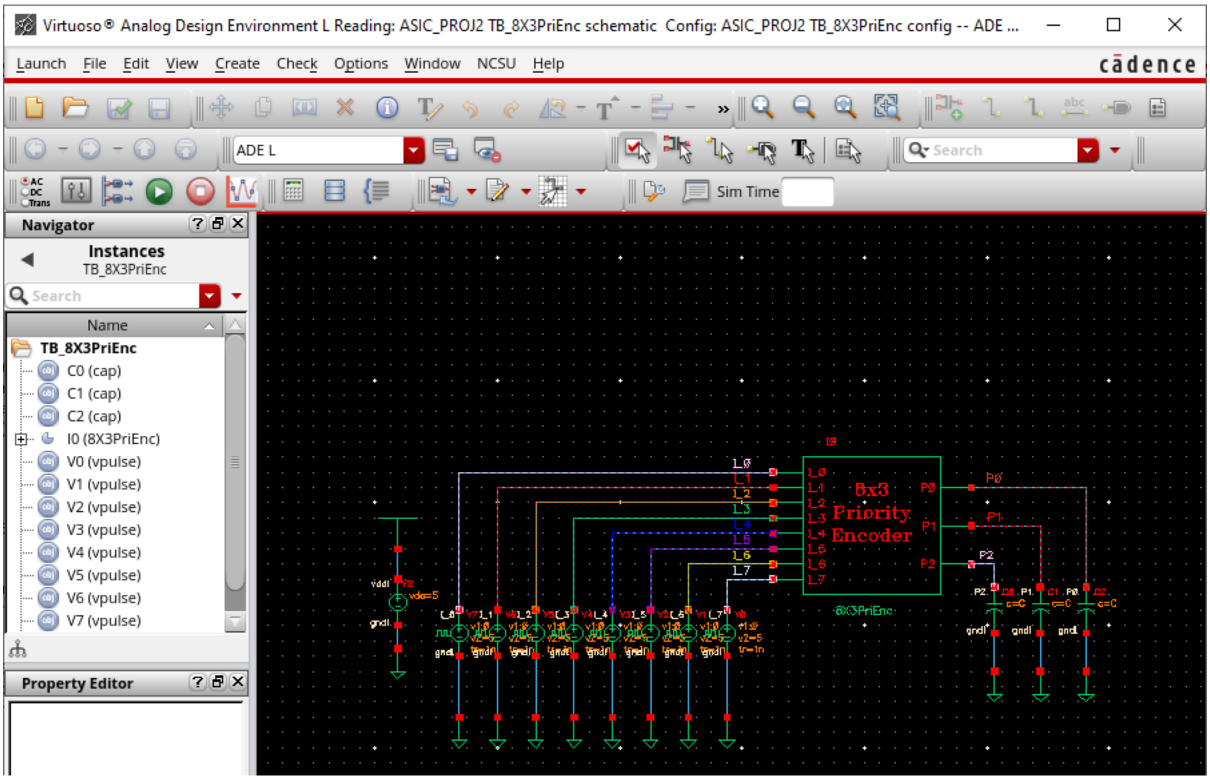
Stop List: spectre

Constraint List:

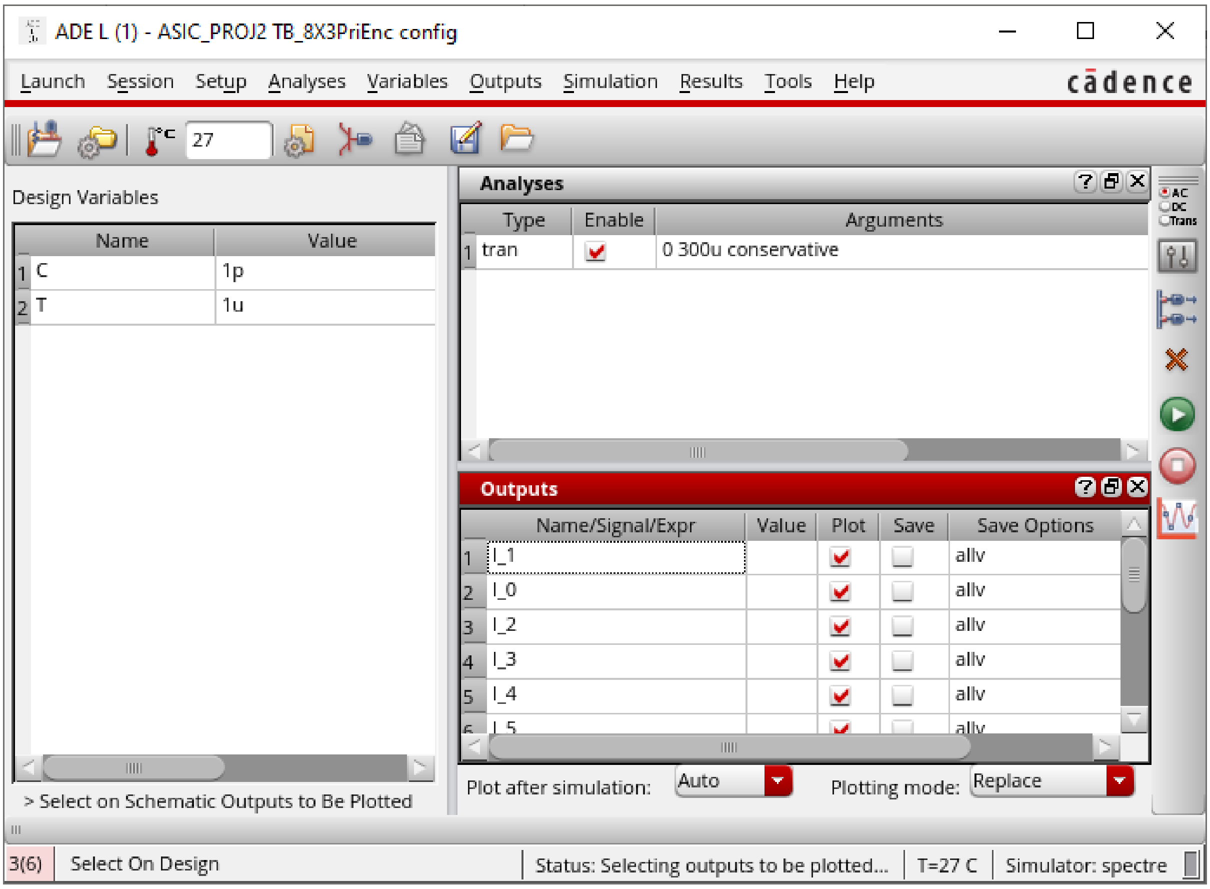
Cell Bindings

Library	Cell	View Found	View To Use	Inherited View List
ASIC_PROJ2	8X3PriEnc	analog_extracted	analog_extracted	spectre cmos_sch cm...
ASIC_PROJ2	TB_8X3PriEnc	schematic		spectre cmos_sch cm...
NCSU_Analog_Parts	cap	spectre		spectre cmos_sch cm...
NCSU_Analog_Parts	nmos4	spectre		spectre cmos_sch cm...
NCSU_Analog_Parts	pcapacitor	spectre		spectre cmos_sch cm...
NCSU_Analog_Parts	pmos4	spectre		spectre cmos_sch cm...
NCSU_Analog_Parts	vdc	spectre		spectre cmos_sch cm...
NCSU_Analog_Parts	vpulse	spectre		spectre cmos_sch cm...

TB_8x3PriEnc config view



Virtuoso® Analog Design Environment L Reading: ASIC_PROJ2 TB_8X3PriEnc schematic Config: ASIC_PROJ2 TB_8X3PriEnc config -- ADE ...



ADE L (1) - ASIC_PROJ2 TB_8X3PriEnc config

Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help

27

Design Variables

	Name	Value
1	C	1p
2	T	1u

Analyses

	Type	Enable	Arguments
1	tran	☑	0 300u conservative

Outputs

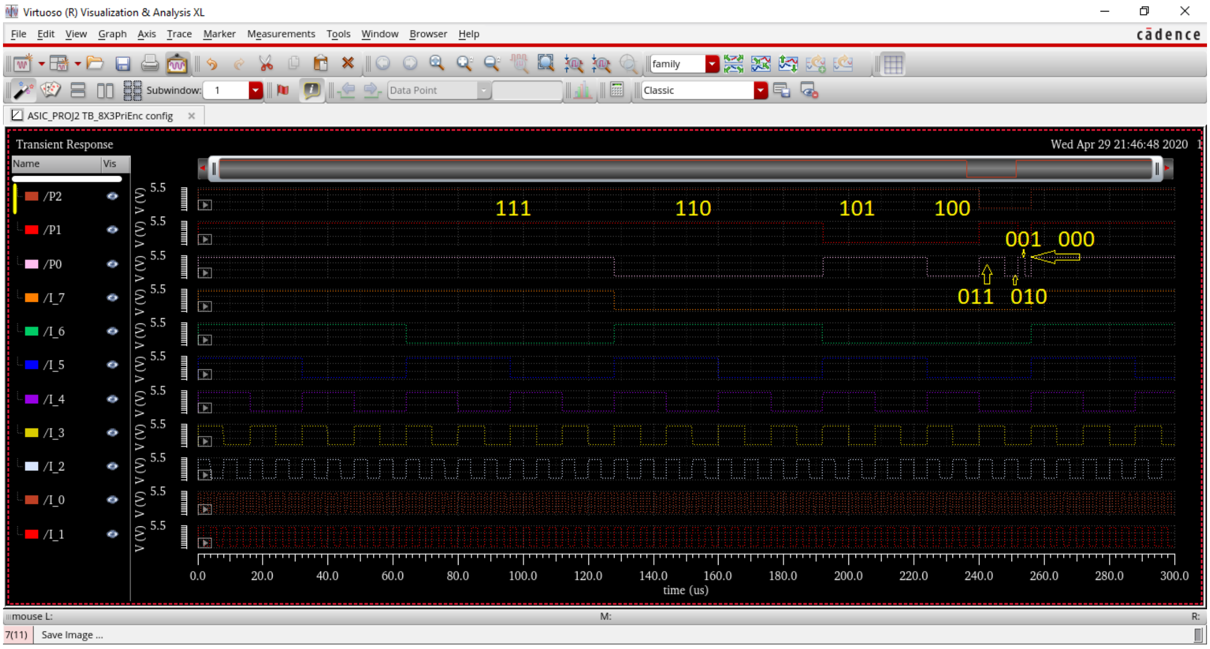
	Name/Signal/Expr	Value	Plot	Save	Save Options
1	I_1		☑	□	allv
2	I_0		☑	□	allv
3	I_2		☑	□	allv
4	I_3		☑	□	allv
5	I_4		☑	□	allv
6	I_5		☑	□	allv

Plot after simulation: Auto   Plotting mode: Replace

> Select on Schematic Outputs to Be Plotted

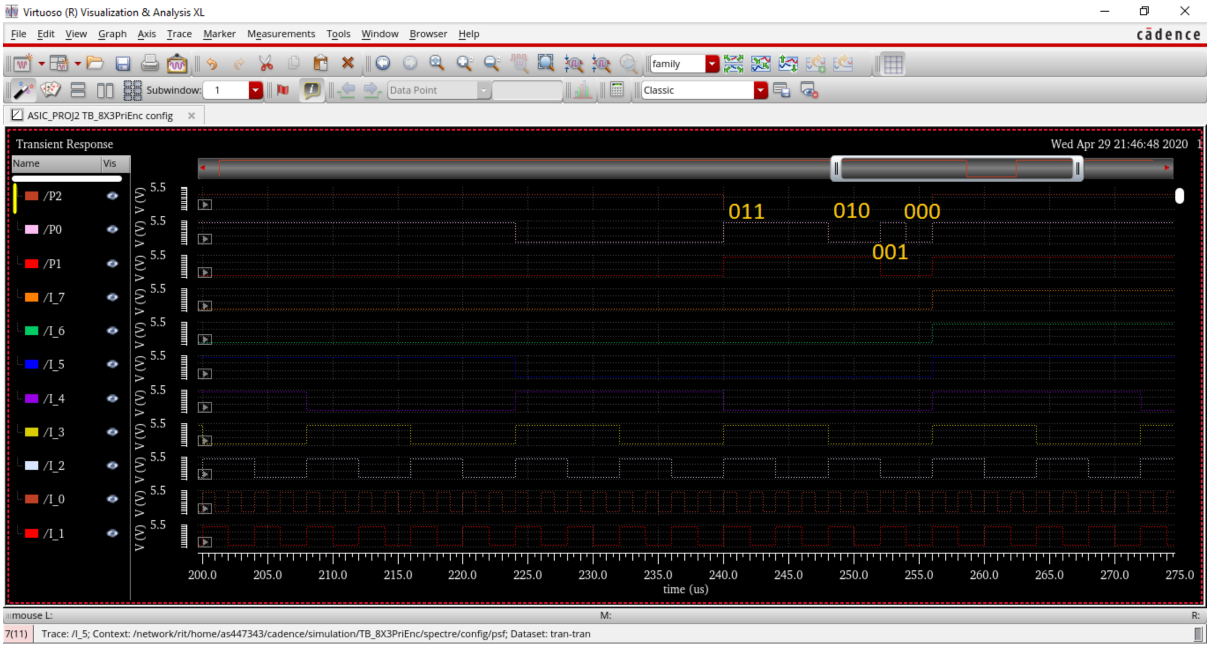
3(6) Select On Design   Status: Selecting outputs to be plotted...   T=27 C   Simulator: spectre

TB_8x3PriEnc ADE L



ADE L output

We zoom in to get a better view of the smaller variables.


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cādence
Subwindow: 1
Data Point
family
Classic
ASIC_PROJ2 TB_8X3PriEnc config
Transient Response
Wed Apr 29 21:46:48 2020
Name
Vis
/P2
/P0
/P1
/I_7
/I_6
/I_5
/I_4
/I_3
/I_2
/I_0
/I_1
V (V)
5.5
011
010
000
001
200.0
205.0
210.0
215.0
220.0
225.0
230.0
235.0
240.0
245.0
250.0
255.0
260.0
265.0
270.0
275.0
time (us)
mouse L:
M:
R:
7(11)
Trace: /I_5; Context: /network/rit/home/as447343/cadence/simulation/TB_8X3PriEnc/spectre/config/psf; Dataset: tran-tran

Waveform, Zoomed in

The waveform confirms the functionality of the 8x3 Priority Encoder and follows the values from the truth table. Hence the circuit is verified and is working perfectly!