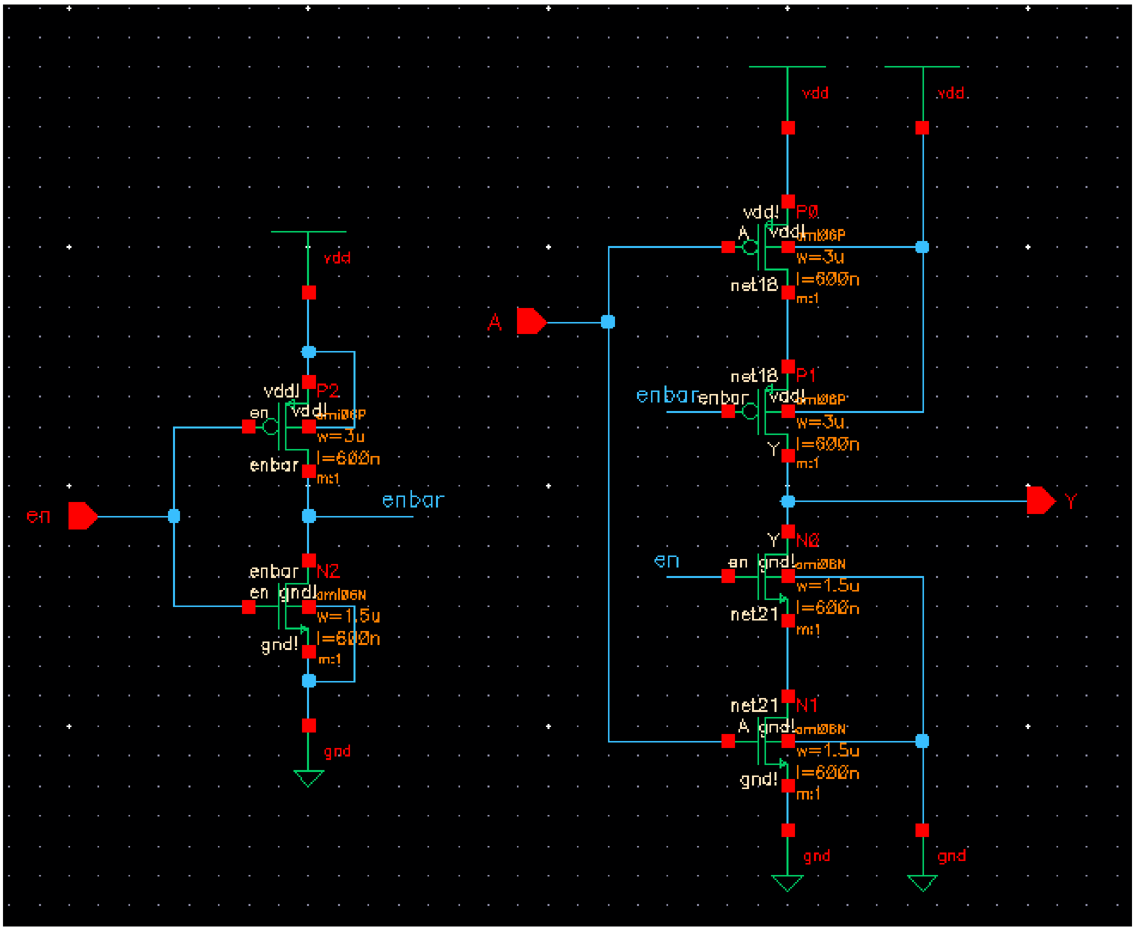
Lab 2, Digital ASIC Design - ECE521

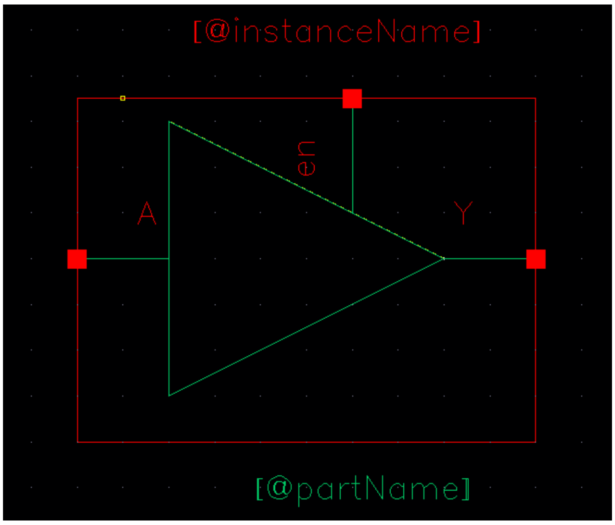
Arijit Sengupta, 001441748

1) Build TBUFX1

For this, we use minimum-size transistors as shown below.

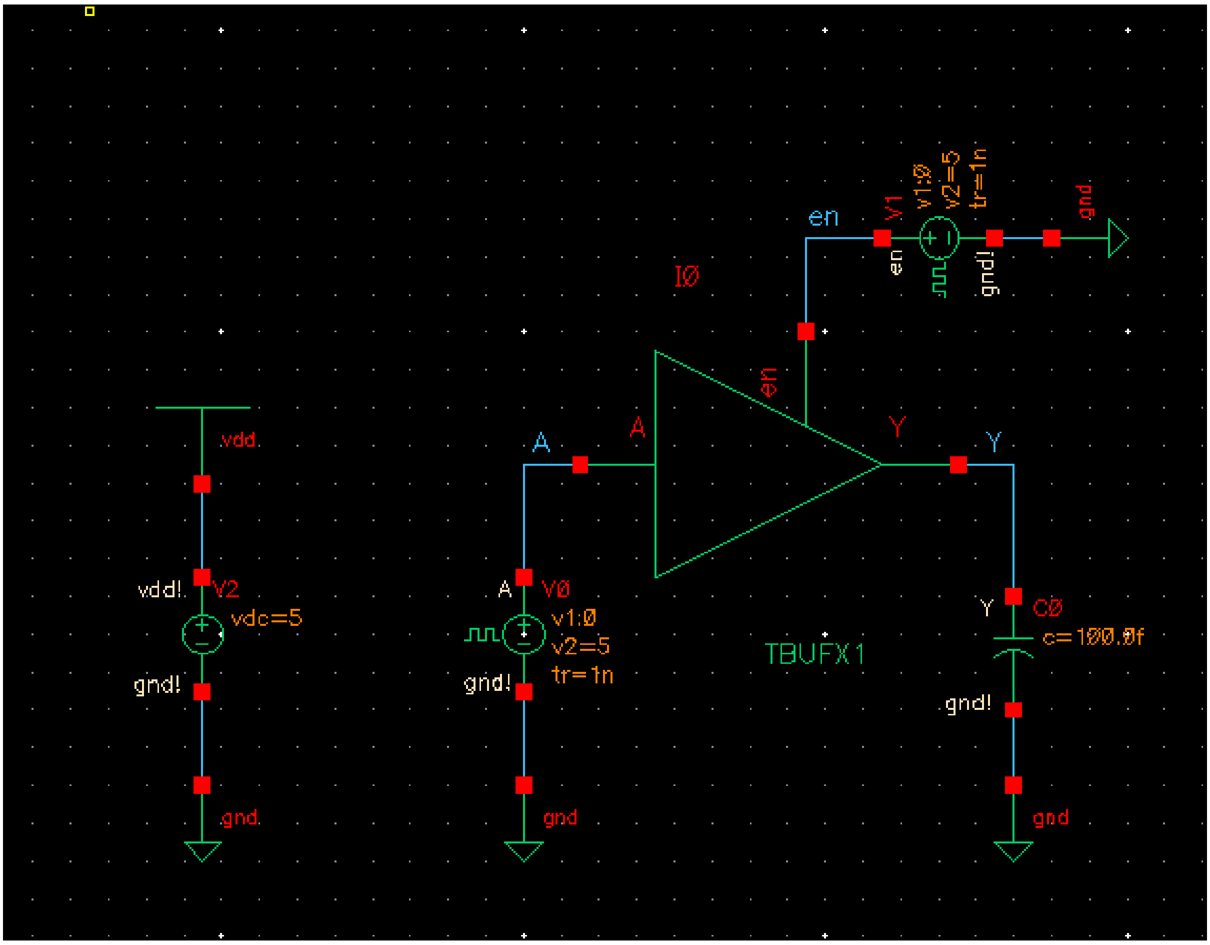


TBUFX1 Schematic



TBUFX1 Symbol

To ensure that the above schematic works fine, we build a test bench to test the TBUFX1.



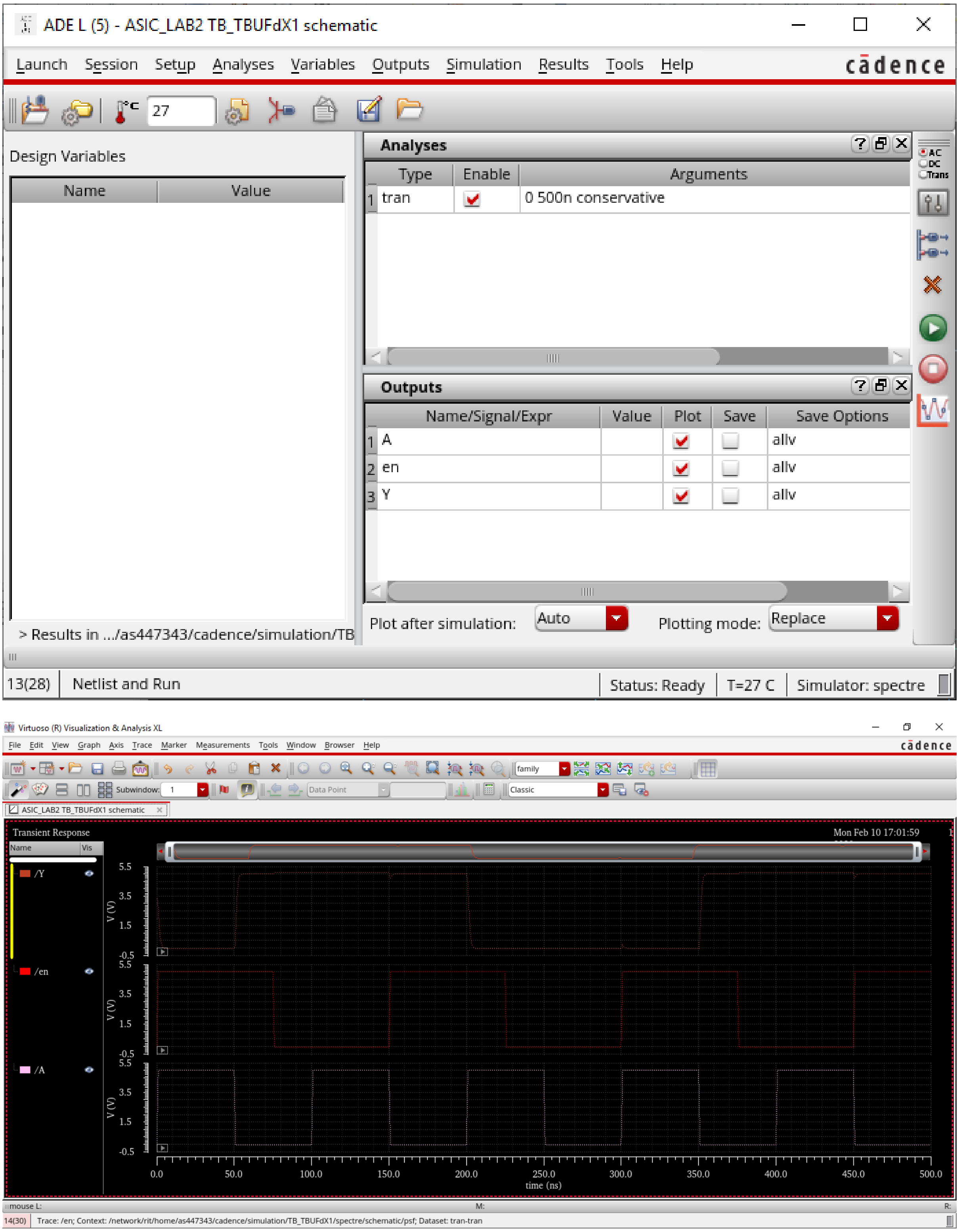
TB_TBUFX1 Schematic

The inputs A and enbar are as follows:

A: V1 – 0V, V2 – 5V, Rise/Fall time – 1ns, Delay – 0ns, Pulse width – 49ns, Period – 100ns

enbar: V1 – 0V, V2 – 5V, Rise/Fall time – 1ns, Delay – 0ns, Pulse width – 74ns, Period – 150ns

Cap = 100fF



ADE L (5) - ASIC_LAB2 TB_TBUFdX1 schematic

Design Variables

Name	Value

Analyses

	Type	Enable	Arguments
1	tran	☑	0 500n conservative

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	A		☑	□	allv
2	en		☑	□	allv
3	Y		☑	□	allv

Plot after simulation: Auto

Plotting mode: Replace

> Results in .../as447343/cadence/simulation/TB

13(28) Netlist and Run Status: Ready T=27 C Simulator: spectre

Virtuoso (R) Visualization & Analysis XL

14(30) Trace: /en; Context: /network/rit/home/as447343/cadence/simulation/TB_TBUFdX1/spectre/schematic/psf; Dataset: tran-tran

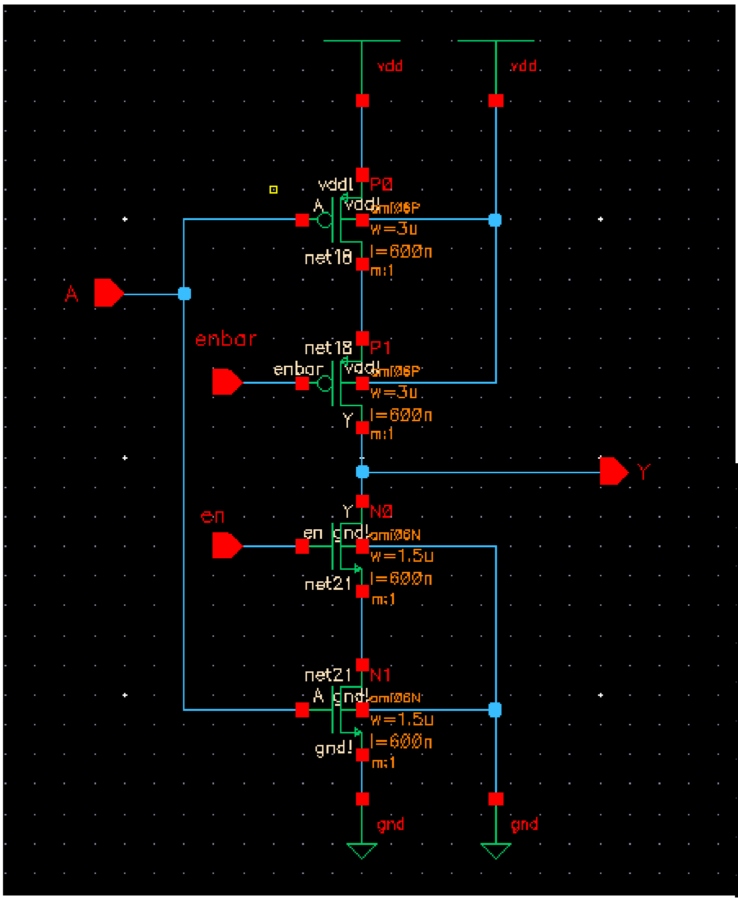
TB_TBUFX1 ADE L and Output Waveform

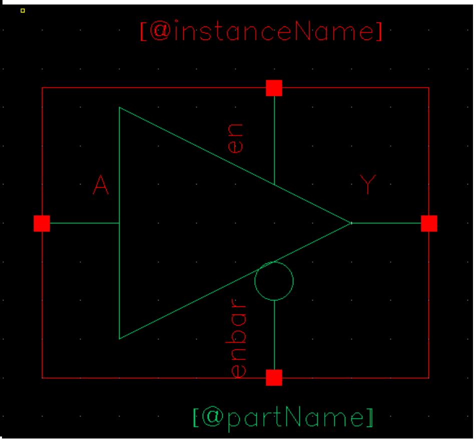
This shows that the output is in accordance to the theoretical values - when en = 0, Y = Z (high impedance, holds previous state) and when en = 1, Y = A’ (A bar).

2) Build TBUFdX1

This is almost identical to TBUFX1; however it is meant to save some area when we use it build our flip flop. To save area, it has two complementary inputs: *en* and *enbar*. We copy the TBUFX1 cell and rename it as TBUFdX1. Now, it is time to make the necessary changes.

Firstly, we delete the inverter generating enbar fron en. Now, we add an input terminal to the pmos named *enbar* and to the nmos named *en* as below:





TBUFdX1 Schematic

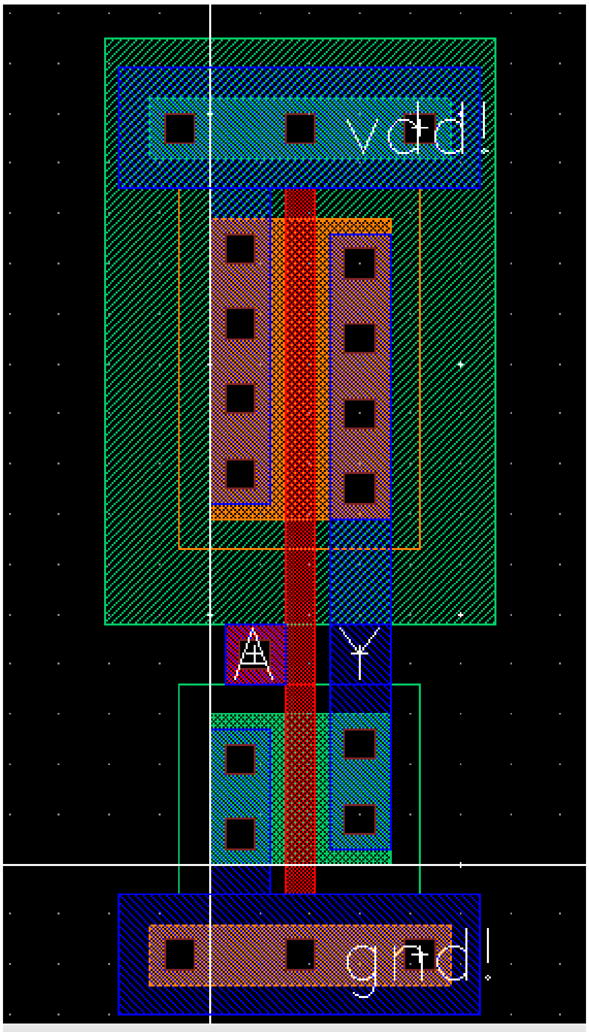
TBUFdX1 Symbol

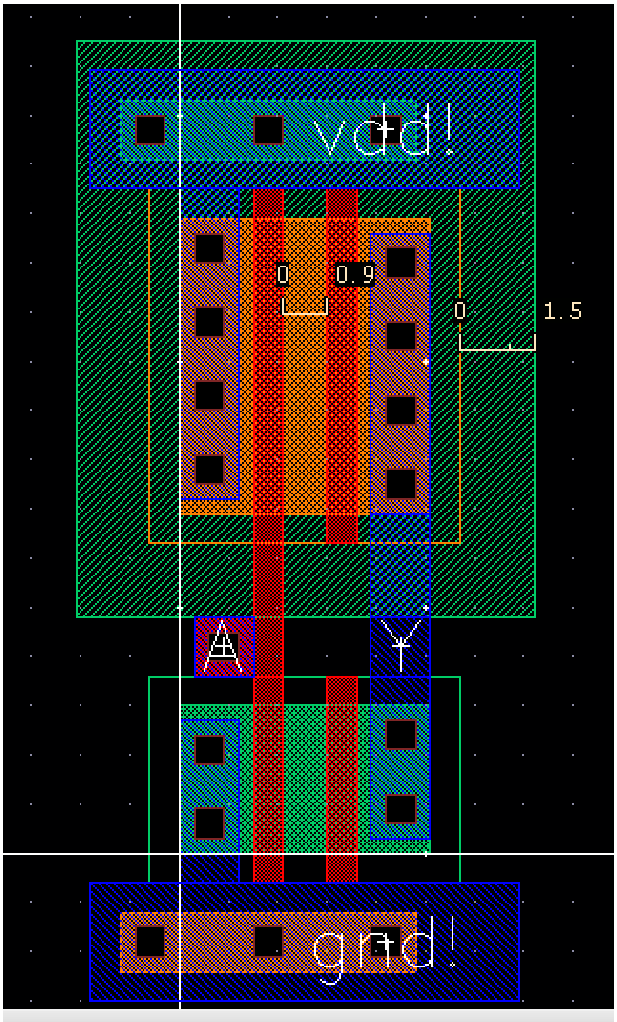
Since we'll be using multiple instances of this cell to make the DFFPOSX1, we also need to build the layout, extracted and analog_extracted views of this cell.

Looking closely at the schematic, it is seen that if we copy the INVX2 layout, it'll be the easiest to implement the layout of this cell, since we will only require to place a pmos and an nmos in series with the pre-existing layout that we made in the last semester.

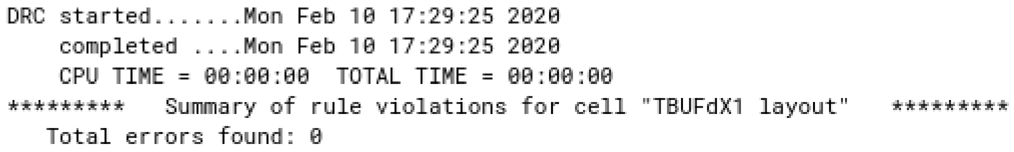
So, we copy the INVX2 layout from Lab8 of ECE520 into the ASIC_LAB2 folder and rename it as TBUFdX1 layout.

We can keep input A and output Y as-is from the INVX2 layout. We'll just need to add two more transistors in series with the two existing transistors, so the first step is shift everything to the right by 5λ to add the poly layers in between.



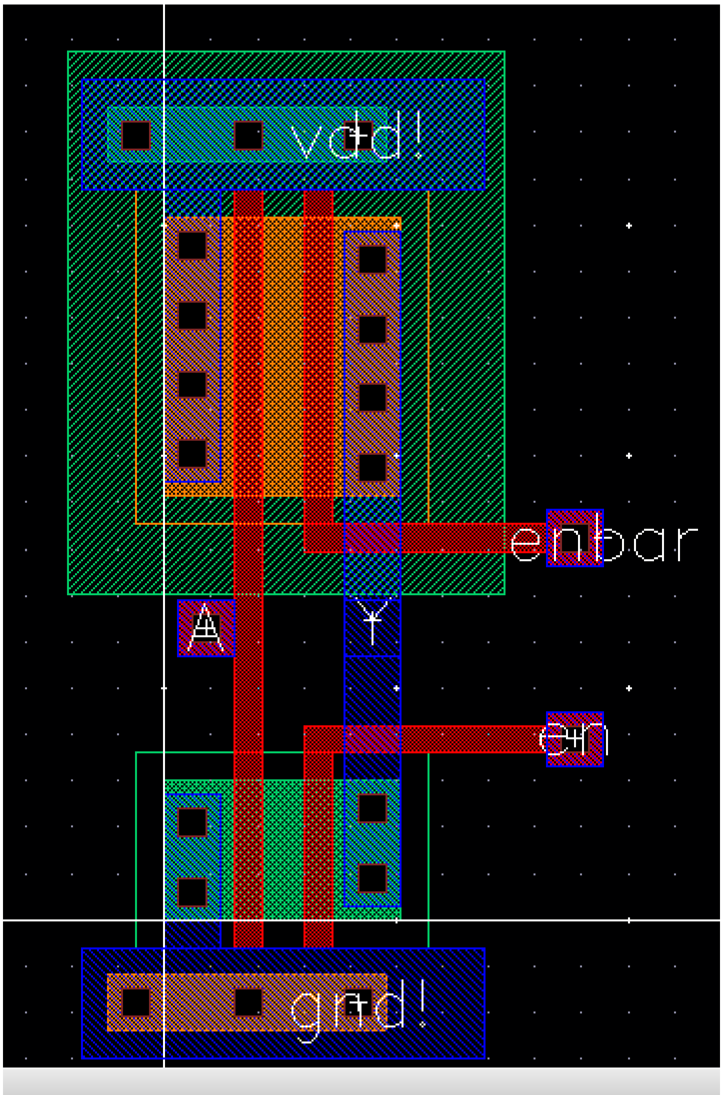


We run DRC. No errors, great.

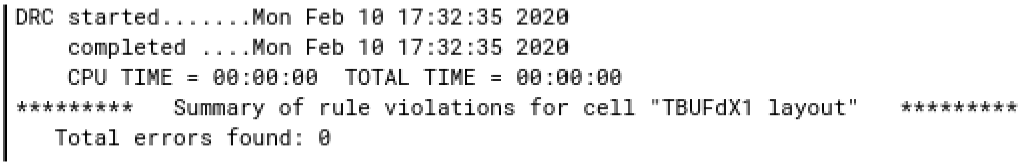


```
DRC started.......Mon Feb 10 17:29:25 2020
    completed ....Mon Feb 10 17:29:25 2020
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "TBUFdX1 layout"   *********
   Total errors found: 0
```

The next step that remains now is making the pads for en and enbar, and our layout will be done. To ensure modularity, we build the en and enbar pads on the right, instead od dragging them to the left.

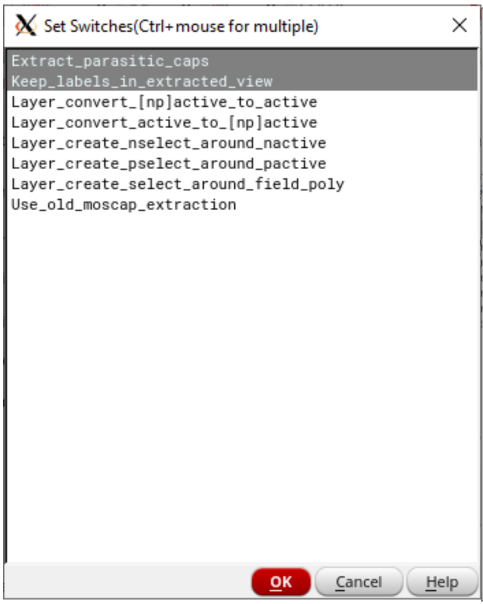


This is the final layout of TBUFdX1. We now run DRC for a final check and get no errors.



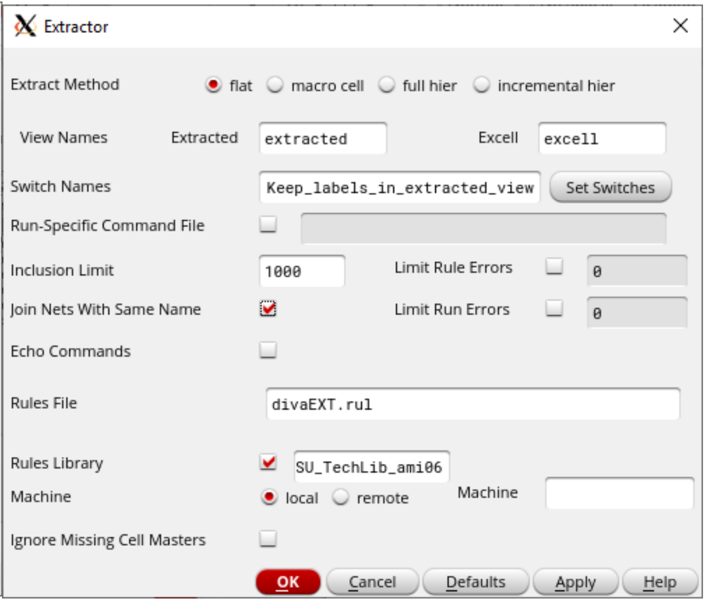
```
DRC started.......Mon Feb 10 17:32:35 2020
    completed ....Mon Feb 10 17:32:35 2020
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "TBUFdX1 layout"   *********
   Total errors found: 0
```

Now it I time to build the extracted view and run LVS.



Set Switches(Ctrl+mouse for multiple)

```
Extract_parasitic_caps
Keep_labels_in_extracted_view
Layer_convert_[np]active_to_active
Layer_convert_active_to_[np]active
Layer_create_nselect_around_nactive
Layer_create_pselect_around_pactive
Layer_create_select_around_field_poly
Use_old_moscap_extraction
```



Extractor

Extract Method ● flat ○ macro cell ○ full hier ○ incremental hier

View Names Extracted: extracted Excell: excell

Switch Names: Keep_labels_in_extracted_view

Run-Specific Command File □

Inclusion Limit: 1000 Limit Rule Errors □ 0

Join Nets With Same Name ☑ Limit Run Errors □ 0

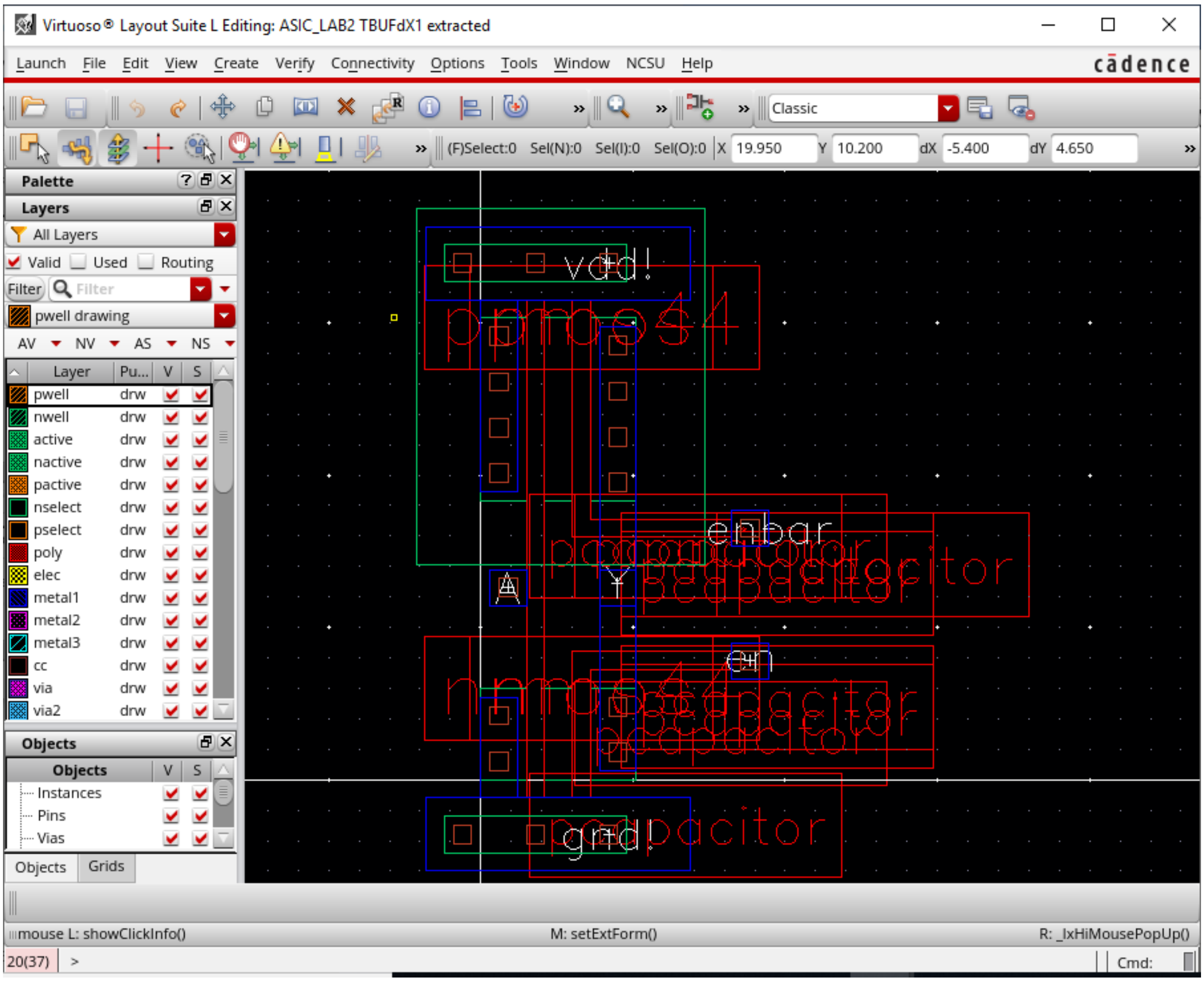
Echo Commands □

Rules File: divaEXT.rul

Rules Library ☑ SU_TechLib_ami06

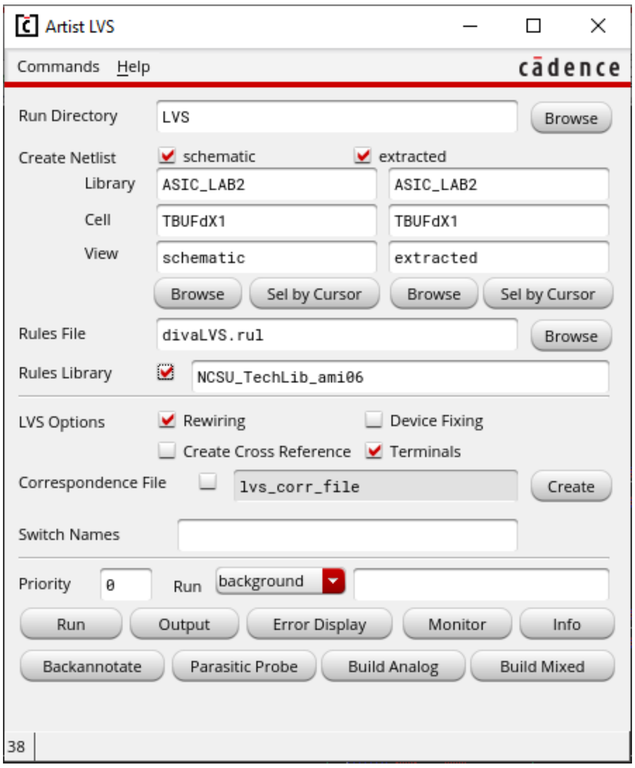
Machine ● local ○ remote Machine:

Ignore Missing Cell Masters □



Virtuoso® Layout Suite L Editing: ASIC_LAB2 TBUFdX1 extracted

TBUFdX1 extracted view



Artist LVS

Run Directory: LVS

Create Netlist: ☑ schematic ☑ extracted

	schematic	extracted
Library	ASIC_LAB2	ASIC_LAB2
Cell	TBUFdX1	TBUFdX1
View	schematic	extracted

Rules File: divaLVS.rul

Rules Library: ☑ NCSU_TechLib_ami06

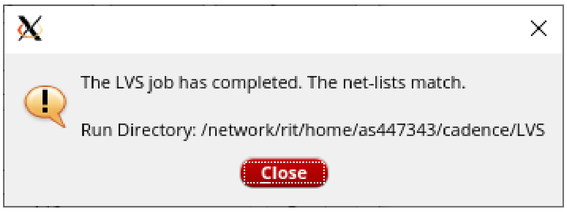
LVS Options: ☑ Rewiring □ Device Fixing □ Create Cross Reference ☑ Terminals

Correspondence File: □ lvs_corr_file

Switch Names:

Priority: 0 Run: background

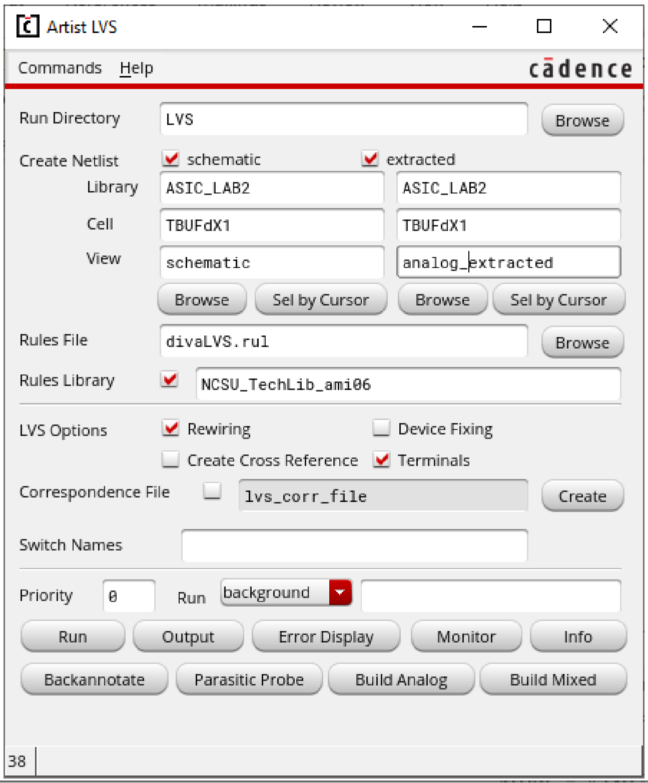
38



The LVS job has completed. The net-lists match.

Run Directory: /network/rit/home/as447343/cadence/LVS

The net-lists match. The final step is to build the analog_extracted view.



Artist LVS

Run Directory: LVS

Create Netlist: ☑ schematic ☑ extracted

	schematic	extracted
Library	ASIC_LAB2	ASIC_LAB2
Cell	TBUFdX1	TBUFdX1
View	schematic	analog_extracted

Rules File: divaLVS.rul

Rules Library: ☑ NCSU_TechLib_ami06

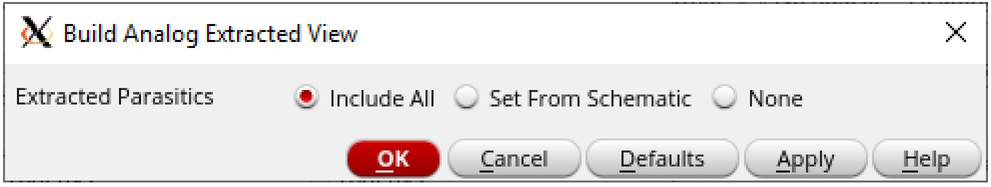
LVS Options: ☑ Rewiring □ Device Fixing □ Create Cross Reference ☑ Terminals

Correspondence File: □ lvs_corr_file

Switch Names:

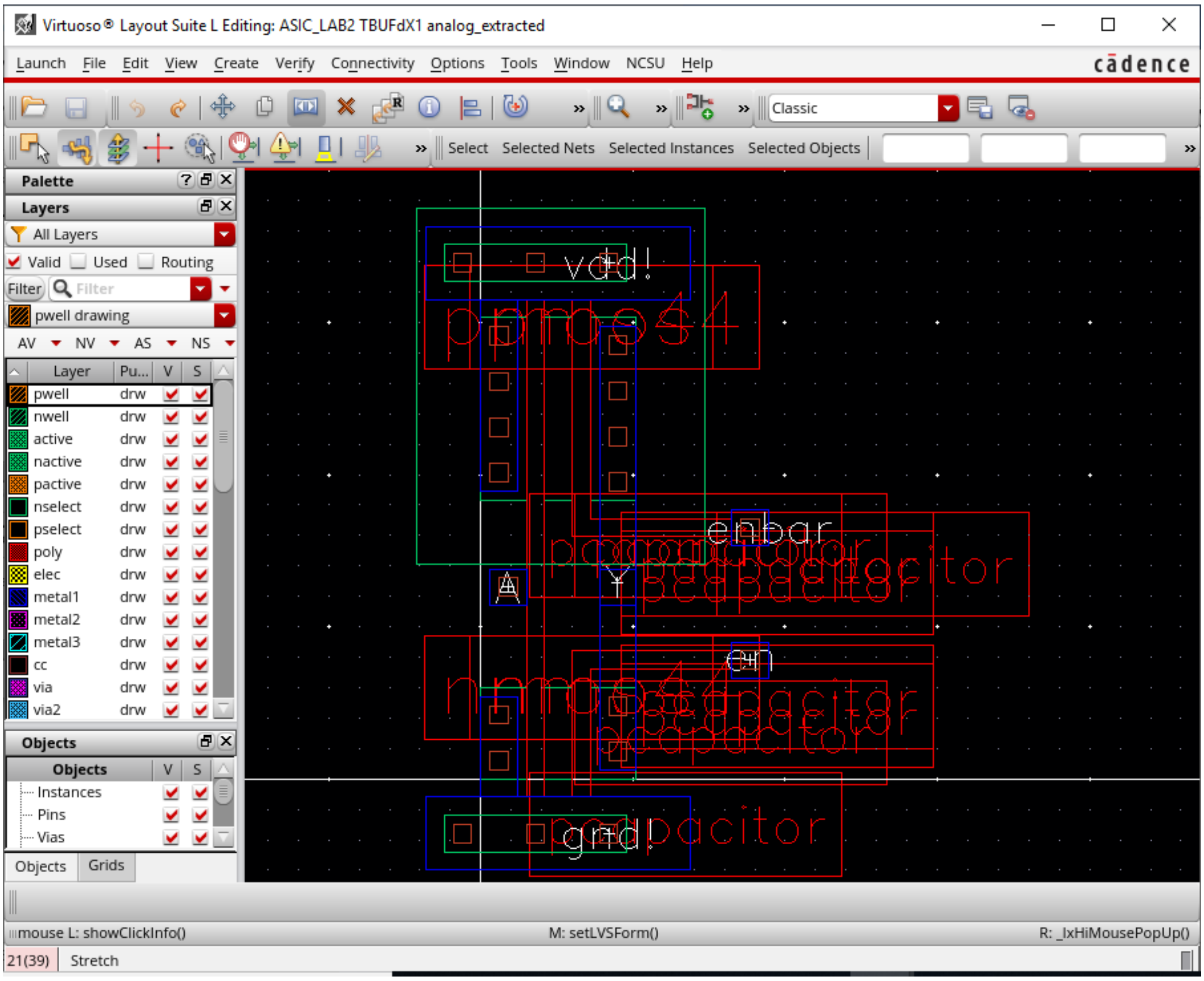
Priority: 0 Run: background

38



Build Analog Extracted View

Extracted Parasitics: ● Include All ○ Set From Schematic ○ None


Virtuoso® Layout Suite L Editing: ASIC_LAB2 TBUFdX1 analog_extracted
Launch File Edit View Create Verify Connectivity Options Tools Window NCSU Help
cadence
Classic
Select Selected Nets Selected Instances Selected Objects
Palette
Layers
All Layers
Valid Used Routing
Filter
pwell drawing
AV NV AS NS
vdd!
pmos4
enbar
A
Y
capacitor
pcapacitor
en
nmos4
gnd!
Objects
Objects
Grids
Stretch

☑ Valid □ Used □ Routing

Layer	Pu...	V	S
pwell	drw	✓	✓
nwell	drw	✓	✓
active	drw	✓	✓
nactive	drw	✓	✓
pactive	drw	✓	✓
nselect	drw	✓	✓
pselect	drw	✓	✓
poly	drw	✓	✓
elec	drw	✓	✓
metal1	drw	✓	✓
metal2	drw	✓	✓
metal3	drw	✓	✓
cc	drw	✓	✓
via	drw	✓	✓
via2	drw	✓	✓

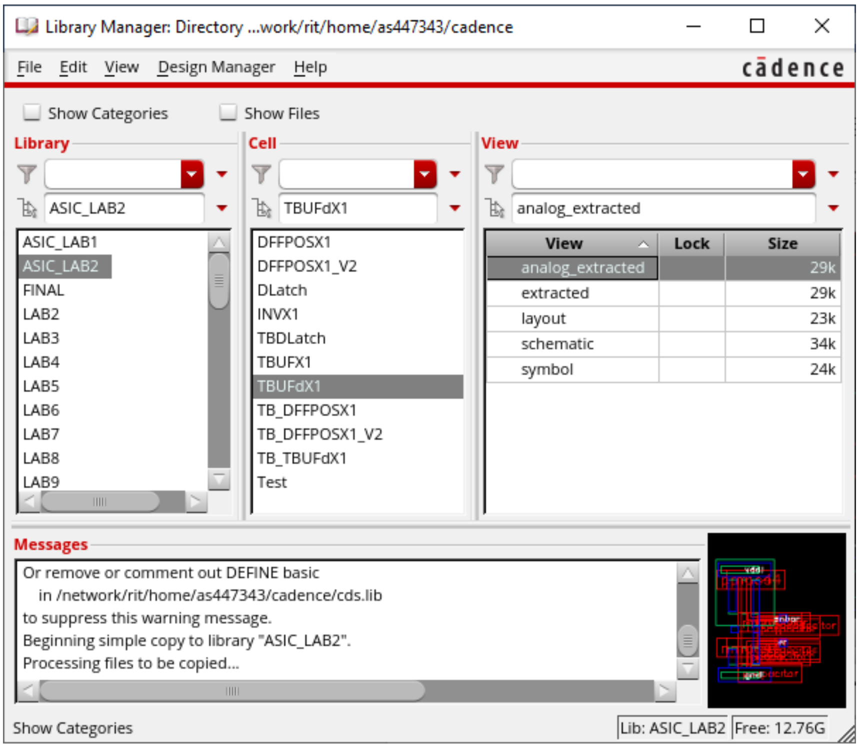
Objects	V	S
Instances	✓	✓
Pins	✓	✓
Vias	✓	✓

mouse L: showClickInfo() M: setLVSForm() R: _lxHiMousePopUp()

21(39) Stretch

TBUFdX1 analog_extracted view

Now we have 5 views for the TBUFdX1:


Library Manager: Directory ...work/rit/home/as447343/cadence
File Edit View Design Manager Help
cadence
Show Categories
Show Files
Library
Cell
View
Messages
Show Categories

Library: ASIC_LAB2

ASIC_LAB1
ASIC_LAB2
FINAL
LAB2
LAB3
LAB4
LAB5
LAB6
LAB7
LAB8
LAB9

Cell: TBUFdX1

DFFPOSX1
DFFPOSX1_V2
DLatch
INVX1
TBDLatch
TBUFX1
TBUFdX1
TB_DFFPOSX1
TB_DFFPOSX1_V2
TB_TBUFdX1
Test

View: analog_extracted

View	Lock	Size
analog_extracted		29k
extracted		29k
layout		23k
schematic		34k
symbol		24k

```
Or remove or comment out DEFINE basic
   in /network/rit/home/as447343/cadence/cds.lib
to suppress this warning message.
Beginning simple copy to library "ASIC_LAB2".
Processing files to be copied...
```

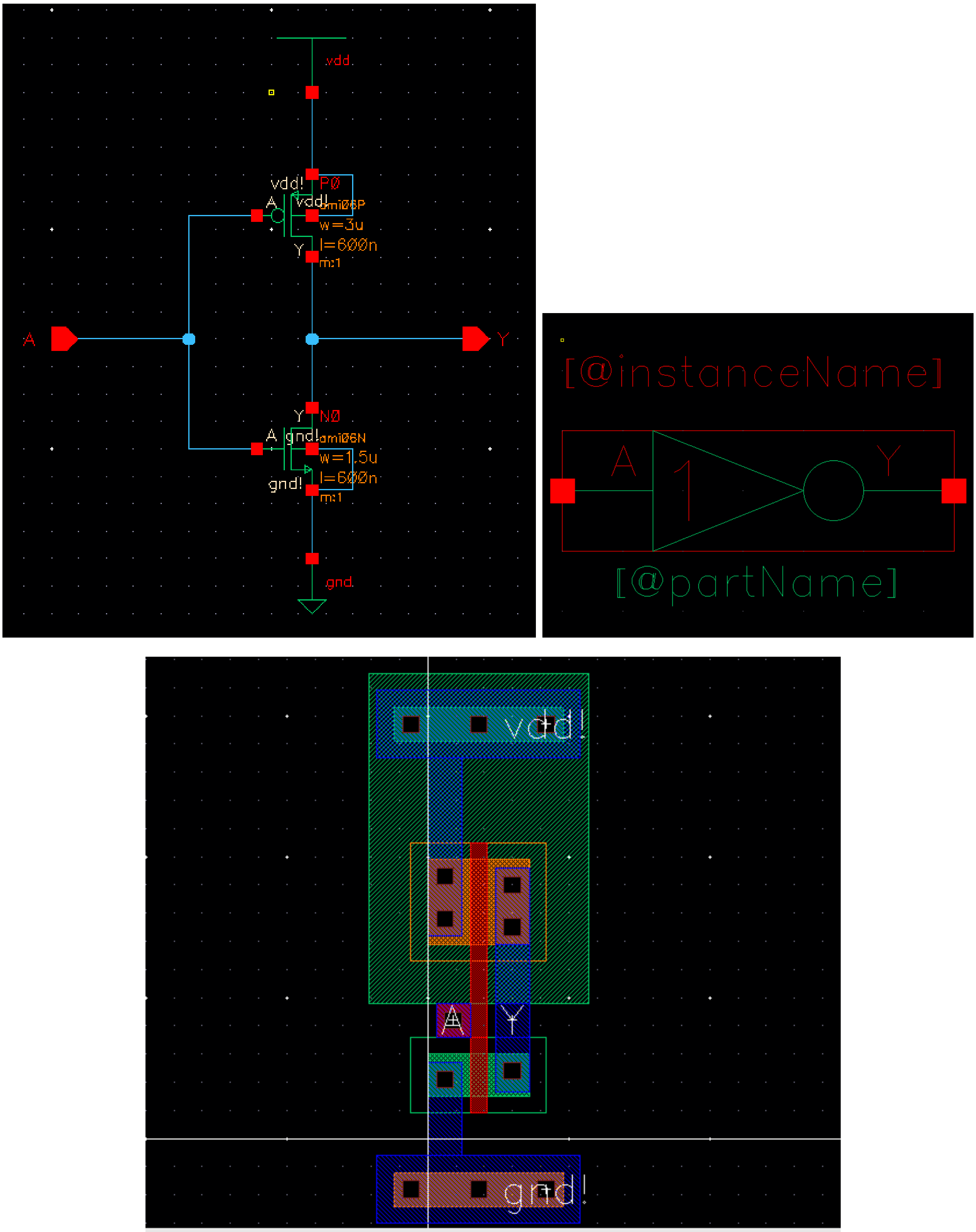
Lib: ASIC_LAB2 Free: 12.76G

3) Build DFFPOSX1

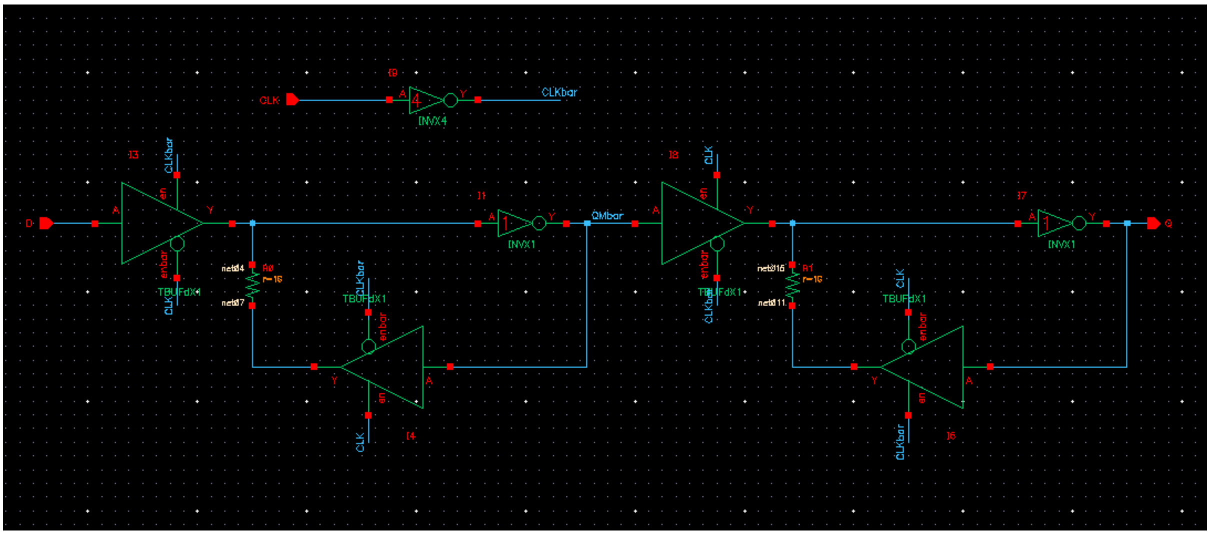
DFFPOSX1 is the most common of the three flip-flops we will use. The only cells we are using are:

TBUFdX1 and INVX1. And we will use INVX4 to invert the CLK (clock) signal.

Since we had already created INVX1 and INVX4 cells during ECE520, we will copy the same into our ASIC_LAB2 folder.



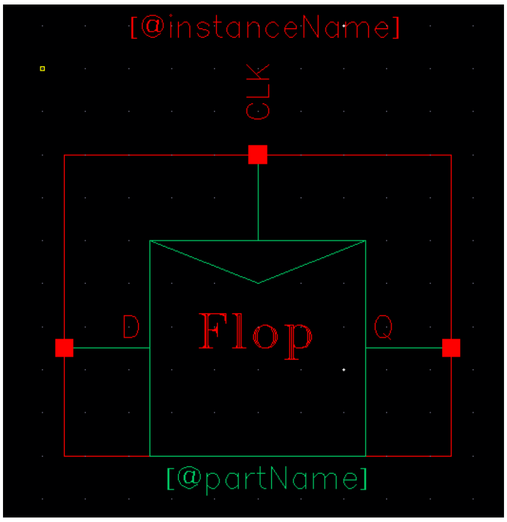
INVX1 Schematic, Symbol and Layout views



DFFPOSX1 schematic

The reason we use INVX4 with the clock is for a better driving capability without making compromise on the area. Among the INVX1, INVX2 and INVX4 which have the similar cross-sectional area, the INVX4 has the best driving capability, hence used with the clock. The outputs of the two TBUFdX1 cells in the master and slave are shorted respectively with a resistor placed in between. The resistor here serves two purposes:

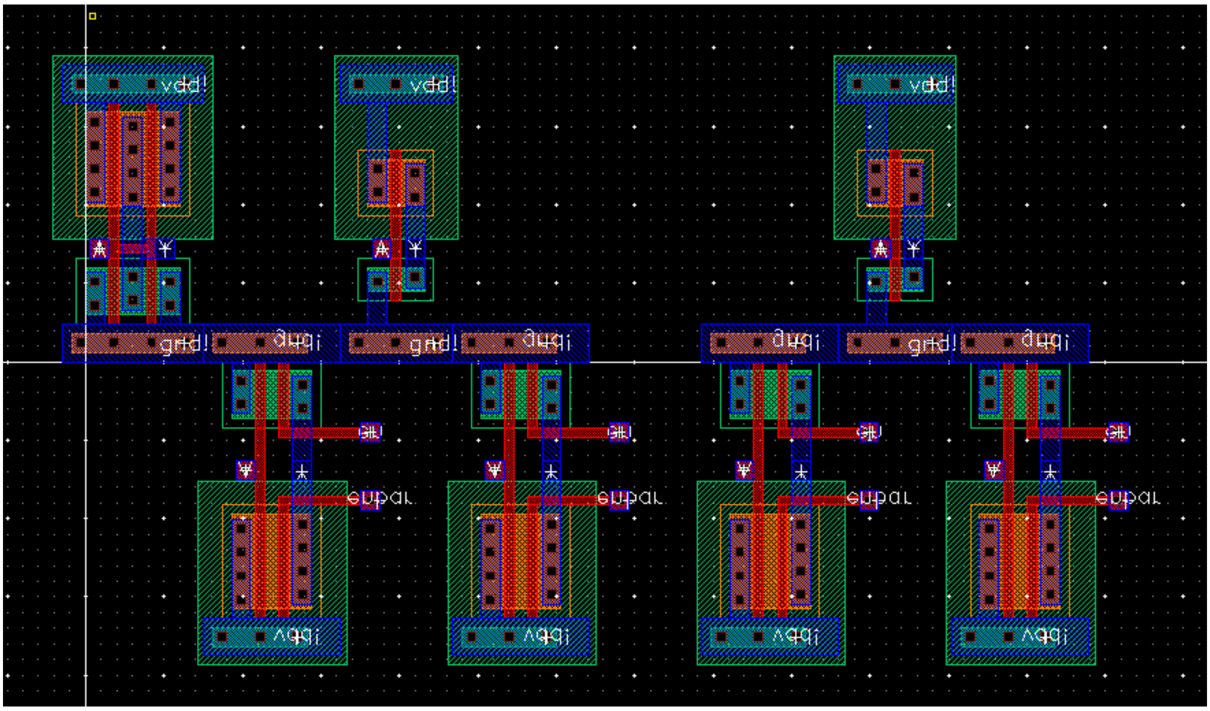
1. It prevents the direct shorting between two output terminals.
2. For testing the "Z" using a testbench, which basically represents a high impedance and holds onto the previous value, a very high resistor value ensures the same. For our experiment, we have used resistance in the 100M-1G ohm range since we are clocking our input pulses at nanosecond order. So basically, we are building the high impedance with a resistance.



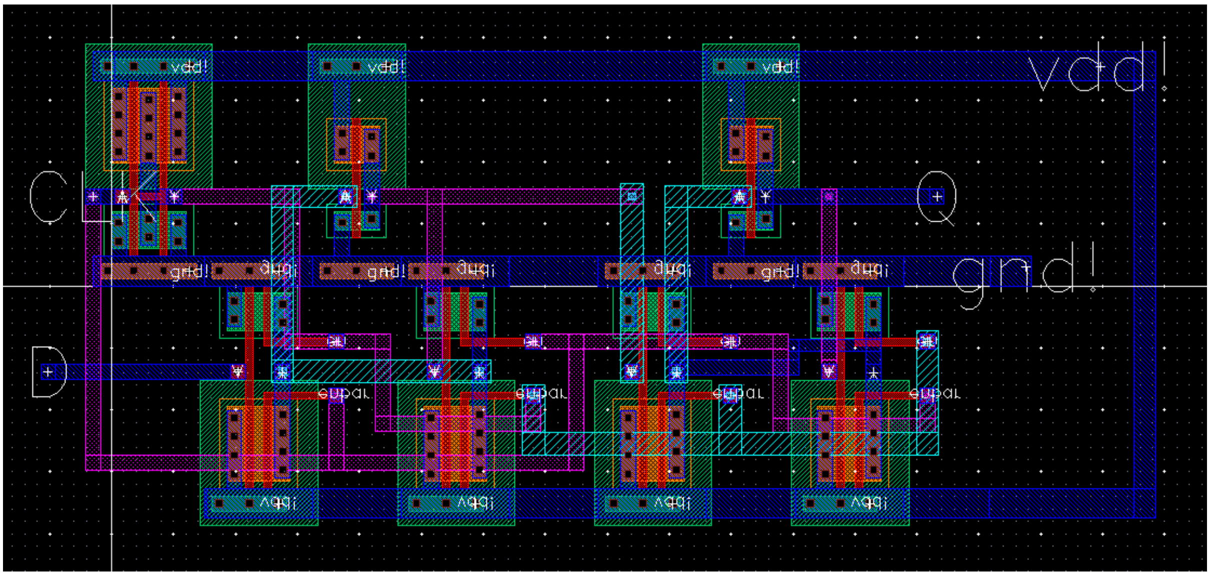
DFFPOSX1 Symbol

Now we must build the layout and test our circuit. Since we have the INVX1, INVX4 and TBUFdX1 layouts already built and tested, we can modularize them and make the necessary connections with metal1, metal2 and metal3.

We need a total of four TBUFdX1, 1 INVX4 for the clock and two INVX1 for the master and slave respectively.

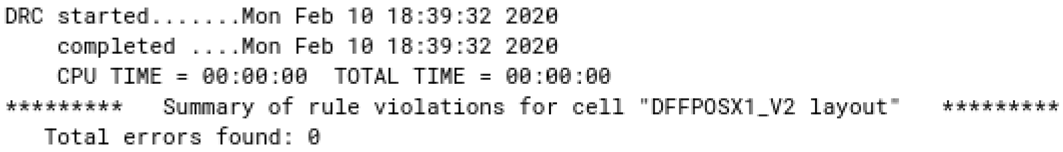


We place them like this in order to avoid routing problems and create one common gnd! terminal easily. It is now time to make the connections, referring the schematic.

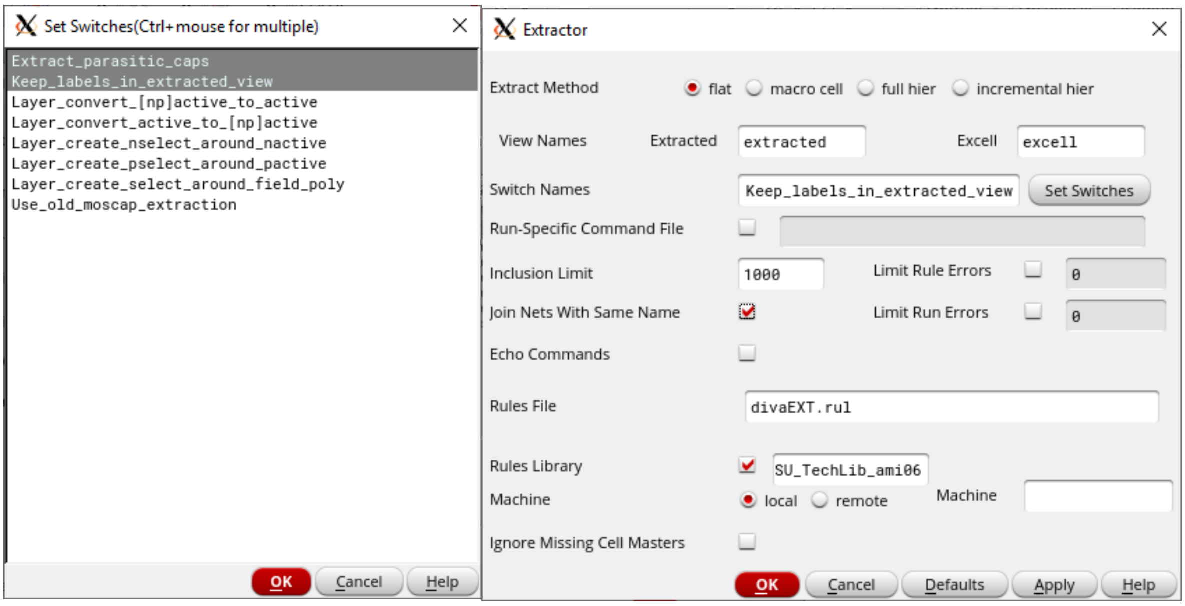


The completed layout looks like this. The two vdd!s have been joined since the layout can only have a single vdd! and gnd! terminals.

We verify DRC and get no errors.


```
DRC started.......Mon Feb 10 18:39:32 2020
    completed ....Mon Feb 10 18:39:32 2020
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "DFFPOSX1_V2 layout"   *********
   Total errors found: 0
```

Now we must create the extracted view and do LVS.



Set Switches(Ctrl+mouse for multiple)

```
Extract_parasitic_caps
Keep_labels_in_extracted_view
Layer_convert_[np]active_to_active
Layer_convert_active_to_[np]active
Layer_create_nselect_around_nactive
Layer_create_pselect_around_pactive
Layer_create_select_around_field_poly
Use_old_moscap_extraction
```

Extractor

Extract Method ● flat ○ macro cell ○ full hier ○ incremental hier

View Names Extracted extracted Excell excell

Switch Names Keep_labels_in_extracted_view

Run-Specific Command File □

Inclusion Limit 1000 Limit Rule Errors □ 0

Join Nets With Same Name ☑ Limit Run Errors □ 0

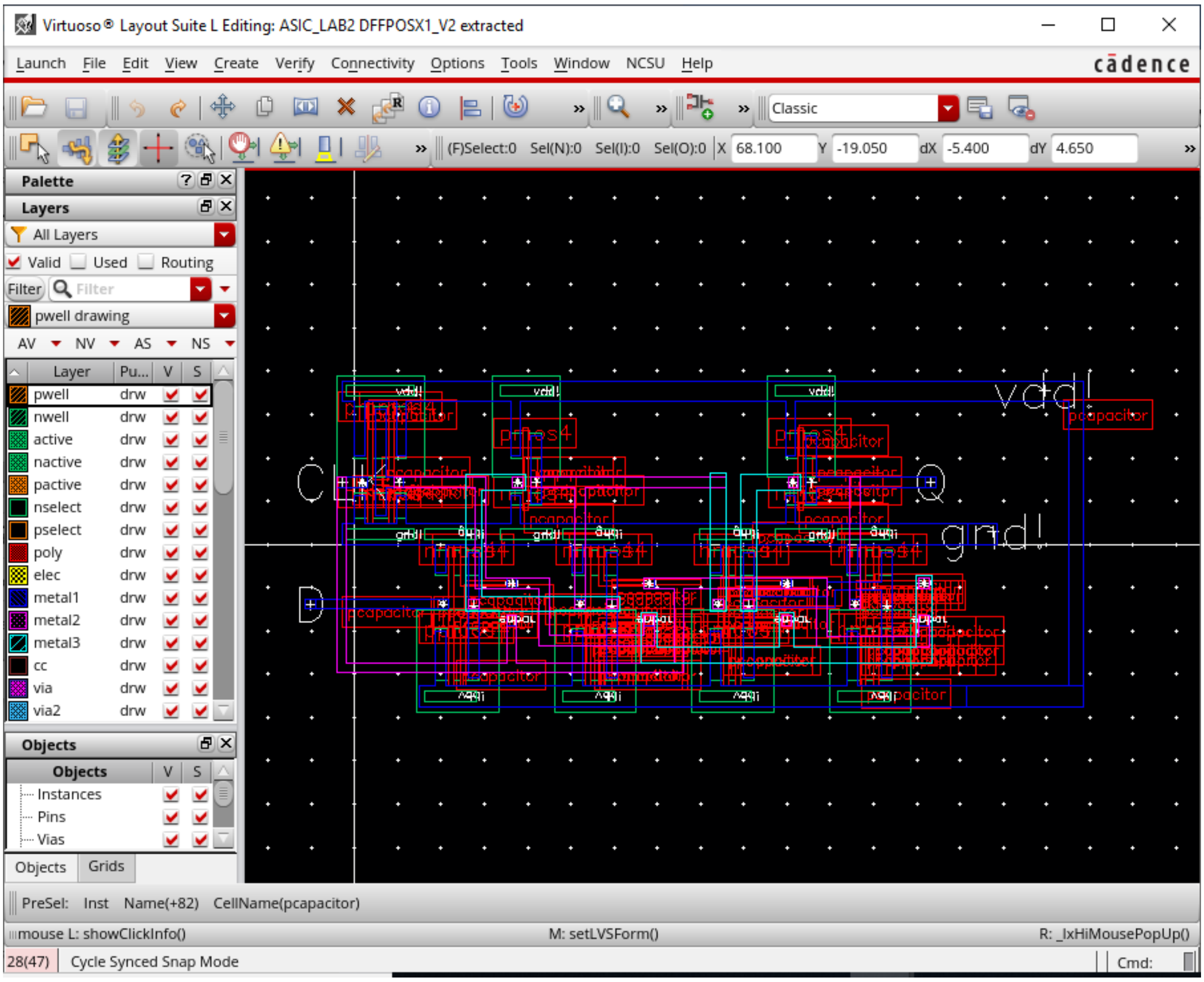
Echo Commands □

Rules File divaEXT.rul

Rules Library ☑ SU_TechLib_ami06

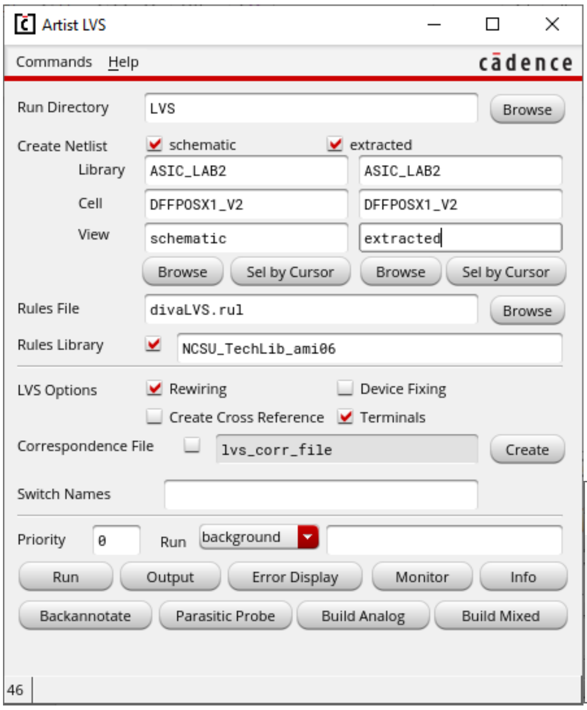
Machine ● local ○ remote Machine

Ignore Missing Cell Masters □



Virtuoso® Layout Suite L Editing: ASIC_LAB2 DFFPOSX1_V2 extracted

DFFPOSX1 extracted view



Artist LVS

Run Directory: LVS

Create Netlist: ☑ schematic ☑ extracted

Library: ASIC_LAB2 | ASIC_LAB2

Cell: DFFPOSX1_V2 | DFFPOSX1_V2

View: schematic | extracted

Rules File: divaLVS.rul

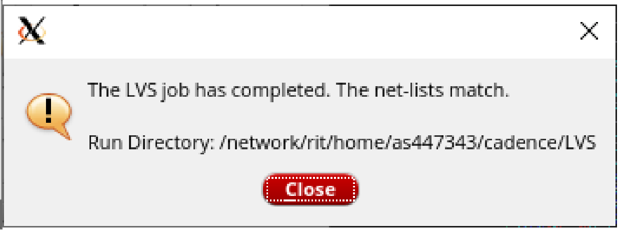
Rules Library: ☑ NCSU_TechLib_ami06

LVS Options: ☑ Rewiring □ Device Fixing □ Create Cross Reference ☑ Terminals

Correspondence File: □ lvs_corr_file

Switch Names:

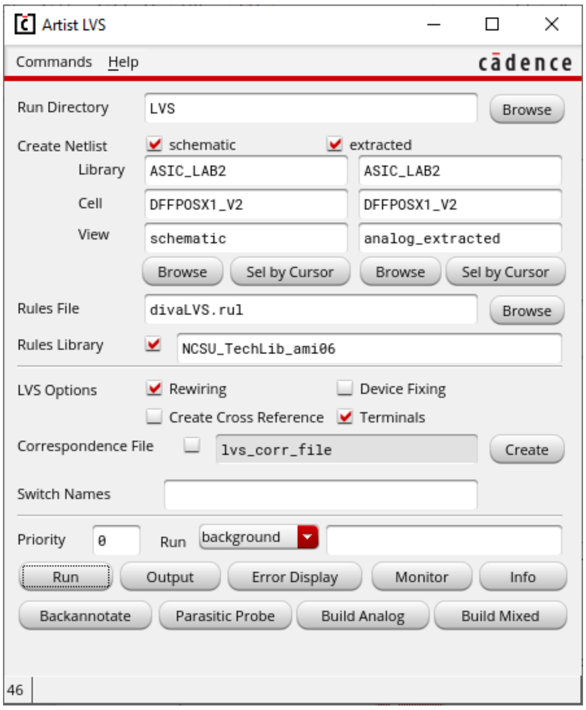
Priority: 0 Run: background



The LVS job has completed. The net-lists match.

Run Directory: /network/rit/home/as447343/cadence/LVS

Now we will build the analog_extracted view.



Artist LVS

Run Directory: LVS

Create Netlist: ☑ schematic ☑ extracted

Library: ASIC_LAB2 | ASIC_LAB2

Cell: DFFPOSX1_V2 | DFFPOSX1_V2

View: schematic | analog_extracted

Rules File: divaLVS.rul

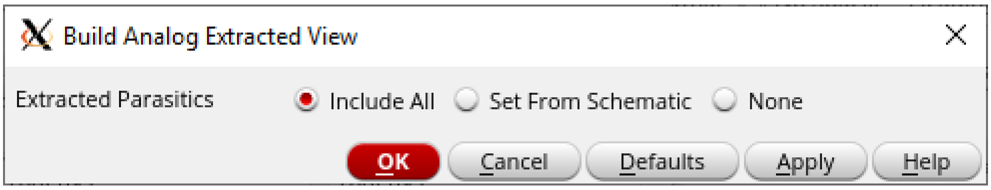
Rules Library: ☑ NCSU_TechLib_ami06

LVS Options: ☑ Rewiring □ Device Fixing □ Create Cross Reference ☑ Terminals

Correspondence File: □ lvs_corr_file

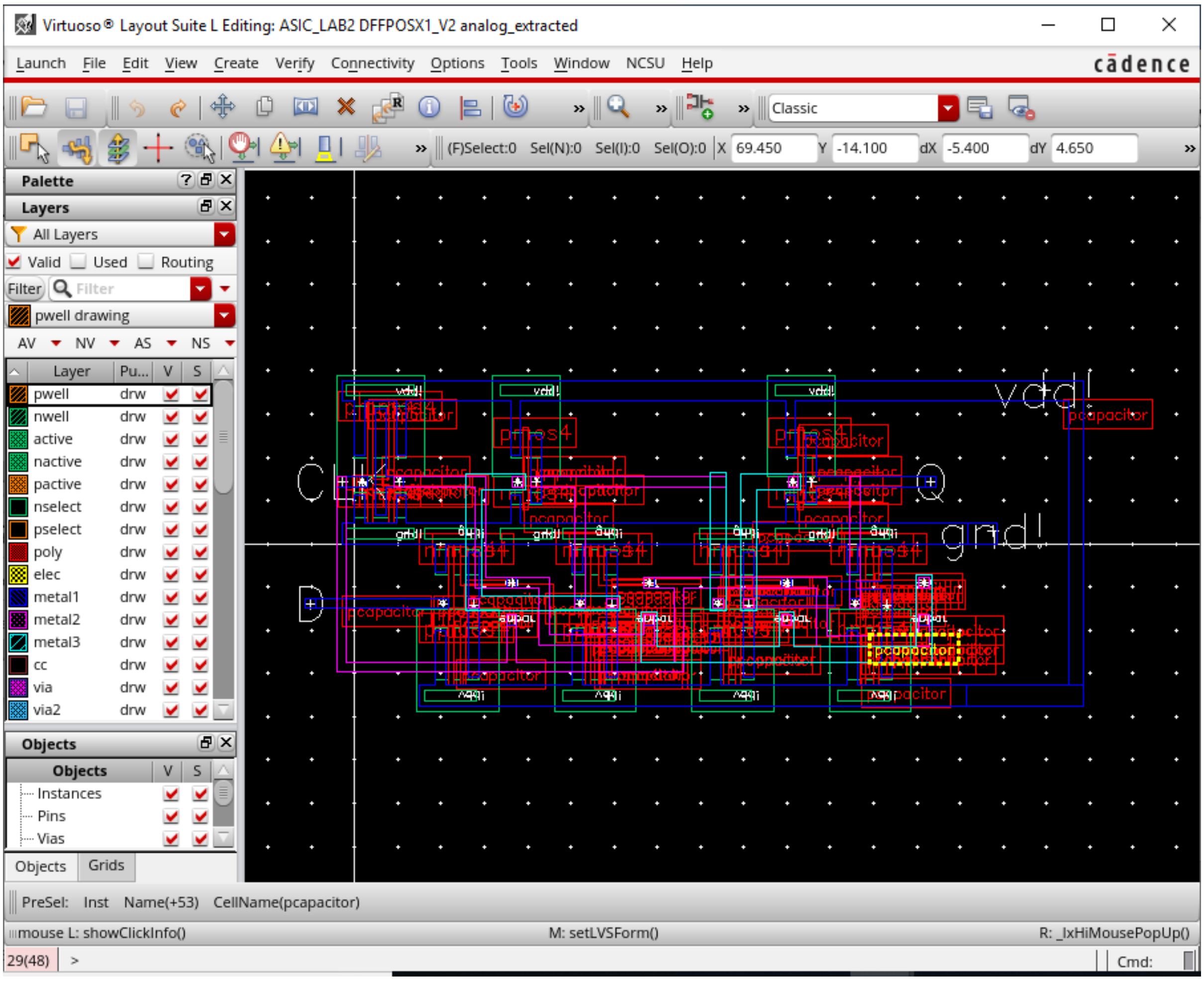
Switch Names:

Priority: 0 Run: background



Build Analog Extracted View

Extracted Parasitics: ● Include All ○ Set From Schematic ○ None



(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X 69.450 Y -14.100 dX -5.400 dY 4.650

Layer	Pu...	V	S
pwell	drw	☑	☑
nwell	drw	☑	☑
active	drw	☑	☑
nactive	drw	☑	☑
pactive	drw	☑	☑
nselect	drw	☑	☑
pselect	drw	☑	☑
poly	drw	☑	☑
elec	drw	☑	☑
metal1	drw	☑	☑
metal2	drw	☑	☑
metal3	drw	☑	☑
cc	drw	☑	☑
via	drw	☑	☑
via2	drw	☑	☑

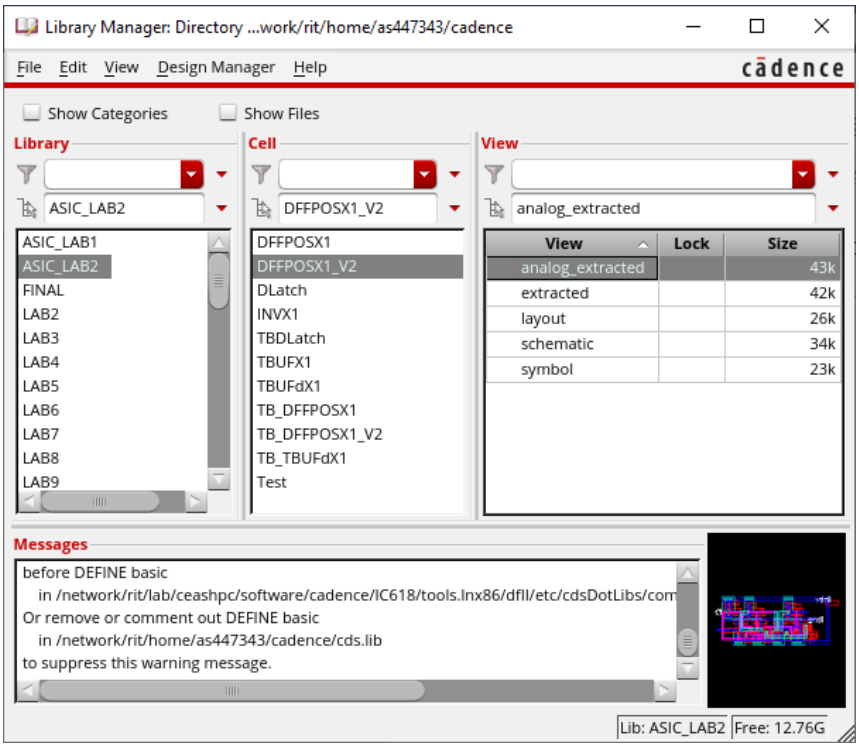
PreSel: Inst Name(+53) CellName(pcapacitor)

mouse L: showClickInfo() M: setLVSForm() R: _lxHiMousePopUp()

29(48) > Cmd:

DFFPOSX1 analog_extracted view

Now we have 5 views for the DFFPOSX1:


Library Manager: Directory ...work/rit/home/as447343/cadence
File Edit View Design Manager Help
cadence
Show Categories
Show Files
Library
Cell
View
Messages

Library: ASIC_LAB2 — Cell: DFFPOSX1_V2 — View: analog_extracted

Library: ASIC_LAB1, ASIC_LAB2, FINAL, LAB2, LAB3, LAB4, LAB5, LAB6, LAB7, LAB8, LAB9

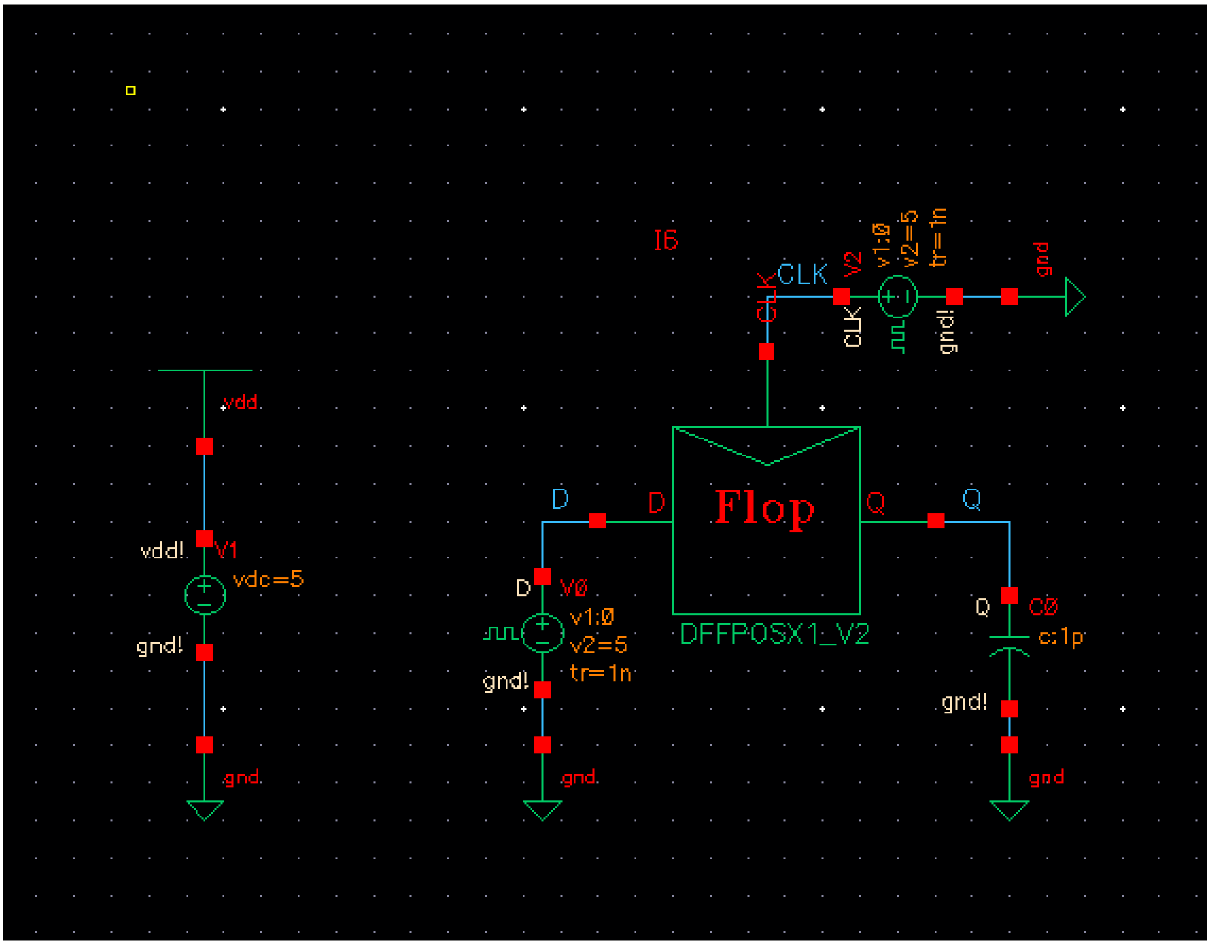
Cell: DFFPOSX1, DFFPOSX1_V2, DLatch, INVX1, TBDLatch, TBUFX1, TBUFdX1, TB_DFFPOSX1, TB_DFFPOSX1_V2, TB_TBUFdX1, Test

View	Lock	Size
analog_extracted		43k
extracted		42k
layout		26k
schematic		34k
symbol		23k

```
before DEFINE basic
   in /network/rit/lab/ceashpc/software/cadence/IC618/tools.lnx86/dfII/etc/cdsDotLibs/com
Or remove or comment out DEFINE basic
   in /network/rit/home/as447343/cadence/cds.lib
to suppress this warning message.
```

Lib: ASIC_LAB2 Free: 12.76G

Now we will create a testbench to test the DFFPOSX1 cell that we created.



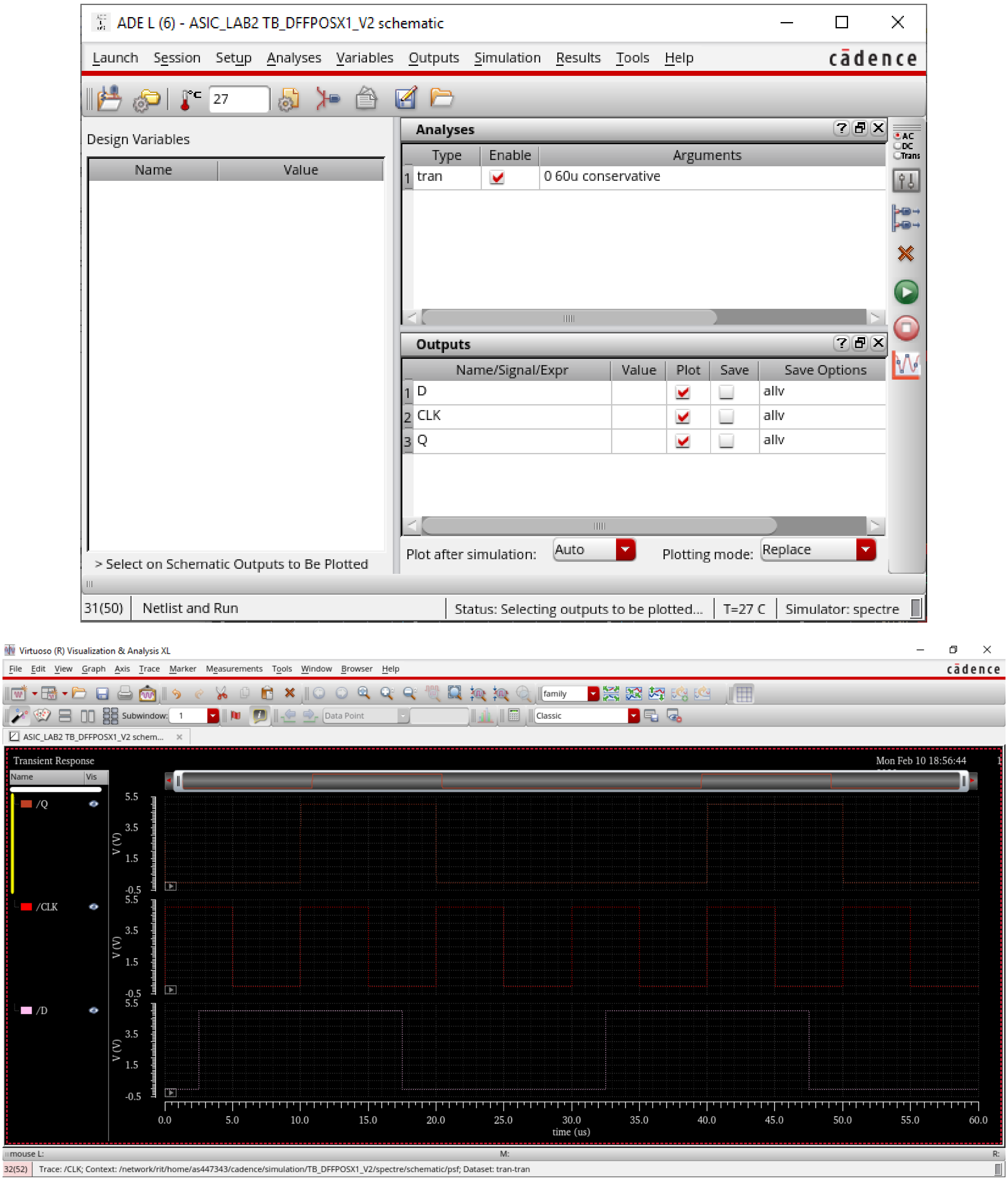
TB_DFFPOSX1 schematic

The values of D, CLK and C0 are as follows:

CLK: V1 – 0V, V2 – 5V, Delay – 0ns, Rise/Fall time – 1ns, Pulse width - 5µs, Period - 10µs

D: V1 – 0V, V2 – 5V, Delay – 2.5µs, Rise/Fall time – 1ns, Pulse width - 15µs, Period - 30µs

C0: 1pF



ADE L (6) - ASIC_LAB2 TB_DFFPOSX1_V2 schematic

Analyses

	Type	Enable	Arguments
1	tran	✓	0 60u conservative

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	D		✓	□	allv
2	CLK		✓	□	allv
3	Q		✓	□	allv

Plot after simulation: Auto   Plotting mode: Replace

> Select on Schematic Outputs to Be Plotted

31(50) | Netlist and Run | Status: Selecting outputs to be plotted... | T=27 C | Simulator: spectre

Virtuoso (R) Visualization & Analysis XL

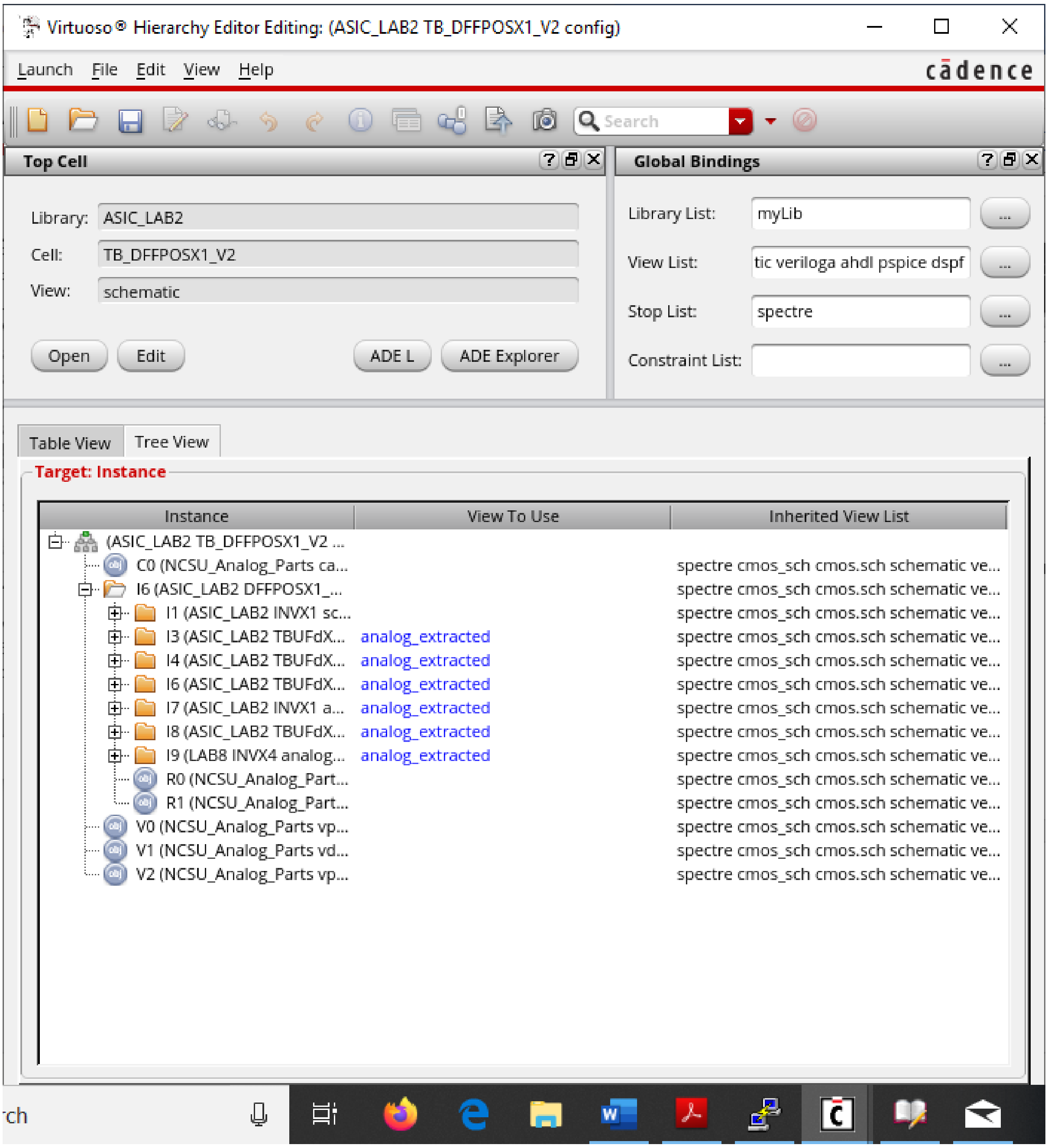
32(52) | Trace: /CLK; Context: /network/rit/home/as447343/cadence/simulation/TB_DFFPOSX1_V2/spectre/schematic/psf; Dataset: tran-tran

TB_DFFPOSX1 Schematic-only ADE L and Output Waveform

As seen from the output Q, it matches with the class notes and hence is working fine according to the following principle:

- When CLK rises, D is copied to Q
- At all other times, Q holds its value

Now we must verify the working of the flip-flop taking the layout and parasitic components into account. For that we will build the config view of the test bench TB_DFFPOSX1 and do the same analysis.

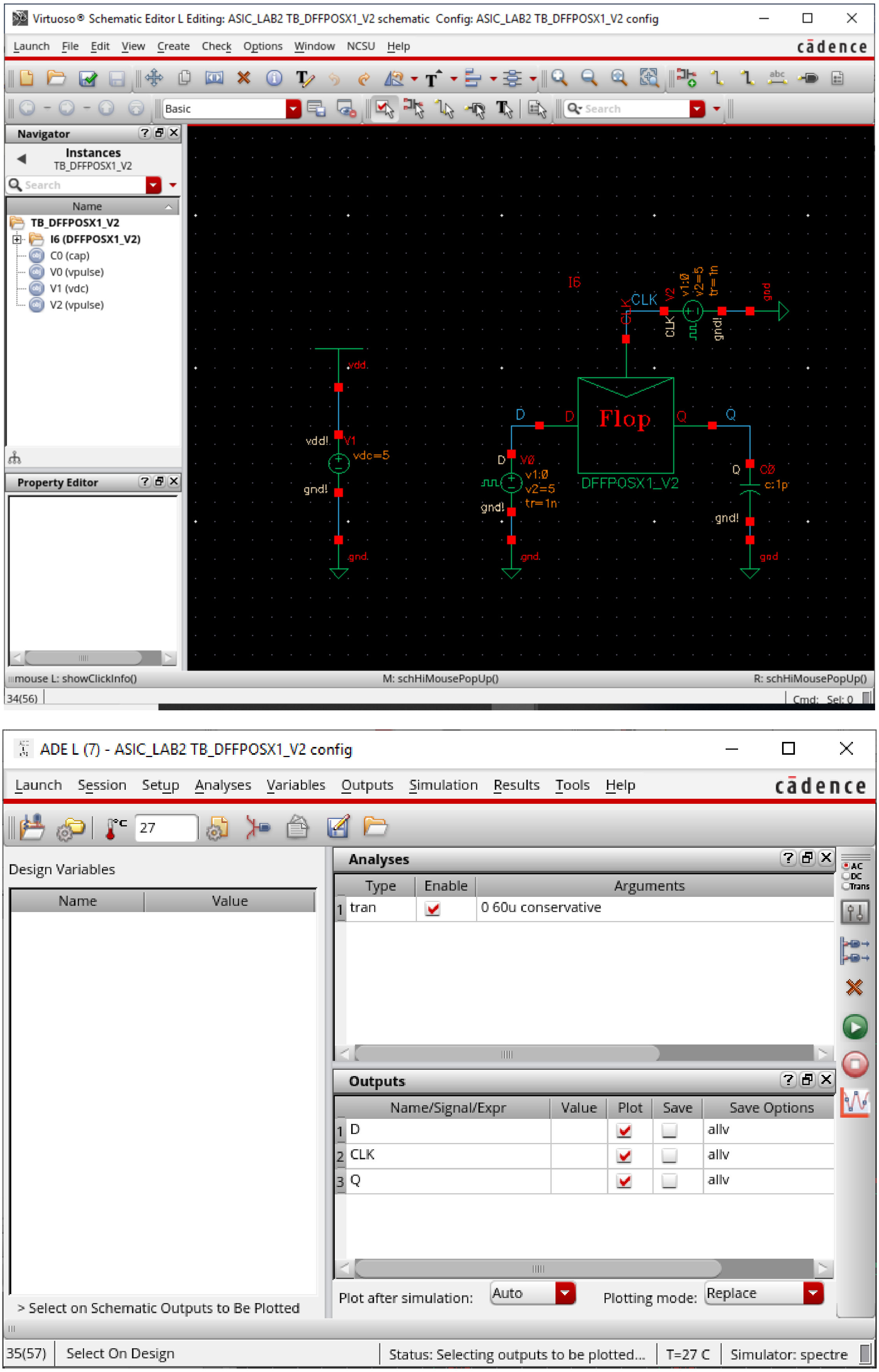


Library: ASIC_LAB2
Cell: TB_DFFPOSX1_V2
View: schematic

Library List: myLib
View List: tic veriloga ahdl pspice dspf
Stop List: spectre
Constraint List:

Instance	View To Use	Inherited View List
(ASIC_LAB2 TB_DFFPOSX1_V2 ...		
C0 (NCSU_Analog_Parts ca...		spectre cmos_sch cmos.sch schematic ve...
I6 (ASIC_LAB2 DFFPOSX1_...		spectre cmos_sch cmos.sch schematic ve...
I1 (ASIC_LAB2 INVX1 sc...		spectre cmos_sch cmos.sch schematic ve...
I3 (ASIC_LAB2 TBUFdX...	analog_extracted	spectre cmos_sch cmos.sch schematic ve...
I4 (ASIC_LAB2 TBUFdX...	analog_extracted	spectre cmos_sch cmos.sch schematic ve...
I6 (ASIC_LAB2 TBUFdX...	analog_extracted	spectre cmos_sch cmos.sch schematic ve...
I7 (ASIC_LAB2 INVX1 a...	analog_extracted	spectre cmos_sch cmos.sch schematic ve...
I8 (ASIC_LAB2 TBUFdX...	analog_extracted	spectre cmos_sch cmos.sch schematic ve...
I9 (LAB8 INVX4 analog...	analog_extracted	spectre cmos_sch cmos.sch schematic ve...
R0 (NCSU_Analog_Part...		spectre cmos_sch cmos.sch schematic ve...
R1 (NCSU_Analog_Part...		spectre cmos_sch cmos.sch schematic ve...
V0 (NCSU_Analog_Parts vp...		spectre cmos_sch cmos.sch schematic ve...
V1 (NCSU_Analog_Parts vd...		spectre cmos_sch cmos.sch schematic ve...
V2 (NCSU_Analog_Parts vp...		spectre cmos_sch cmos.sch schematic ve...

We set the cell instances of the TBUFdX1, INVX1 and INVX4 as *analog_extracted*. This will take the layout based parasitics into account.



Type	Enable	Arguments
tran	☑	0 60u conservative

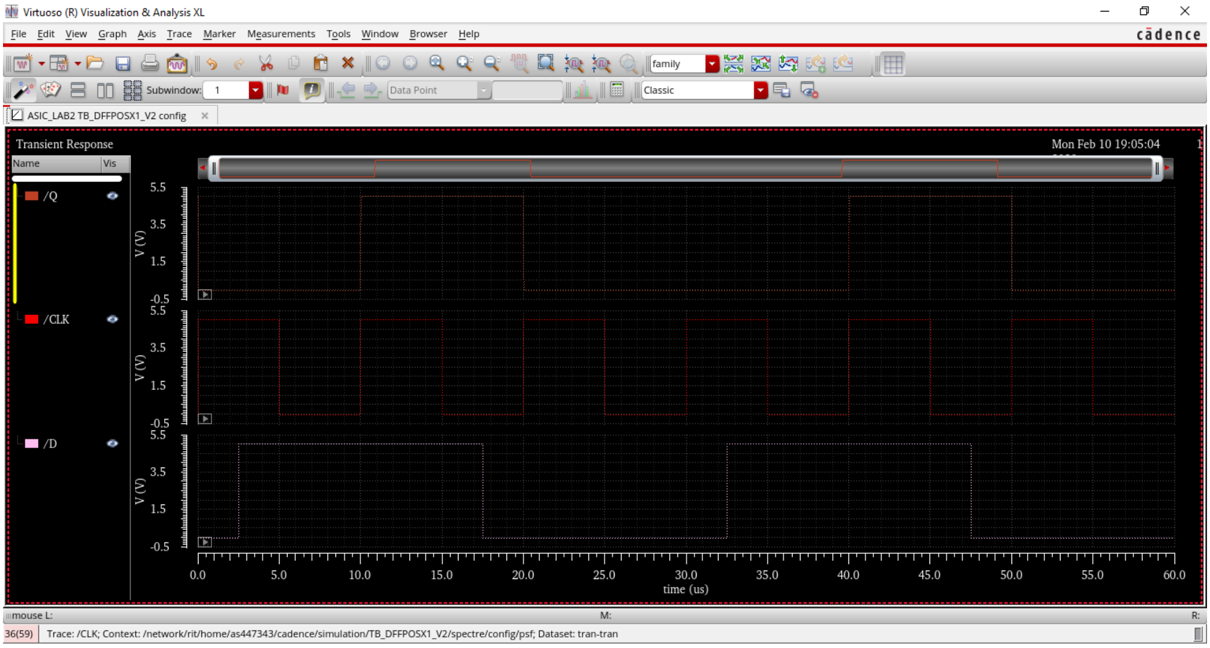
	Name/Signal/Expr	Value	Plot	Save	Save Options
1	D		☑	☐	allv
2	CLK		☑	☐	allv
3	Q		☑	☐	allv

Plot after simulation: Auto Plotting mode: Replace

> Select on Schematic Outputs to Be Plotted

35(57) Select On Design Status: Selecting outputs to be plotted... T=27 C Simulator: spectre

TB_DFFPOSX1 config ADE L



36(59) Trace: /CLK; Context: /network/rit/home/as447343/cadence/simulation/TB_DFFPOSX1_V2/spectre/config/psf; Dataset: tran-tran

TB_DFFPOSX1 Output Waveform including parasitics

Both the waveforms are identical and matches with the lecture slides. It confirms that the cells are performing correctly.