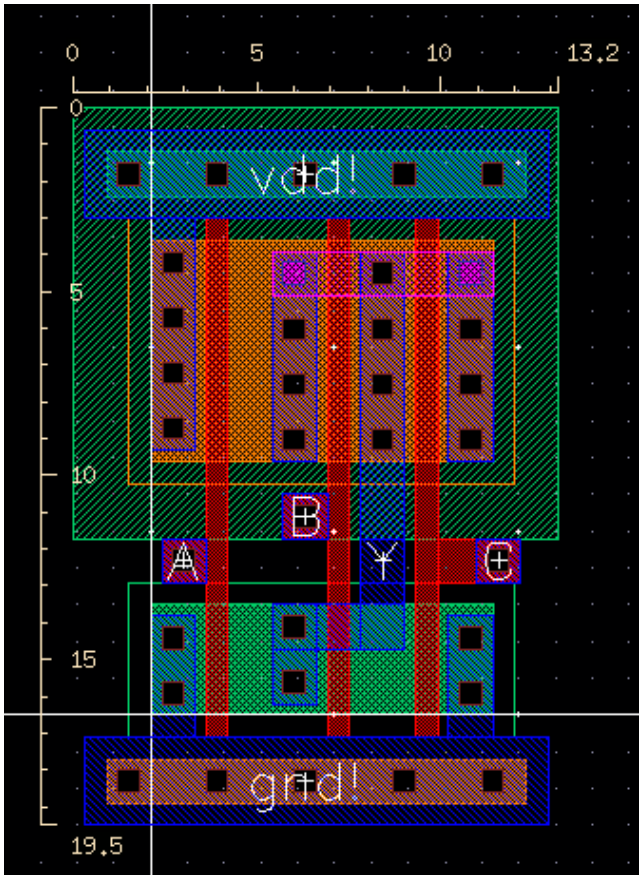
Project 1, ECE 521 – Digital ASIC Design

Name: Arijit Sengupta, ID: 001441748

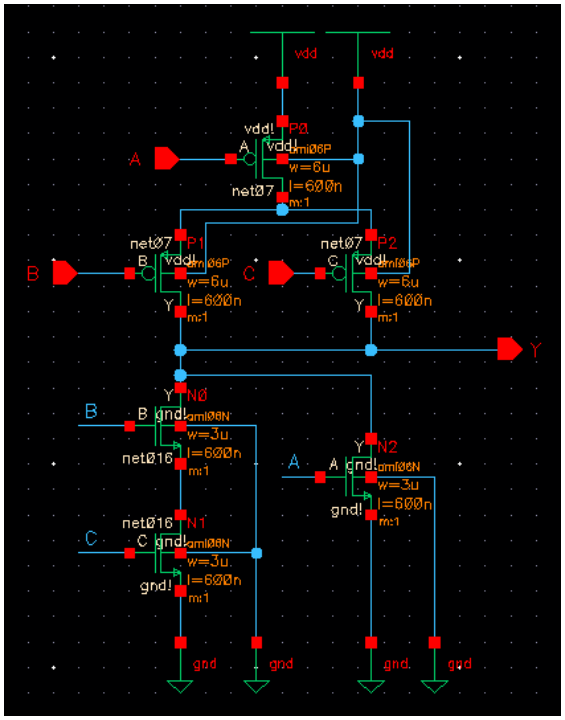
Cell Name	Area (μ^2)	Delay (ps)			
		A->Y	B->Y	C->Y	D->Y
AOI21X1	257.40	141.14	109.1	141.14	N/A
AOI22X1	355.77	280.7	143.1	143.1	205.8
OAI21X1	301.28	132.4	240.8	292.9	N/A
OAI22X1	345.15	224.6	126.6	144.1	228.8
TBUFdX1	205.02	196.1	N/A	N/A	N/A
DFFPOSX1	1766.79	428.3 (CLK->Q)	N/A	N/A	N/A
MUX2X1	789.93	292.6	263.5	202.4 (S->Y)	N/A
INVX1	152.10	168.0	N/A	N/A	N/A
INVX2	152.10	129.2	N/A	N/A	N/A
INVX4	198.90	88.32	N/A	N/A	N/A
INVX8	304.20	76.25	N/A	N/A	N/A
NOR2X1	193.05	114.2	187.7	N/A	N/A
NAND2X1	198.90	287.6	254.7	N/A	N/A
XOR2X1	441.68	246.5	263.0	N/A	N/A
XNOR2X1	441.68	270.4	314.8	N/A	N/A

Schematic, Symbol and Layout of Standard Cells:

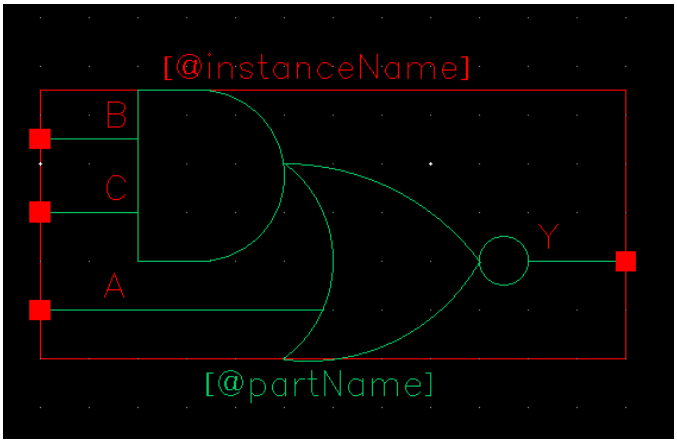
AOI21X1:



AOI21X1 Layout

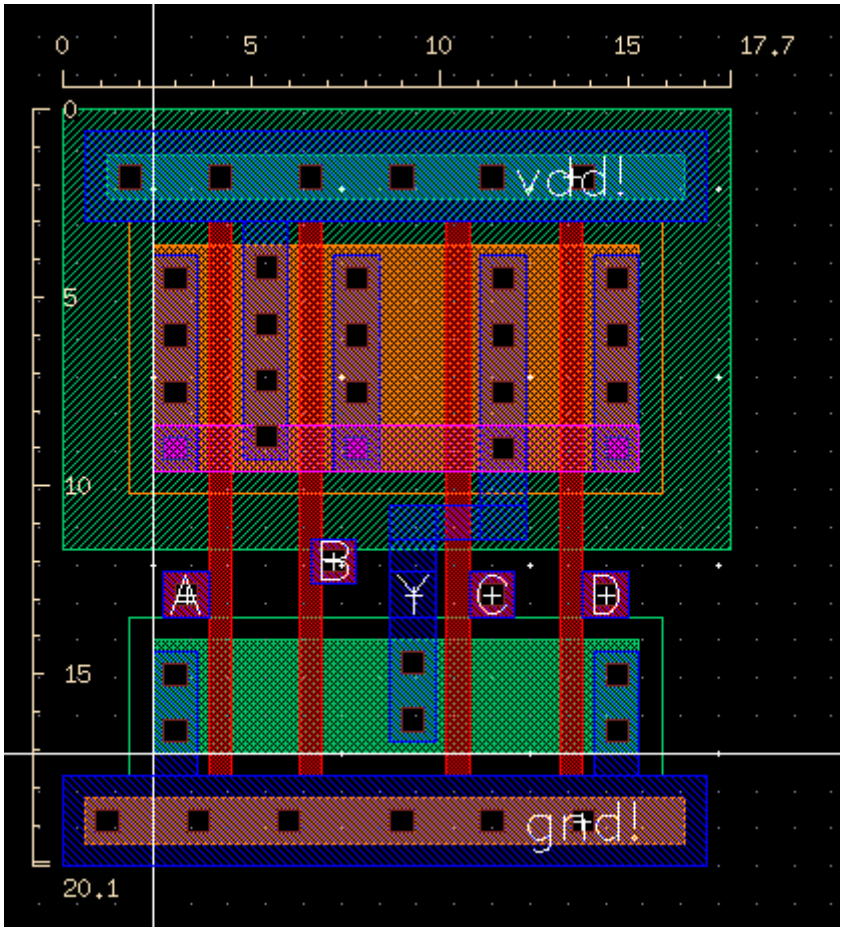


AOI21X1 Schematic

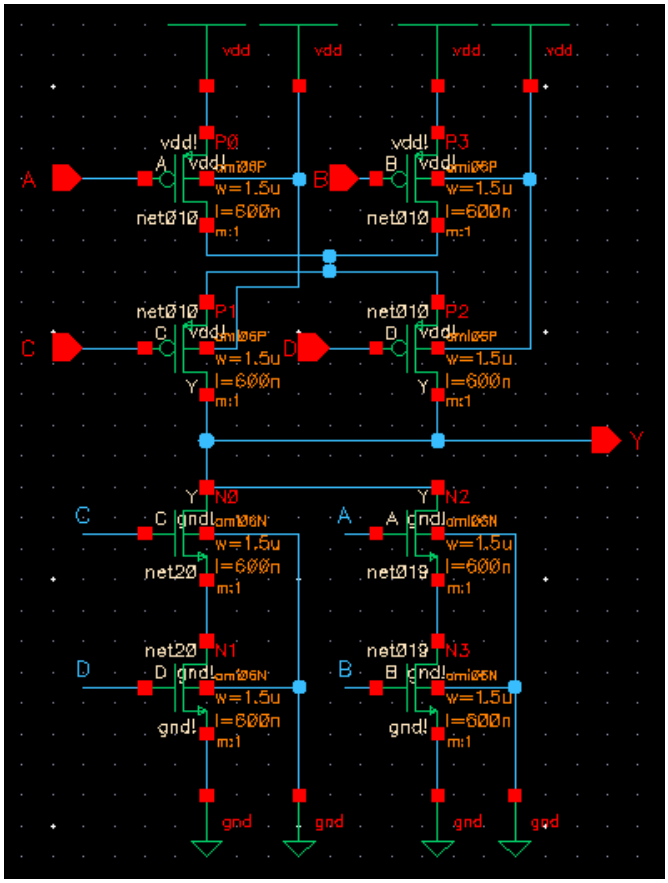


AOI21X1 Symbol

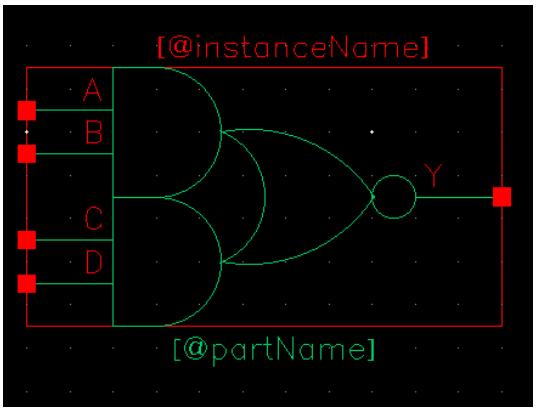
AOI22X1:



AOI22X1 Layout

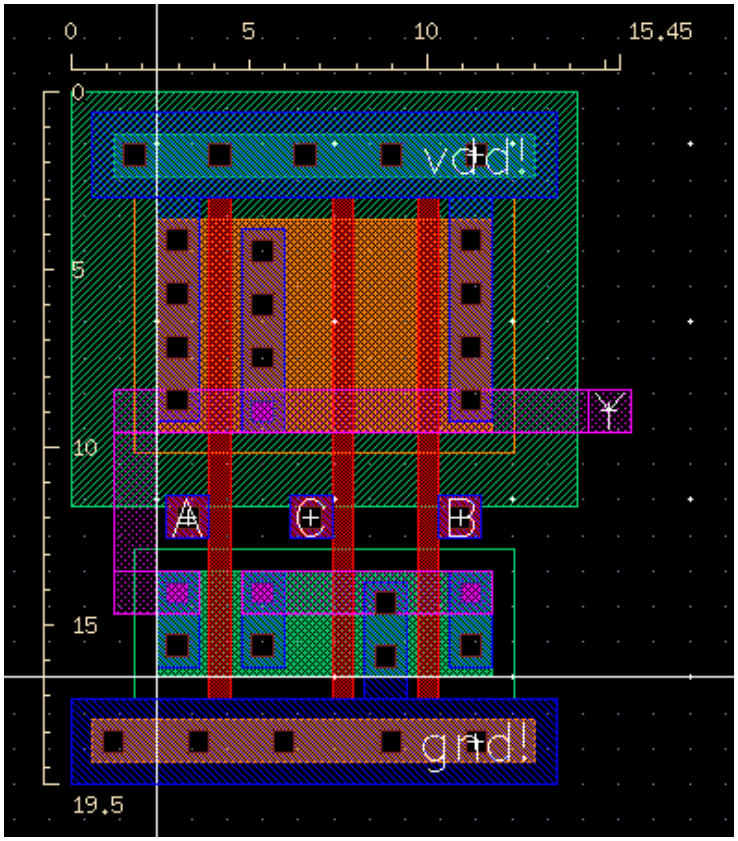


AOI22X1 Schematic

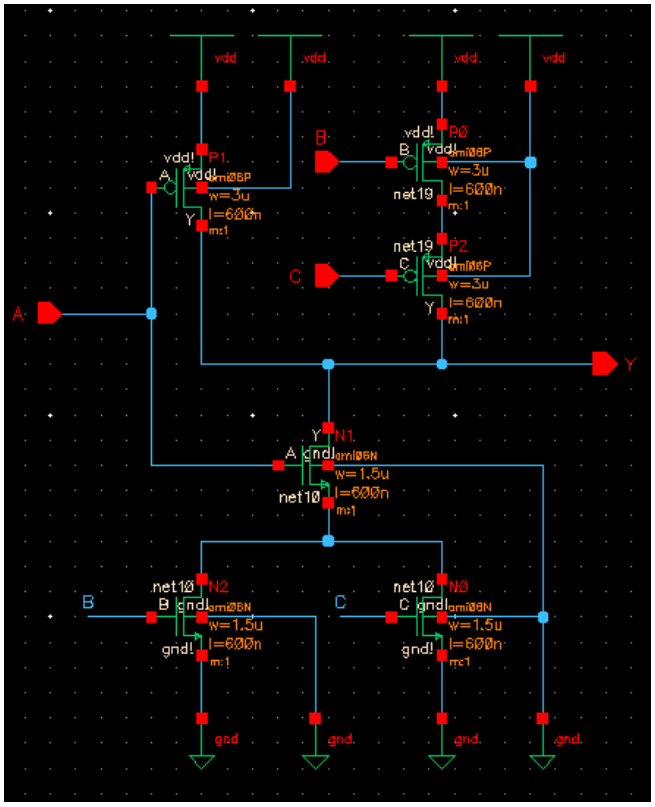


AOI22X1 Symbol

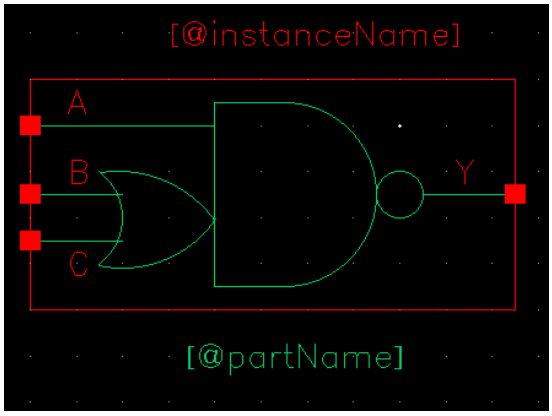
OAI21X1:



OAI21X1 Layout

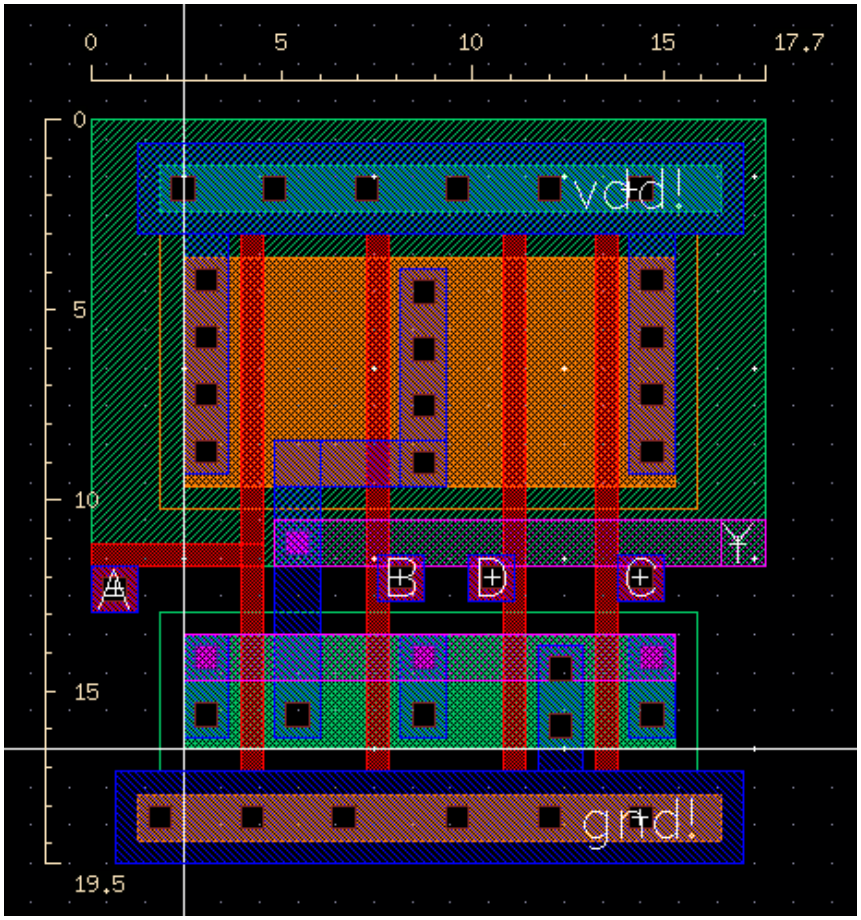


OAI21X1 Schematic

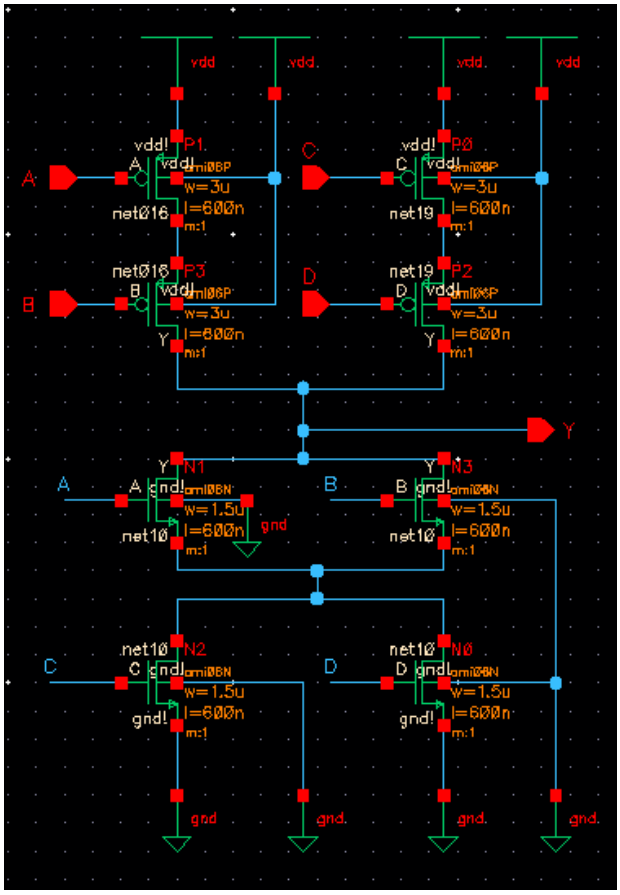


OAI21X1 Symbol

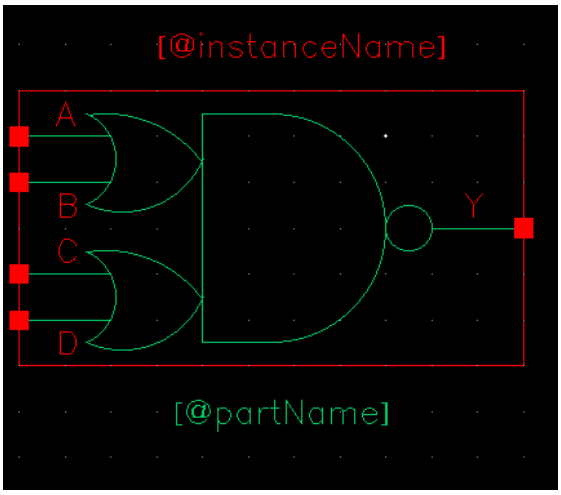
OAI22X1:



OAI22X1 Layout

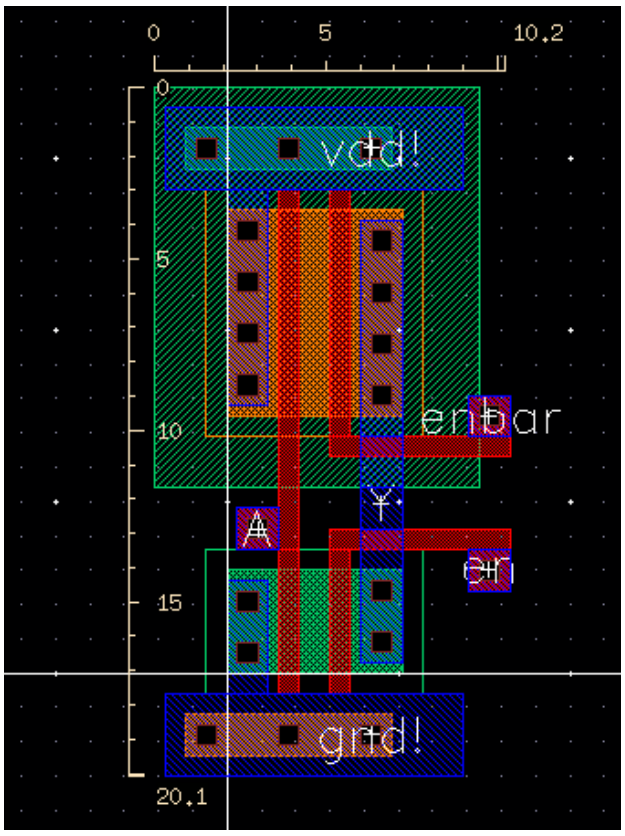


OAI22X1 Schematic

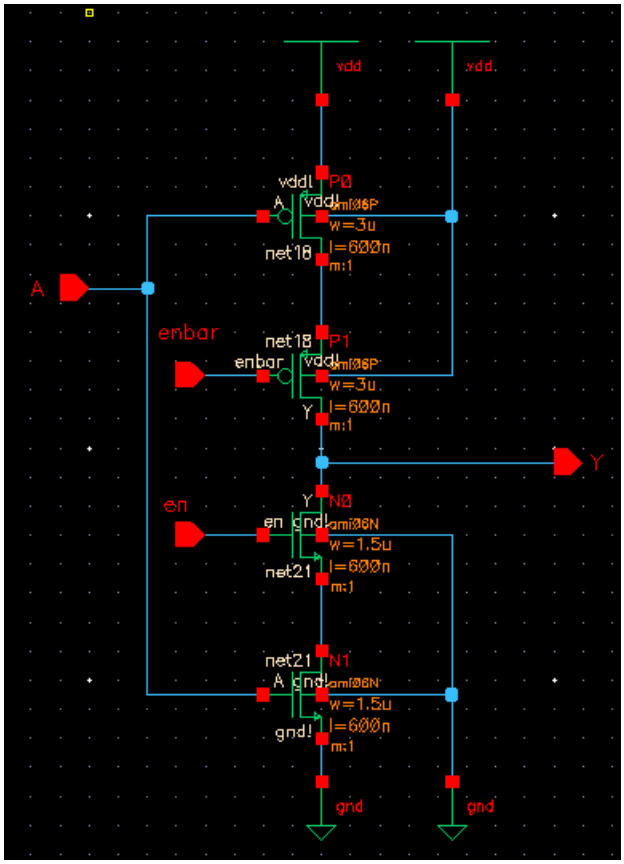


OAI22X1 Symbol

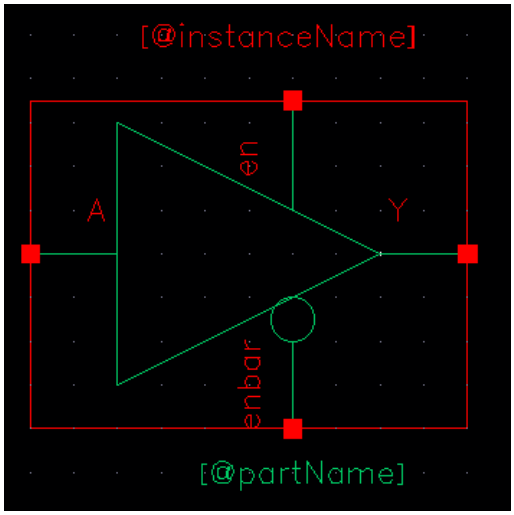
TBUFdX1:



TBUFdX1 Layout

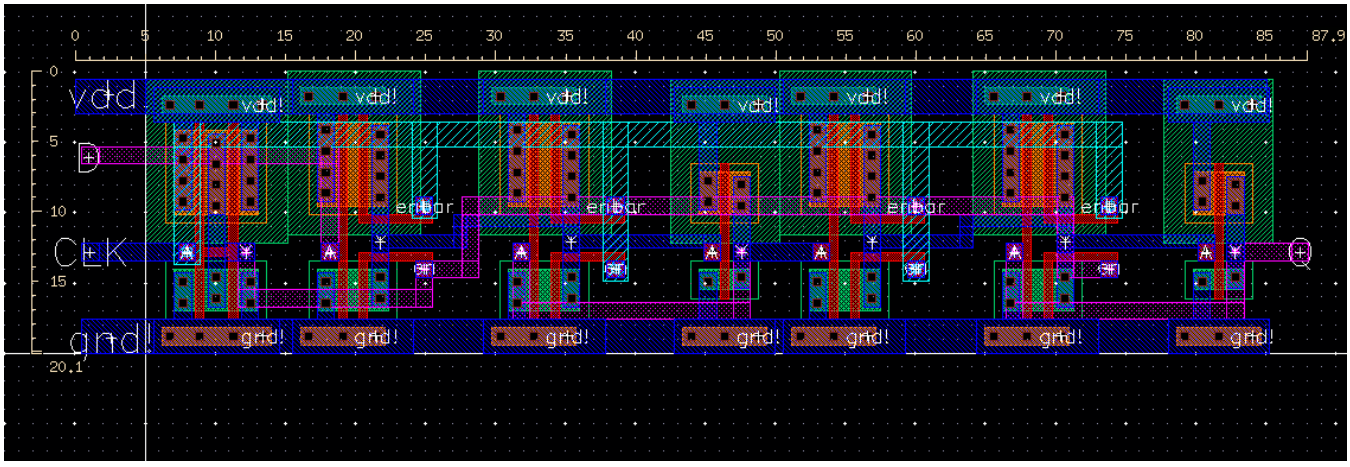


TBUFdX1 Schematic

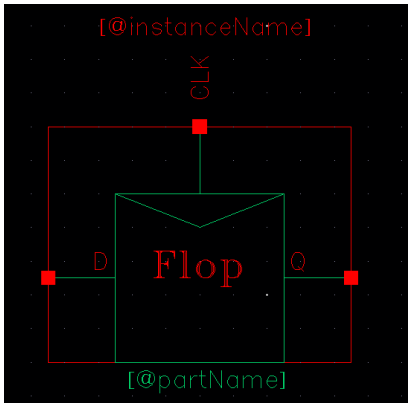


TBUFdX1 Symbol

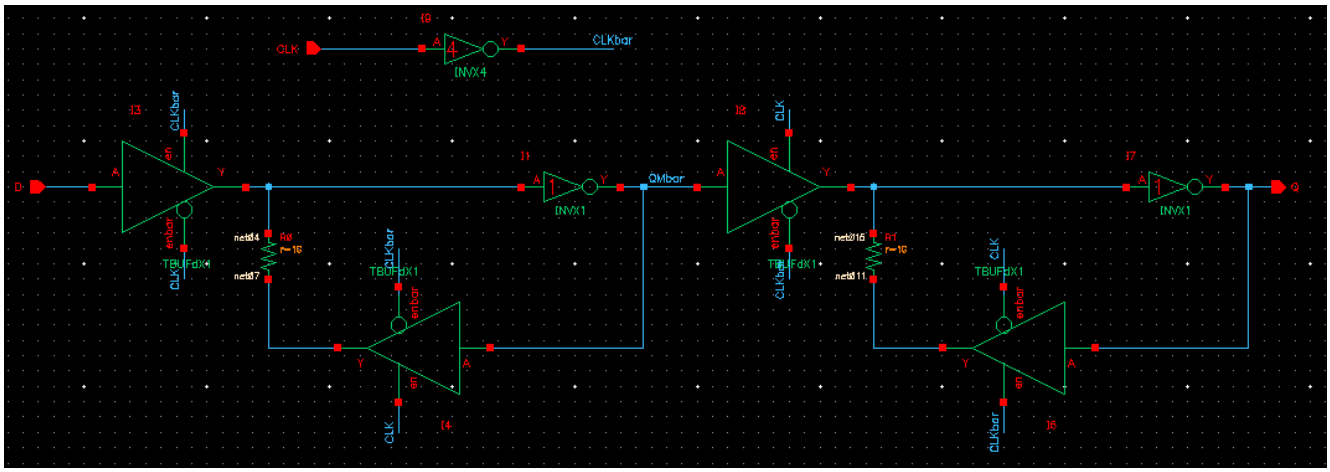
DFFPOSX1:



DFFPOSX1 Layout

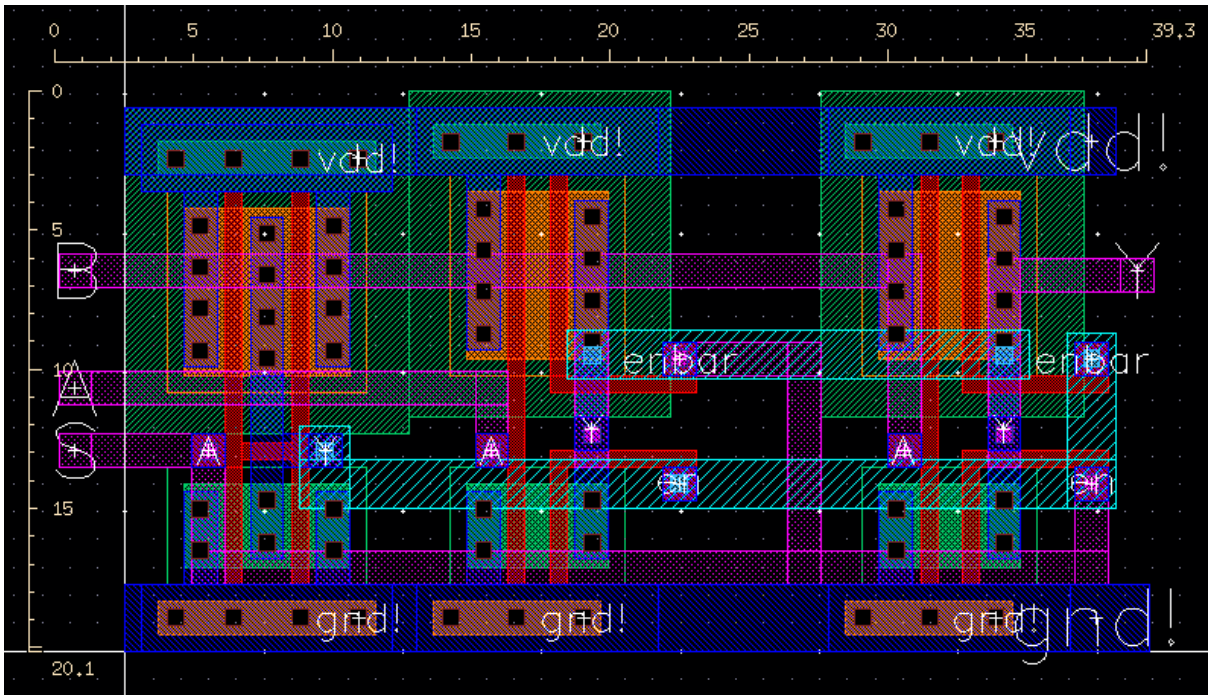


DFFPOSX1 Symbol

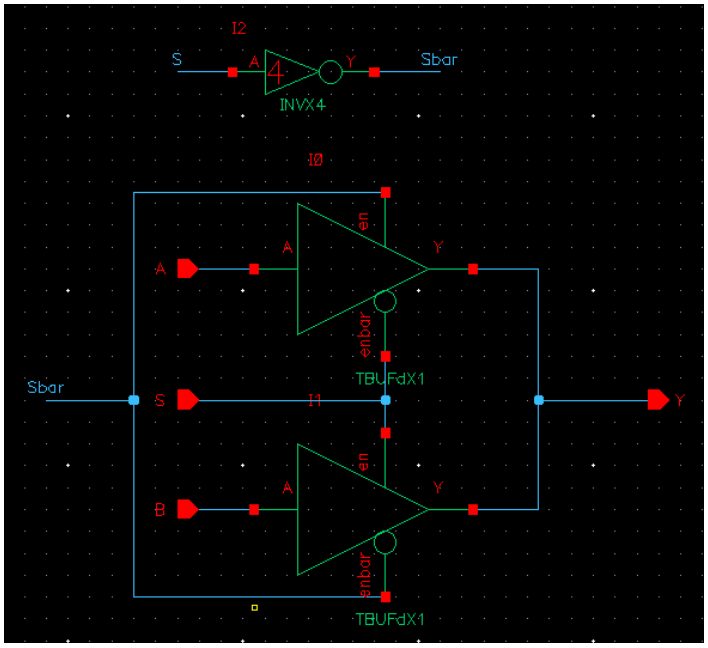


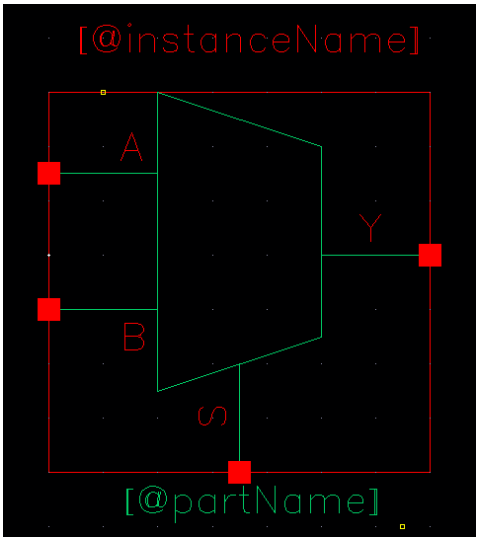
DFFPOSX1 Schematic

MUX2X1:



MUX2X1 Layout

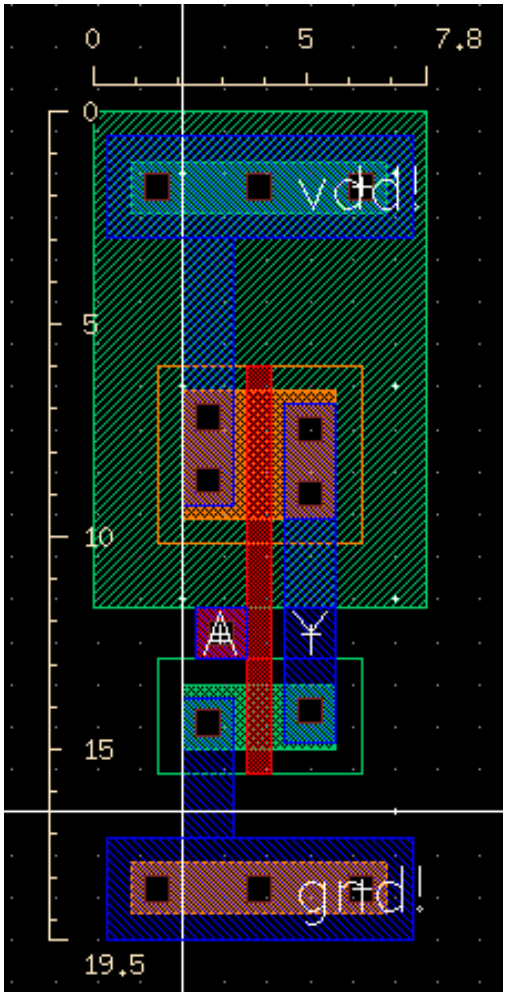


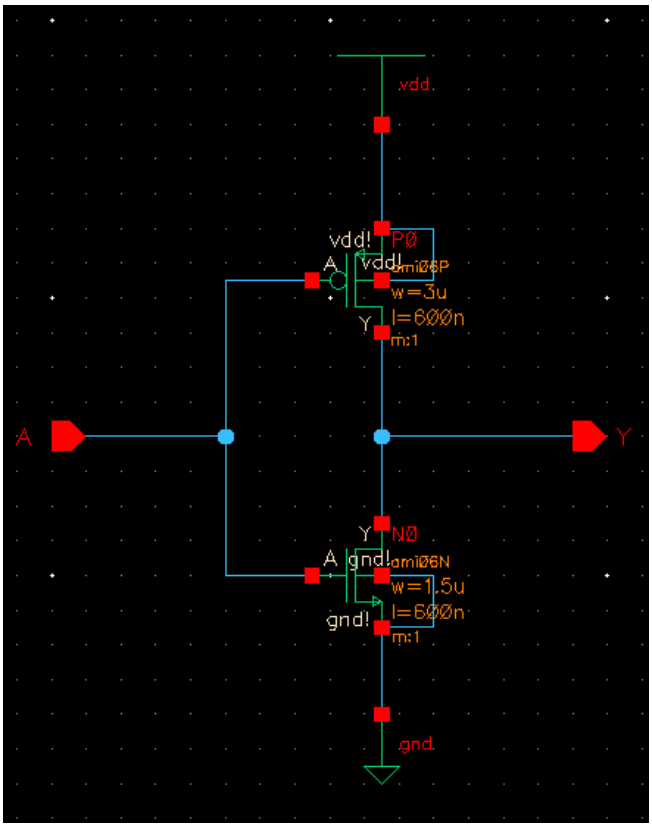


MUX2X1 Schematic

MUX2X1 Symbol

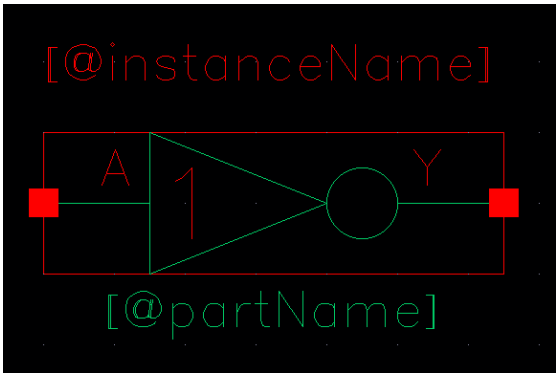
INVX1:





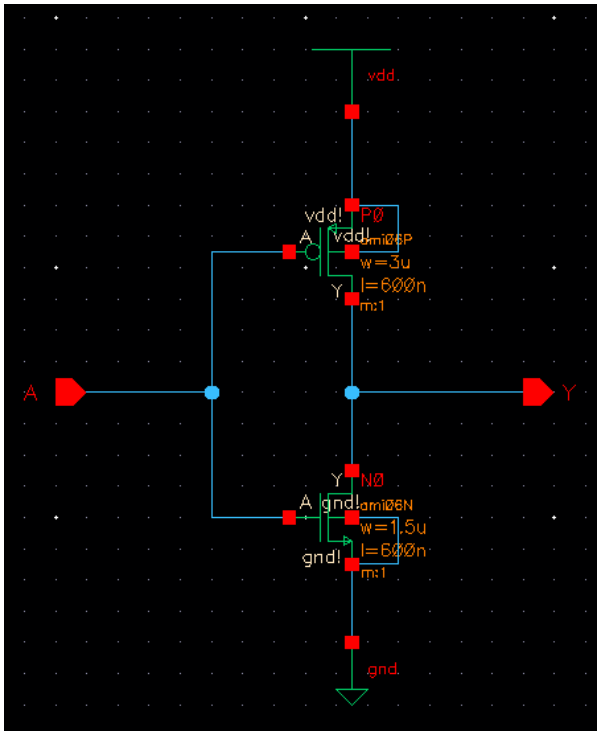
INVX1 Layout

INVX1 Schematic

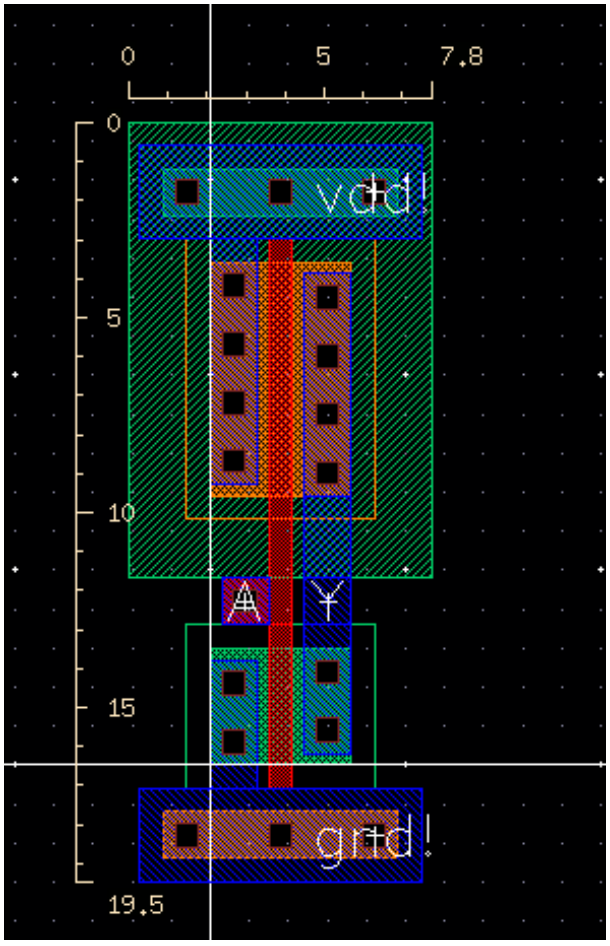


INVX1 Symbol

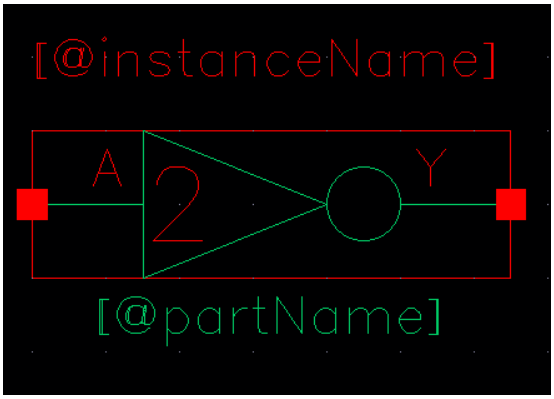
INVX2:



INVX2 Schematic

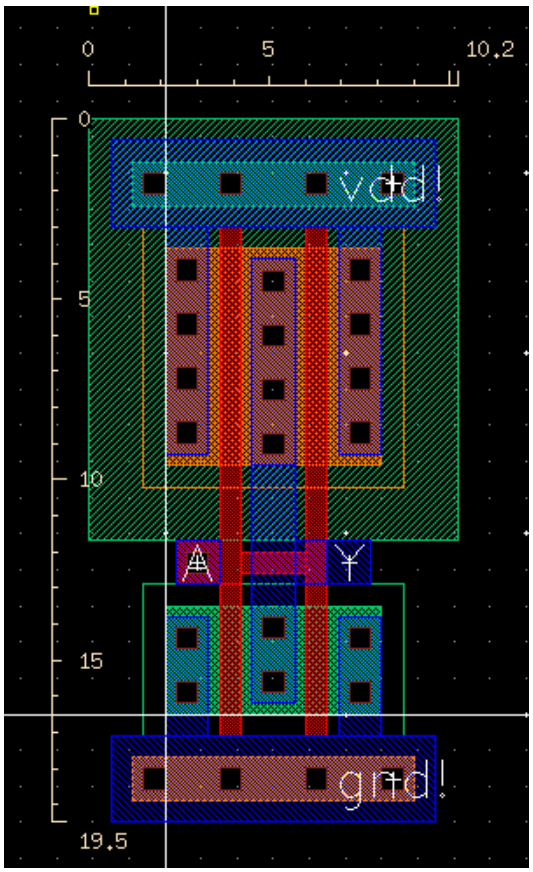


INVX2 Layout

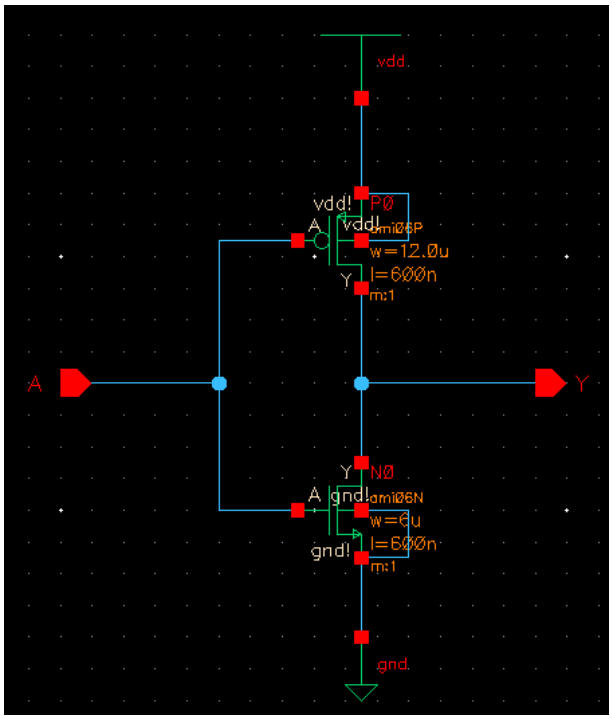


INVX2 Symbol

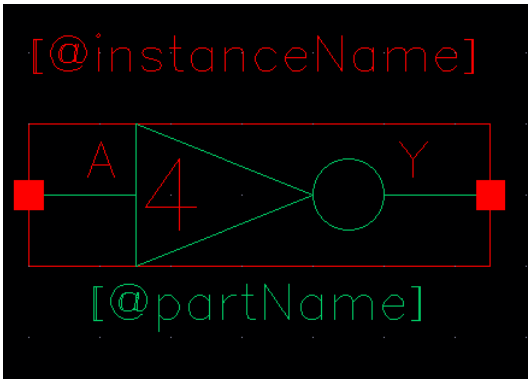
INVX4:



INVX4 Layout

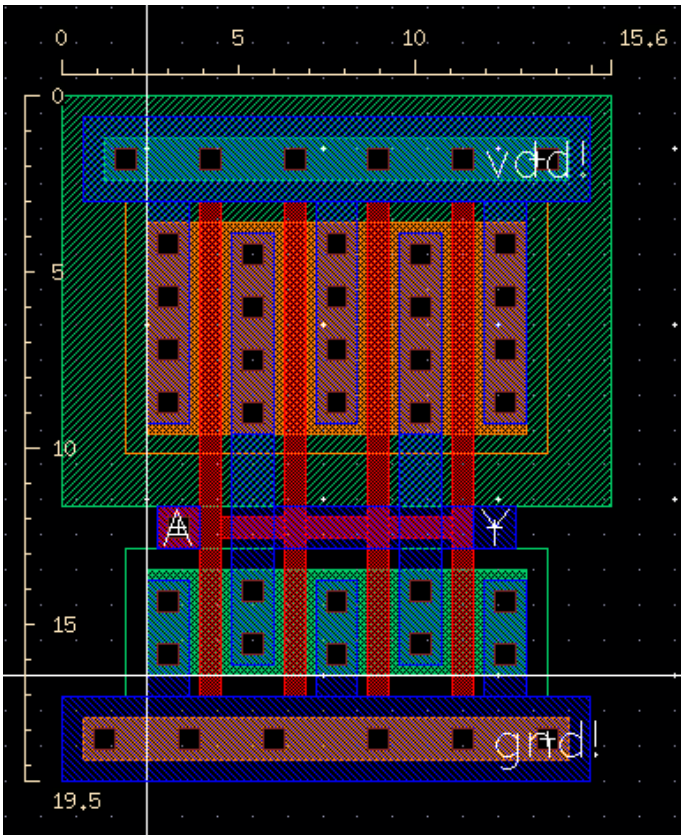


INVX4 Schematic

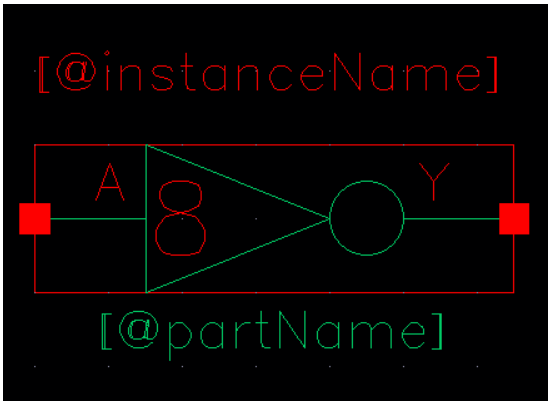


INVX4 Symbol

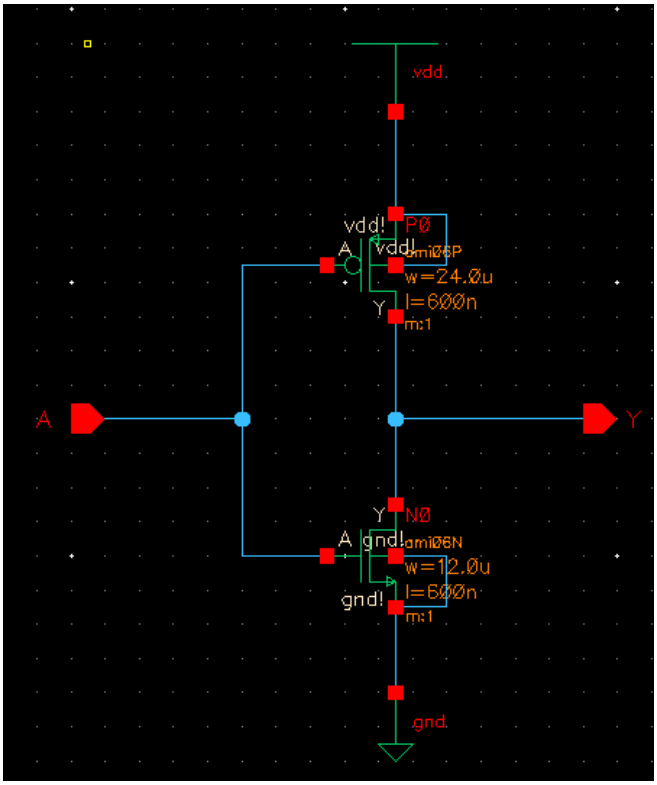
INVX8:



INVX8 Layout

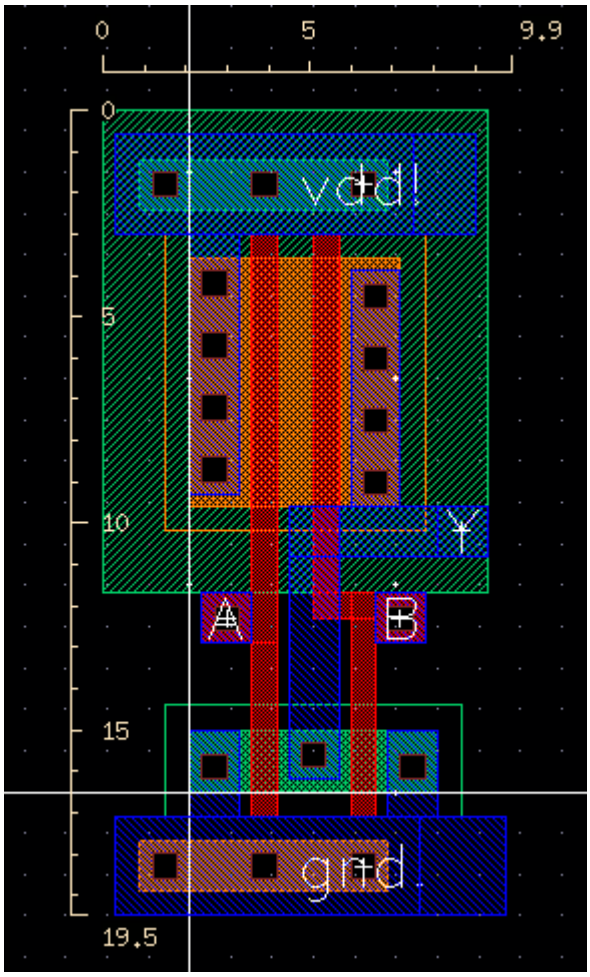


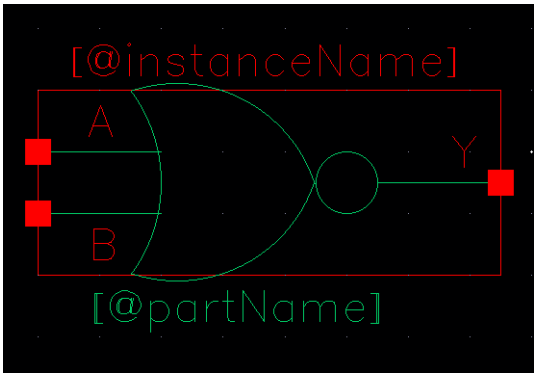
INVX8 Symbol



INVX8 Schematic

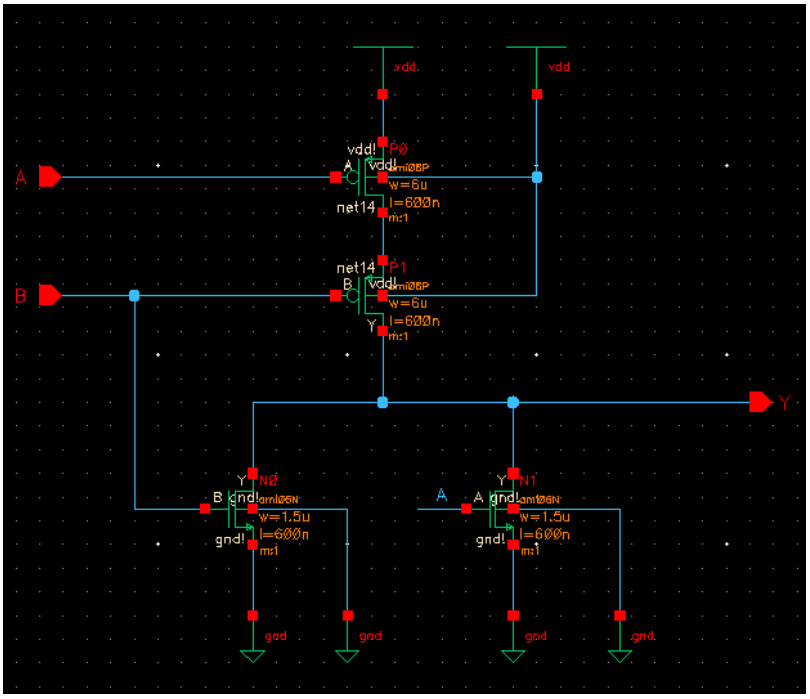
NOR2X1:





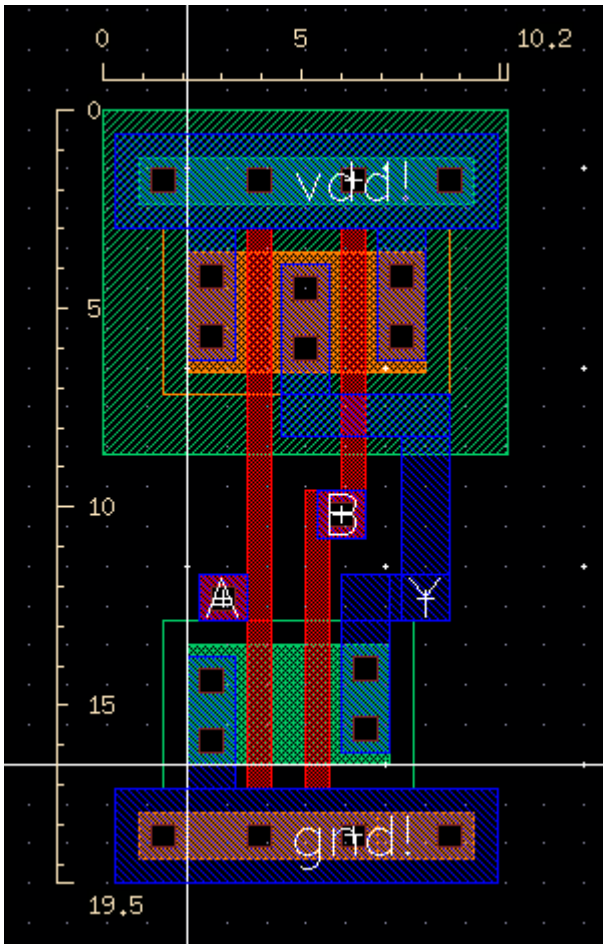
NOR2X1 Layout

NOR2X1 Symbol

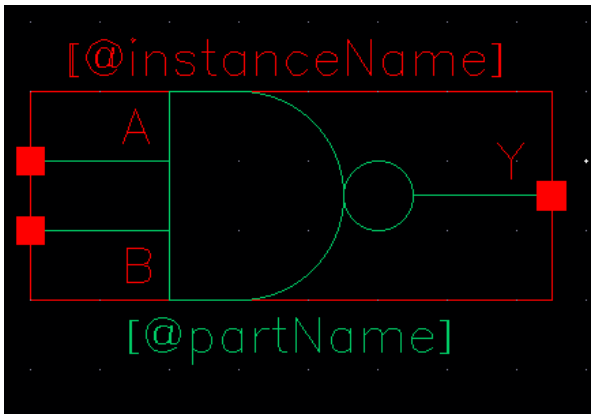


NOR2X1 Schematic

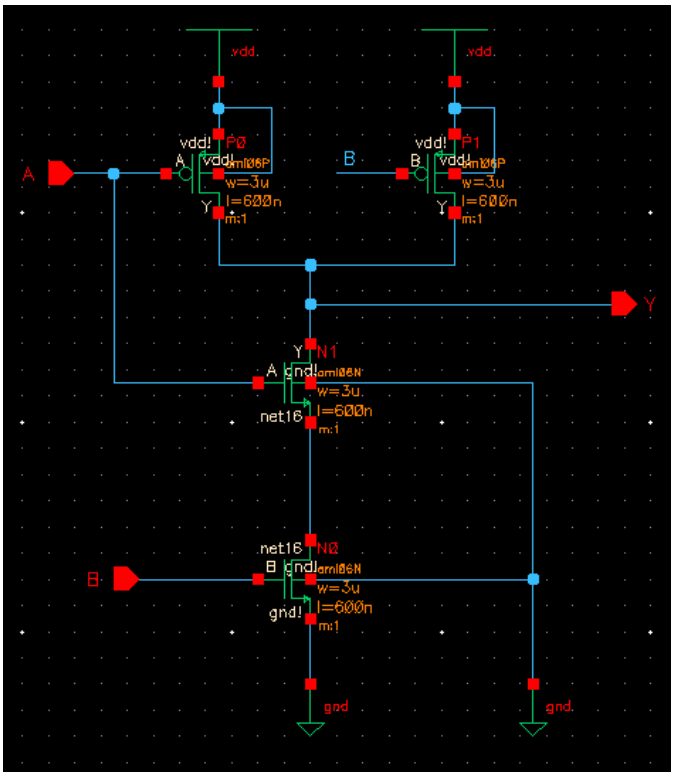
NAND2X1:



NAND2X1 Layout

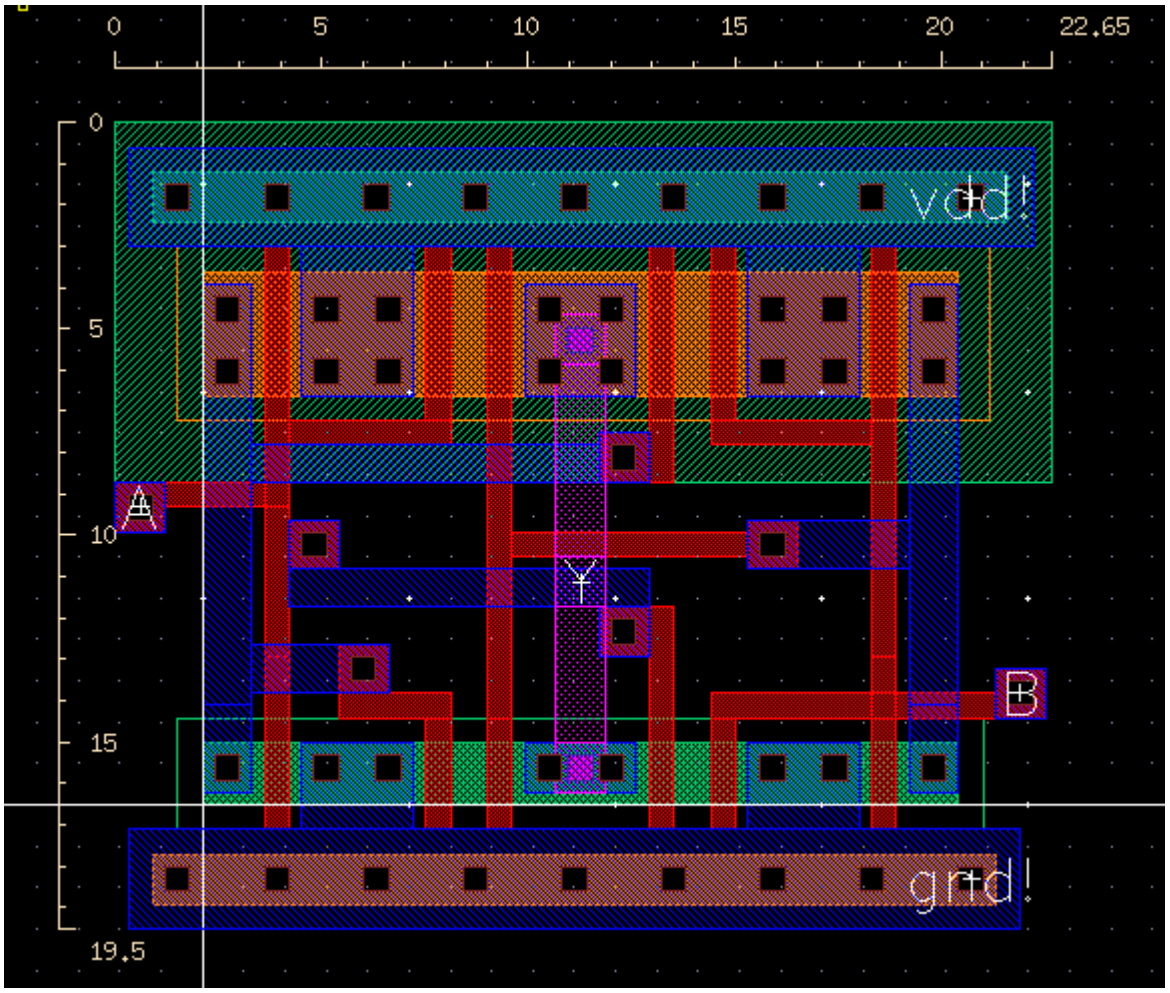


NAND2X1 Symbol

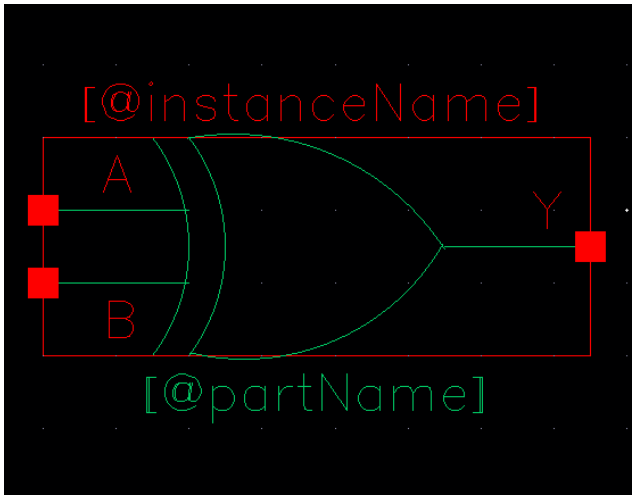


NAND2X1 Schematic

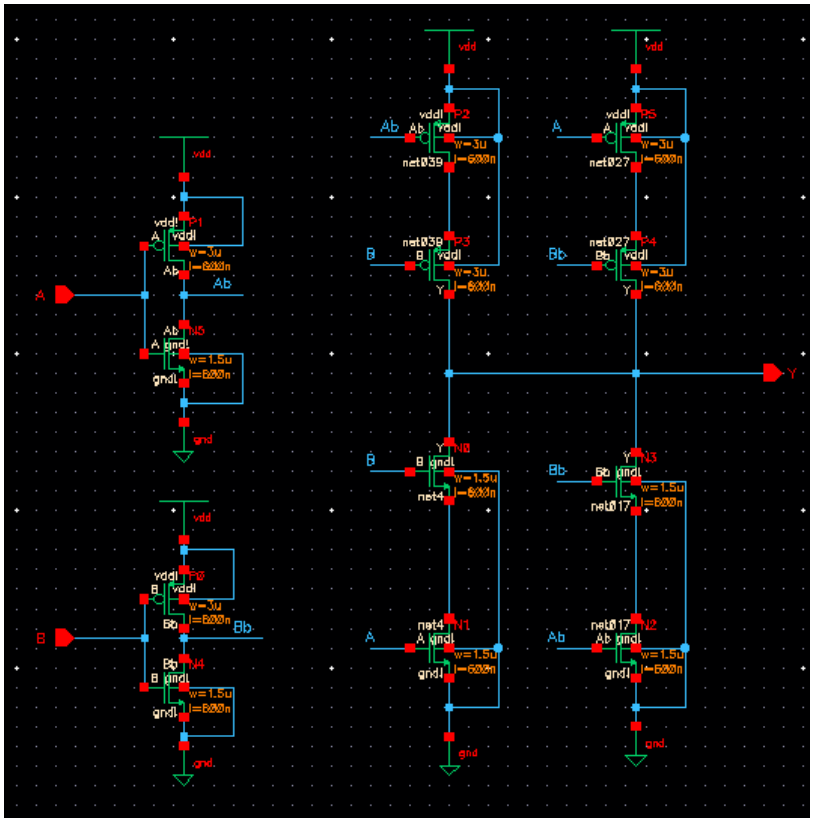
XOR2X1:



XOR2X1 Layout

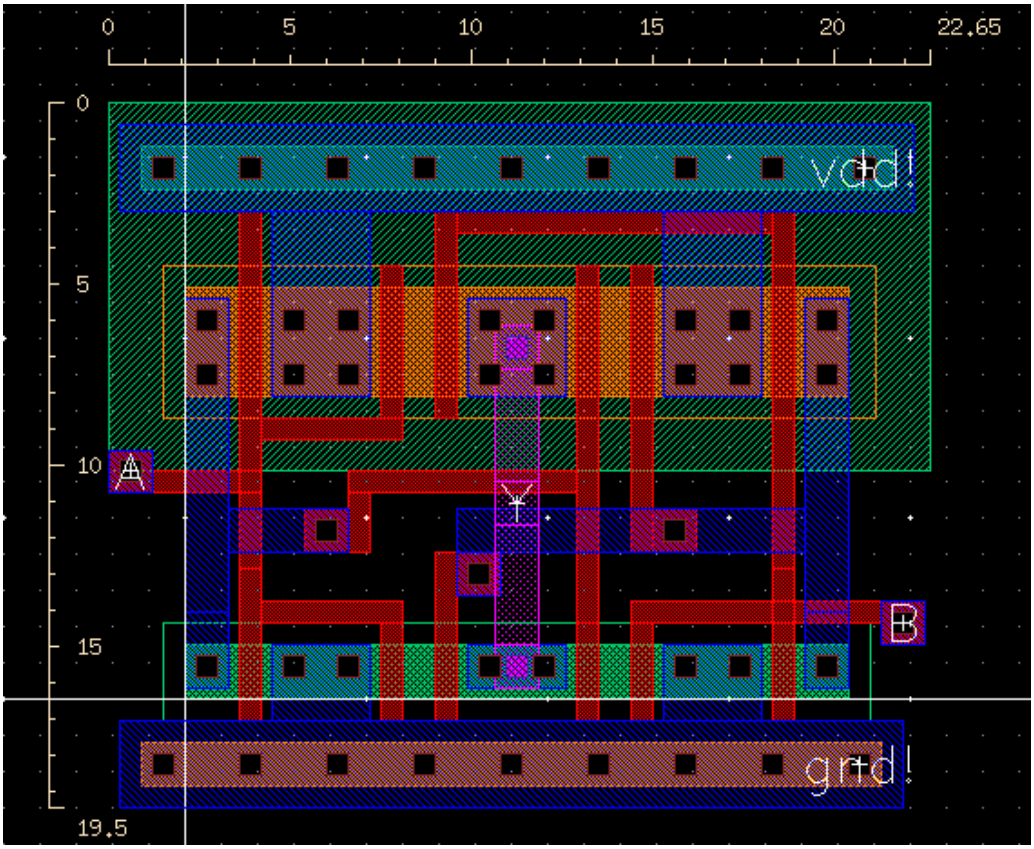


XOR2X1 Symbol

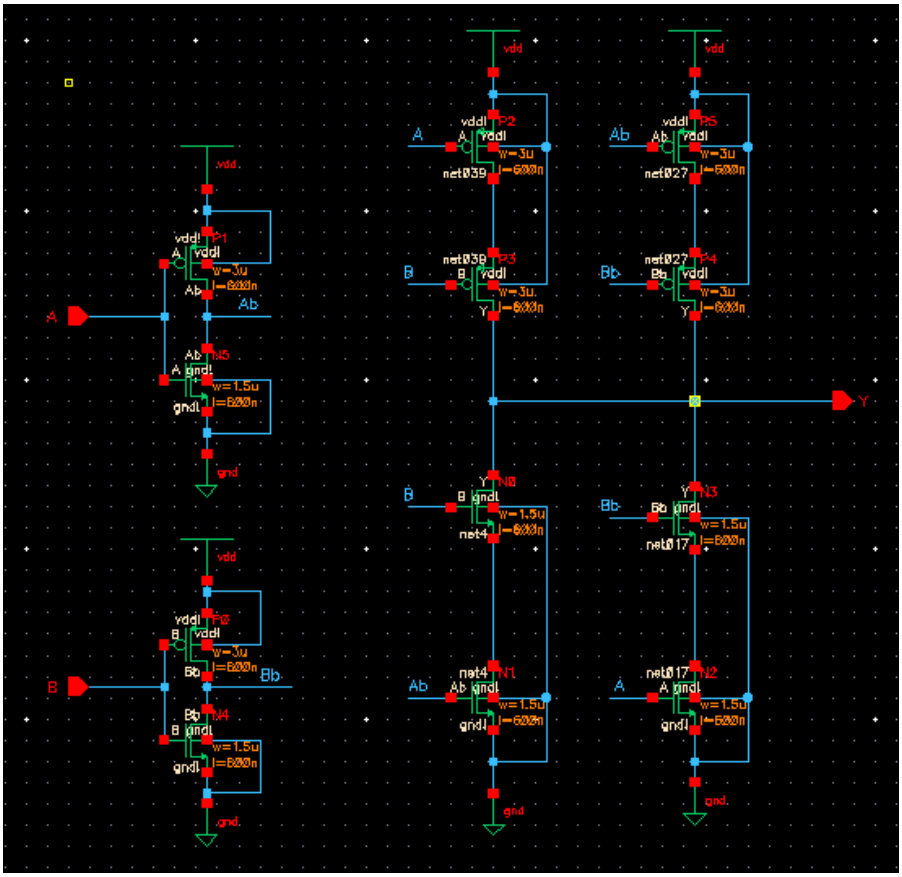


XOR2X1 Schematic

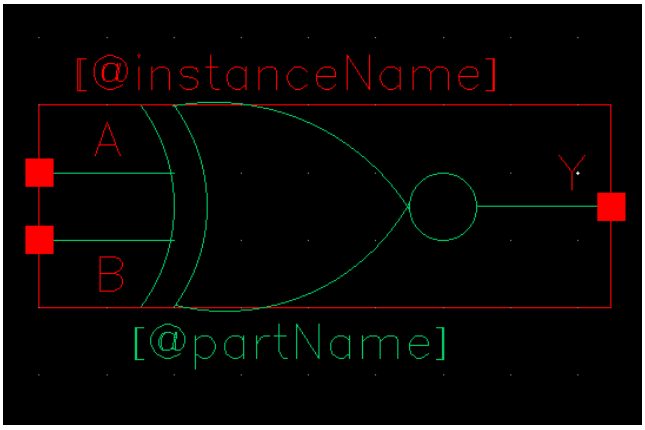
XNOR2X1:



XNOR2X1 Layout

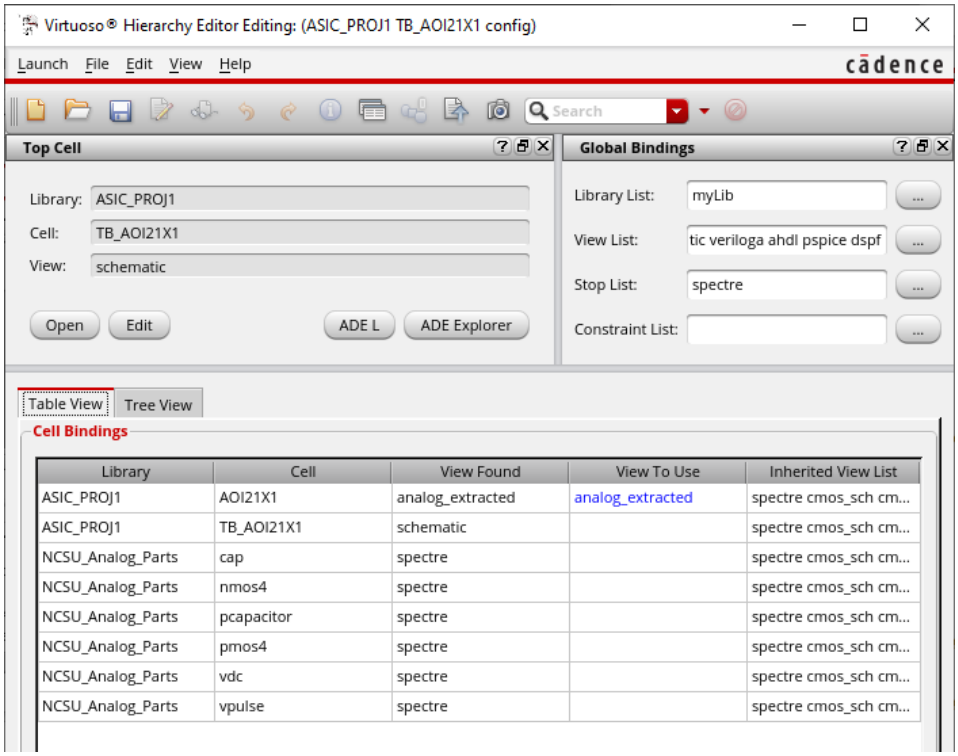


XNOR2X1 Schematic

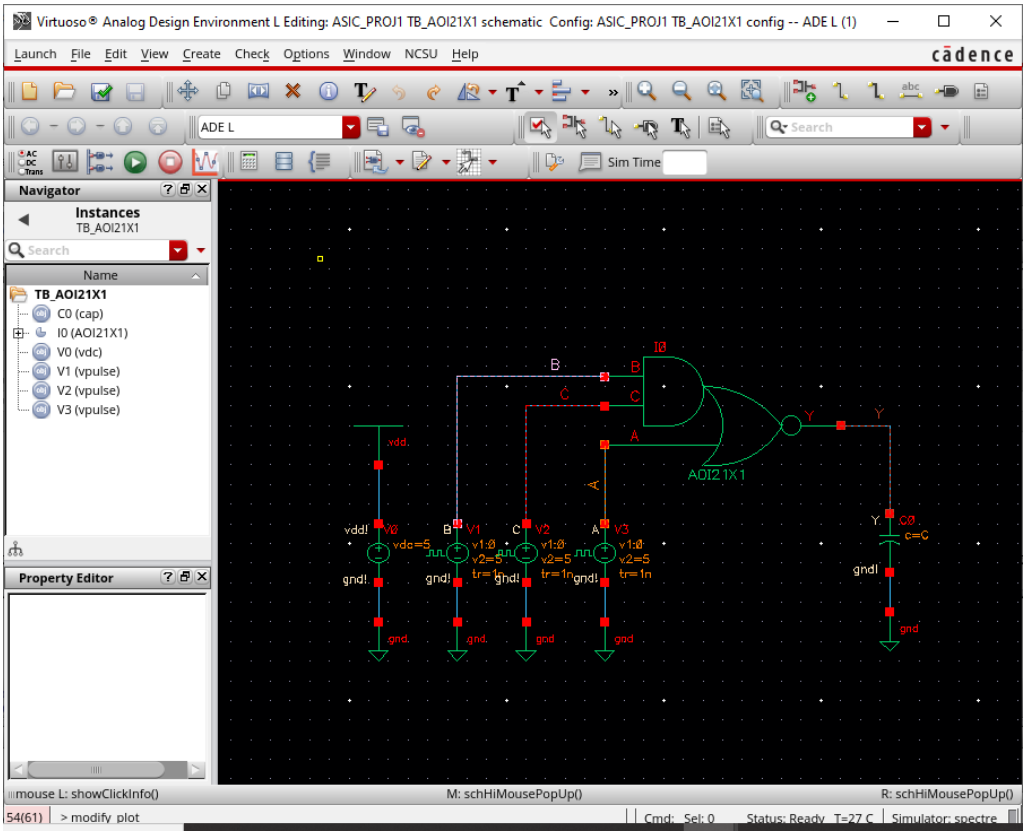


XNOR2X1 Symbol

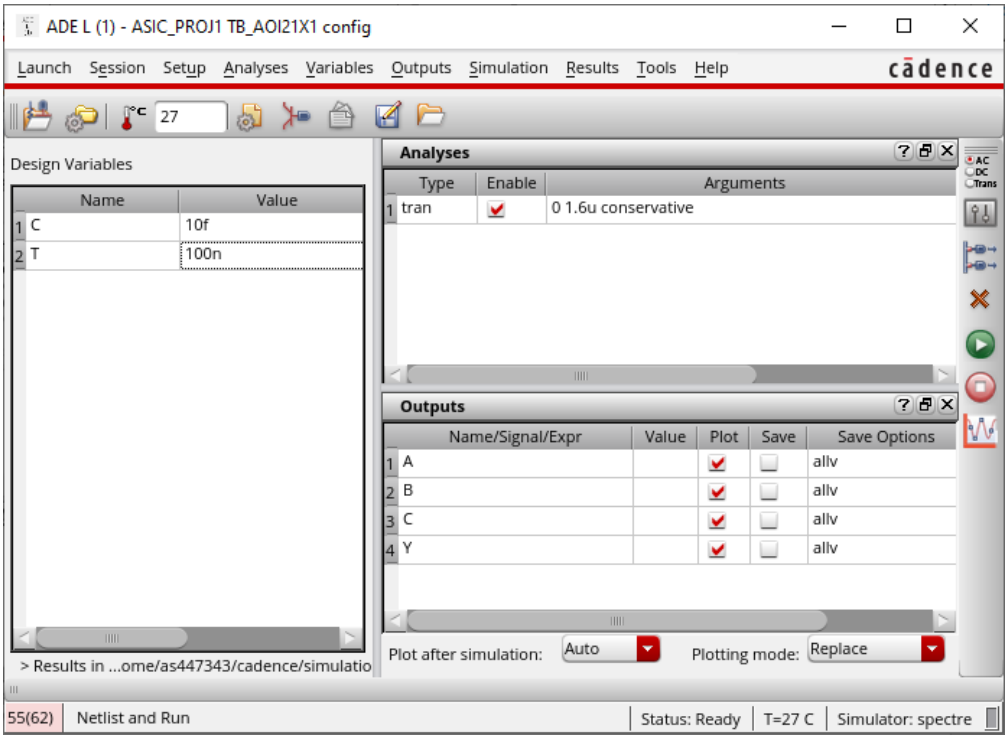
Testbenches, Delay Calculation of Layout-based config view: (example shown for 1 cell, AOI21X1)



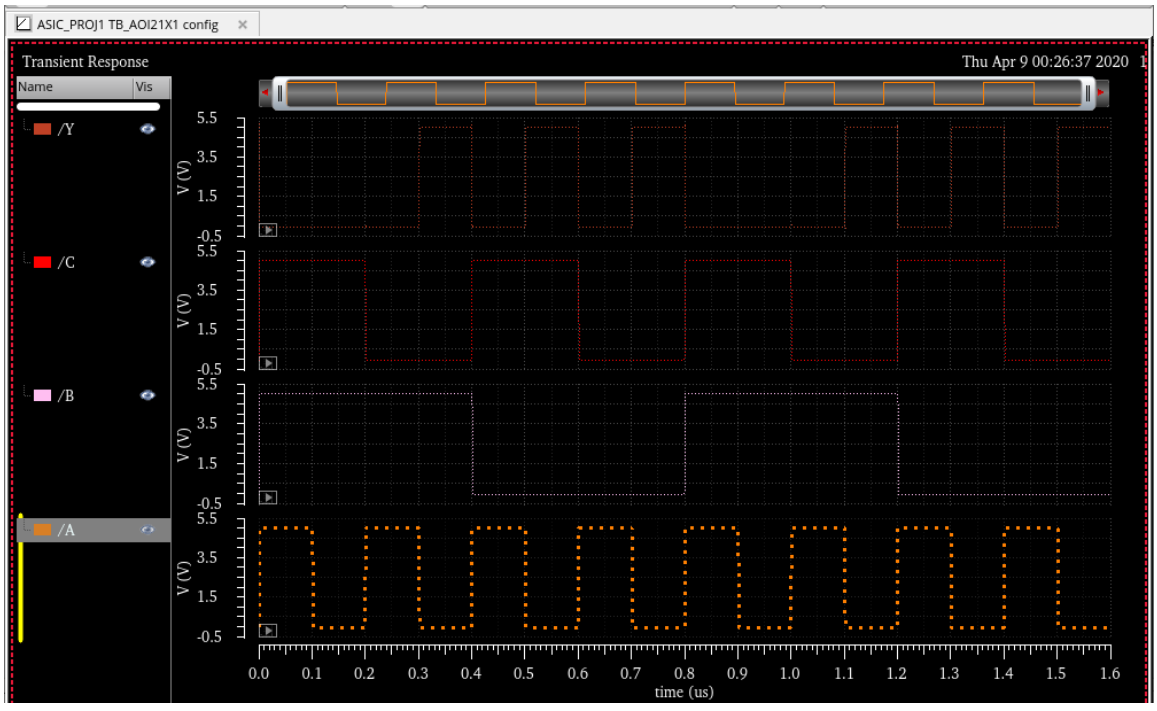
TB_AOI21X1 Config view



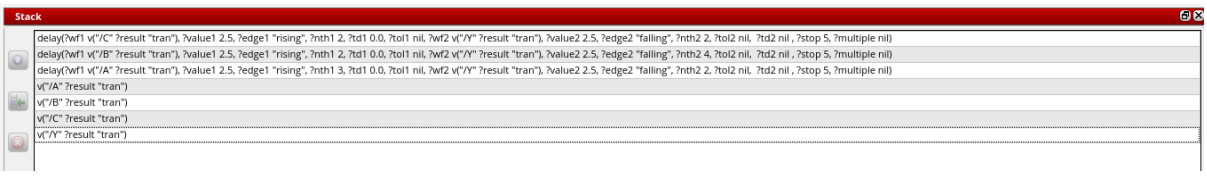
TB_AOI21X1 Schematic view



TB_AOI21X1 ADE L



TB_AOI21X1 Waveform



TB_AOI21X1 Calculator Stack