# IECE 520 – Introduction to VLSI – Lab 2 NCSU SDK

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Initialization: A directory named **cadence** is created to keep all the files under one folder.

- mkdir cadence
- cd cadence
- pwd

This ensures that we are currently working in the newly created cadence directory.

***1) Get our 0.6µm NCSU Technology Library working.***

The NCSU CDK is installed into a new directory named **TechLibs** under the Cadence directory through the following steps:

- mkdir TechLibs
- cd TechLibs
- cp $CDK_DIR_SRC/ncsu-cdk-1.6.0.beta.tar.gz .
- umask 000
- tar -zxpvf ncsu-cdk-1.6.0.beta.tar.gz
- cd ..

Few environment variables are exported and displayed:

- export CDK_DIR="$HOME/cadence/TechLibs/ncsu-cdk-1.6.0.beta"
- echo $HOME
- echo $CDK_DIR

***2) Understand how to modify your .bash profile(in your home directory ~/) to simplify the handling of the environment variables and certain files Cadence needs.***

Using vi editor, the .bash profile is modified to automate some of the steps:

- export CDK_DIR="$HOME/cadence/Techlibs/ncsu-cdk-1.6.0.beta"
- cd cadence
- module load cadence

Some files are copied into the local work area (in the ~/cadence directory):

- cp $CDK_DIR/cdssetup/cdsinit .cdsinit
- cp $CDK_DIR/cdssetup/cds.lib cds.lib

Then, we include some basic functions

- echo "INCLUDE $CDS_SITE/share/cdssetup/cds.lib" >> cds.lib

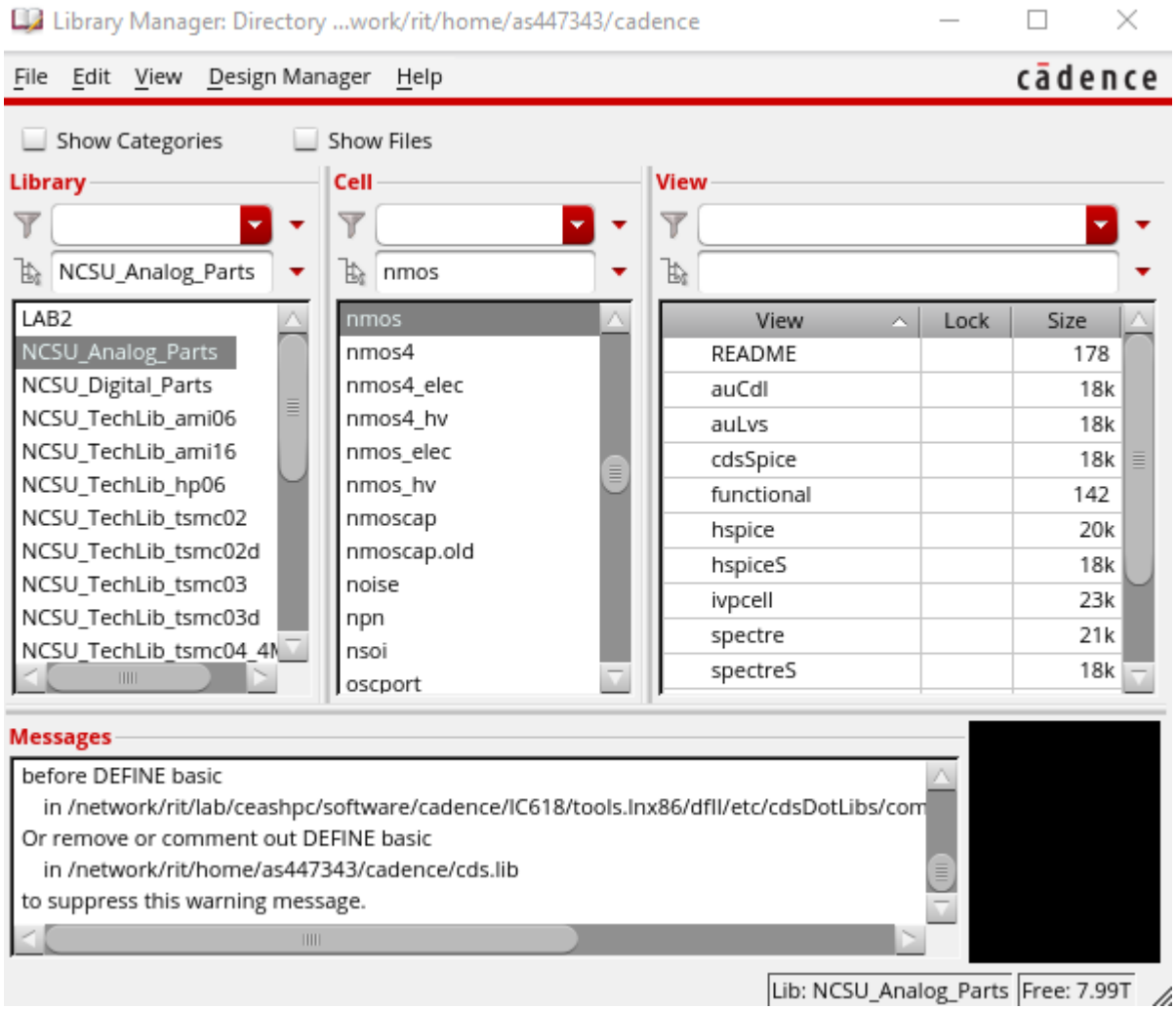
and view the contents by

- cat cds.lib

Finally we run virtuoso& to see the **Library Manager.**

***3) Understand Library Manager, Path Manager, and Cadence directory/file structure.***

The nmos and pmos cells are copied from the NCSU_Analog_Parts folder to ~/cadence directory.

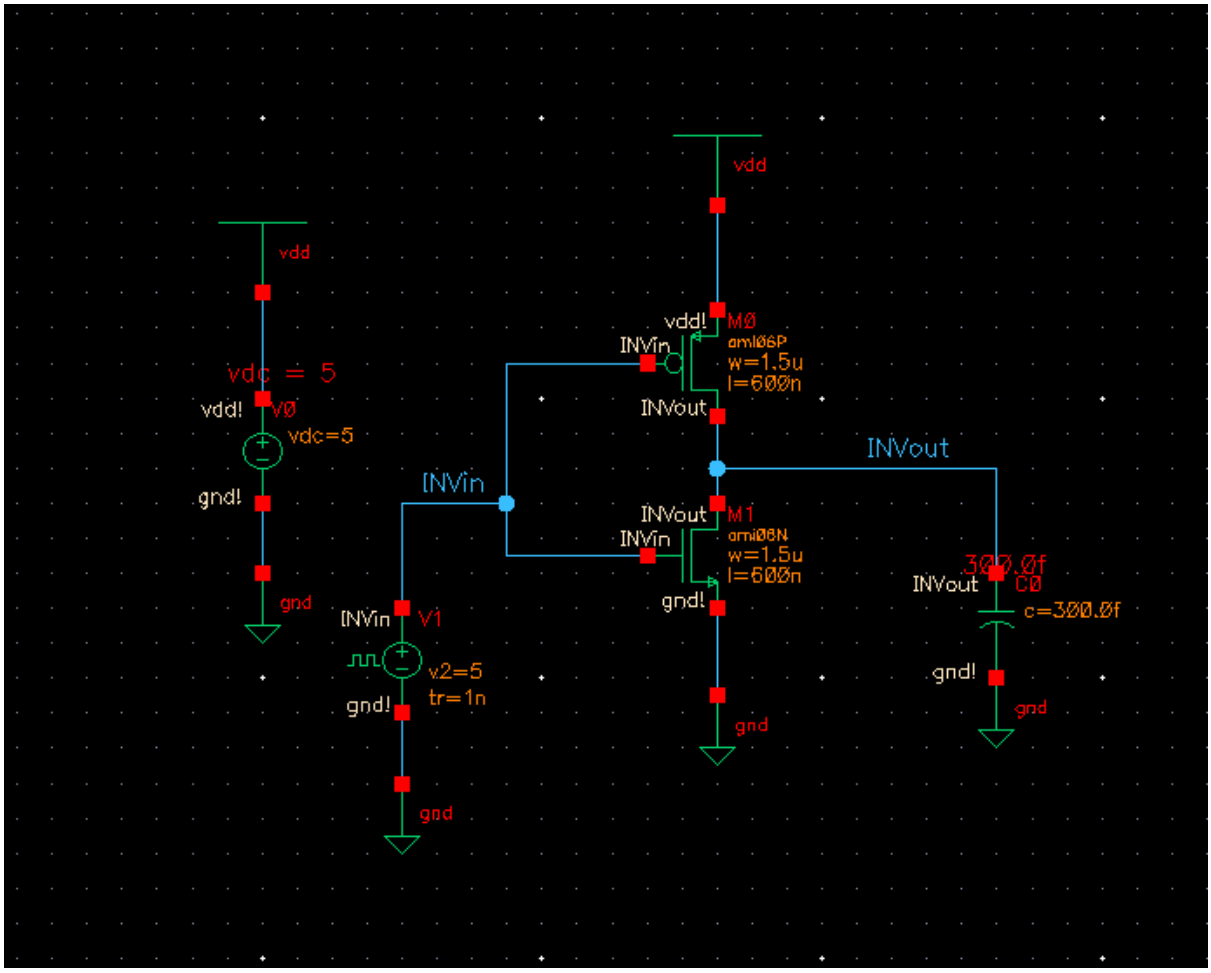



To associate the 0.6µm technology library with my LAB2 design library, go to Tools > Technology File Manager > Attach in the CIW.

***4) Get the Schematic Editor working. Understand how to work with library and cell views. Draw a simple inverter schematic using PMOS and NMOS from the NCSU Technology library.***

In the Library Manager, choosing File > New > Cell View, I created a new cell inside the LAB2 library named **TBnverter.**

The NCSU_TechLib_ami06tech library is attached to the LAB2 design library. To draw the inverter circuit, vdc, vpulse, cap, vdd, and gnd from the NCSU_Analog_Parts are copied into my LAB2 directory and a simple inverter schematic is drawn which looks like this:




- The capacitance (cap) value is set to 1pF by default. It is changed to 0.3pF.
- The value of vdc is set to 5V.
- For the vpulse, voltage 1 & voltage 2 are set to 0V and 5V respectively. Delay Time= 1ns, Pulse width= 50ns, Rise Time= Fall Time= 1ns.

***5) Simulating your inverter using Analog Design Environment (ADE)***

The Analog Design Environment (ADE) is launched from the schematic editor by Launch > ADE L.

The simulator is changed to Cadence's native **Spectre**.

- Setup > Simulator/Directory/Host
- Simulator changed to spectre
- Project Directory kept ~/cadence/simulation
- Host Mode local kept

Models for the nmos and pmos are chosen by going to Setup > Model Libraries and adding

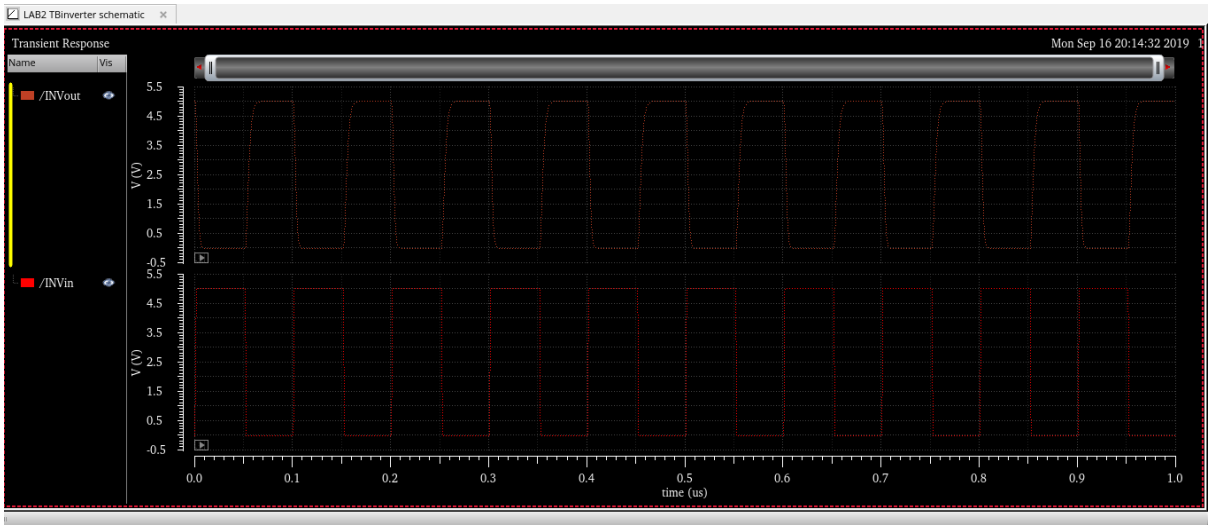
- ~/cadence/TechLibs/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m
- ~/cadence/TechLibs/ncsu-cdk-1.6.0.beta/models/spectre/standalone /ami06P.m

under Global Model files.

A transient analysis is performed from Analyses > Choose and checking *tran.* For Stop Time, 1u is chosen and *Enabled* and *conservative* are checked.

Next Outputs > To Be Plotted > Select on Design is chosen and output and input are renamed to **INVout** and **INVin** respectively.

The simulation is run by Simulation > Netlist and Run and the following plot is obtained:

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Output and IC/nodeset summary:
                save   2       (current)
                save   6       (voltage)

    tran: time = 26.17 ns    (2.62 %), step = 6.545 ns     (655 m%)
    tran: time = 77.69 ns    (7.77 %), step = 3.663 ns     (366 m%)
    tran: time = 127.9 ns    (12.8 %), step = 7.404 ns     (740 m%)
    tran: time = 175.2 ns    (17.5 %), step = 2.78 ns      (278 m%)
    tran: time = 228 ns      (22.8 %), step = 7.459 ns     (746 m%)
    tran: time = 275.2 ns    (27.5 %), step = 2.778 ns     (278 m%)
    tran: time = 328 ns      (32.8 %), step = 7.455 ns     (746 m%)
    tran: time = 375.2 ns    (37.5 %), step = 2.778 ns     (278 m%)
    tran: time = 428 ns      (42.8 %), step = 7.455 ns     (745 m%)
    tran: time = 475.2 ns    (47.5 %), step = 2.778 ns     (278 m%)
    tran: time = 528 ns      (52.8 %), step = 7.454 ns     (745 m%)
    tran: time = 575.2 ns    (57.5 %), step = 2.778 ns     (278 m%)
    tran: time = 628 ns      (62.8 %), step = 7.453 ns     (745 m%)
    tran: time = 675.2 ns    (67.5 %), step = 2.778 ns     (278 m%)
    tran: time = 728 ns      (72.8 %), step = 7.452 ns     (745 m%)
    tran: time = 775.2 ns    (77.5 %), step = 2.778 ns     (278 m%)
    tran: time = 828 ns      (82.8 %), step = 7.452 ns     (745 m%)
    tran: time = 875.2 ns    (87.5 %), step = 2.778 ns     (278 m%)
    tran: time = 928 ns      (92.8 %), step = 7.451 ns     (745 m%)
    tran: time = 975.2 ns    (97.5 %), step = 2.778 ns     (278 m%)
Number of accepted tran steps =             946

Maximum value achieved for any signal of each quantity:
V: V(INVout) = 5.004 V
I: I(V0:p) = 305.2 uA
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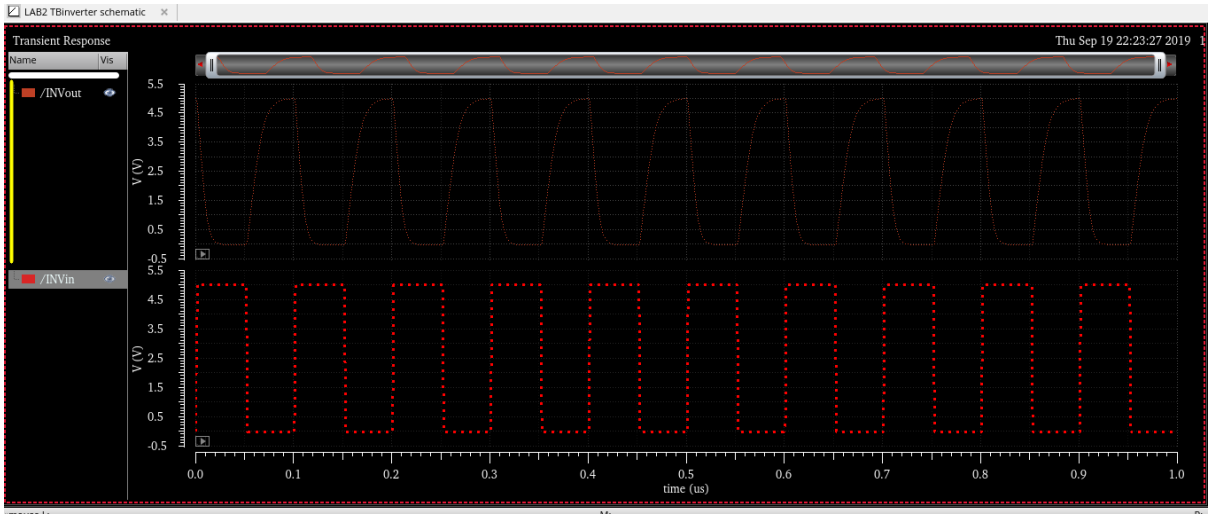
Thus, the inverter logic is verified from the simulated waveform.

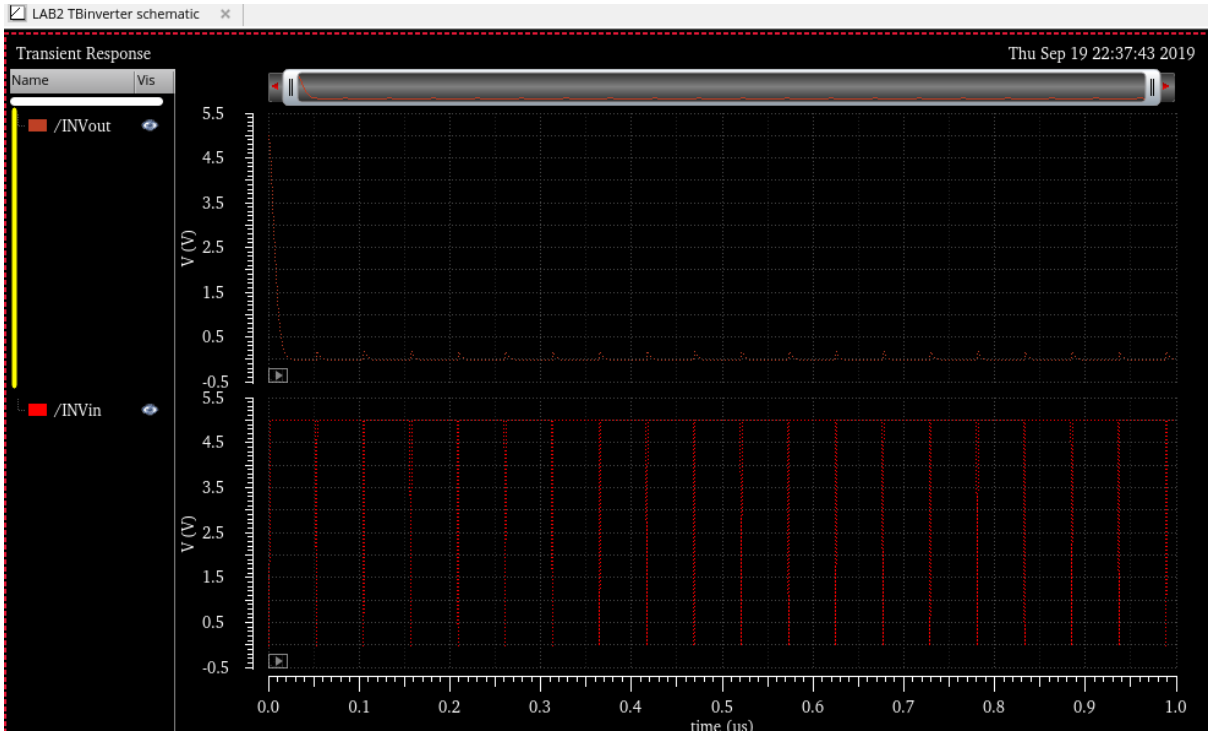
After simulation, the state is saved as **INV1CAP300f100n** where INV1 means a single inverter, 300f designates the load (300fF) and 100n is the period of the pulses.

The simulation is re-run for capacitor (load) 1pF and the state is saved as **INV1CAP1p100n**.




The delay in between change of state is much more in this case due to increase of the capacitor load which holds more charge.

The pulse period is now lowered to 10ns (10x faster) keeping the capacitor as 1pFa and all other parameters same. The state is saved as **INV1CAP1p10n**.




The output shows the rapid state change due to very high frequency, but since the 0 (0 V) input is for a negligible duration compared to 1 (5 V) input, the waveform is asymmetrical compared to the previous simulations.