ECE420/520: Lab3 Report – Symbol Editor

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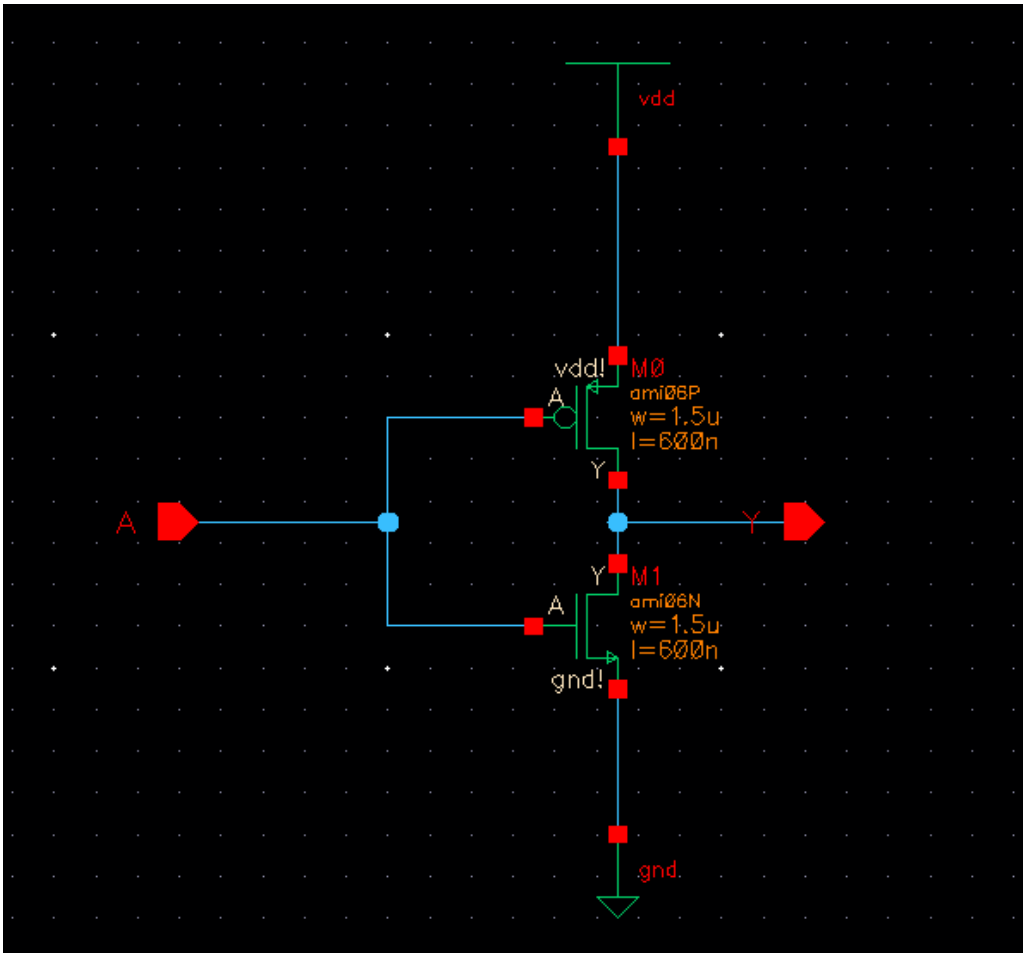
In this lab, the goal is to achieve multiple milestones:

1) Learn how to work with the Symbol Editor.

2) Create symbols for an inverter and a nor gate.

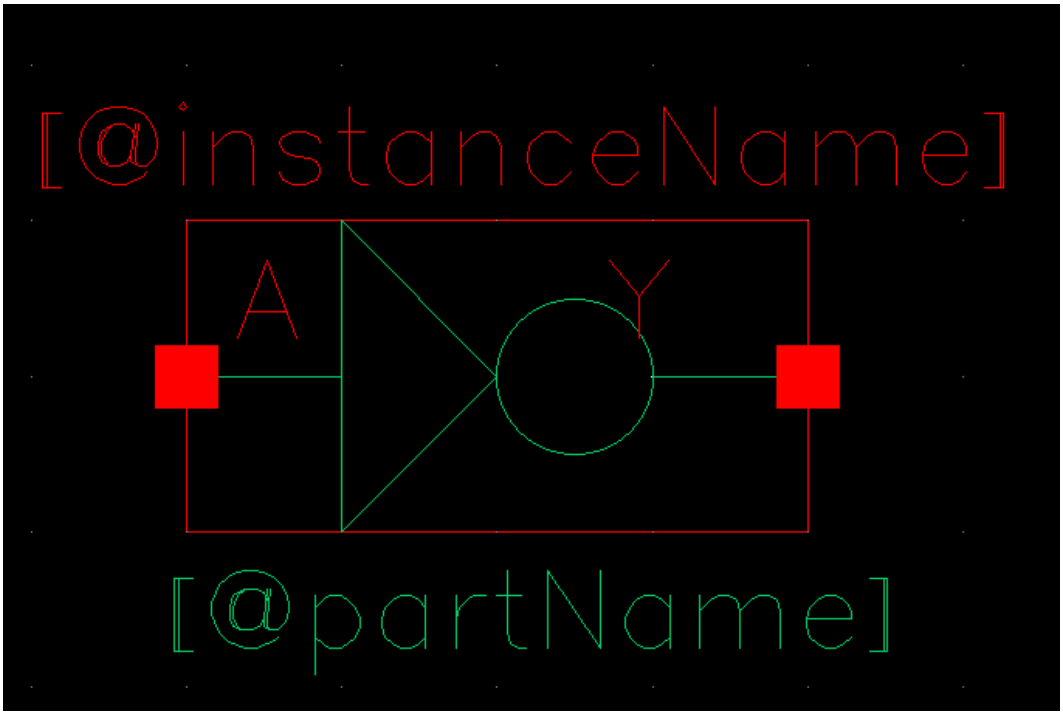
3) Simulate a simple digital circuit with multiple gates in it and simulate it.

Inverter Schematic:



Now to create a symbol for the inverter, Create -> Cellview -> From Cellview. In the box named *To View Name*, **symbol** is chosen**.**

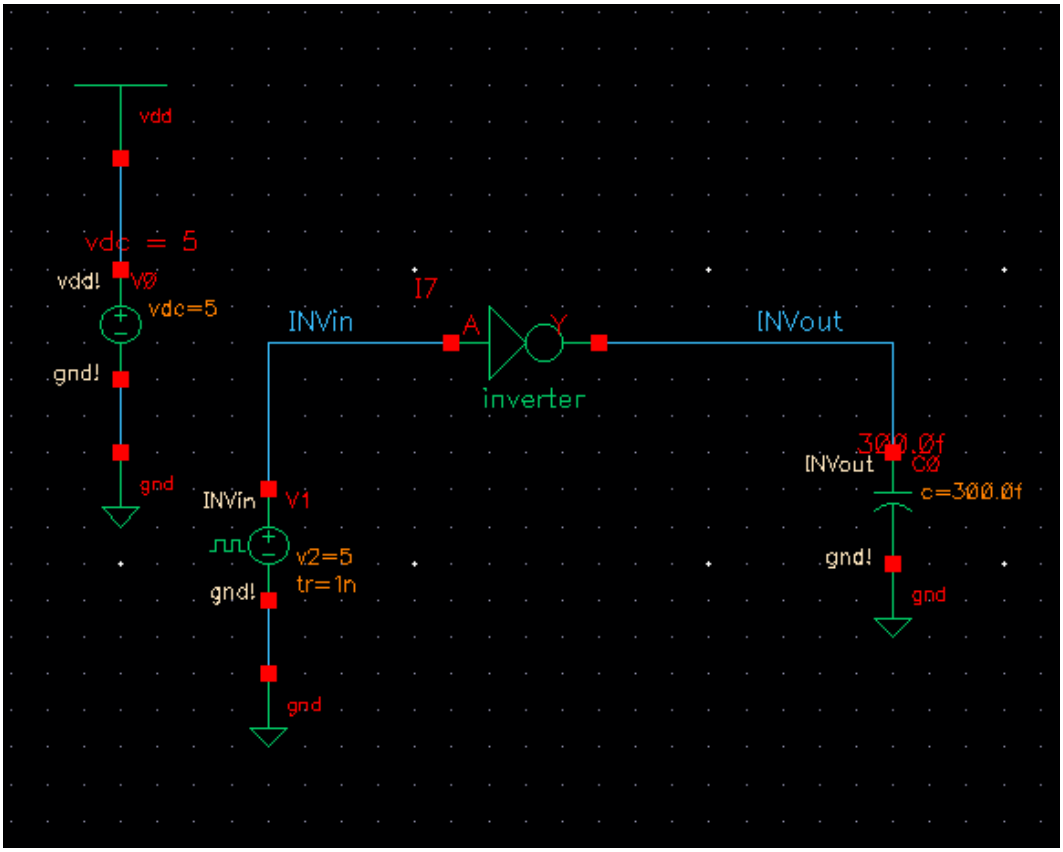
The final **inverter symbol**:



where red stuff is the electrical stuff and green stuff is the cosmetic stuff.

Now replacing the symbol in the **TBinverter** created in lab 2, the transient analysis is performed.

Circuit diagram:



The **output results** are similar to the ones obtained in the previous lab and establishes that the inverter works correctly:

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Output and IC/nodeset summary:
                 save   2       (current)
                 save   6       (voltage)

    tran: time = 26.17 ns    (2.62 %), step = 6.545 ns     (655 m%)
    tran: time = 78.63 ns    (7.86 %), step = 4.472 ns     (447 m%)
    tran: time = 127.7 ns    (12.8 %), step = 7.299 ns     (730 m%)
    tran: time = 178.7 ns    (17.9 %), step = 4.514 ns     (451 m%)
    tran: time = 227.8 ns    (22.8 %), step = 7.337 ns     (734 m%)
    tran: time = 278.7 ns    (27.9 %), step = 4.508 ns     (451 m%)
    tran: time = 327.8 ns    (32.8 %), step = 7.344 ns     (734 m%)
    tran: time = 378.7 ns    (37.9 %), step = 4.507 ns     (451 m%)
    tran: time = 427.8 ns    (42.8 %), step = 7.354 ns     (735 m%)
    tran: time = 478.7 ns    (47.9 %), step = 4.506 ns     (451 m%)
    tran: time = 527.8 ns    (52.8 %), step = 7.364 ns     (736 m%)
    tran: time = 578.7 ns    (57.9 %), step = 4.505 ns     (450 m%)
    tran: time = 627.9 ns    (62.8 %), step = 7.375 ns     (737 m%)
    tran: time = 678.7 ns    (67.9 %), step = 4.503 ns     (450 m%)
    tran: time = 727.9 ns    (72.8 %), step = 7.381 ns     (738 m%)
    tran: time = 778.7 ns    (77.9 %), step = 4.503 ns     (450 m%)
    tran: time = 827.9 ns    (82.8 %), step = 7.387 ns     (739 m%)
    tran: time = 878.7 ns    (87.9 %), step = 4.502 ns     (450 m%)
    tran: time = 927.9 ns    (92.8 %), step = 7.393 ns     (739 m%)
    tran: time = 978.7 ns    (97.9 %), step = 4.502 ns     (450 m%)
Number of accepted tran steps =             946

Maximum value achieved for any signal of each quantity:
V: V(INVout) = 5.004 V
I: I(V0:p) = 305.2 uA
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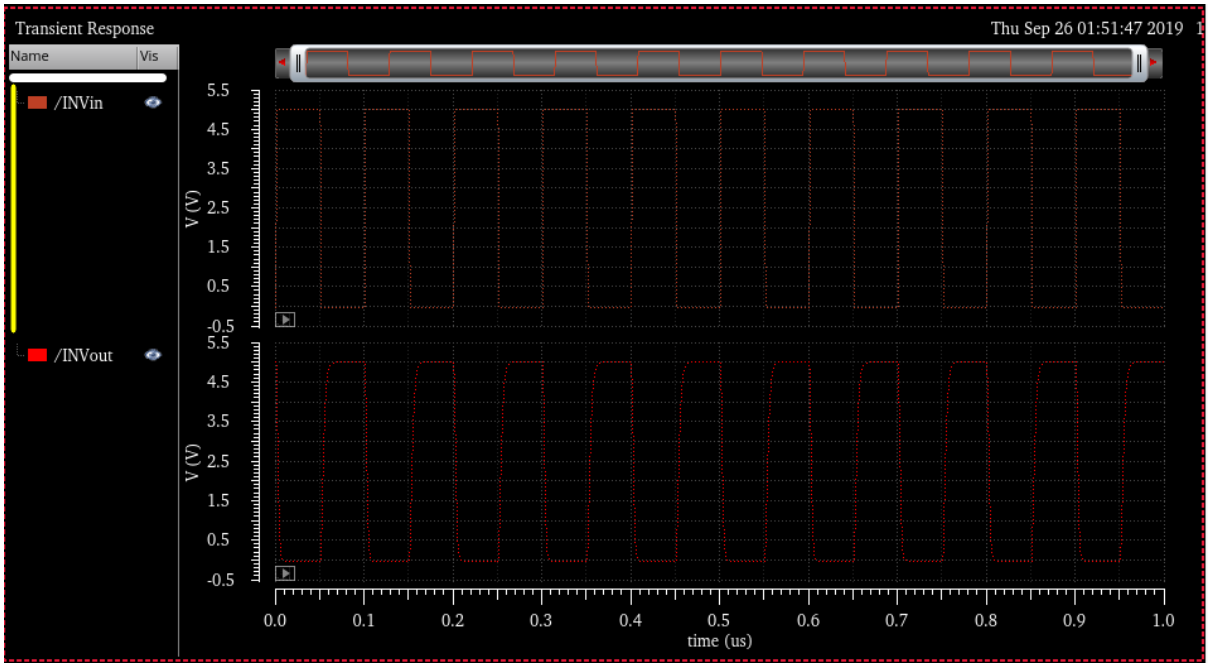
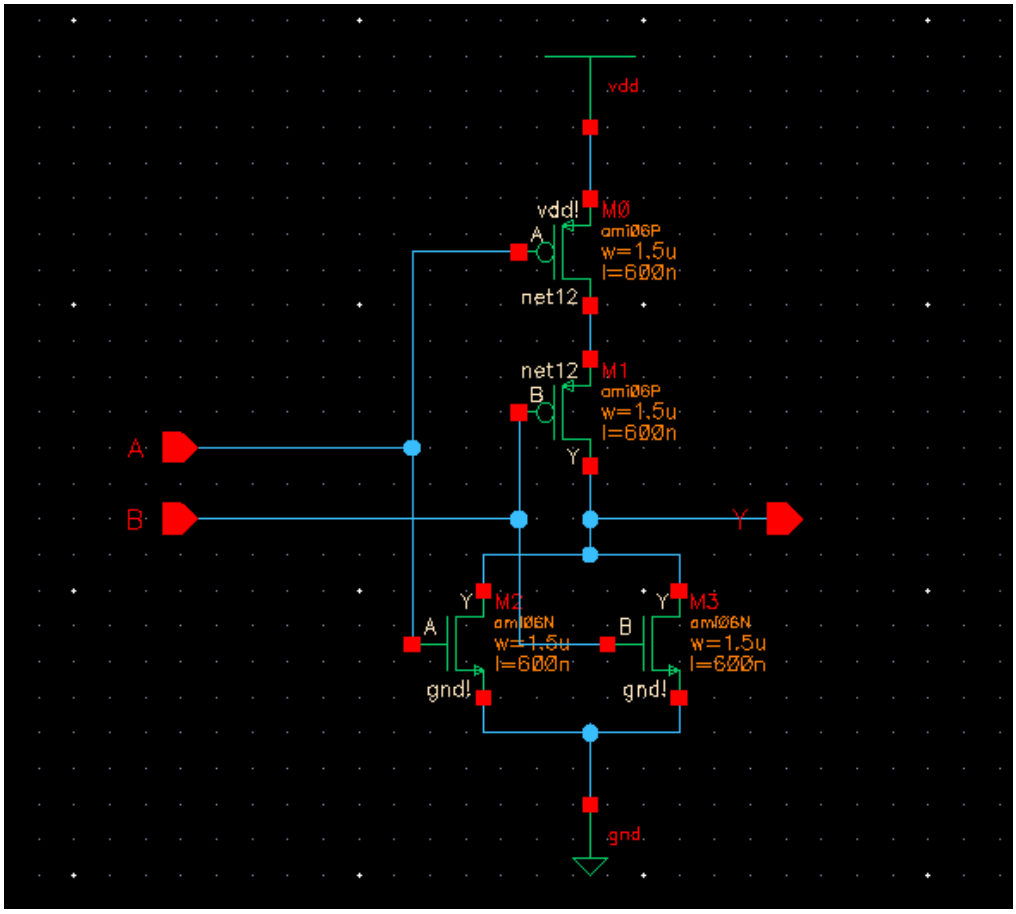
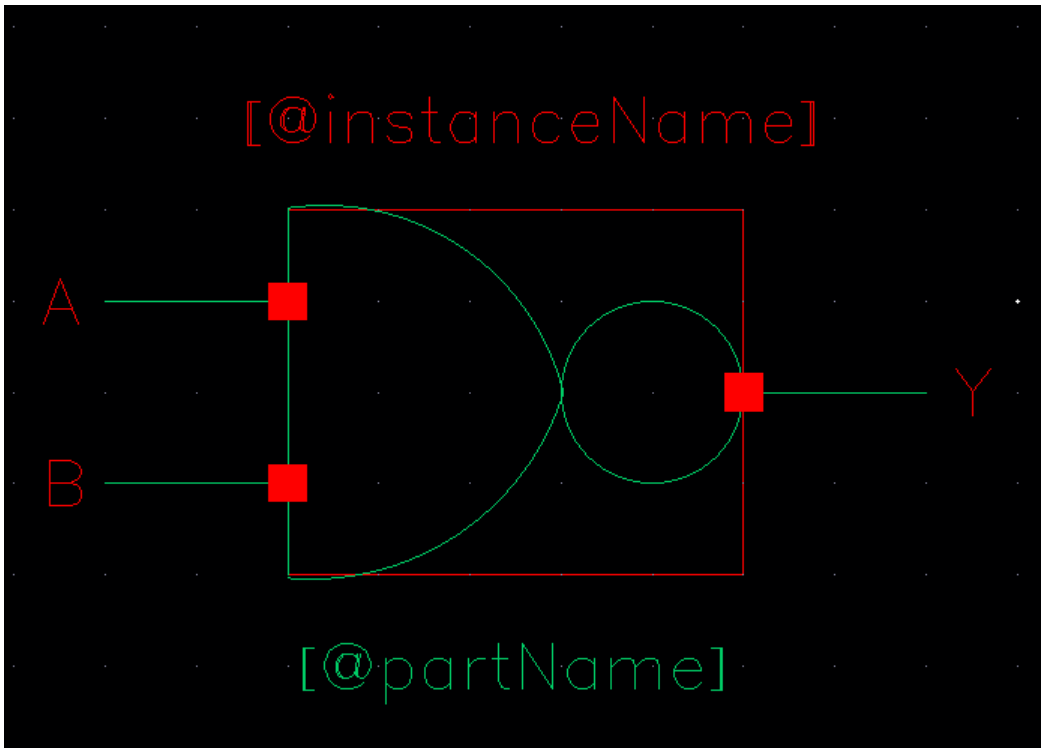


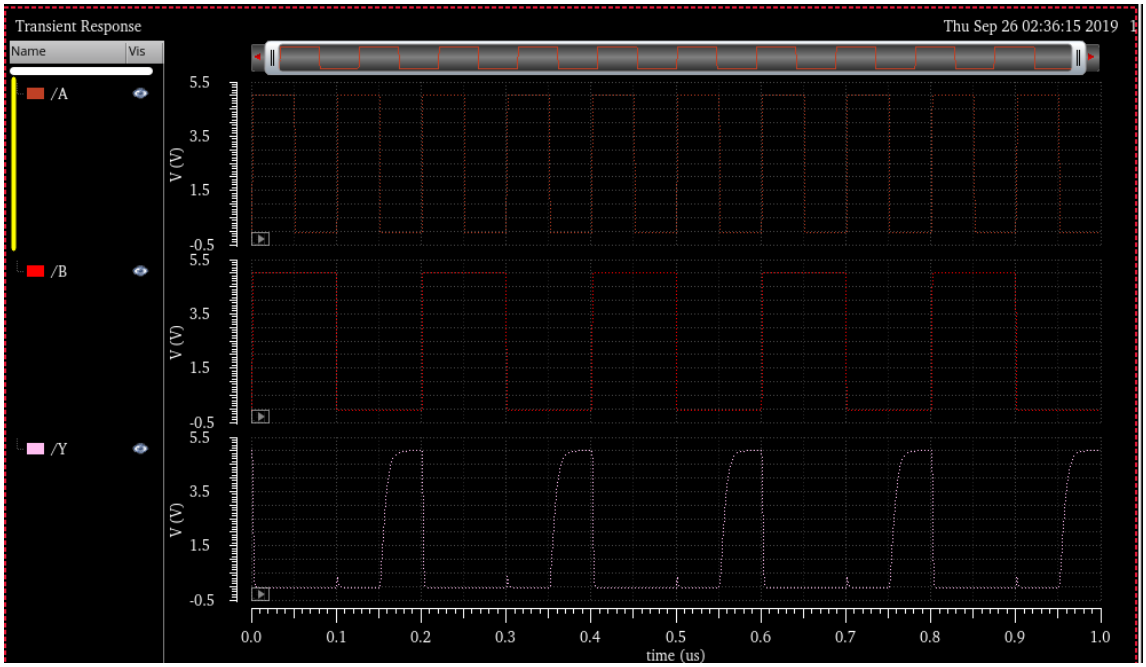
NOR Gate Schematic:



The final **nor gate symbol**:



The **output results**:



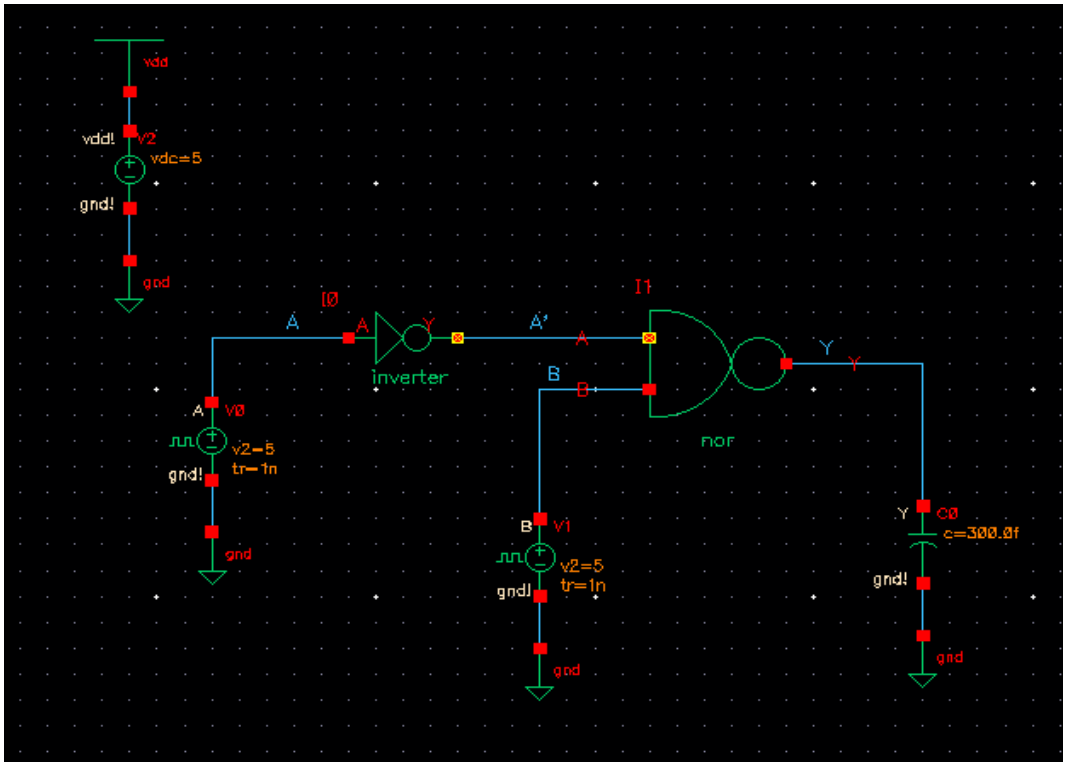
The output shows only when both the inputs are LOW (0), the output is HIGH (1). Hence, the NOR gate is verified.

Implementing a simple Boolean Function: Y= AB'

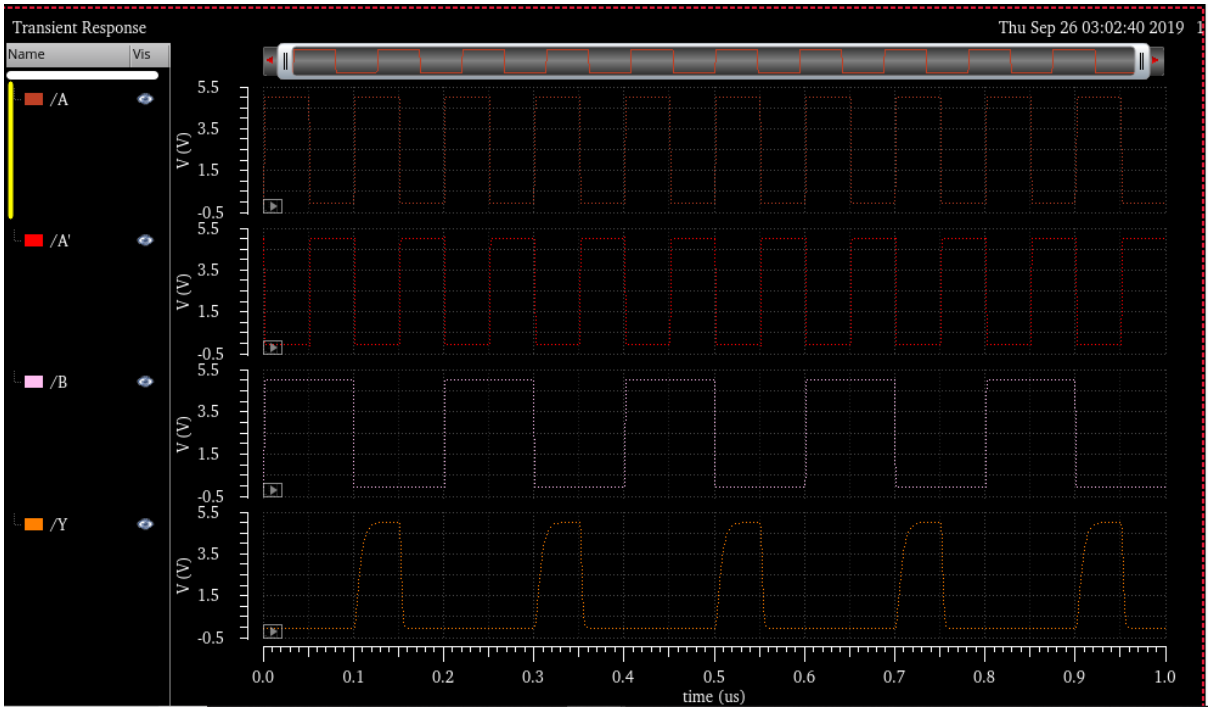
Simplification: Y= AB'= (A'+B)'= **NOR (NOT (A), B)**

Hence, the Boolean function Y can be achieved using a NOR gate and an inverter.

The circuit schematic:



The **output results**:



The output shows only when the inputs A is HIGH (1) and B is LOW (0), the output is HIGH (1). Hence, the expression is verified from the truth table below.

Truth Table:

A	**B**	**A'**	**Y**
0	0	1	0
0	1	1	0
1	0	0	1
1	1	0	0