ECE520 Introduction to VLSI: Project 1

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Boolean Function: Y=A'B+B'C'+AC

Truth Table:

A	B	C	Y	Y'
0	0	0	1	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0

Since Y has **2 zeroes** and **6 ones**, we should consider the zeroes in order to create the circuit using PMOS and NMOS transistors for optimal transistor use.

Y= (Y')'= (A'B'C + ABC')'= NOR (A'B'C, ABC')

Now, A'B'C= AND (NOT A, NOT B, C) & ABC'= AND (A, B, NOT C) where the AND gate can be realised using a NAND gate followed by an Inverter.

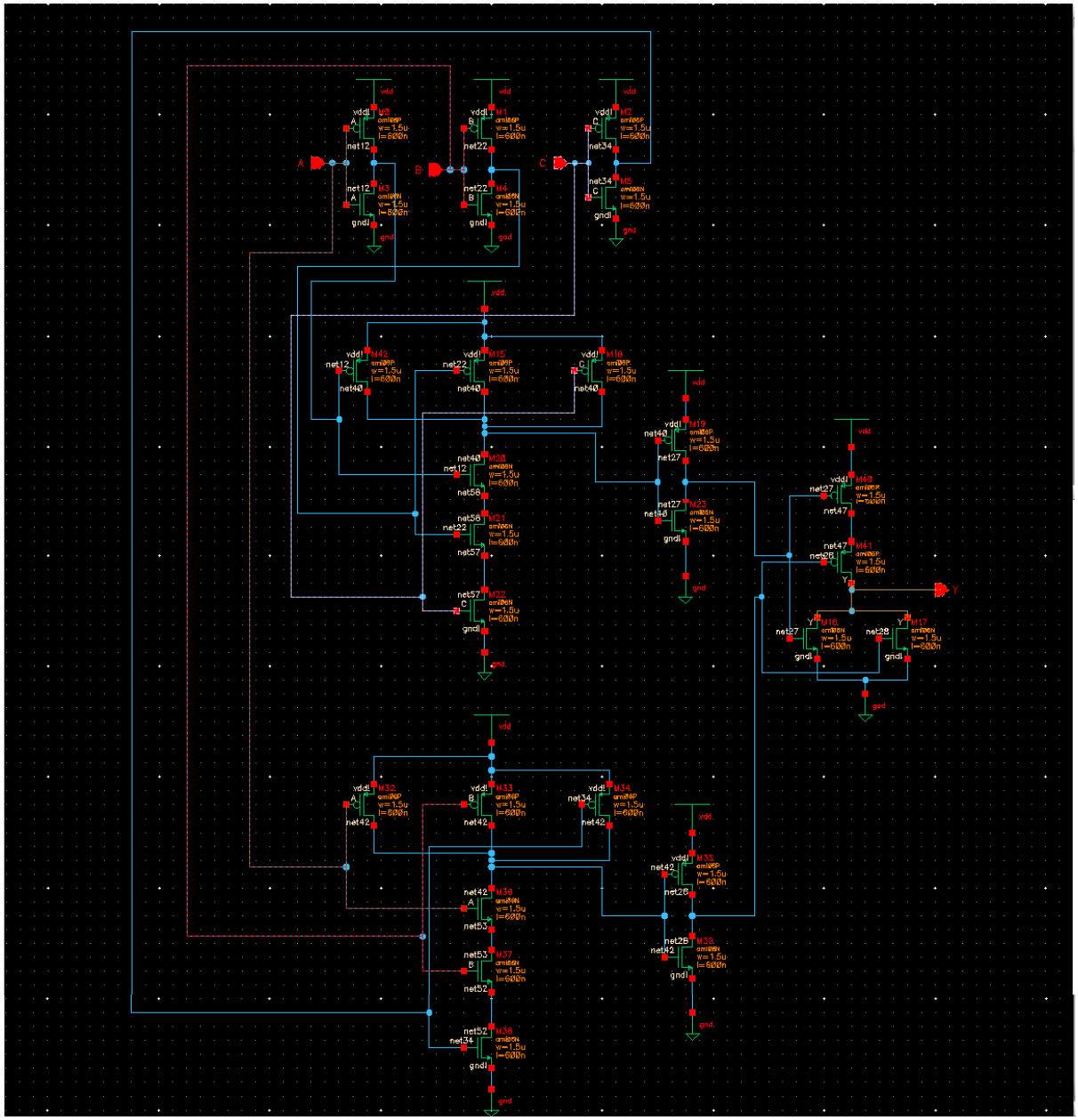
Therefore, **Y = NOR (NOT (NAND (NOT A, NOT B, C)), NOT (NAND (A, B, NOT C)))**

For the first part, the Boolean function is realized using PMOS and NMOS transistors only.

1) yabcMOS

The yabcMOS schematic is shown below:

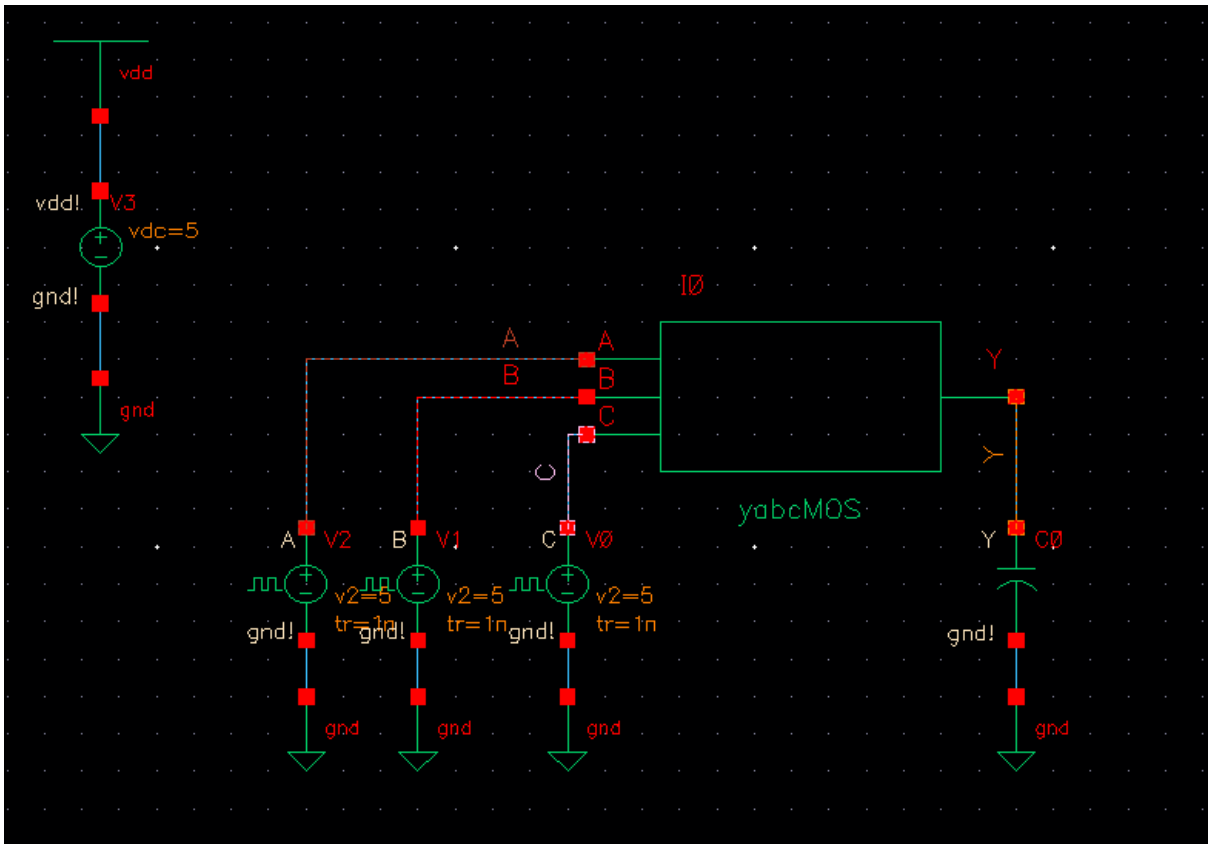
It is designed using the 13 PMOS and 13 NMOS transistors, which is 26 transistors in total. The pull-down and pull-up networks, which are complimentary to one another, are clearly shown as taught in Lecture 1. Six transistors are used in the first stage to obtain the compliments of each input. Sixteen transistors are used in the next stage to obtain the individual three input expressions, A'B'C and ABC' as stated above. In the final stage, four transistors are used to perform the equivalent NOR operation using two PMOS and two NMOS respectively to obtain the required Boolean expression Y.



The **yabcMOS** is saved as a generic symbol to be used in the test bench TByabcMOS, and can be referred to by Shift+X.

The yabcMOS symbol is shown below:

This lets us use the entire yabcMOS circuit inside the test bench and simulate the results. The test bench circuit, TByabcMOS is shown below:



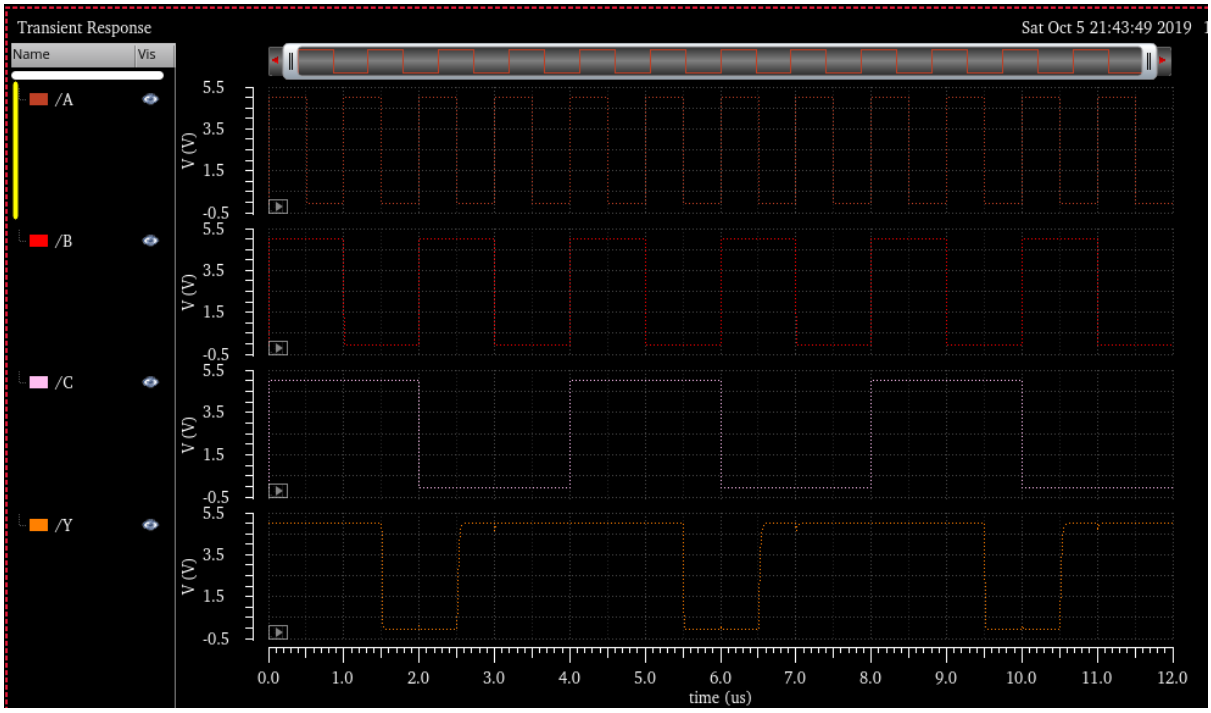
The **vpulse** at the three inputs (A, B, C) are given as follows:

Input	**A**	**B**	**C**
Voltage 2	5 V	5 V	5 V
Pulse Period	1 µs	2 µs	4 µs
Pulse Width	500 ns	1 µs	1 µs
Rise Time	1 ns	1 ns	1 ns
Fall Time	1 ns	1 ns	1 ns
Time Delay	1 ns	1 ns	1 ns

The capacitor value at the output is kept very low at 1 pF.

The transient analysis is run for 12 µs, so that the values can be compared and verified from the truth table.

The output waveform is given below:

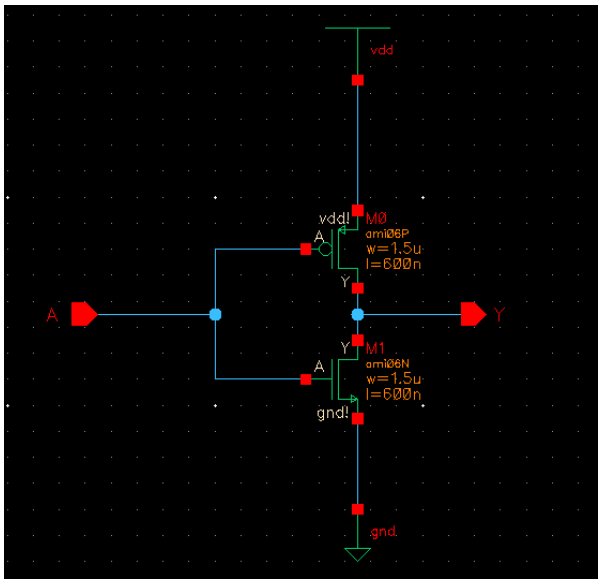


The output Y is completely in accordance to the truth table for all the 8 possible inputs, hence the designed circuit using PMOS and NMOS transistors works correctly.

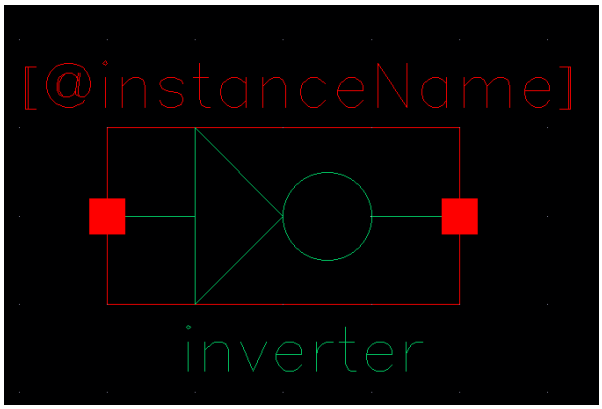
2) yabcGates

To implement the Boolean function Y, only inverter, NAND and NOR gates can be used.
So for that the inverter, NAND (2 input and 3 input) and NOR (2 input and 3 input) are drawn and tested before.

a. Inverter (NOT gate)

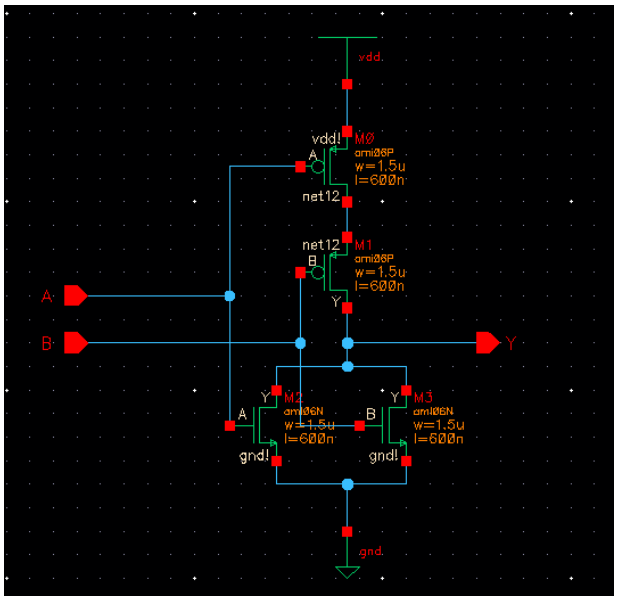


Inverter Schematic

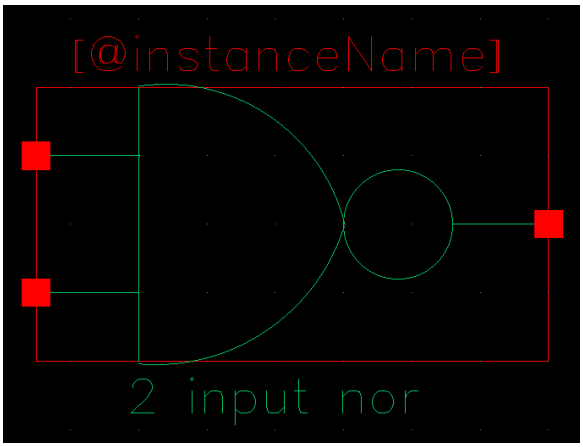


Inverter Symbol

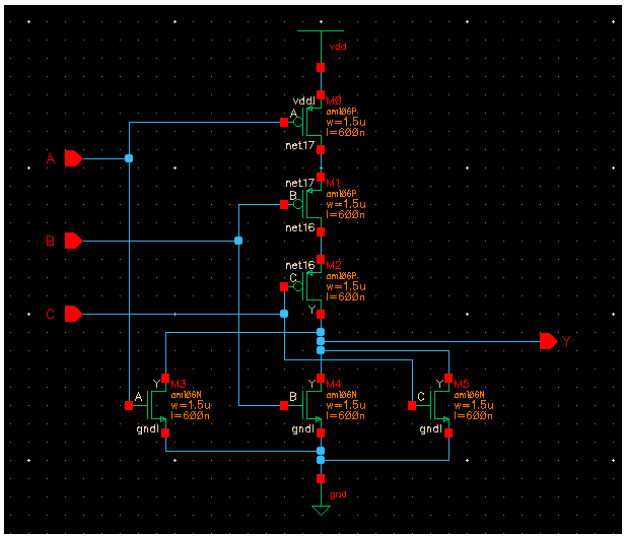
b. NOR Gate



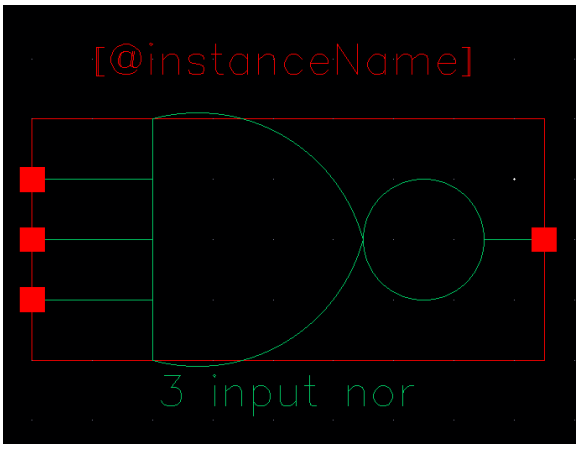
2 Input NOR Schematic



2 Input NOR Symbol

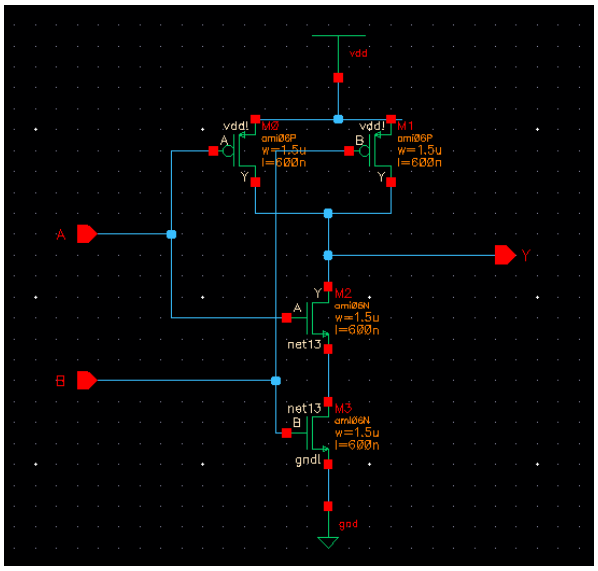


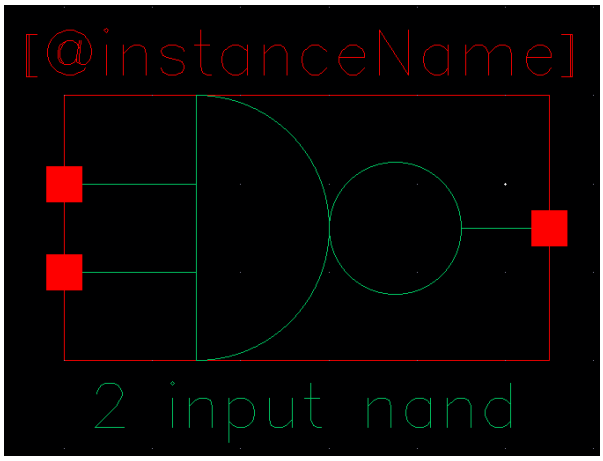
3 Input NOR Schematic



3 Input NOR Symbol

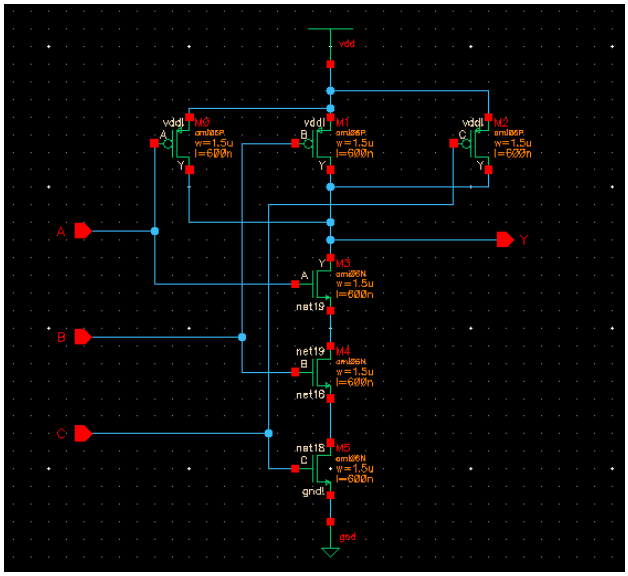
c. NAND Gate

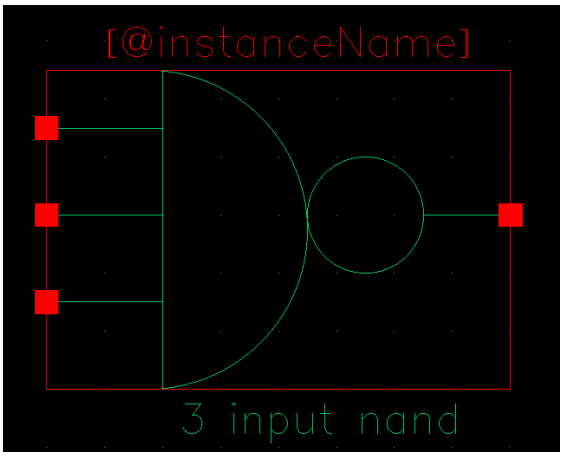




2 input NAND Schematic

2 input NAND Symbol





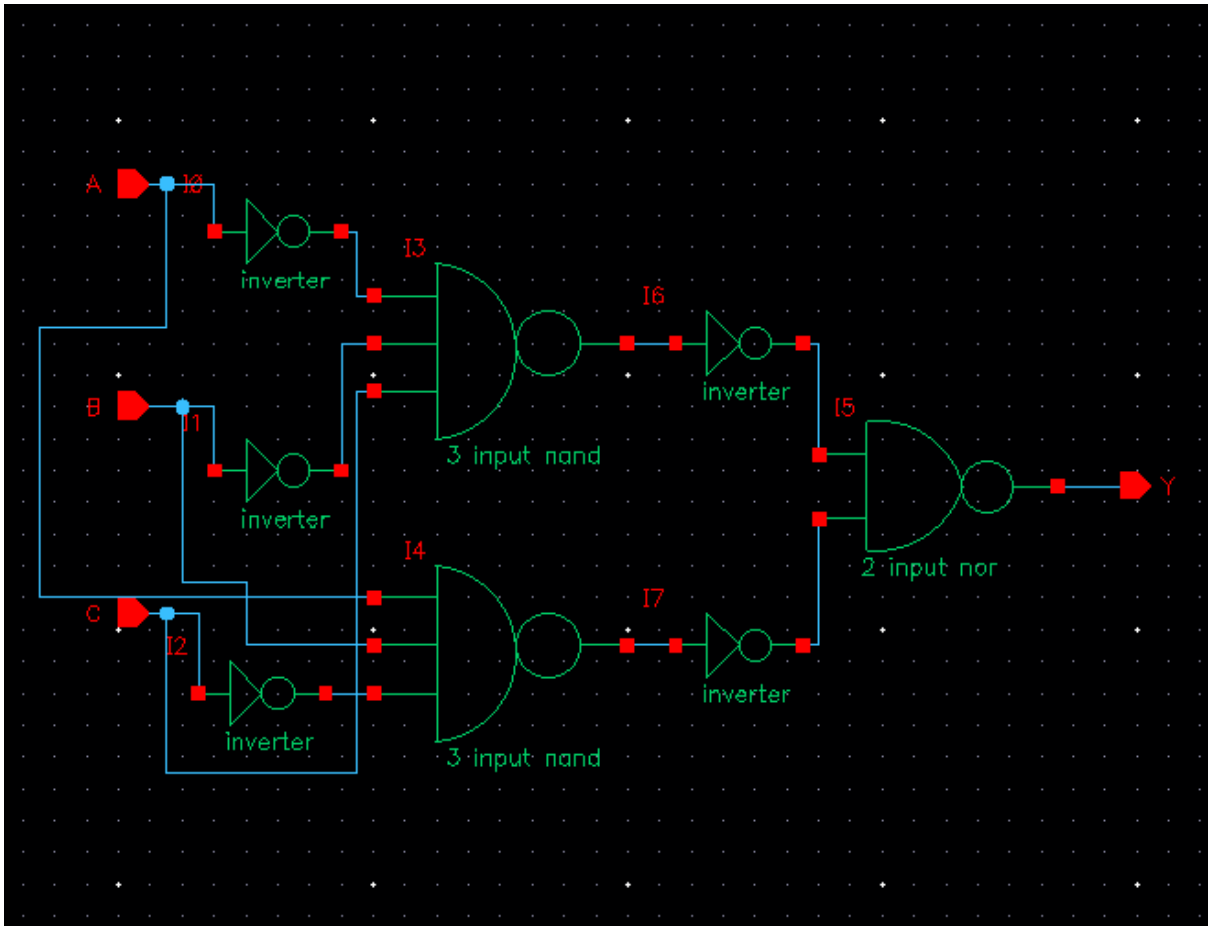
3 input NAND Schematic

3 input NAND Symbol

Now, since the basic gates are designed, the yabcGates schematic is designed using these 3 gates only as discussed above.

Y = NOR (NOT (NAND (NOT A, NOT B, C)), NOT (NAND (A, B, NOT C)))

The yabcGates schematic is shown below:



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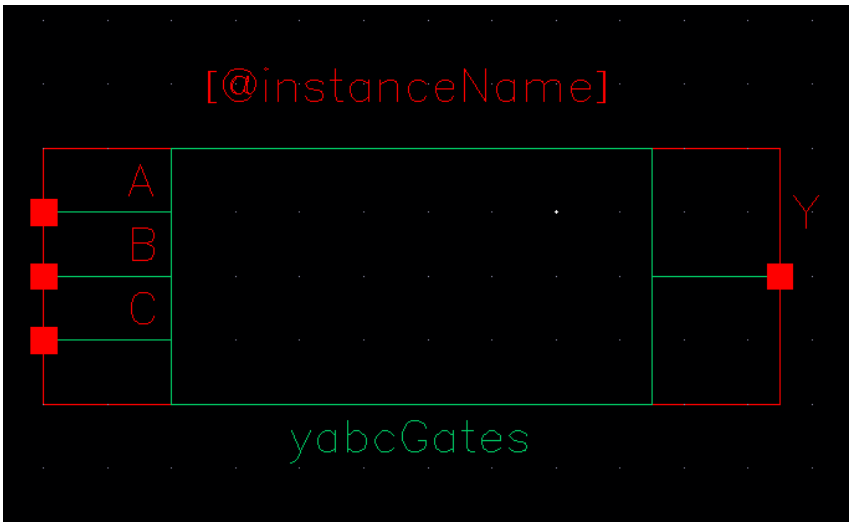
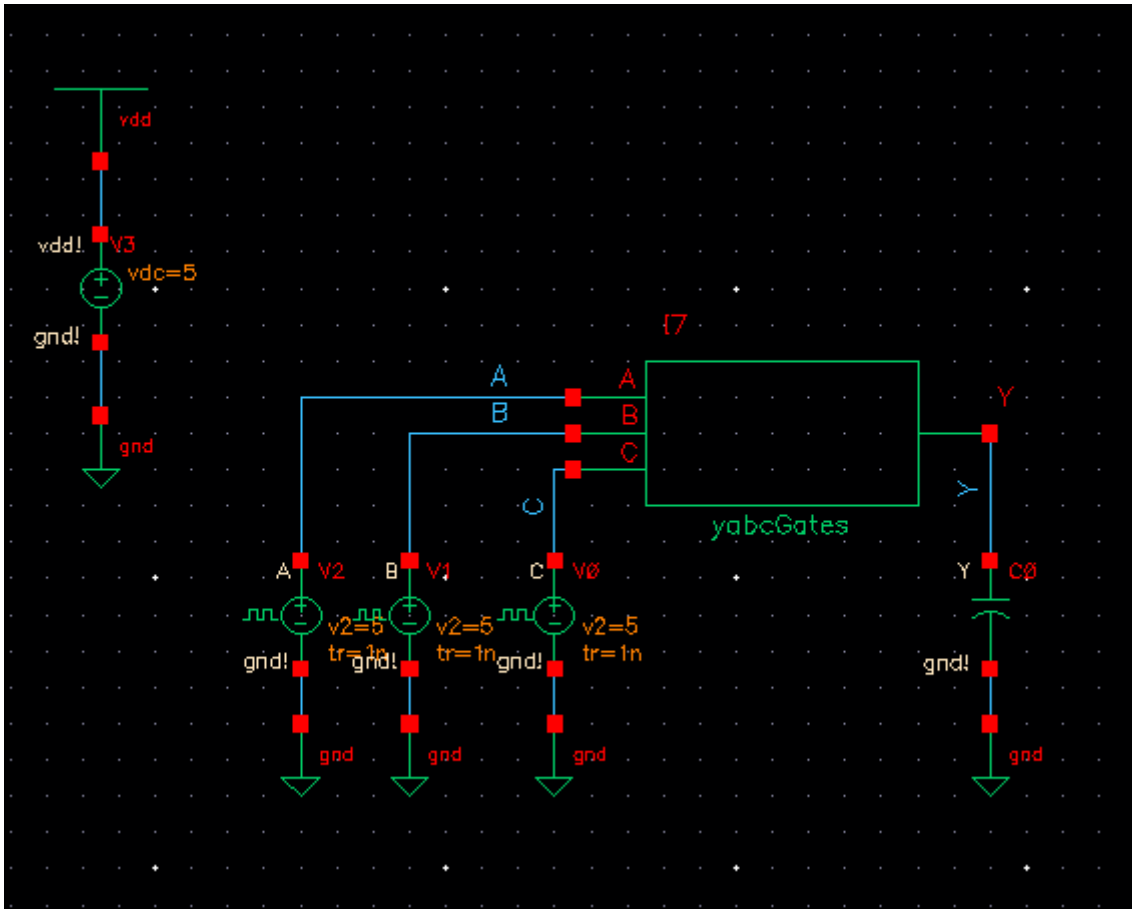


This lets us use the entire yabcGates circuit inside the test bench and simulate the results. The test bench circuit, TByabcGates is shown below:



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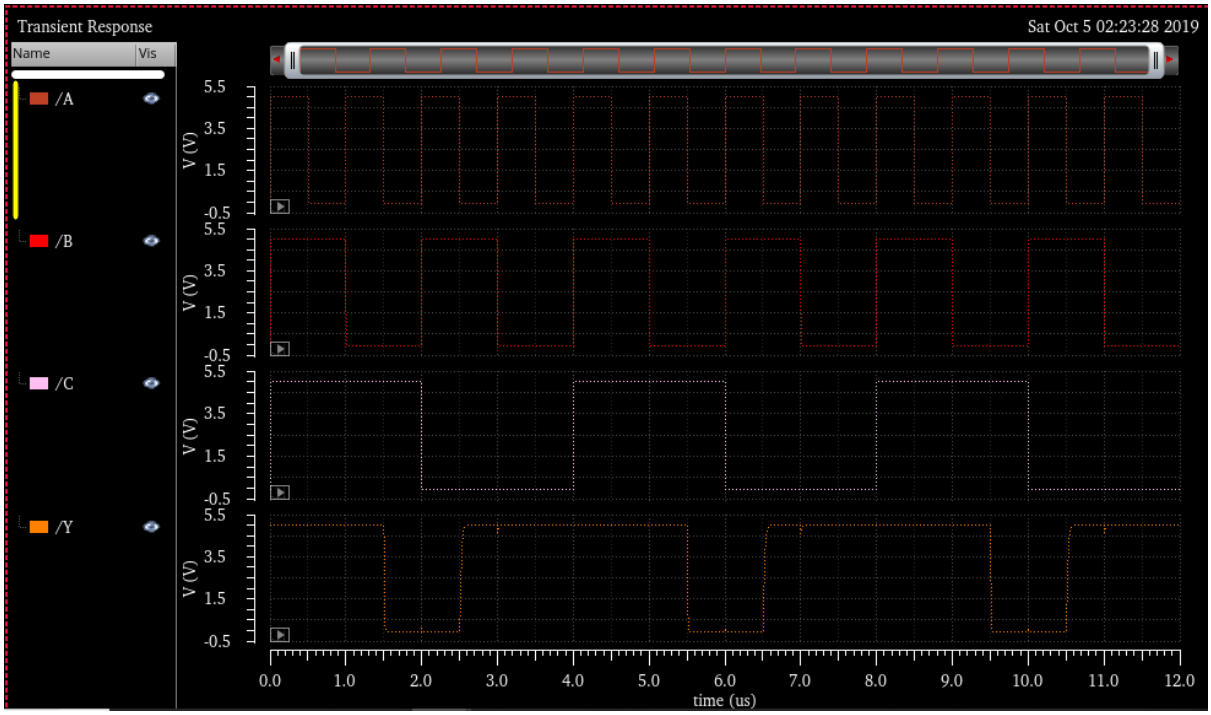

The output Y is completely in accordance to the truth table for all the 8 possible inputs, hence the designed circuit using inverter, NAND and NOR gates works correctly.

Hence, the designing of the Boolean function Y by two different methods is successful.