ECE520 Introduction to VLSI, Project 4

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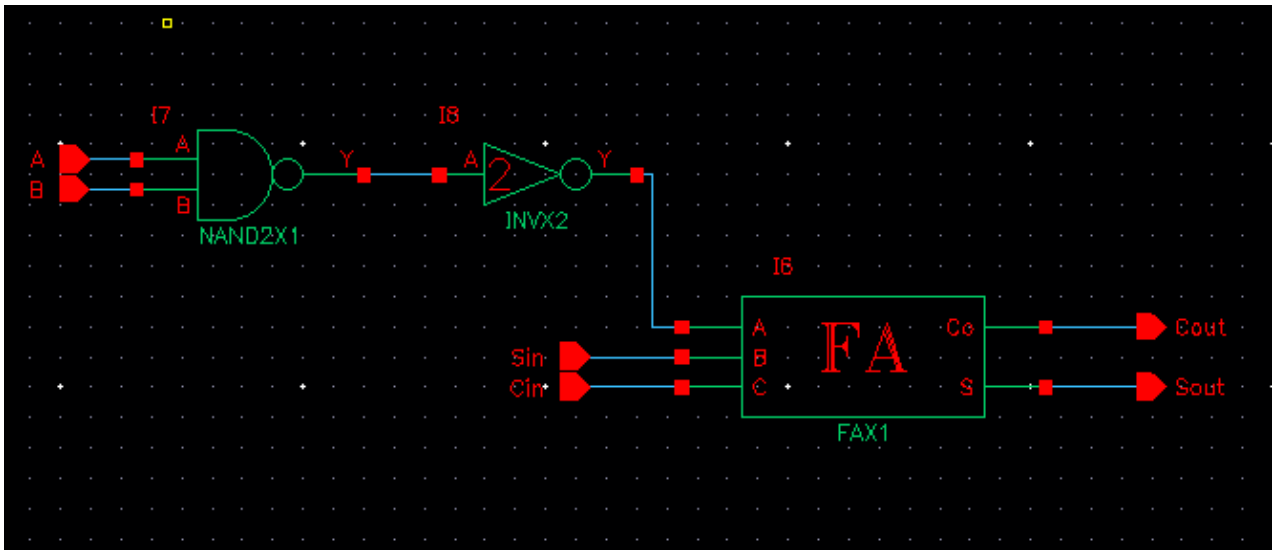
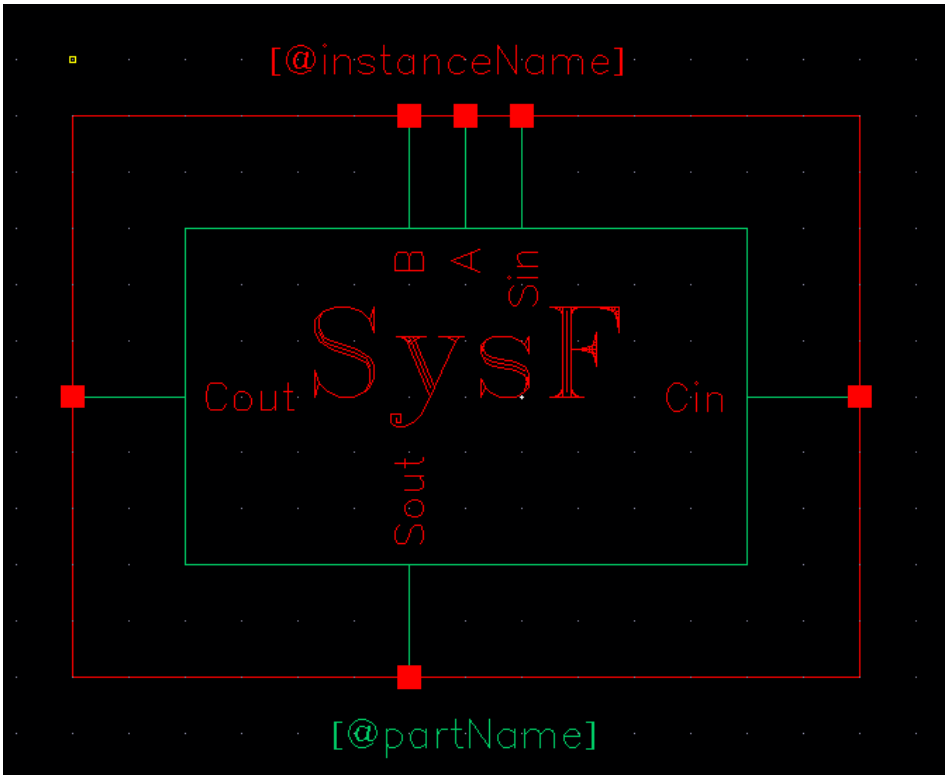
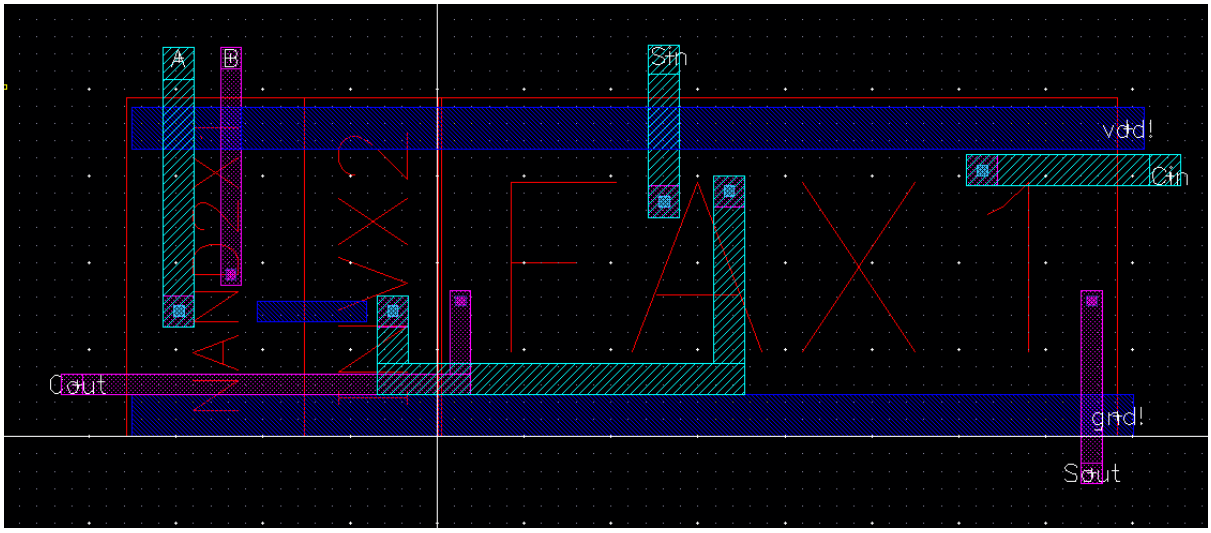
Part A



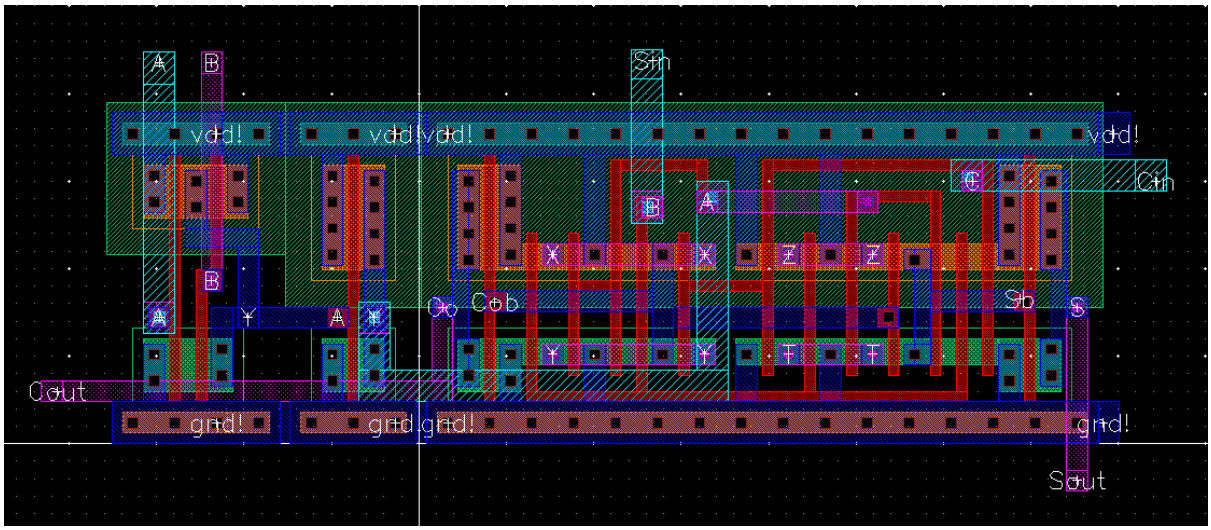
SysF schematic



SysF symbol



SysF layout (Top level)



SysF layout (Lower level)

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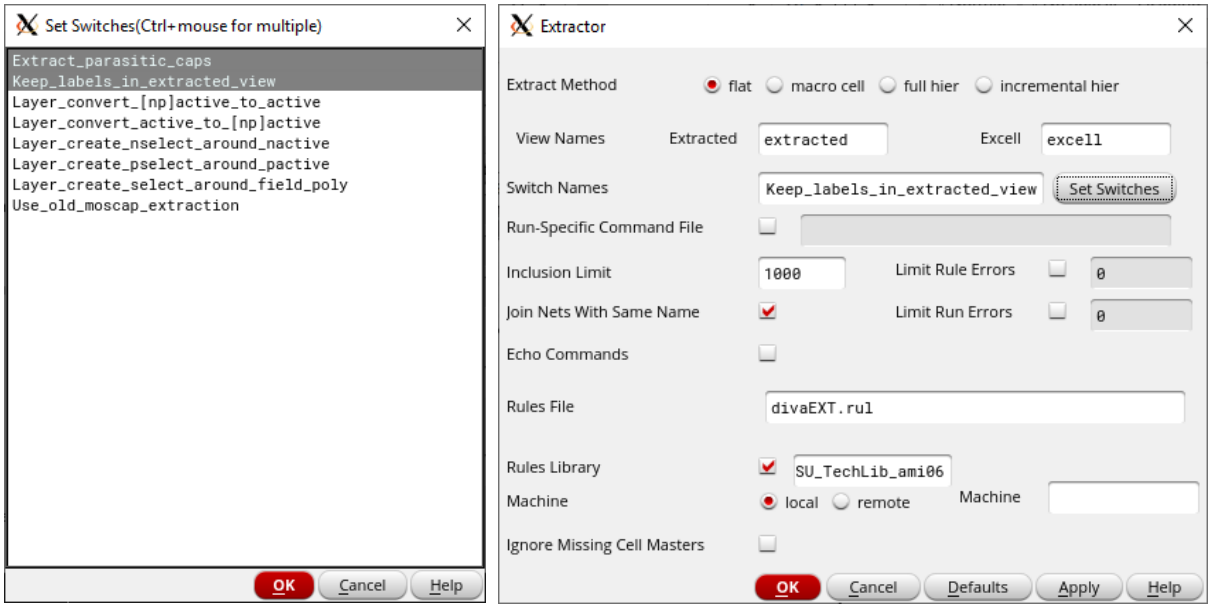
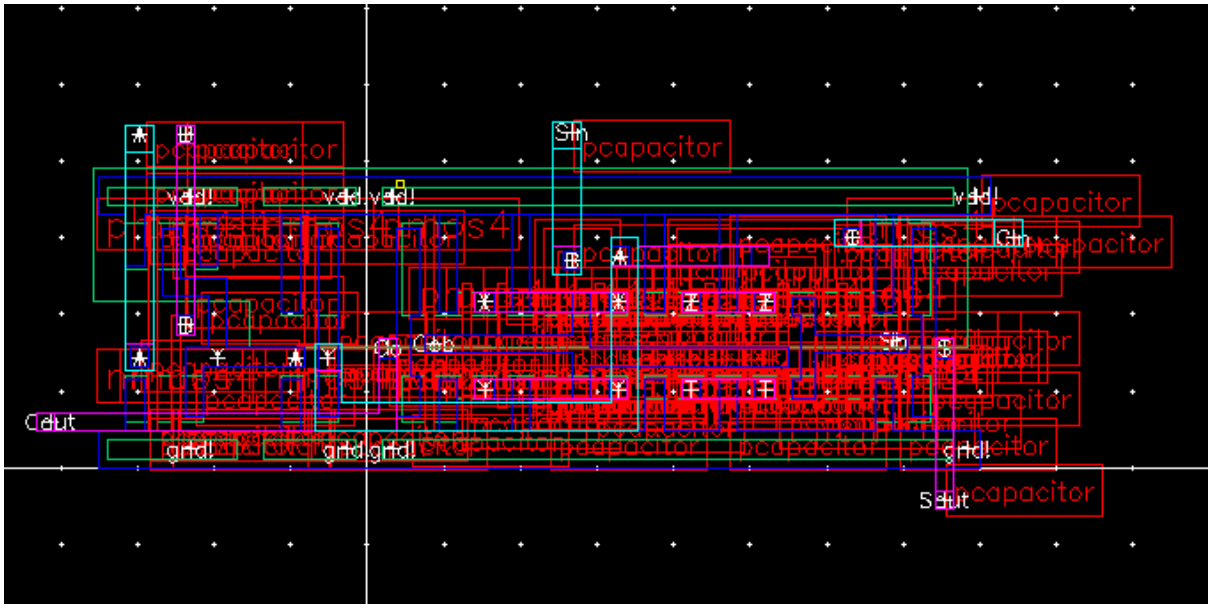
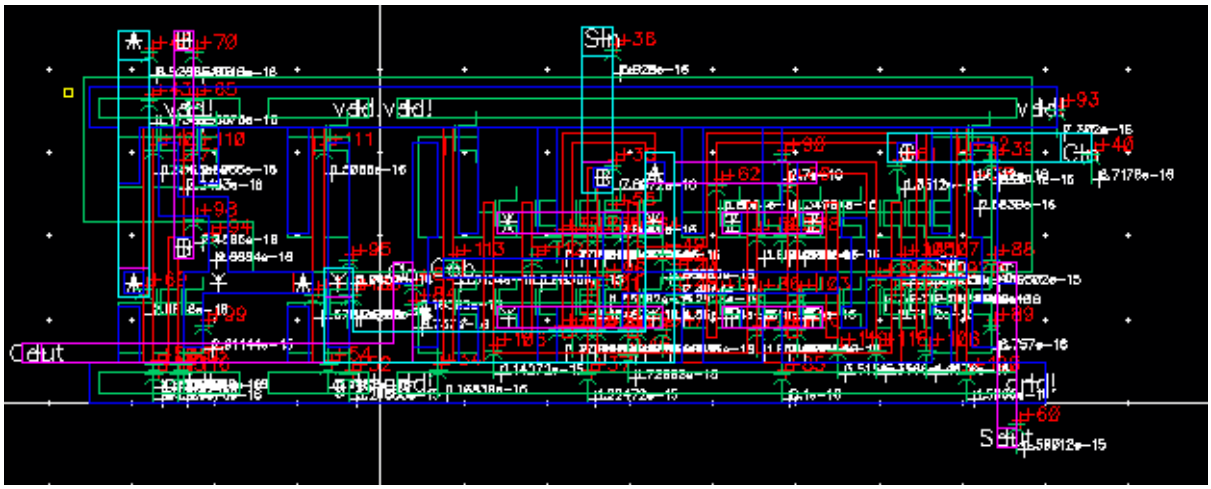




SysF extracted view (Top Level)

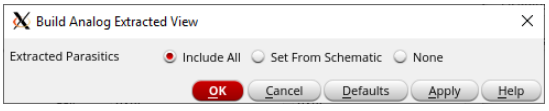


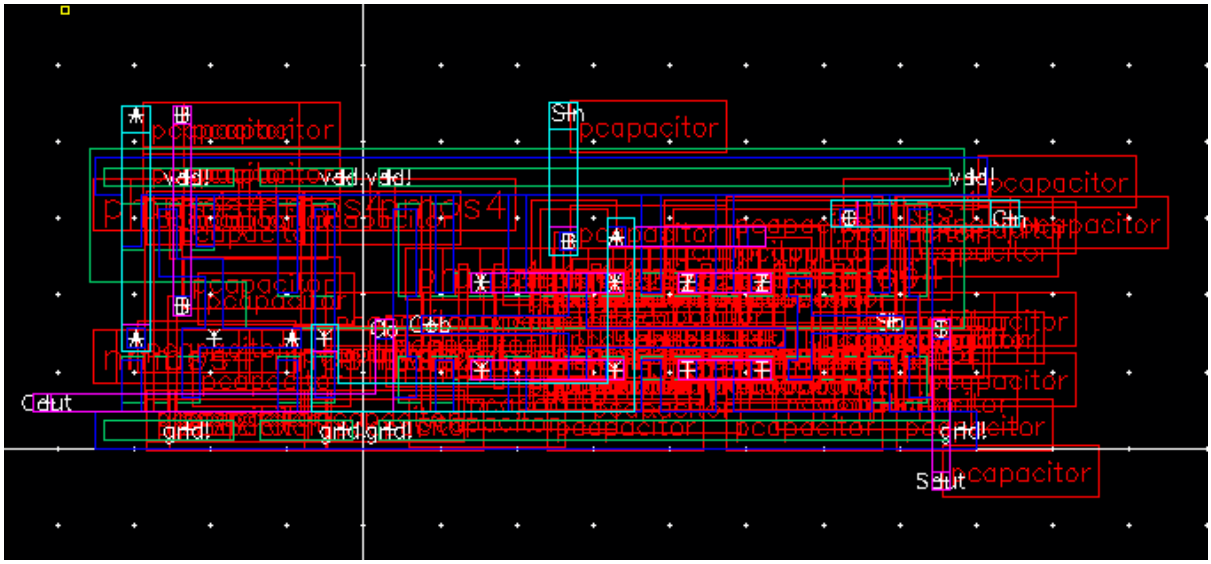
SysF extracted view (Lower Level)


Artist LVS
Commands Help
cadence
Run Directory
LVS
Browse
Create Netlist
schematic
extracted
Library
PROJ4
PROJ4
Cell
SysF
SysF
View
schematic
extracted
Browse
Sel by Cursor
Browse
Sel by Cursor
Rules File
divaLVS.rul
Browse
Rules Library
NCSU_TechLib_ami06
LVS Options
Rewiring
Device Fixing
Create Cross Reference
Terminals
Correspondence File
lvs_corr_file
Create
Switch Names
Priority
0
Run
background
Run
Output
Error Display
Monitor
Info
Backannotate
Parasitic Probe
Build Analog
Build Mixed
22


The LVS job has completed. The net-lists match.
Run Directory: /network/rit/home/as447343/cadence/LVS
Close

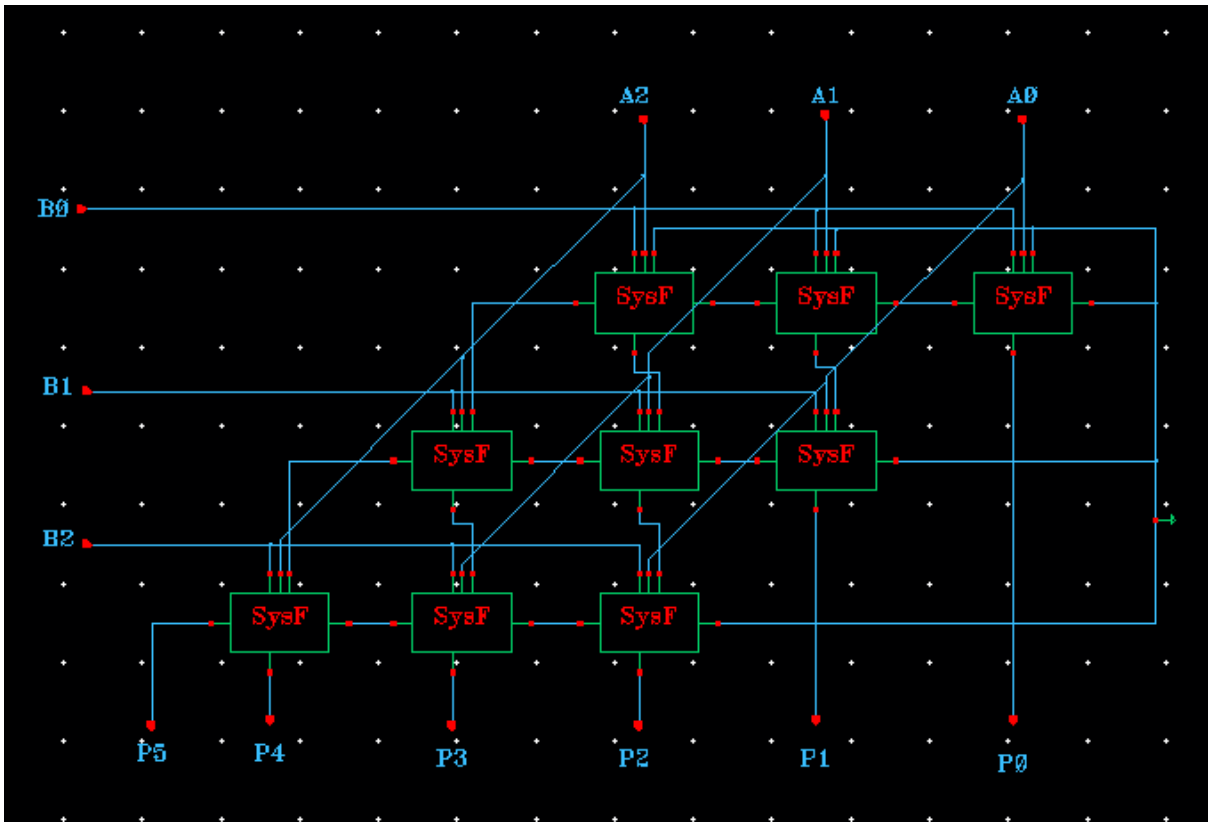

Artist LVS
Commands Help
cadence
Run Directory
LVS
Browse
Create Netlist
schematic
extracted
Library
PROJ4
PROJ4
Cell
SysF
SysF
View
schematic
analog_extracted
Browse
Sel by Cursor
Browse
Sel by Cursor
Rules File
divaLVS.rul
Browse
Rules Library
NCSU_TechLib_ami06
LVS Options
Rewiring
Device Fixing
Create Cross Reference
Terminals
Correspondence File
lvs_corr_file
Create
Switch Names
Priority
0
Run
background
Run
Output
Error Display
Monitor
Info
Backannotate
Parasitic Probe
Build Analog
Build Mixed
22


Build Analog Extracted View
Extracted Parasitics
Include All
Set From Schematic
None
OK
Cancel
Defaults
Apply
Help

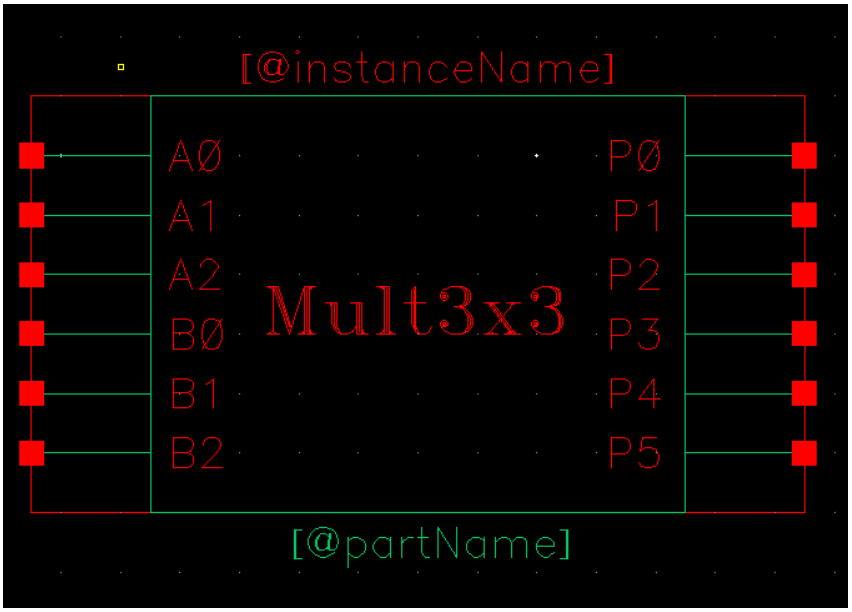


SysF analog extracted view

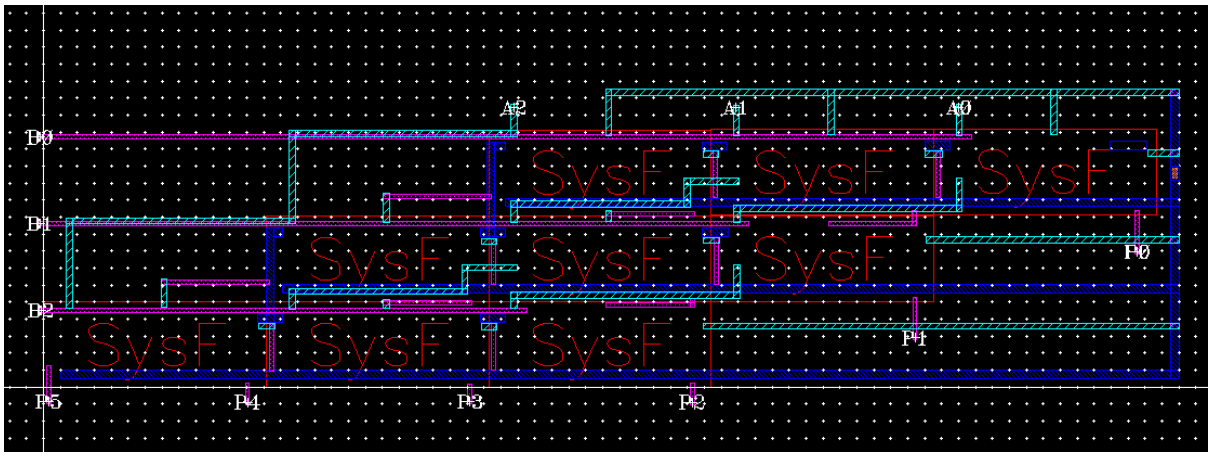
Part B



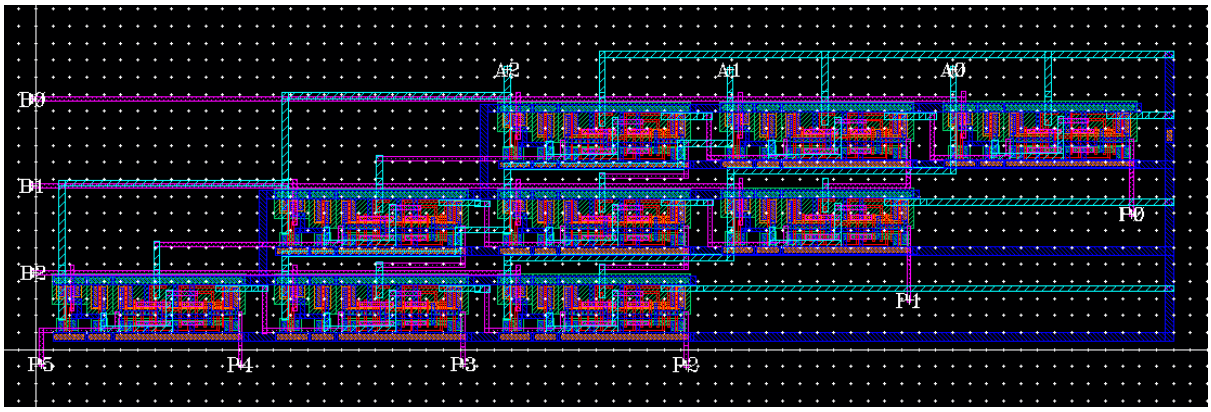
Mult3x3 schematic



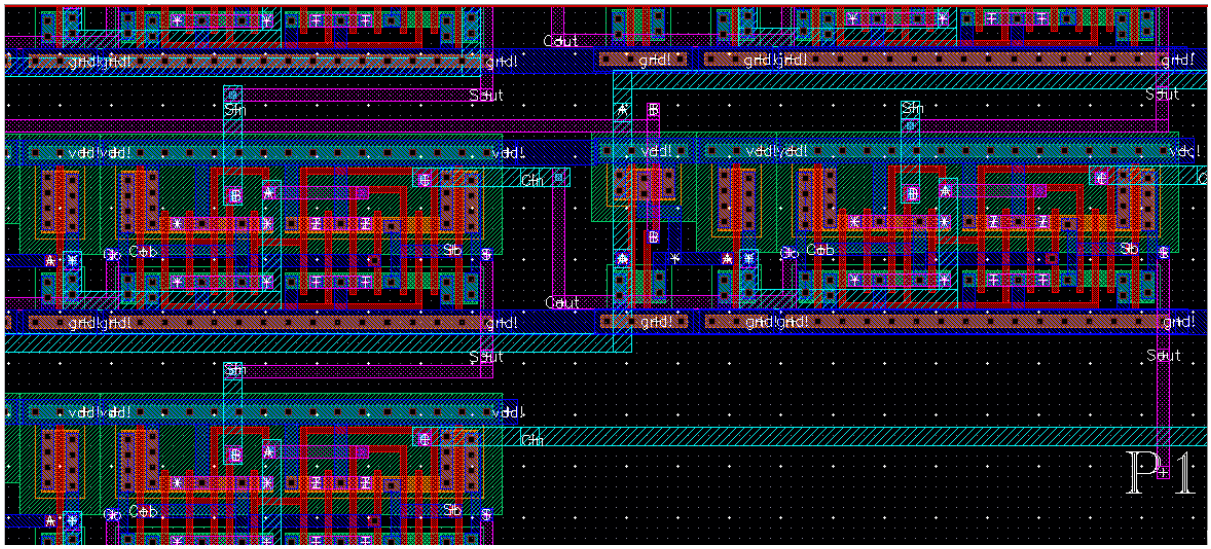
Mult3x3 symbol



Mult3x3 Layout (Top Level)



Mult3x3 Layout (Lower Level)



Mult3x3 Layout (zoomed in to individual SysF cells)

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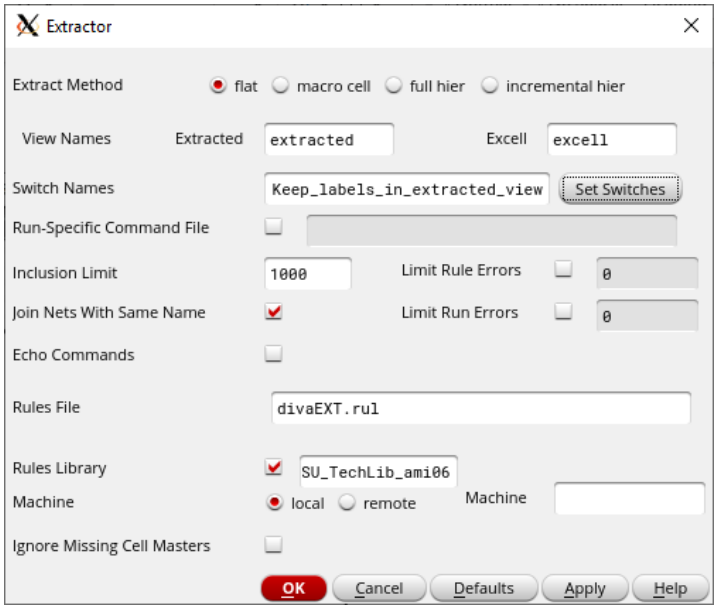
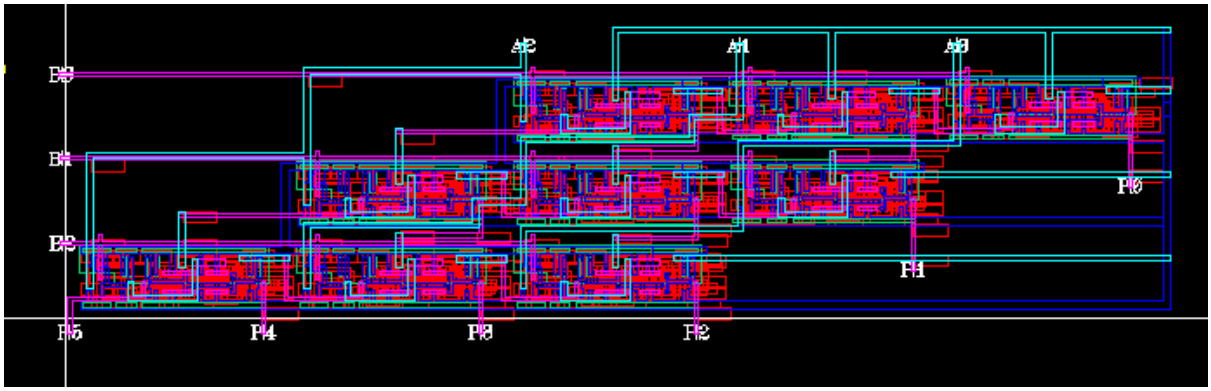
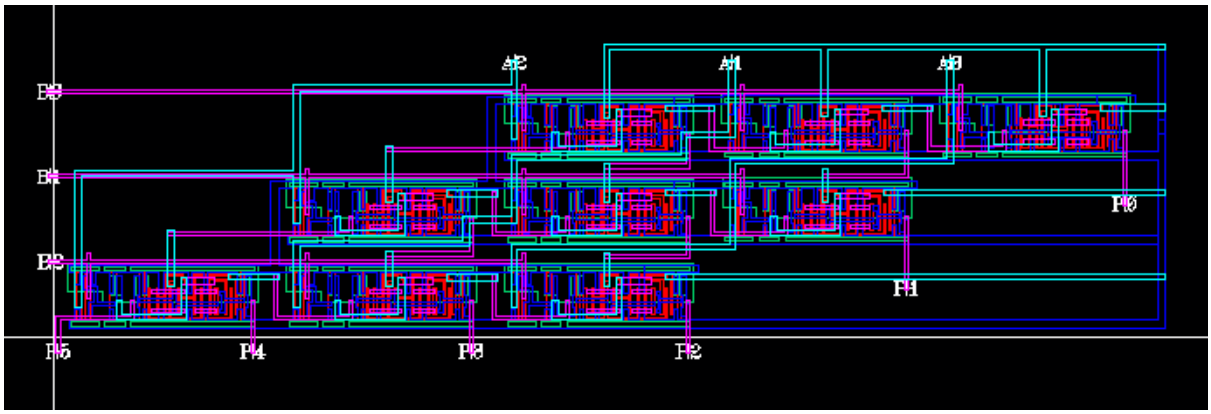
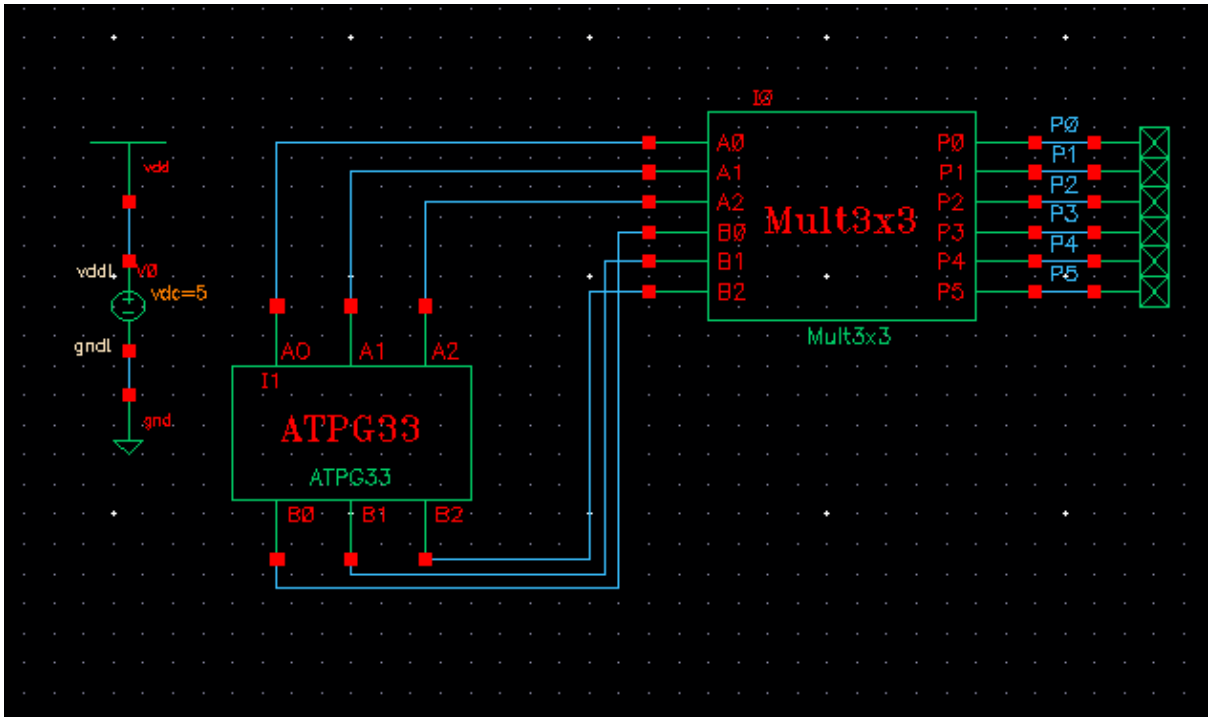




Mult3x3 extracted view (Top Level)



Mult3x3 extracted view (Lower Level)



TBmul33 schematic

Part C

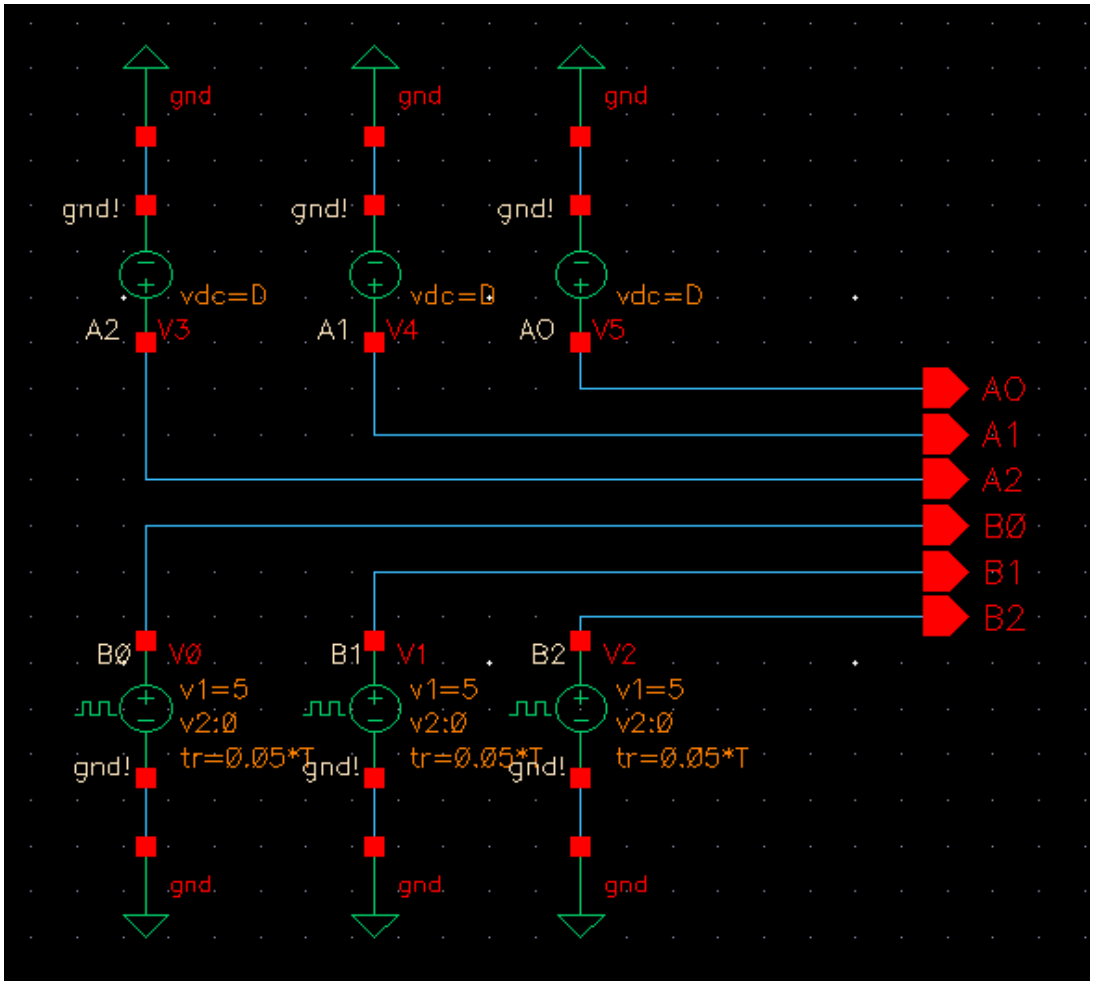
B2	B1	B0	A2	A1	A0	P5	P4	P3	P2	P1	P0
0	0	0	1	1	1	**0**	**0**	**0**	**0**	**0**	**0**
0	0	1	1	1	1	**0**	**0**	**0**	**1**	**1**	**1**
0	1	0	1	1	1	**0**	**0**	**1**	**1**	**1**	**0**
0	1	1	1	1	1	**0**	**1**	**0**	**1**	**0**	**1**
1	0	0	1	1	1	**0**	**1**	**1**	**1**	**0**	**0**
1	0	1	1	1	1	**0**	**1**	**1**	**1**	**1**	**1**
1	1	0	1	1	1	**1**	**0**	**1**	**0**	**1**	**0**
1	1	1	1	1	1	**1**	**1**	**0**	**0**	**0**	**1**

I chose the MSBs B2, B1 and B0 as 3 vpulse with the following values:

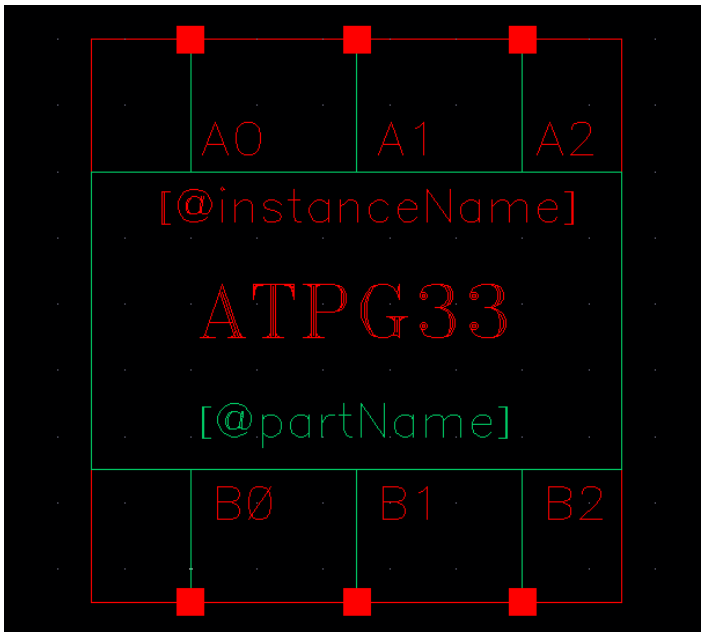
- B2: Period = 4T, Pulse width = 1.95T, Delay = 1ns, Rise time = Fall time = 0.05T
- B1: Period = 2T, Pulse width = 0.95T, Delay = 1ns, Rise time = Fall time = 0.05T
- B0: Period = T, Pulse width = 0.45T, Delay = 1ns, Rise time = Fall time = 0.05T

I added vdc to the LSBs A2, A1, A0 and gave the DC voltage as D (Don't care!). D can be set as 5V (for logic 1) and 0V (for logic 0) during simulation. For our results, since it's a multiplier D=5V will be much more beneficial to yield proper values because multiplying anything by 0 will only return 0.

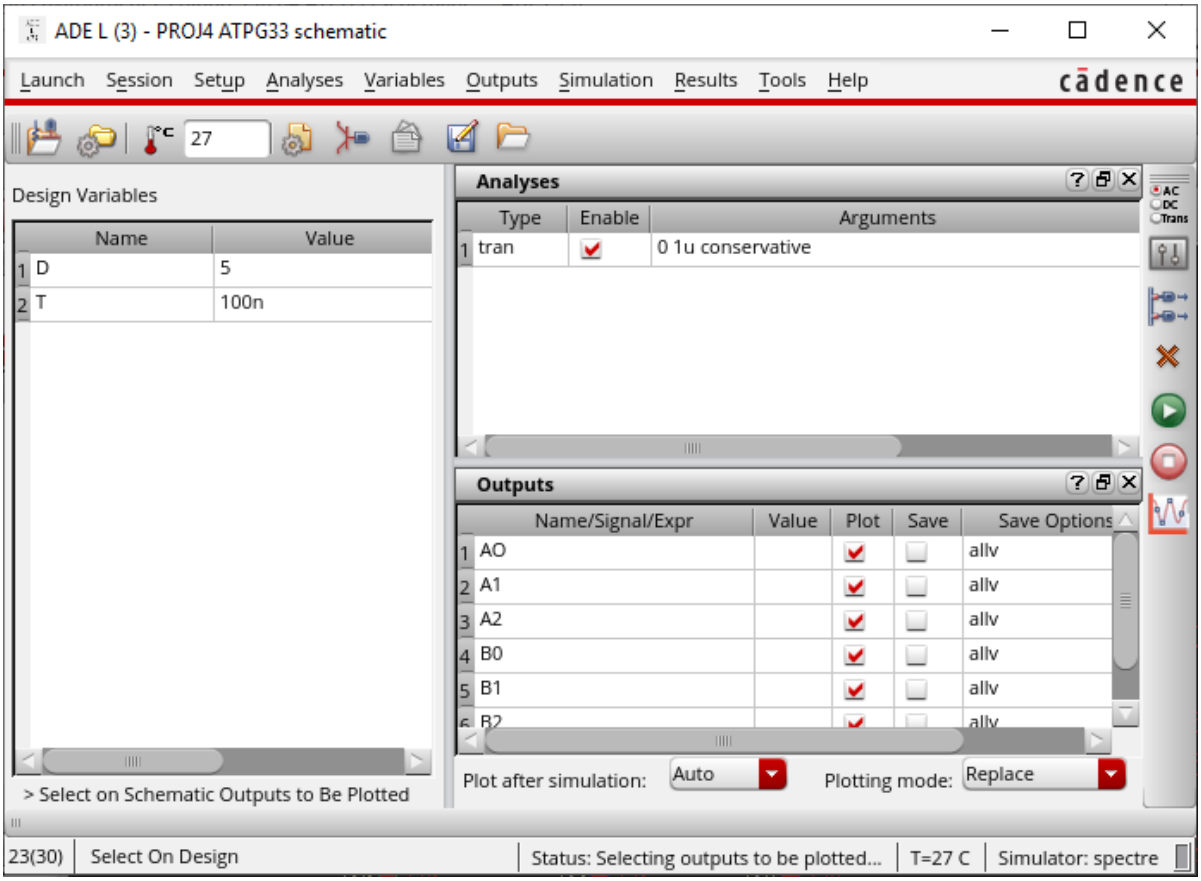
So, we obtain unique values for P5…P0 for these 8 input vectors from the ATPG33.



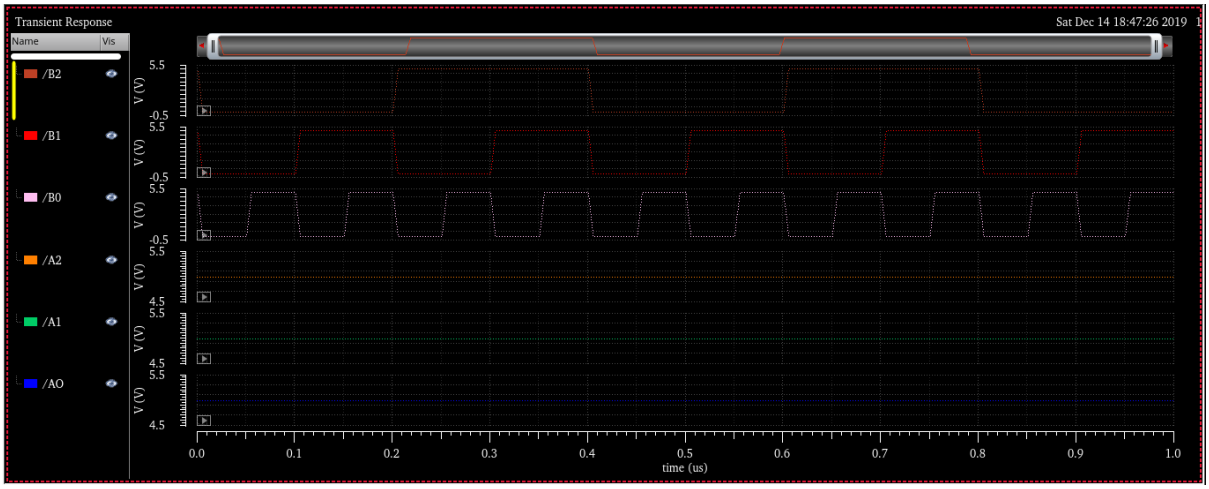
ATPG33 schematic



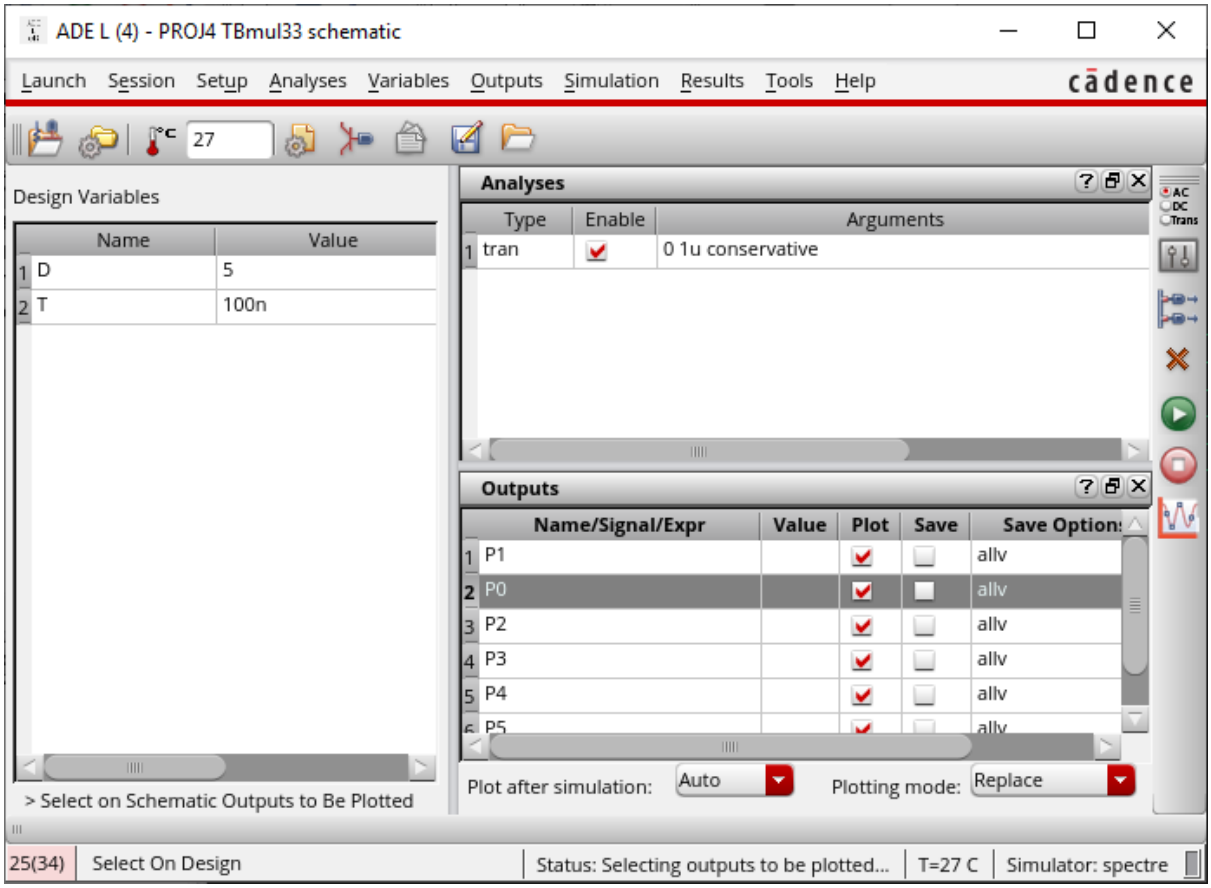
ATPG33 symbol



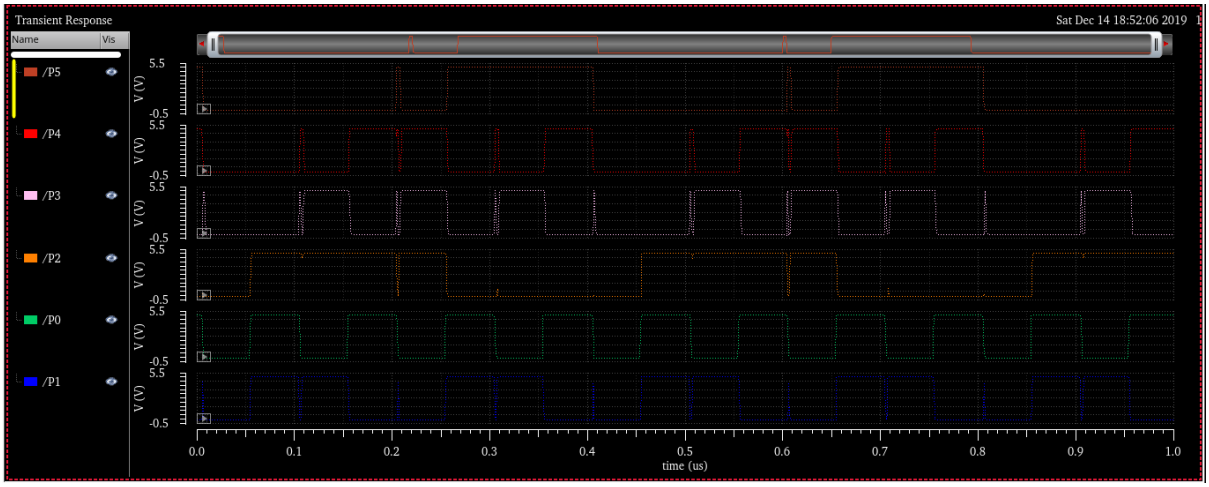
ATPG33 ADE L



ATPG33 output waveform



TBmul33 ADE L



TBmul33 output waveform

The values from the plot matches exactly with the calculated values in the table above. Hence, the circuit works fine.

Part D

B7	B6	B5	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0
0	**0**	**0**	**0**	D	D	D	D	D	D	D	D	D	D	D	D
0	**0**	**0**	**1**	D	D	D	D	D	D	D	D	D	D	D	D
0	**0**	**1**	**0**	D	D	D	D	D	D	D	D	D	D	D	D
0	**0**	**1**	**1**	D	D	D	D	D	D	D	D	D	D	D	D
0	**1**	**0**	**0**	D	D	D	D	D	D	D	D	D	D	D	D
0	**1**	**0**	**1**	D	D	D	D	D	D	D	D	D	D	D	D
0	**1**	**1**	**0**	D	D	D	D	D	D	D	D	D	D	D	D
0	**1**	**1**	**1**	D	D	D	D	D	D	D	D	D	D	D	D
1	**0**	**0**	**0**	D	D	D	D	D	D	D	D	D	D	D	D
1	**0**	**0**	**1**	D	D	D	D	D	D	D	D	D	D	D	D
1	**0**	**1**	**0**	D	D	D	D	D	D	D	D	D	D	D	D
1	**0**	**1**	**1**	D	D	D	D	D	D	D	D	D	D	D	D
1	**1**	**0**	**0**	D	D	D	D	D	D	D	D	D	D	D	D
1	**1**	**0**	**1**	D	D	D	D	D	D	D	D	D	D	D	D
1	**1**	**1**	**0**	D	D	D	D	D	D	D	D	D	D	D	D
1	**1**	**1**	**1**	D	D	D	D	D	D	D	D	D	D	D	D

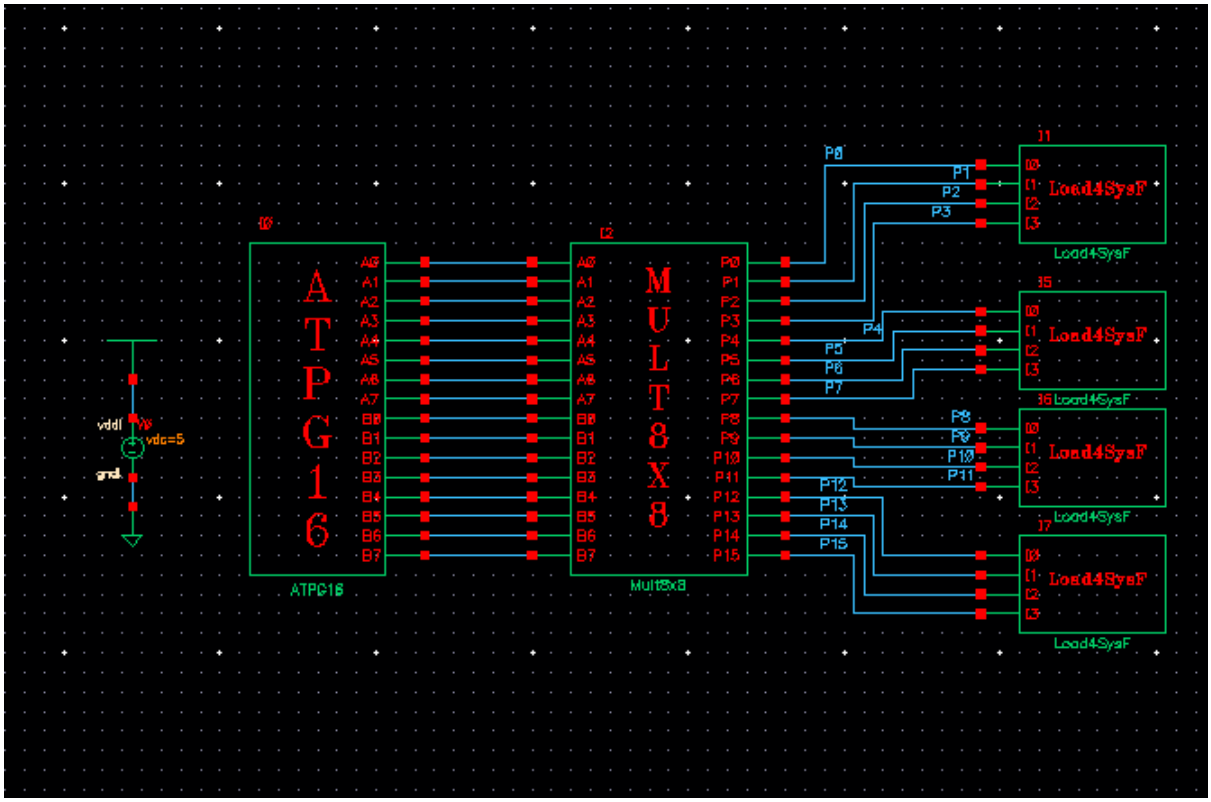
I chose the MSBs B7, B6, B5 and B4 as 4 vpulse with the following values:

- B7: Period = 8T, Pulse width = 3.95T, Delay = 1ns, Rise time = Fall time = 0.05T
- B6: Period = 4T, Pulse width = 1.95T, Delay = 1ns, Rise time = Fall time = 0.05T
- B5: Period = 2T, Pulse width = 0.95T, Delay = 1ns, Rise time = Fall time = 0.05T
- B4: Period = T, Pulse width = 0.45T, Delay = 1ns, Rise time = Fall time = 0.05T

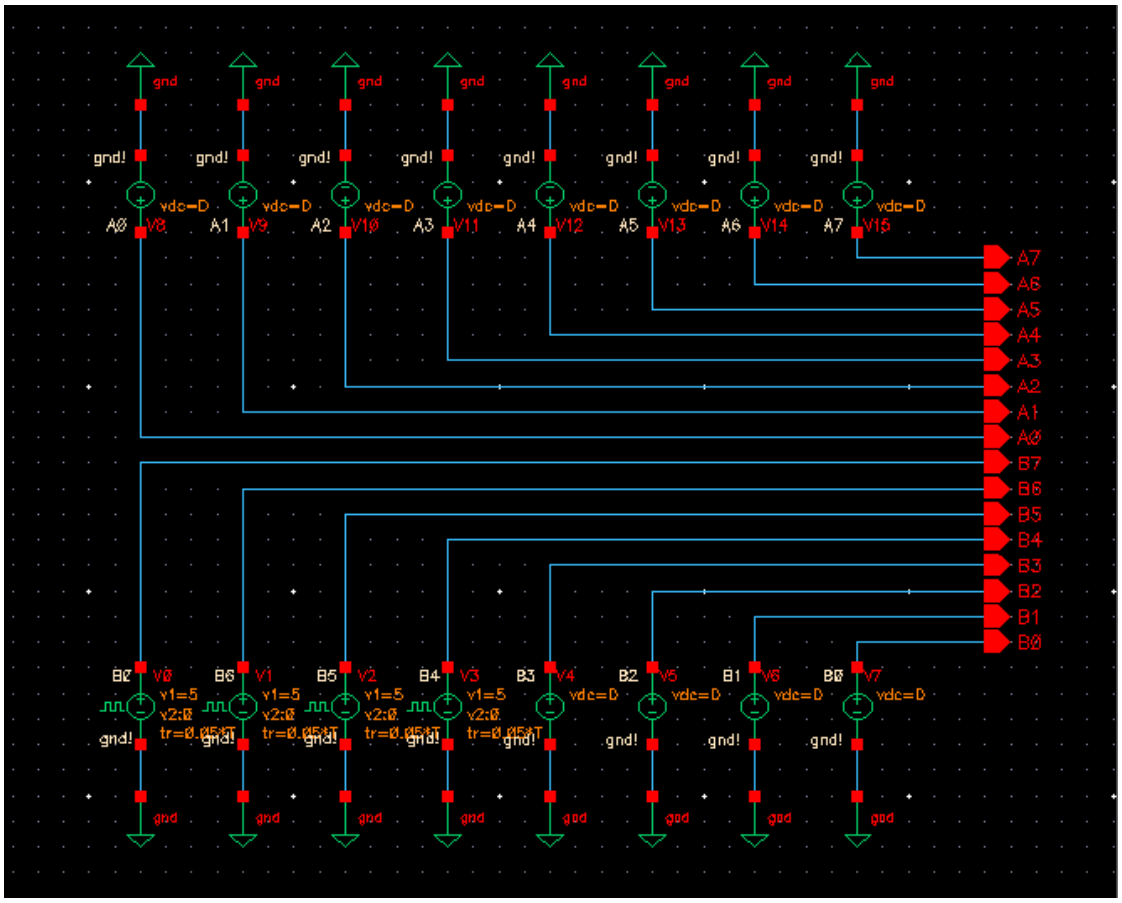
I added vdc to the other bits B3…B0, A7…A0 and gave the DC voltage as D (Don't care!). D can be set as 5V (for logic 1) and 0V (for logic 0) during simulation. For our results, since it's a multiplier **D=5V (logic 1)** will be much more beneficial to yield proper values because multiplying anything by 0 will only return 0.

These 16 values will basically cover about 90% of the 65536 test cases as we can replace any 4-bits with any other 4-bits (say B7…B4 with A7…A4 and obtain similar results). So basically, what we do here is create 2^4 = 16 combinations from 4 input bits, which in turn can be fed to any 4 of the 16 bits and give about the same results as testing all 2^{16} = 65536 combinations.

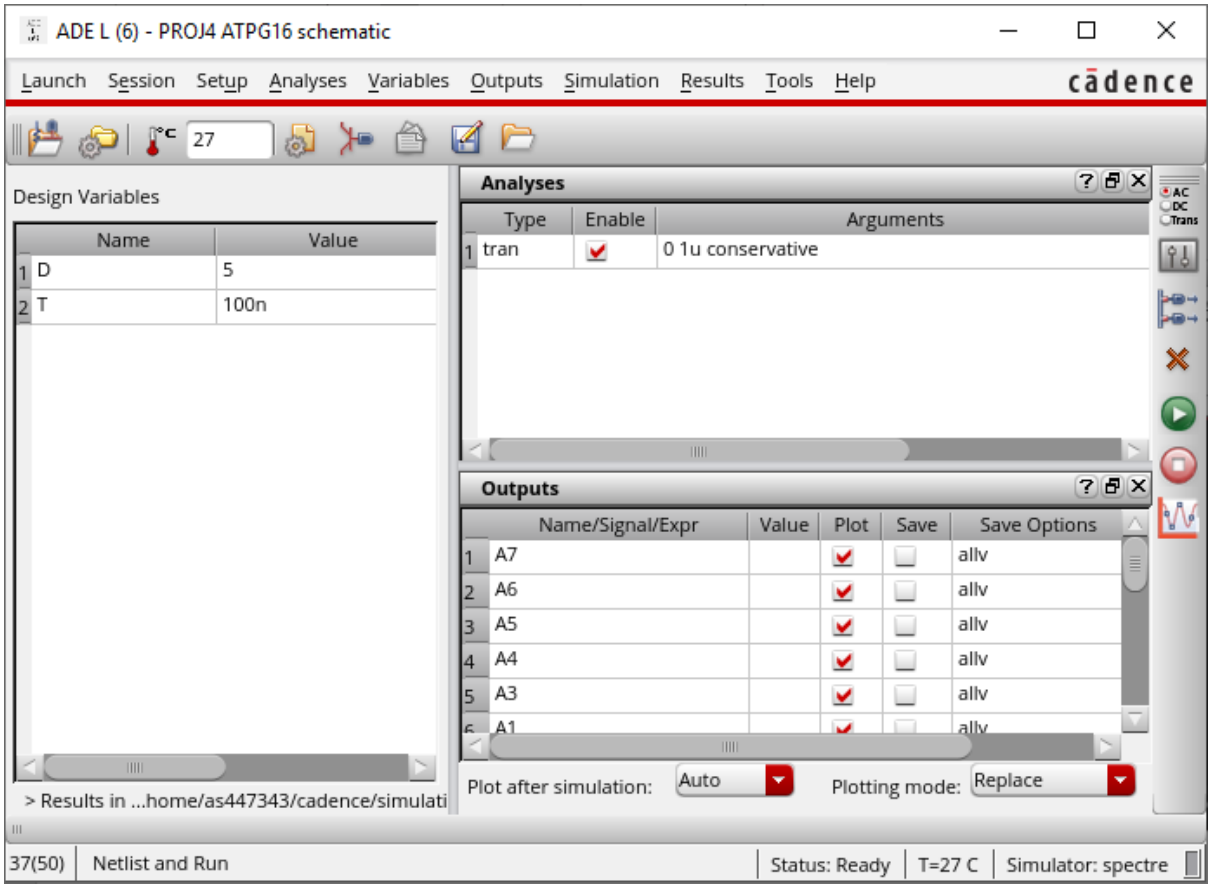
So, we obtain unique values for P15…P0 for these 16 input vectors from the ATPG16.



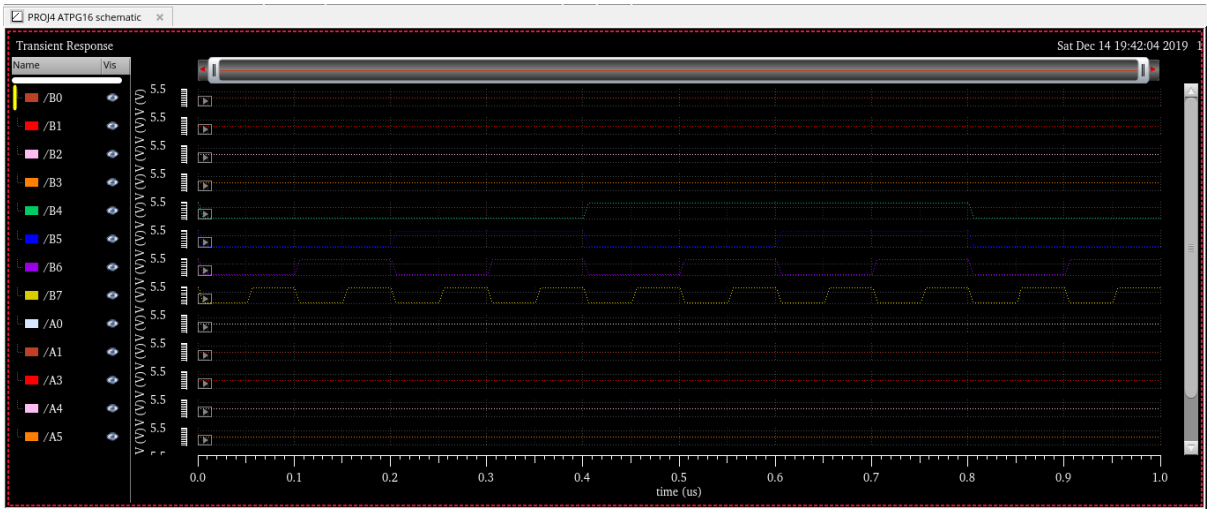
TBmul88 schematic



ATPG16 schematic



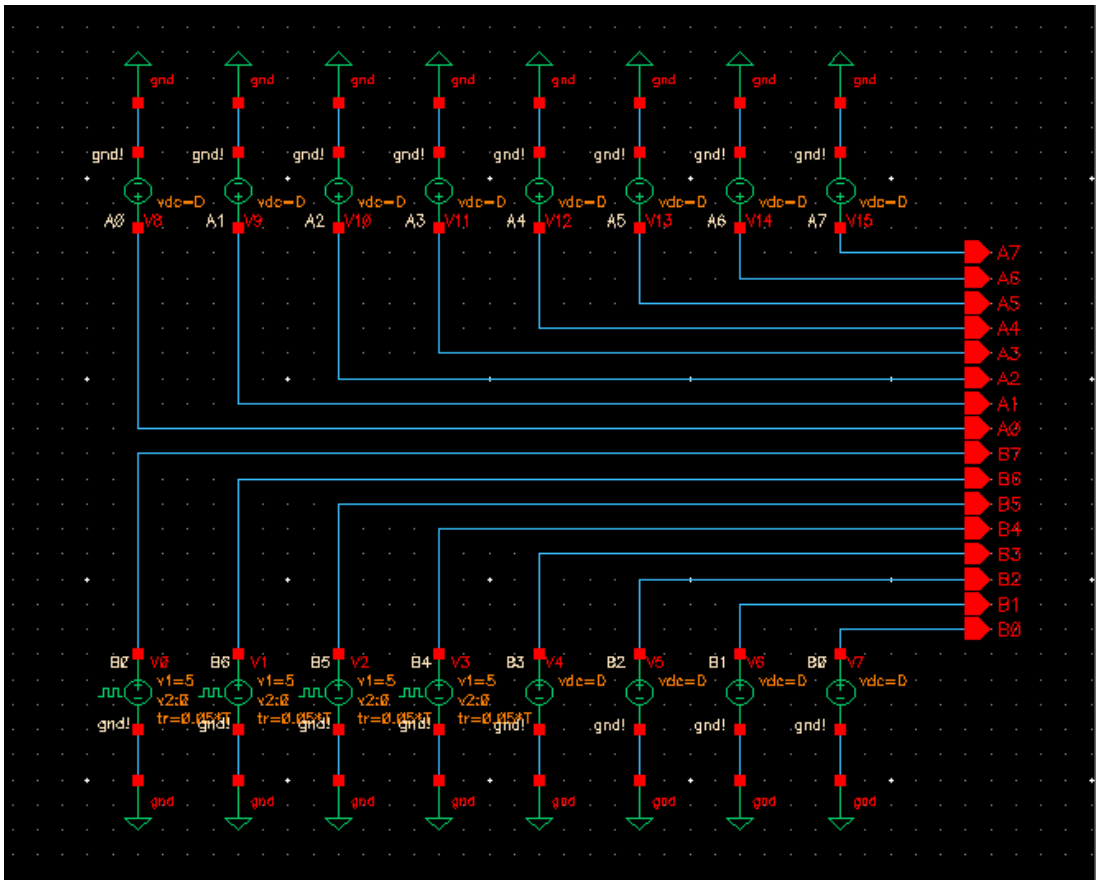
ATPG16 schematic ADE L



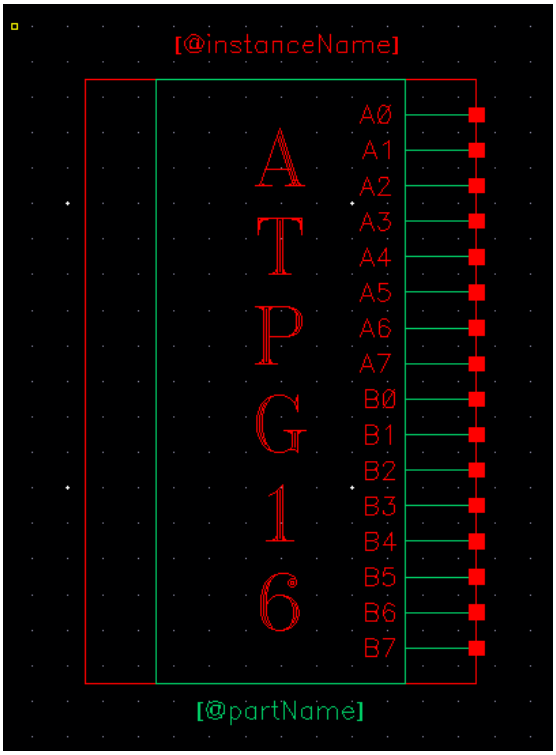
ATPG16 output waveform

The values from the plot matches exactly with the calculated values from the table hence it confirms the circuit will work fine.

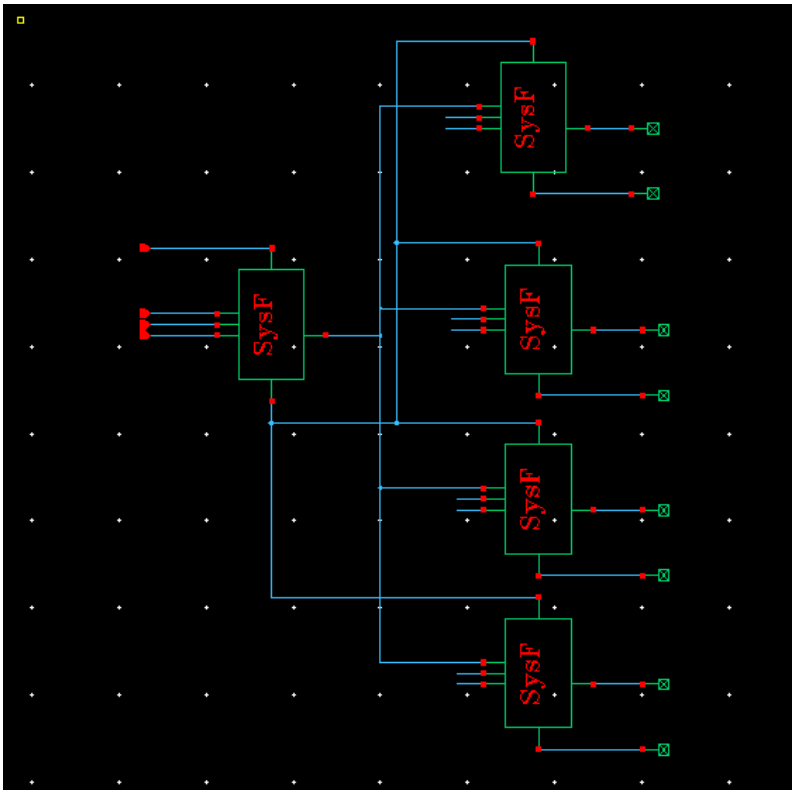
Part E



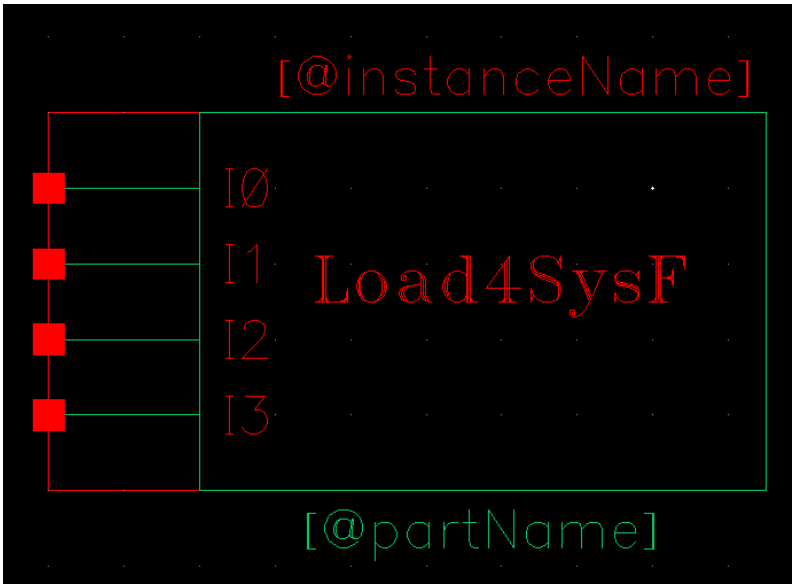
ATPG16 schematic



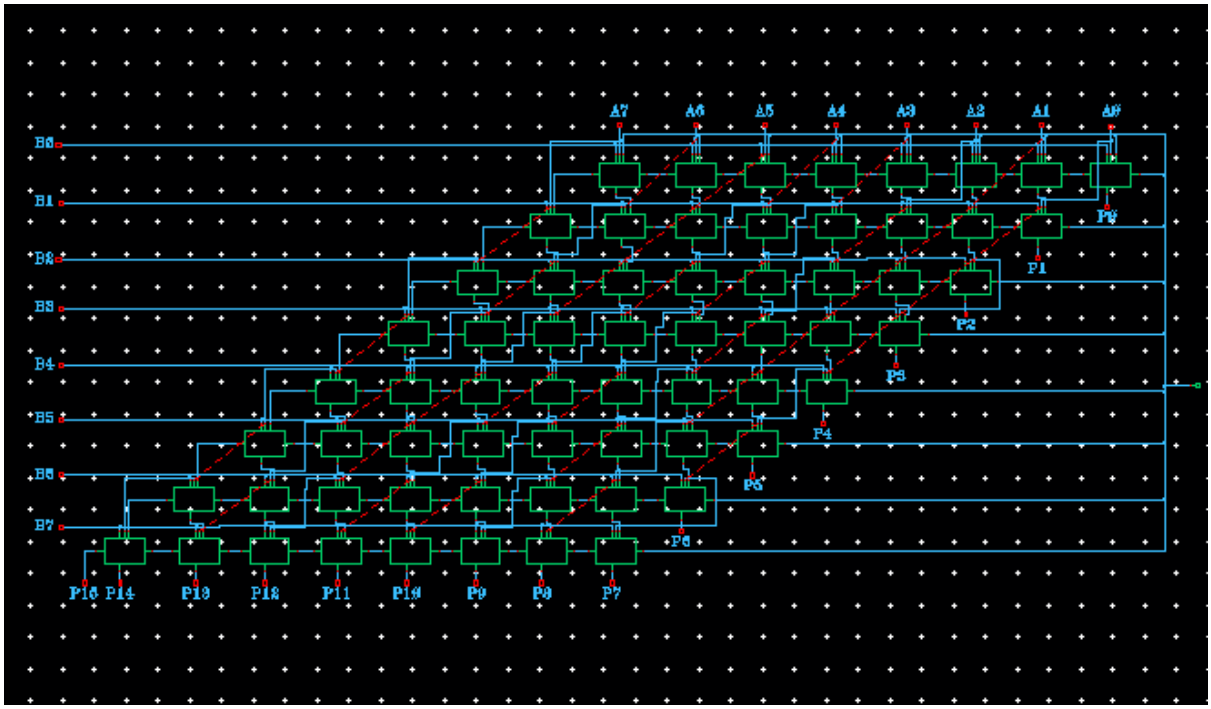
ATPG16 symbol



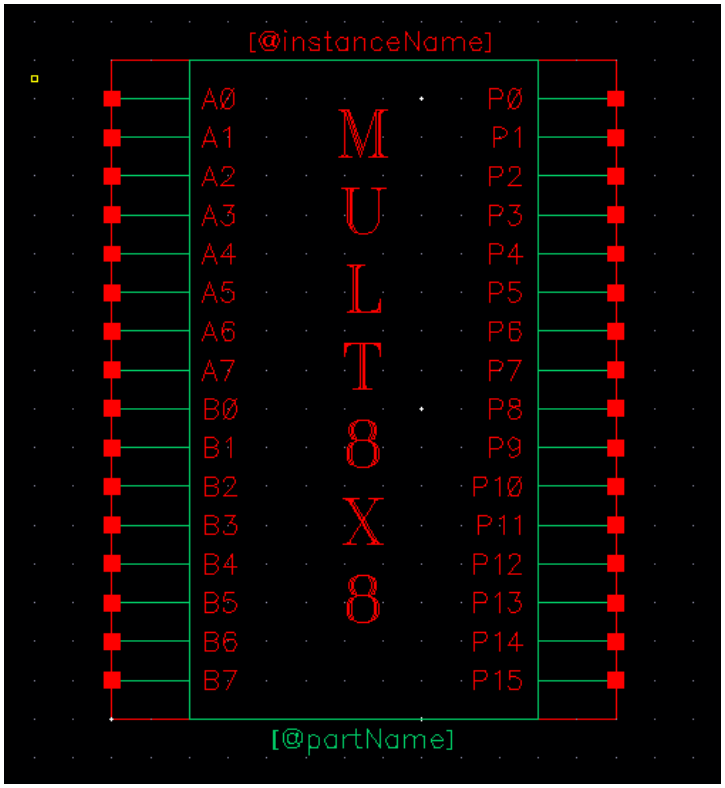
Load4SysF schematic



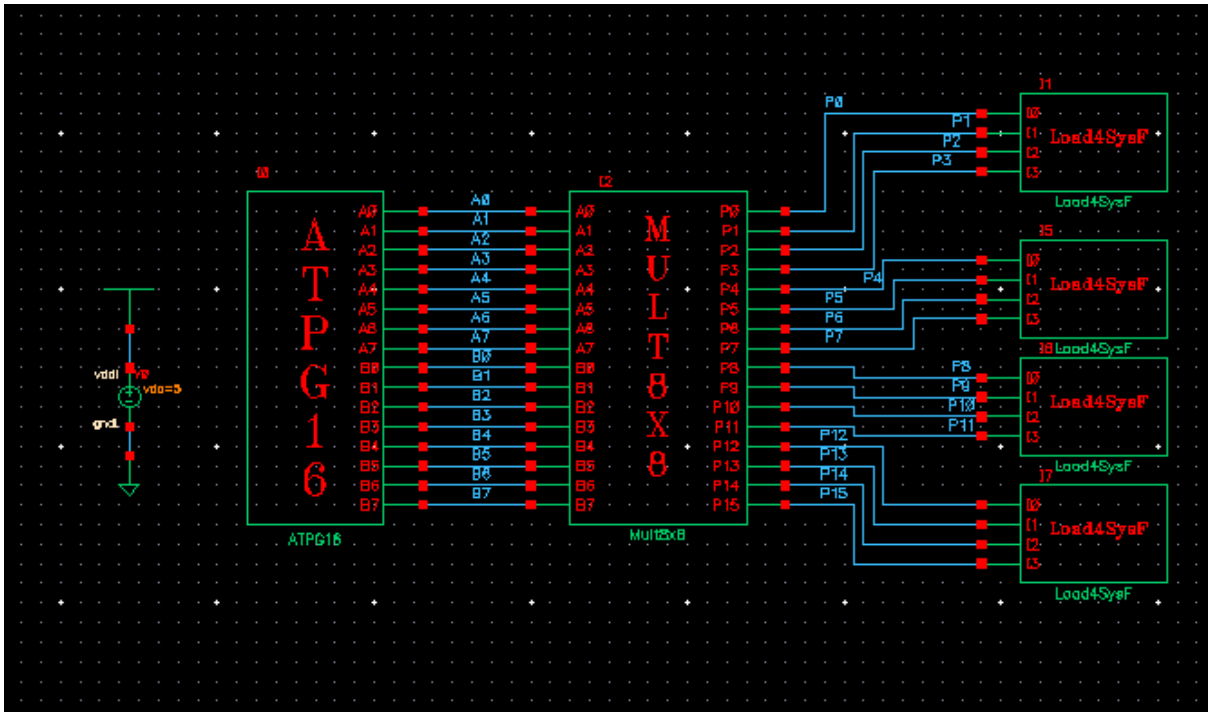
Load4SysF symbol



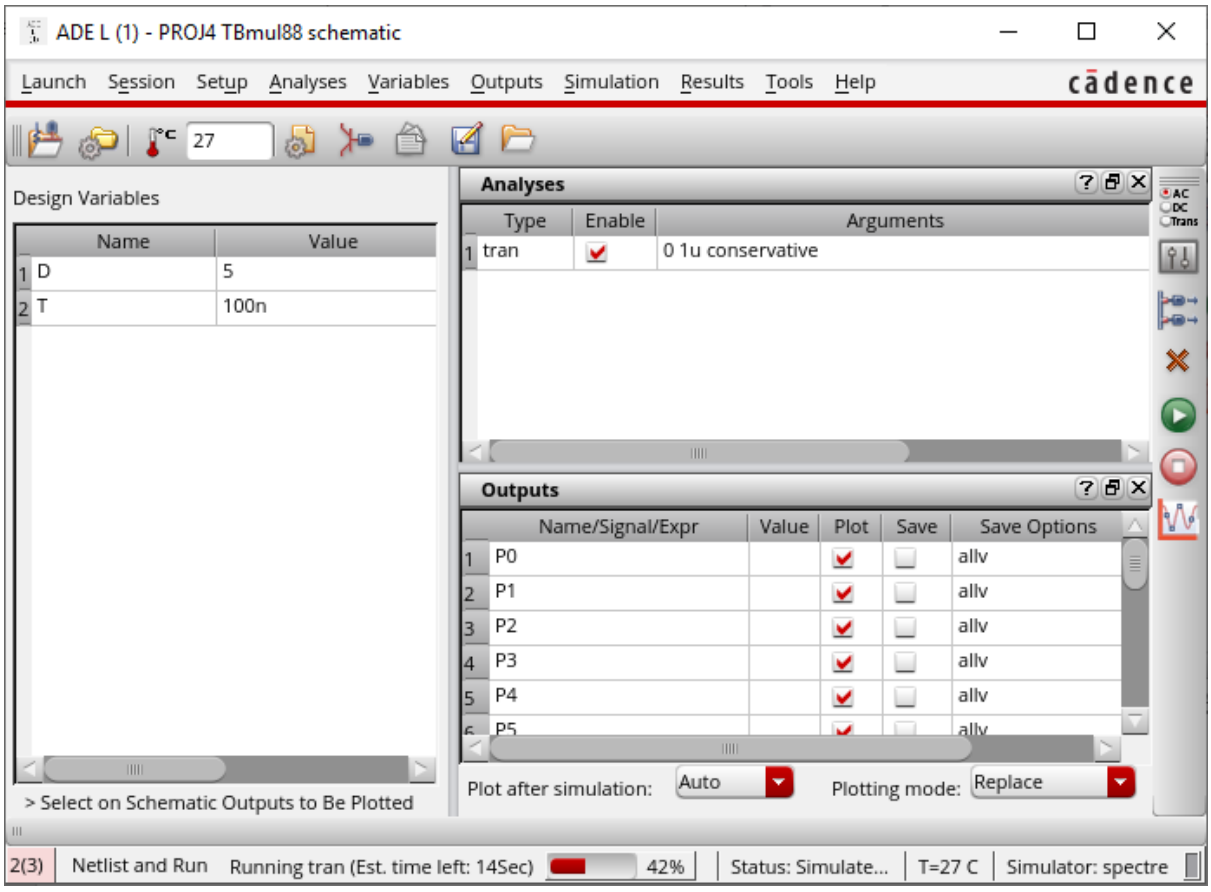
Mult8x8 schematic



Mult8x8 symbol



TBmul88 schematic

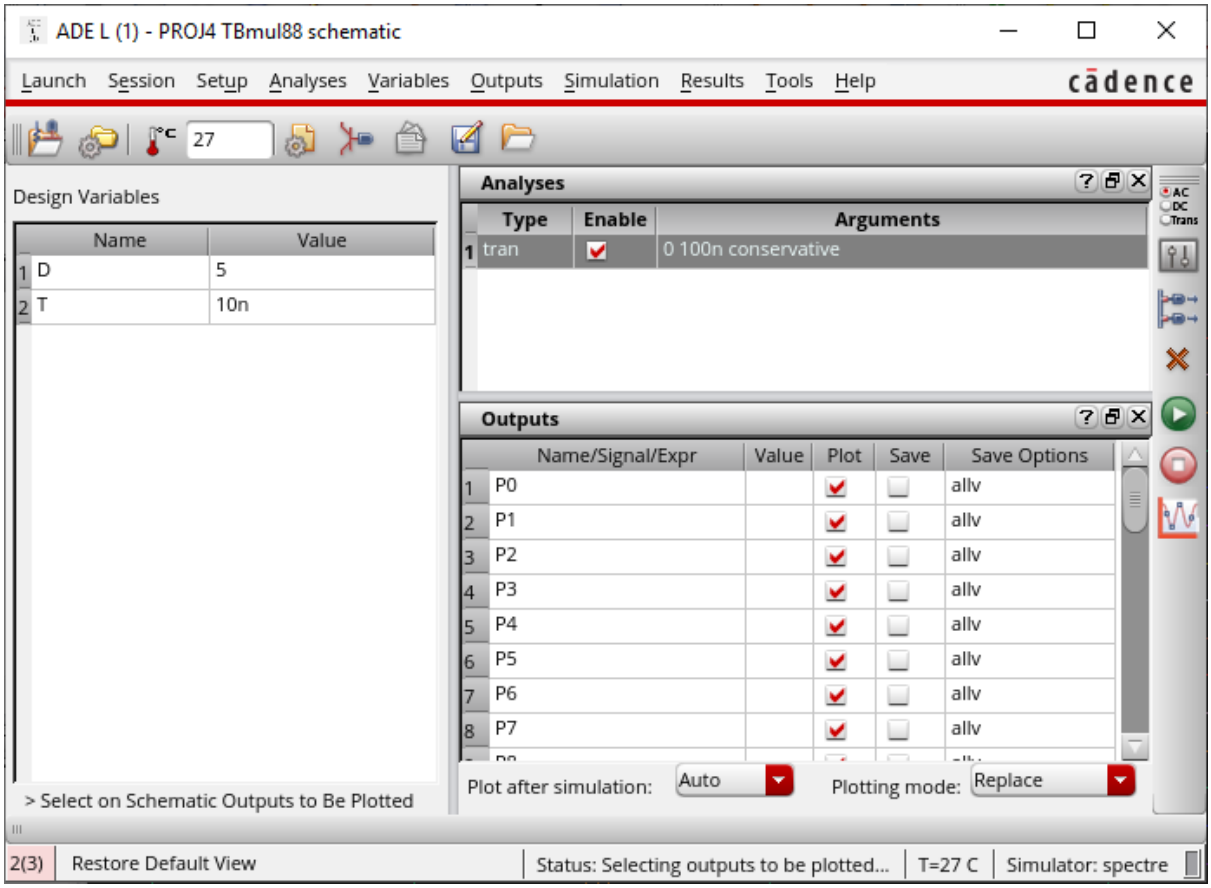


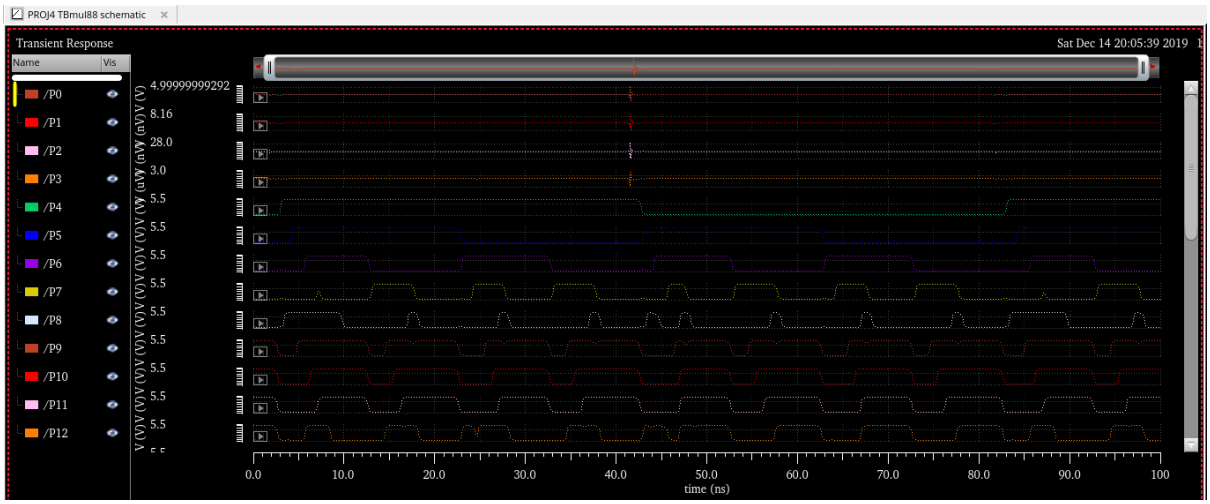
TBmul88 schematic ADE L

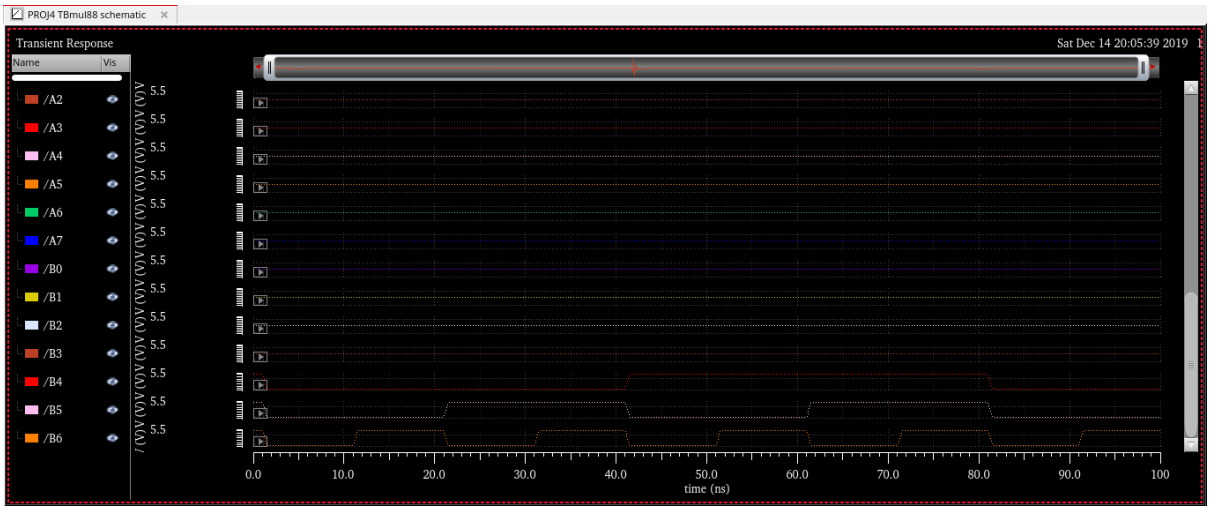
TBmul88 output waveform (schematic only, 10MHz)

The values from the plot matches exactly with the calculated values hence it confirms the circuit works fine.

Now we push it hard and decrease T to 10ns from 100ns. (i.e. we increase the frequency becomes 100MHz from 10MHz!)


ADE L (1) - PROJ4 TBmul88 schematic
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help
cadence
27
Design Variables
Name Value
1 D 5
2 T 10n
Analyses
Type Enable Arguments
1 tran 0 100n conservative
Outputs
Name/Signal/Expr Value Plot Save Save Options
1 P0 allv
2 P1 allv
3 P2 allv
4 P3 allv
5 P4 allv
6 P5 allv
7 P6 allv
8 P7 allv
Plot after simulation: Auto
Plotting mode: Replace
> Select on Schematic Outputs to Be Plotted
2(3) Restore Default View
Status: Selecting outputs to be plotted...
T=27 C
Simulator: spectre

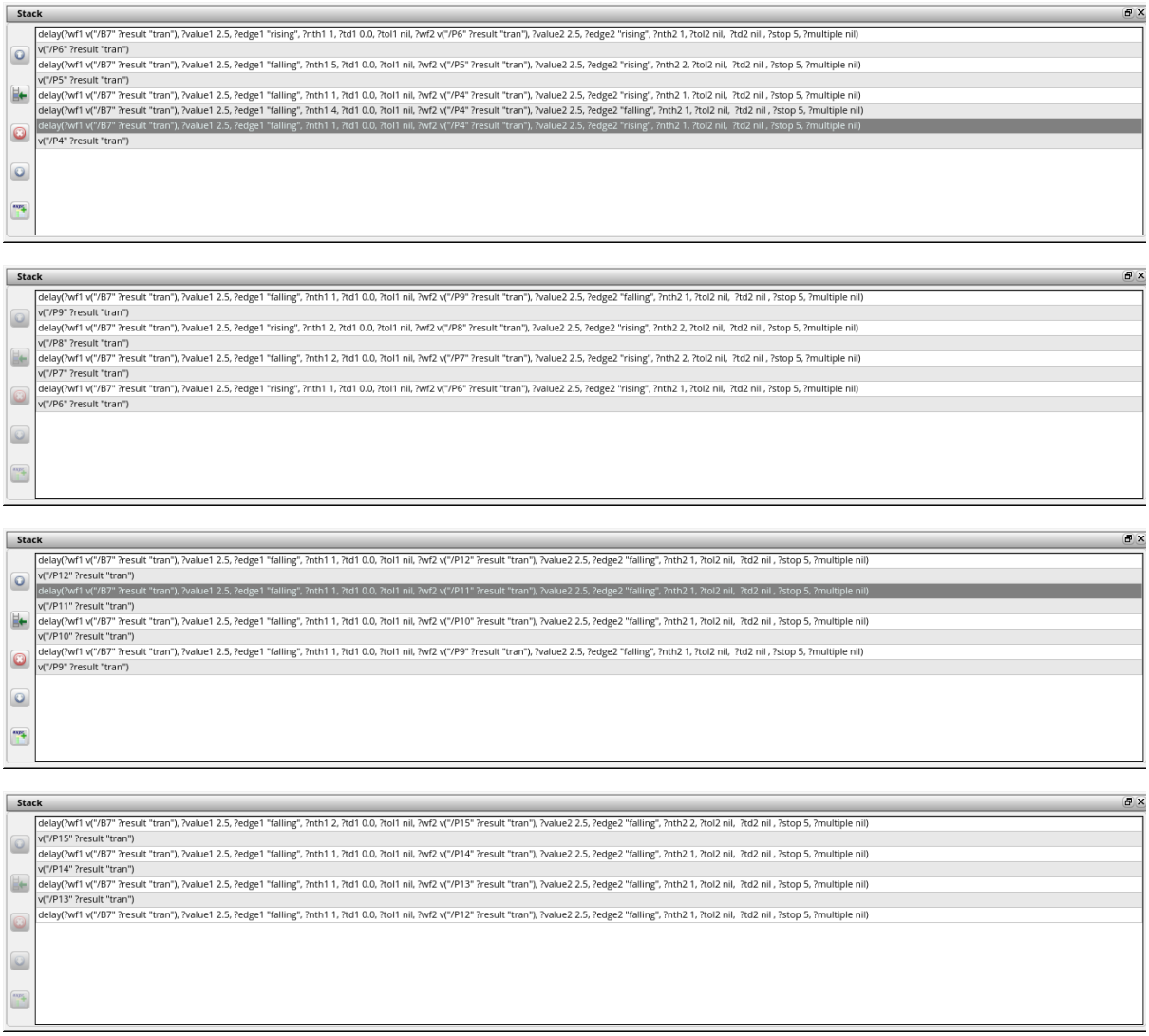

PROJ4 TBmul88 schematic
Transient Response
Sat Dec 14 20:05:39 2019
/P0
/P1
/P2
/P3
/P4
/P5
/P6
/P7
/P8
/P9
/P10
/P11
/P12
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100
time (ns)



TBmul88 output waveform (schematic only, 100MHz)

Propagation delays (schematic only):

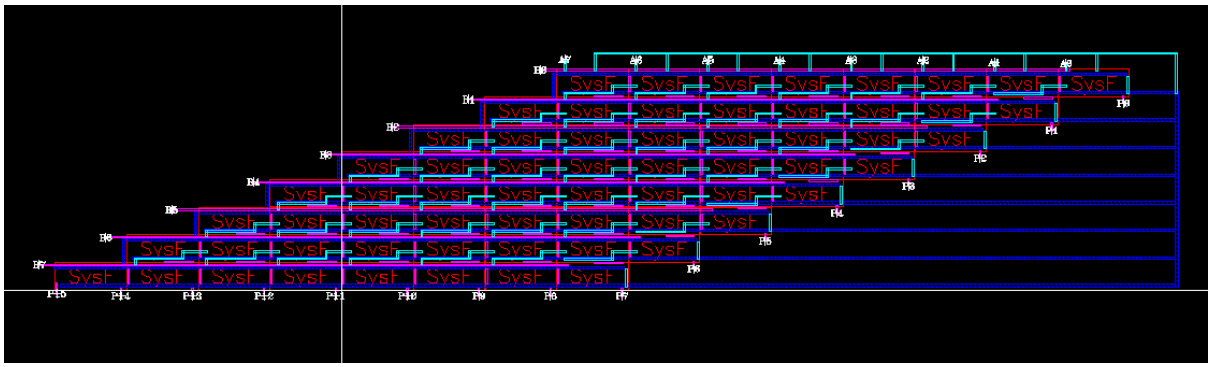
F04 Delay	Expression/Remarks	Value
t_{pd} (P0)	P0 is constant	N/A
t_{pd} (P1)	P1 is constant	N/A
t_{pd} (P2)	P2 is constant	N/A
t_{pd} (P3)	P3 is constant	N/A
t_{pd} (P4)	1.79E-9	1.79ns
t_{pd} (P5)	1.795E-9	**1.795ns**
t_{pd} (P6)	568.9E-12	568.9ps
t_{pd} (P7)	1.781E-9	1.781ns
t_{pd} (P8)	793.8E-12	793.8ps
t_{pd} (P9)	1.419E-9	1.419ns
t_{pd} (P10)	1.423E-9	1.423ns
t_{pd} (P11)	1.42E-9	1.42ns
t_{pd} (P12)	1.42E-9	1.42ns
t_{pd} (P13)	1.435E-9	1.435ns
t_{pd} (P14)	1.413E-9	1.413ns
t_{pd} (P15)	1.336E-9	1.336ns



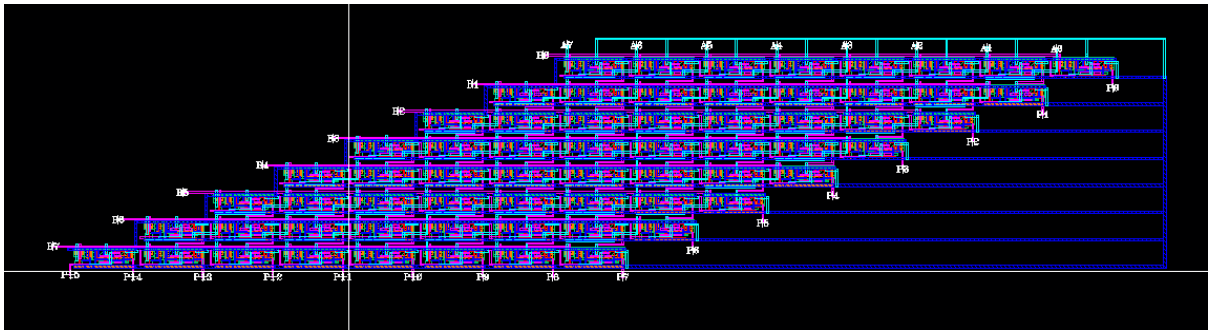
Therefore, the worst-case input-output 50%-50% propagation delay for schematic-only simulation came to be **1.795ns**.

Since we kept the value of D as 1 (5V), hence the lowermost bits remain constant which depends only on the values of A0, B0…A3, B3 and hence the summed values are either constant at 1 or at 0, as evident from the waveform.

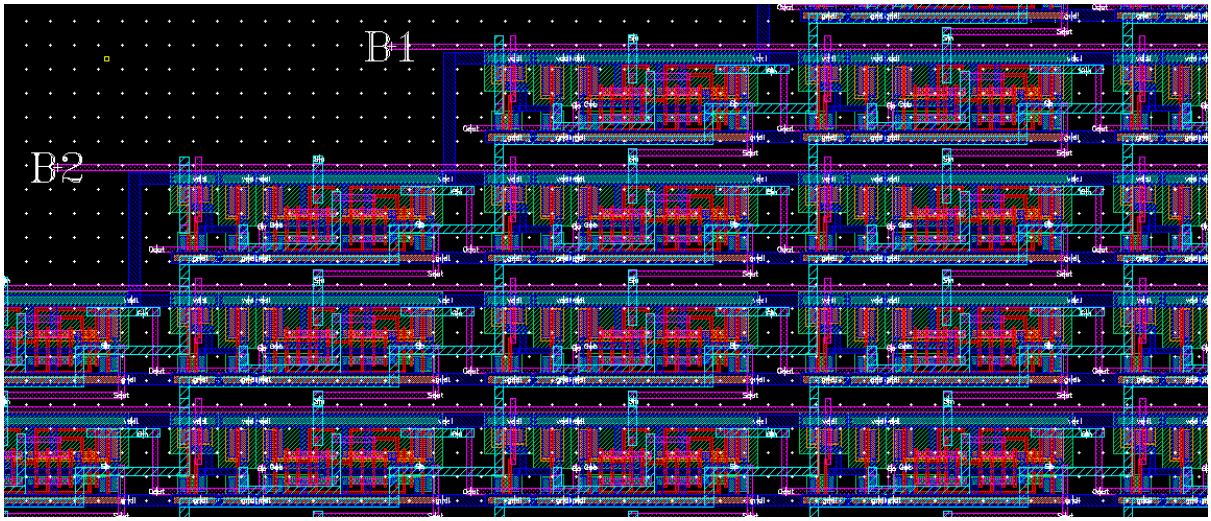
Part F



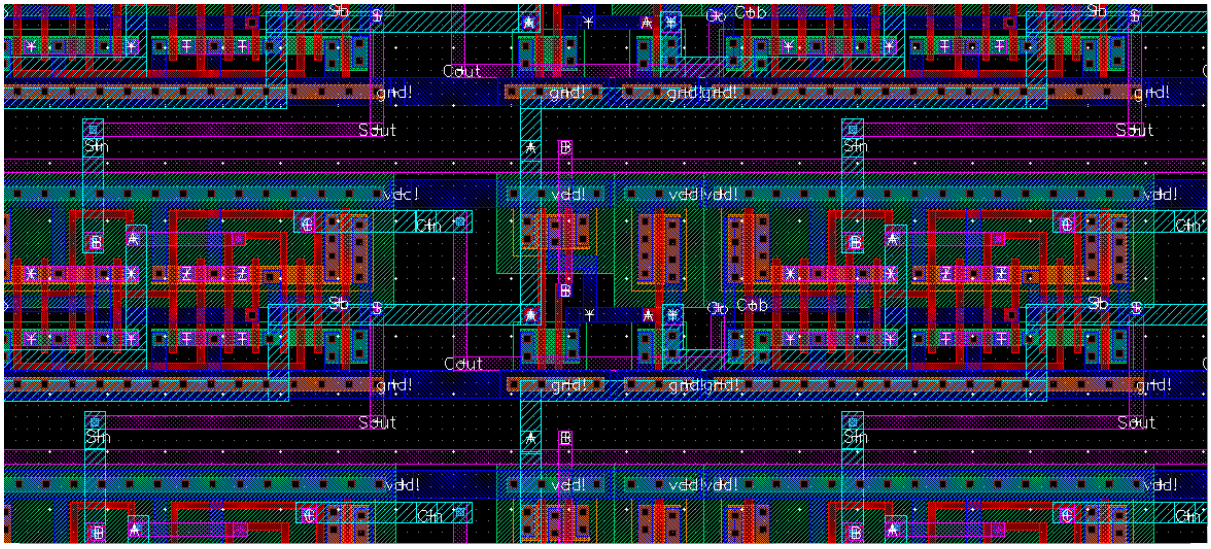
Mult8x8 layout (Top Level)



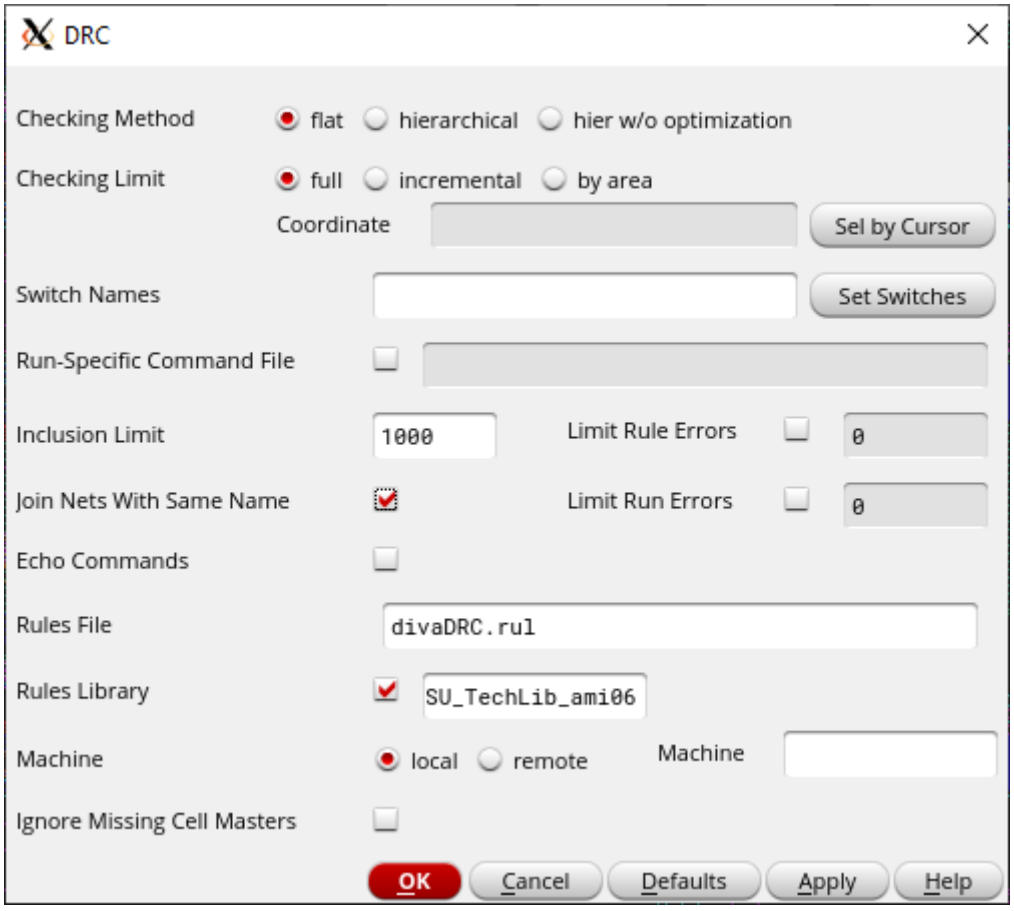
Mult8x8 layout (Lower Level)



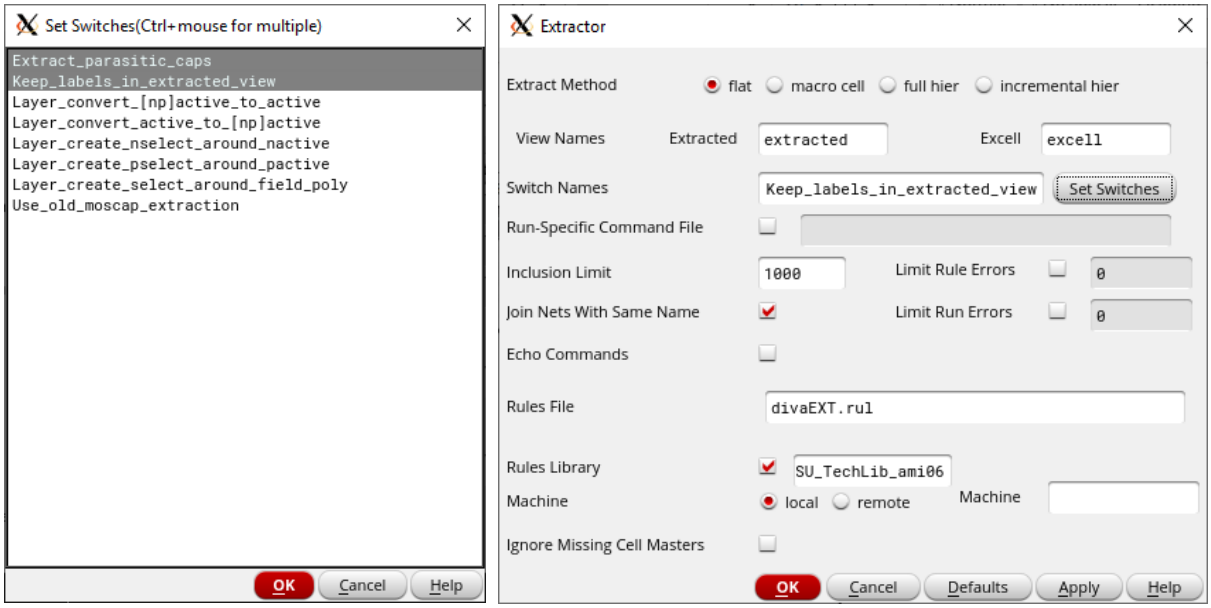
Mult8x8 layout (zoomed in)

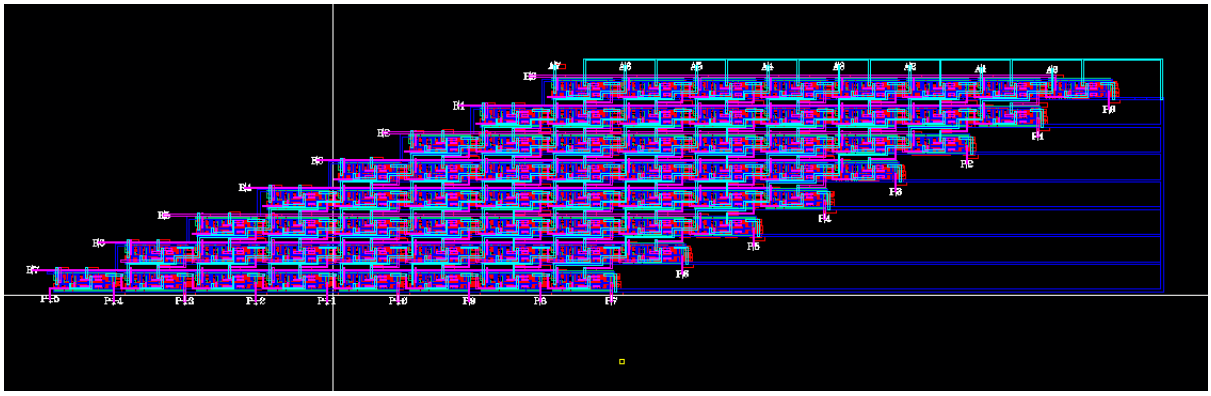


Mult8x8 layout (further zoomed in)

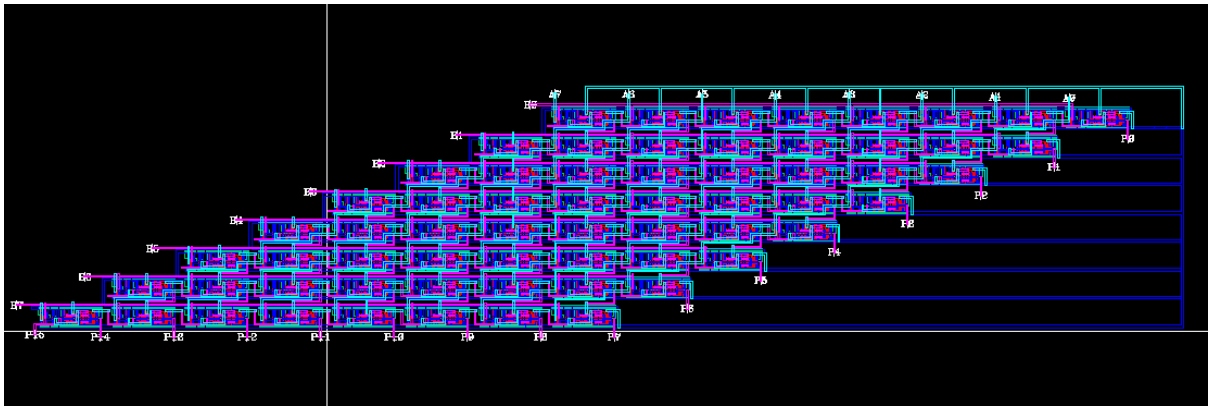



```
DRC started.......Sat Dec 14 21:10:05 2019
    completed ....Sat Dec 14 21:10:06 2019
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
*********   Summary of rule violations for cell "Mult8x8 layout"   *********
   Total errors found: 0
```

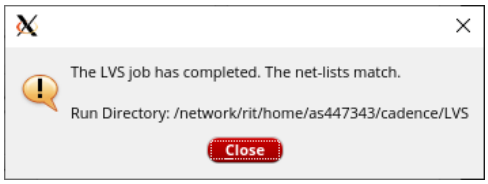




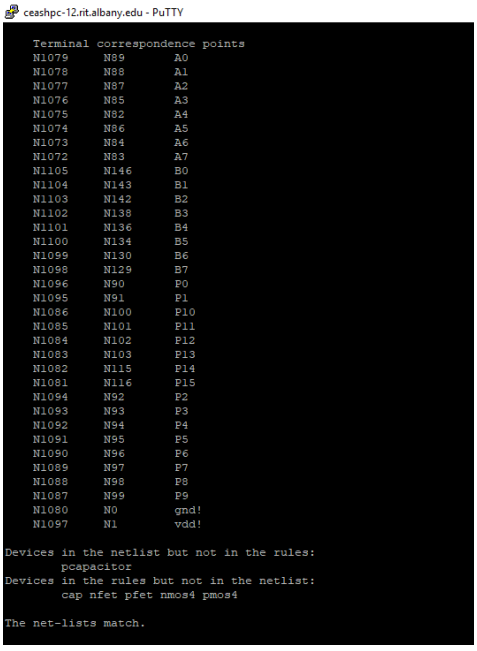
Mult8x8 extracted view (Top Level)

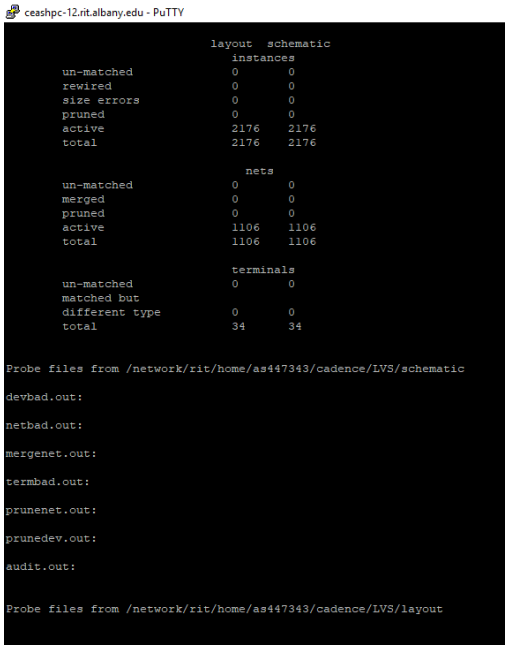


Mult8x8 extracted view (Lower Level)

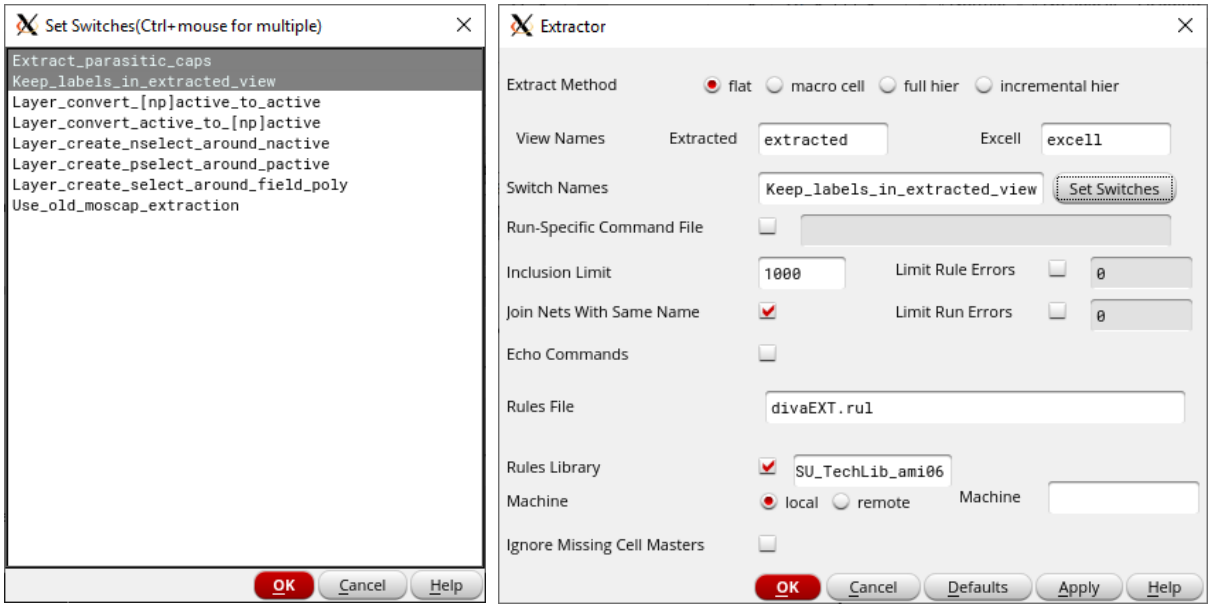


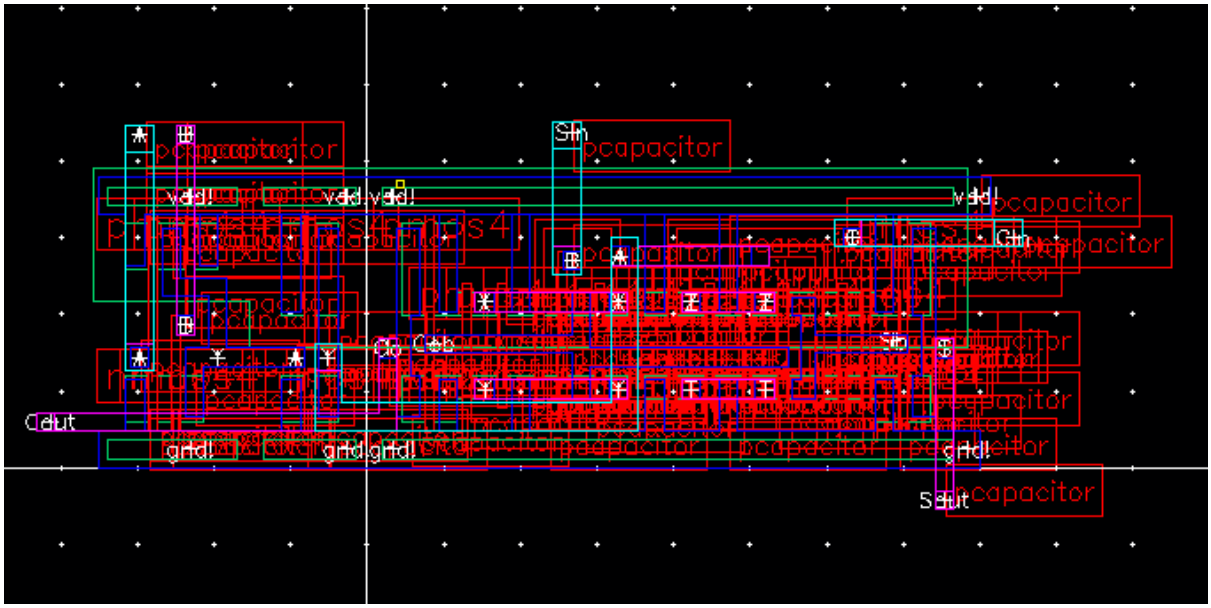
The net-lists match for Mult8x8!



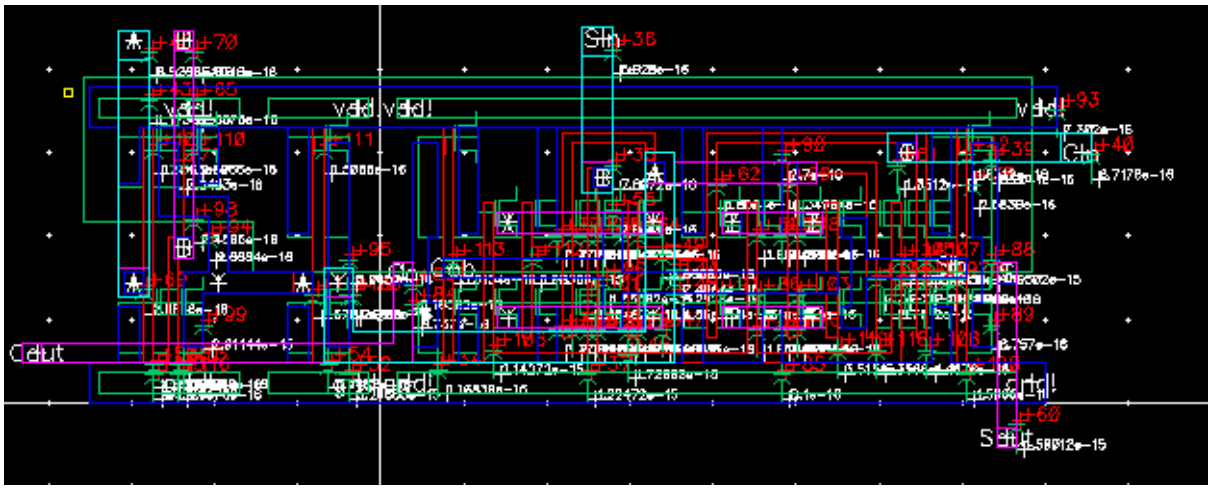


We do ***cat si.out*** to check the LVS file from the terminal.





SysF extracted view (Top Level)

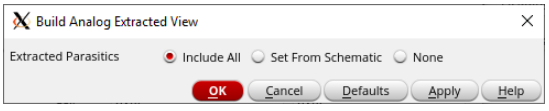


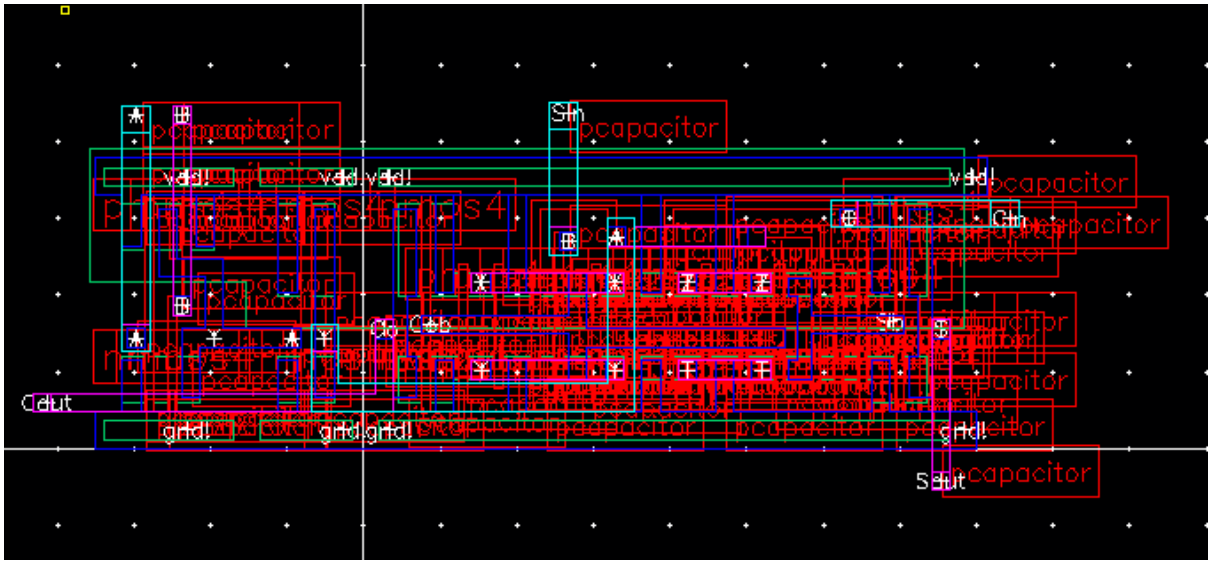
SysF extracted view (Lower Level)


Artist LVS
Commands Help
cadence
Run Directory
LVS
Browse
Create Netlist
schematic
extracted
Library
PROJ4
PROJ4
Cell
SysF
SysF
View
schematic
extracted
Browse
Sel by Cursor
Browse
Sel by Cursor
Rules File
divaLVS.rul
Browse
Rules Library
NCSU_TechLib_ami06
LVS Options
Rewiring
Device Fixing
Create Cross Reference
Terminals
Correspondence File
lvs_corr_file
Create
Switch Names
Priority
0
Run
background
Run
Output
Error Display
Monitor
Info
Backannotate
Parasitic Probe
Build Analog
Build Mixed
22


The LVS job has completed. The net-lists match.
Run Directory: /network/rit/home/as447343/cadence/LVS
Close

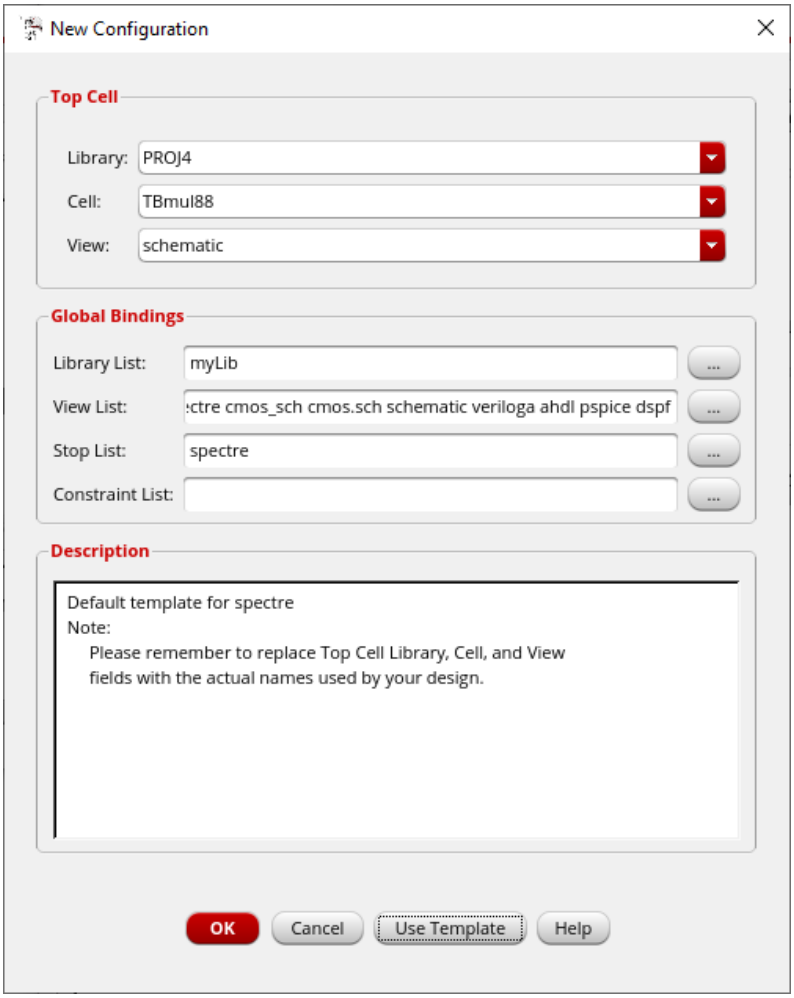

Artist LVS
Commands Help
cadence
Run Directory
LVS
Browse
Create Netlist
schematic
extracted
Library
PROJ4
PROJ4
Cell
SysF
SysF
View
schematic
analog_extracted
Browse
Sel by Cursor
Browse
Sel by Cursor
Rules File
divaLVS.rul
Browse
Rules Library
NCSU_TechLib_ami06
LVS Options
Rewiring
Device Fixing
Create Cross Reference
Terminals
Correspondence File
lvs_corr_file
Create
Switch Names
Priority
0
Run
background
Run
Output
Error Display
Monitor
Info
Backannotate
Parasitic Probe
Build Analog
Build Mixed
22

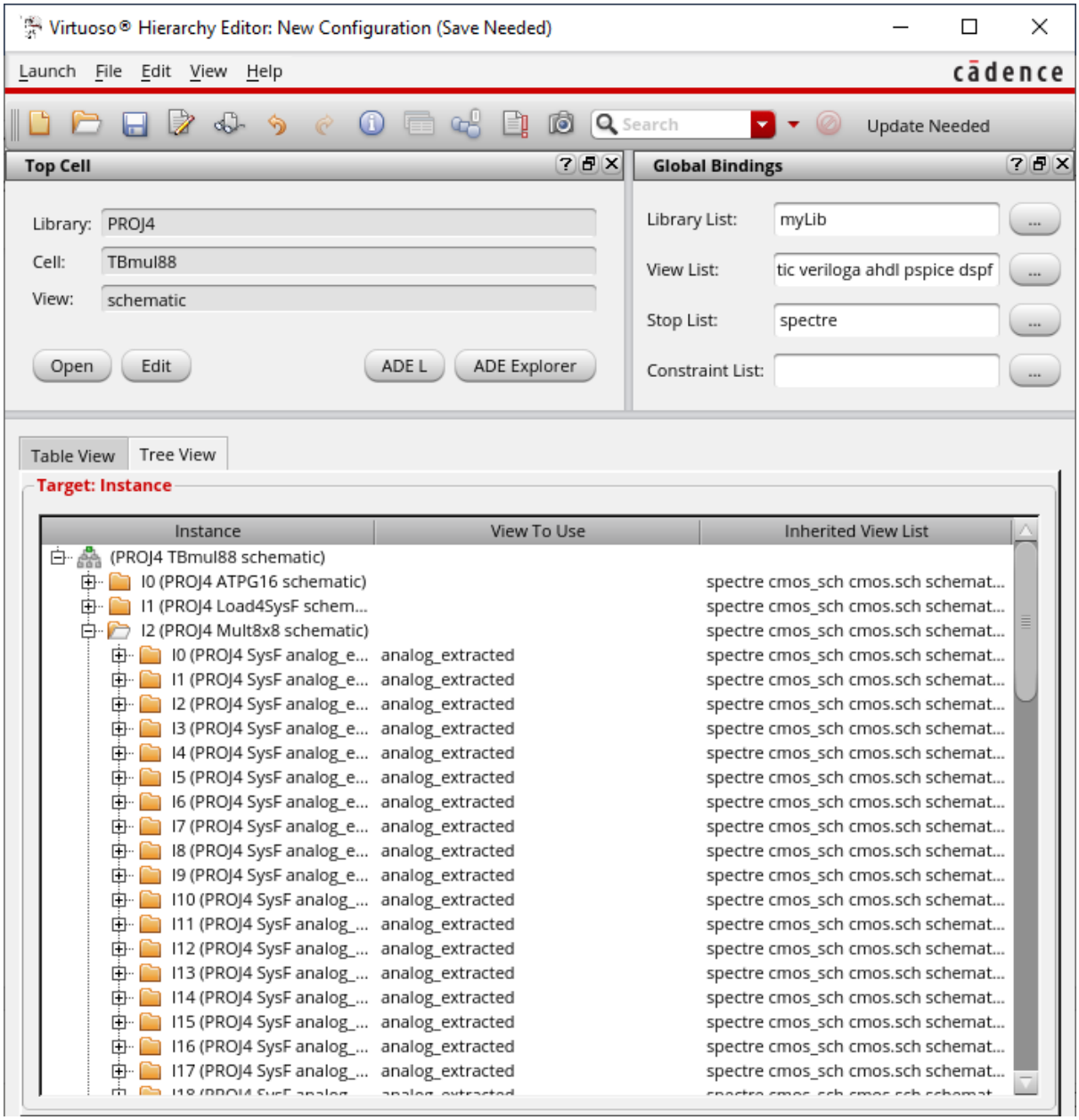

Build Analog Extracted View
Extracted Parasitics
Include All
Set From Schematic
None
OK
Cancel
Defaults
Apply
Help



SysF analog extracted view

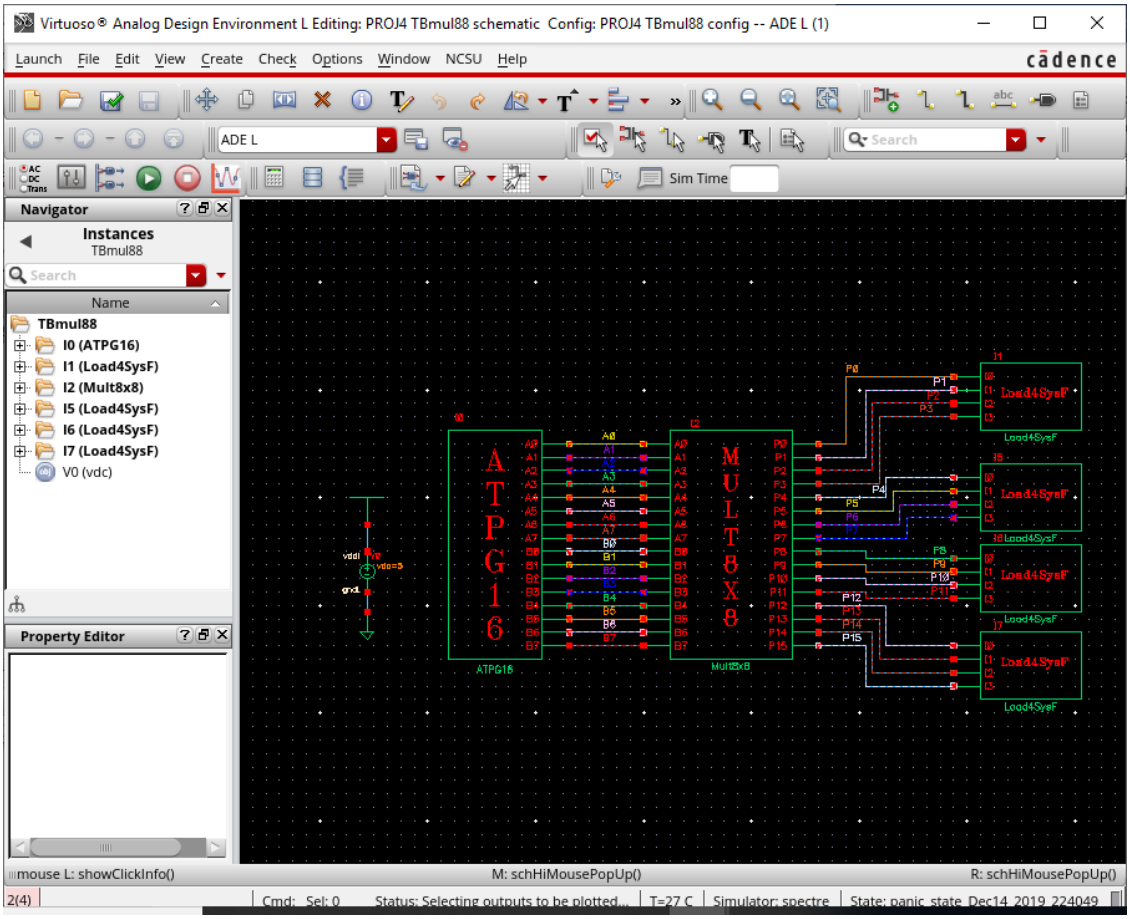
So now, we will simulate the TBmul88 using config view under the same parameters (i.e. T = 10ns and D = 5V) and check the delay.

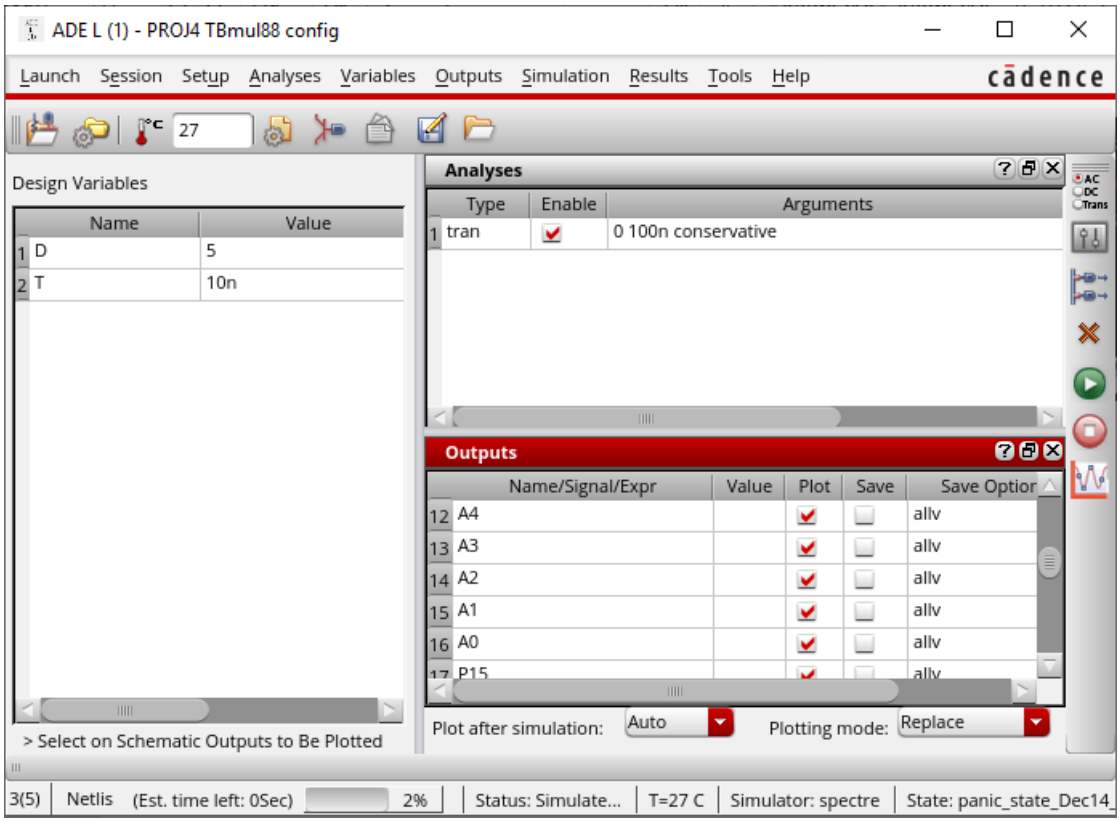




TBmul88 tree view

We set the view for all the SysF to use as analog_extracted and simulate the circuit.



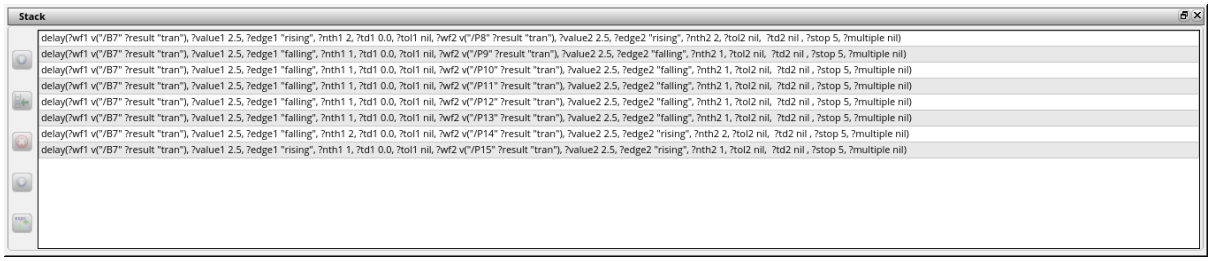


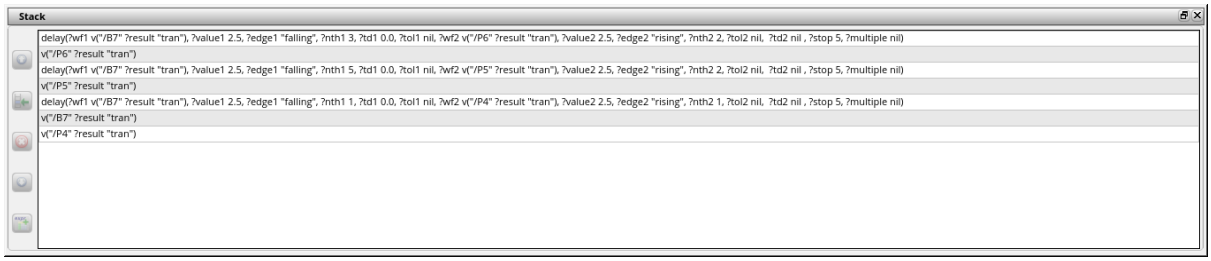
TBmul88 config ADE L

TBmul88 output waveform (including parasitics, 100MHz)

Propagation delays (including parasitics):

F04 Delay	Expression/Remarks	Value
t_{pd} (P0)	P0 is constant	N/A
t_{pd} (P1)	P1 is constant	N/A
t_{pd} (P2)	P2 is constant	N/A
t_{pd} (P3)	P3 is constant	N/A
t_{pd} (P4)	1.706E-9	1.706ns
t_{pd} (P5)	1.709E-9	1.709ns
t_{pd} (P6)	1.689E-9	1.689ns
t_{pd} (P7)	1.698E-9	1.698ns
t_{pd} (P8)	723.5E-12	723.5ps
t_{pd} (P9)	1.151E-9	1.151ns
t_{pd} (P10)	1.117E-9	1.117ns
t_{pd} (P11)	1.12E-9	1.12ns
t_{pd} (P12)	1.134E-9	1.134ns
t_{pd} (P13)	1.154E-9	1.154ns
t_{pd} (P14)	1.764E-9	1.764ns
t_{pd} (P15)	1.966E-9	**1.966ns**





Therefore, the worst-case input-output 50%-50% propagation delay for schematic-only simulation came to be **1.966ns** which is worse than the schematic-only output. Though all the individual delays are not higher, but the worst-case delay is more compared to the previous value. It is very normal that layout parasitics, that too in a huge circuit like this will increase the propagation delay.

Since we kept the value of D as 1 (5V), hence the lowermost bits remain constant which depends only on the values of A0, B0…A3, B3 and hence the summed values are either constant at 1 or at 0, as evident from the waveform.