ECE520: Lab 9 NAND, NOR cell layouts

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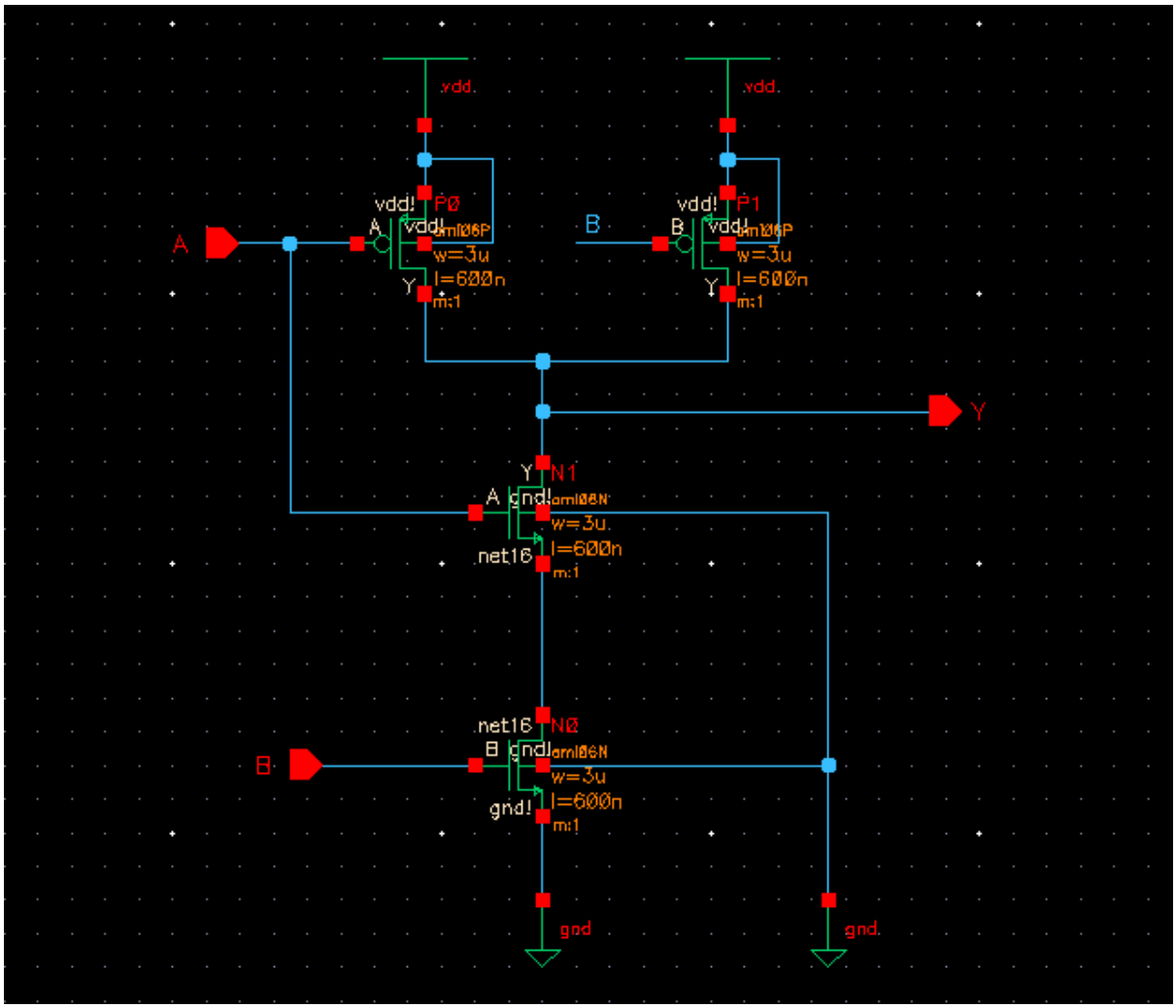
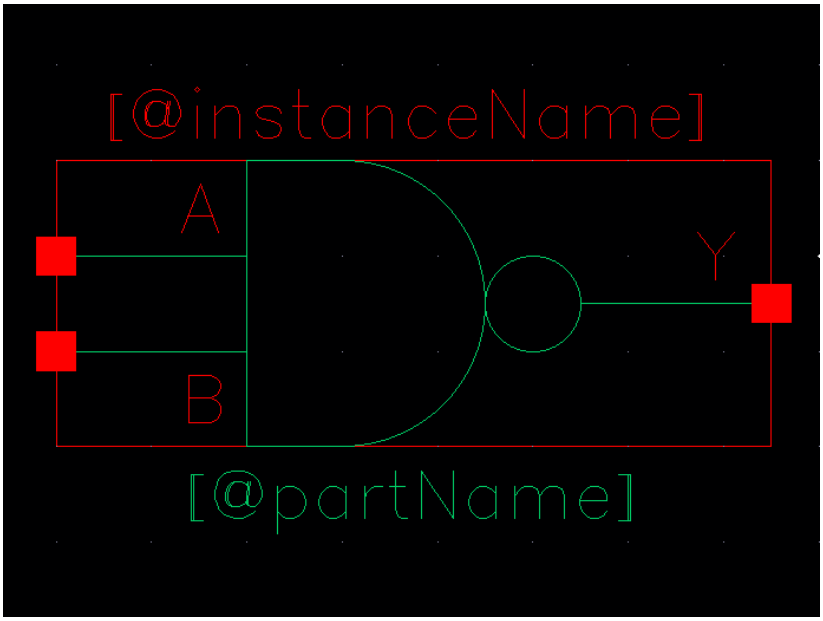
1) Designing a NAND2X1 cell



NAND2X1 Schematic

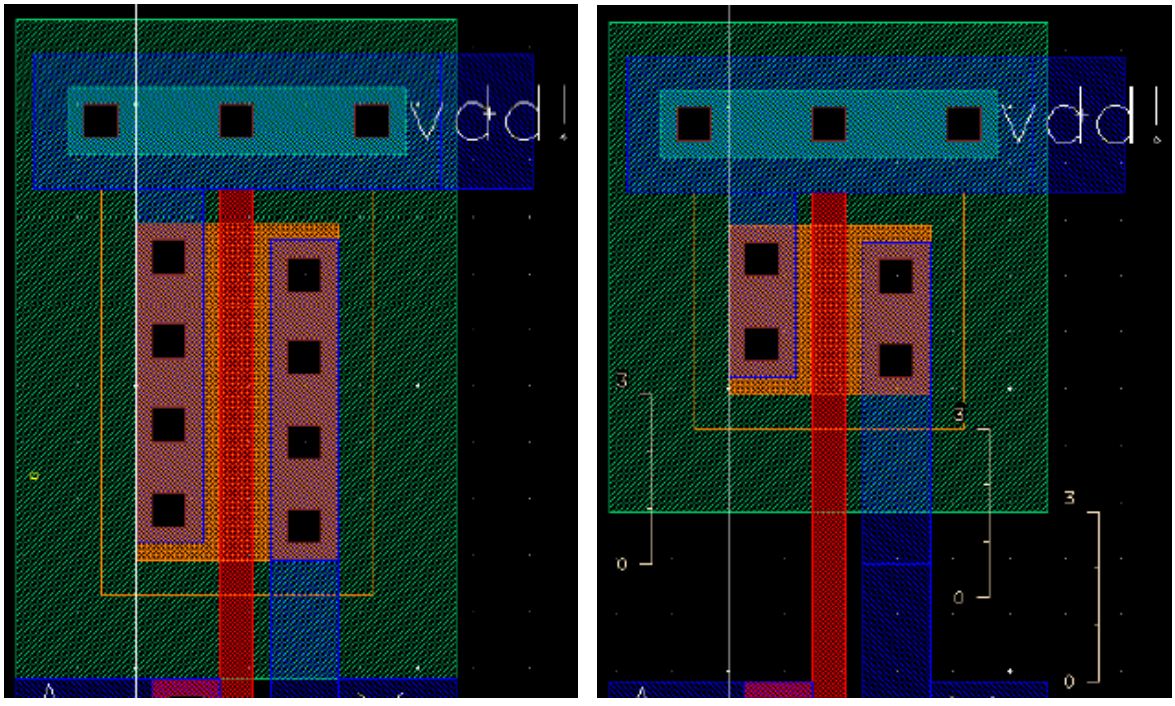
pmos W/L = (3.0µm) / (0.6µm) = 5 W/L=5. This is a **size 2 pmos**.

nmos W/L = (3.0µm) / (0.6µm) = 5 W/L=5. This is a **size 2 nmos**.

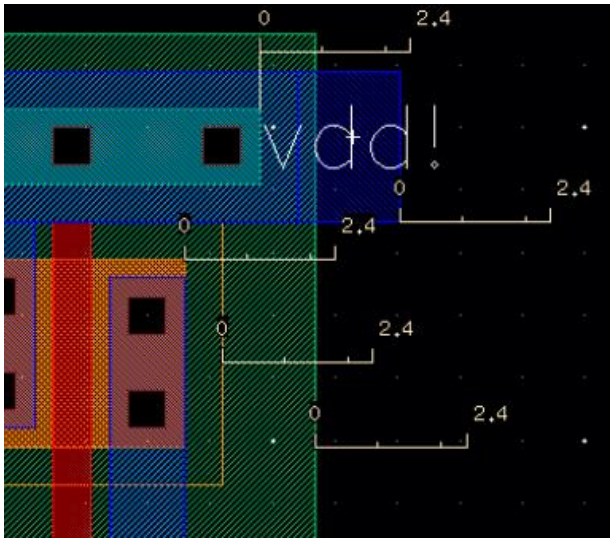


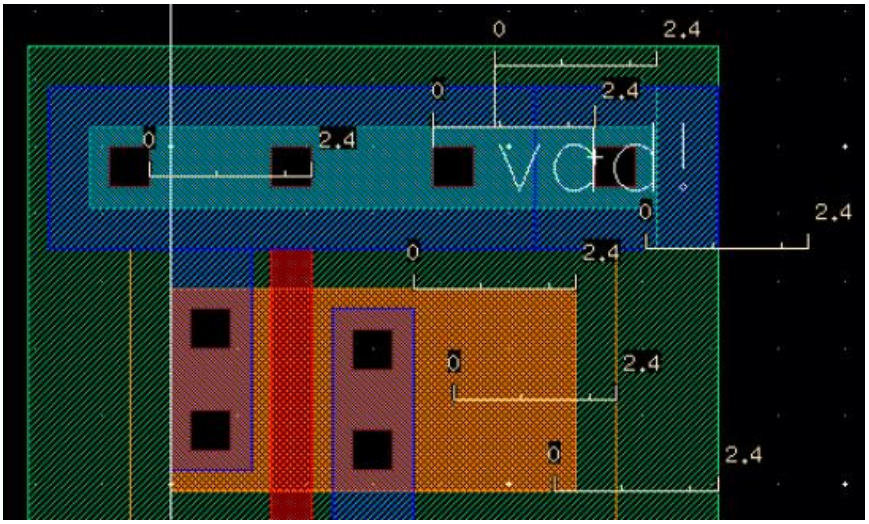
NAND2X1 Symbol

Now we draw the NAND2X1 layout by copying from LAB8 (INVX2 layout) into LAB9 (NAND2X1 layout).

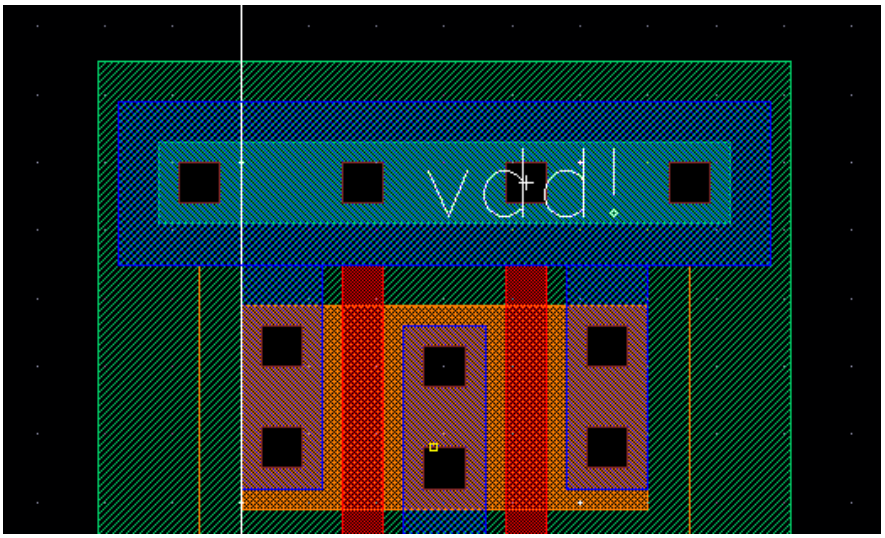


We shrink the pmos transistor by 3µm and then place the second pmos much similar to INVX4 by stretching pactive, nwell, nselect to the right by 2.4µm.

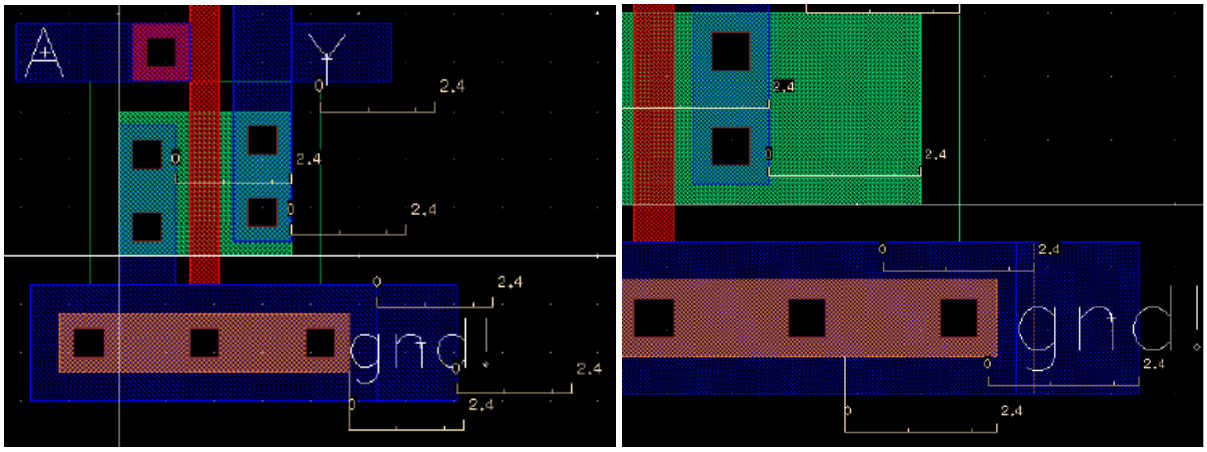




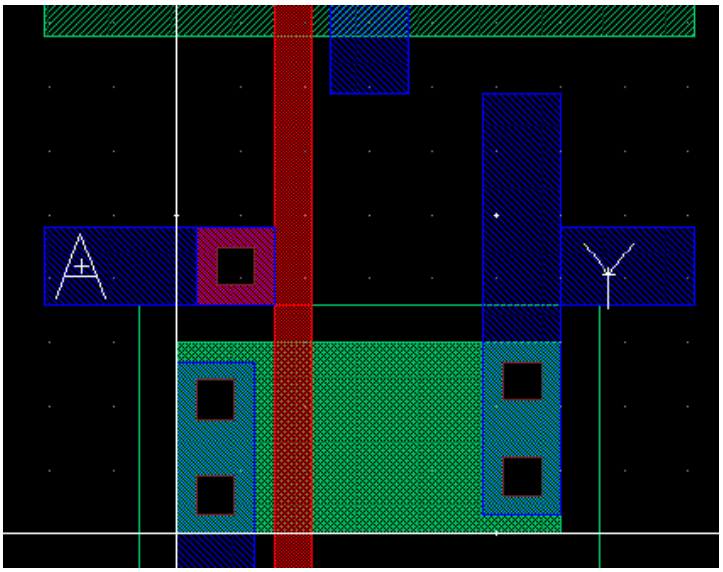
We made enough room to add another pmos transistor in this area so we copy the entire Source (S) area from the left to the right.



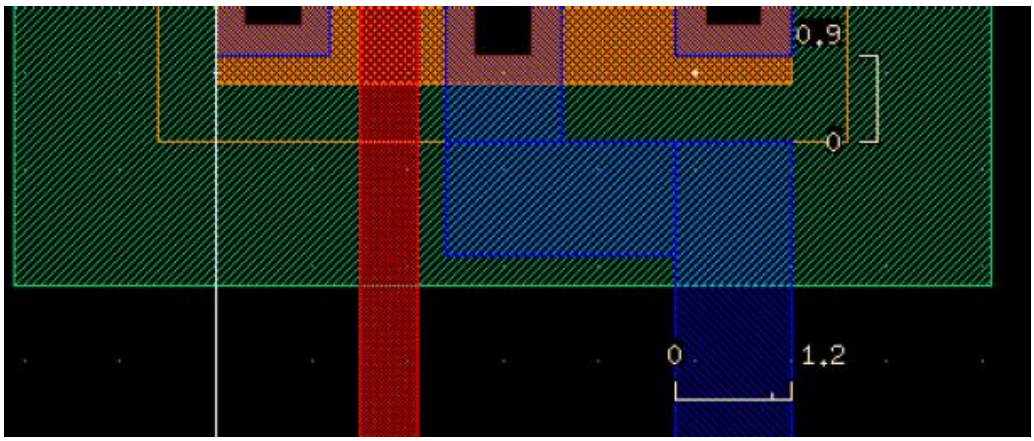
Now we work on the bottom (nmos) area and stretch the entire nmos area to the right by 2.4µm.



We move the “Y” label, the output (Y) pin, 2 contacts, and the metal1 connection that connects to the pmos transistors above.



We re-connect metal1 properly and straighten it out.



We run a DRC check before we go any further and encounter the following errors:

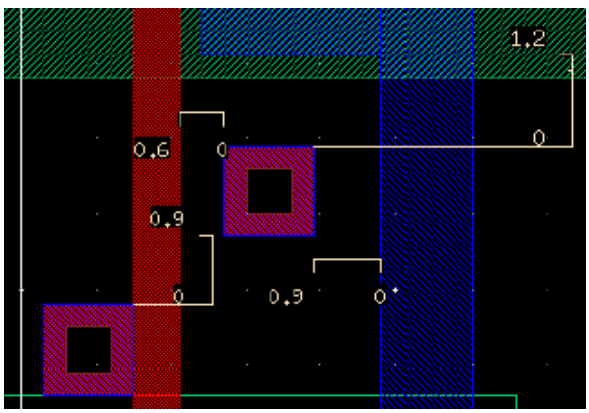
```
*********  Summary of rule violations for cell "NAND2X1 layout"  *********
 # errors  Violated Rules
       1   (SCMOS Rule 4.2) select overlap of active: 0.60 um
       2   Label/Pin is on a net with a different name
       3   Total errors found
```

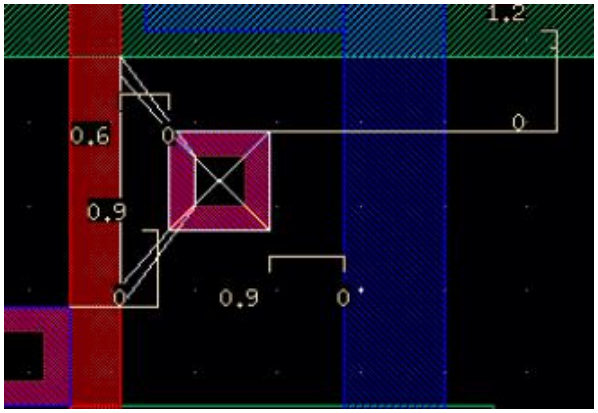
To fix the DRC errors step by step, we delete the pins and labels for A input and Y output and also go to Verify -> Delete All Markers. We run DRC again and see no errors.

```
*********   Summary of rule violations for cell "NAND2X1 layout"   *********
   Total errors found: 0
```

We will construct the “B” input pad with a metal1 connection and the poly line that belongs to B input. We copy every layer that belongs to the A input pad and place on the other side of poly.

After placing this pad for the B input, we run DRC again.





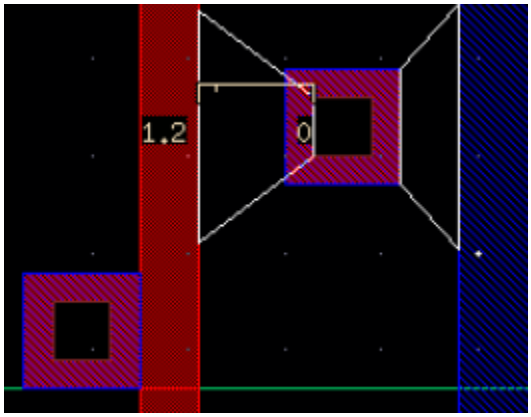
We get the following errors:

```
*********  Summary of rule violations for cell "NAND2X1 layout"  *********
 # errors  Violated Rules
        1  (SCMOS Rule 5.5.b) poly contact to poly spacing: 1.50 um
        1  (SCMOS_SUBM Rule 3.2) poly spacing: 0.90 um
        1  Label/Pin "A" is causing two nets to have the same name.
        3  Total errors found
```

We edit the Terminal Name and change it to B for the pin on the right and run DRC again.

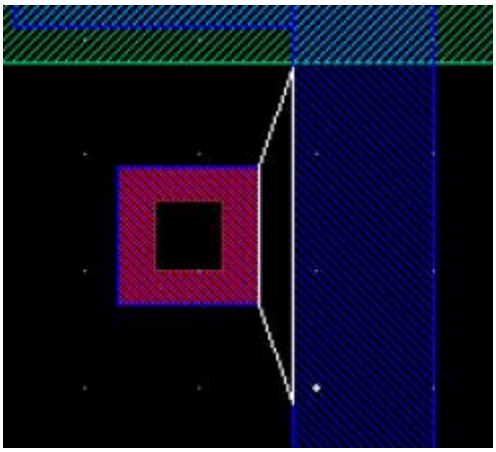
```
*********  Summary of rule violations for cell "NAND2X1 layout"  *********
 # errors  Violated Rules
        1  (SCMOS Rule 5.5.b) poly contact to poly spacing: 1.50 um
        1  (SCMOS Rule 7.2) metal1 spacing: 0.90 um
        2  Total errors found
```

We did fix the poly-poly error, but now we created a metal1-metal1-spacing issue, which should be 3λ minimum.

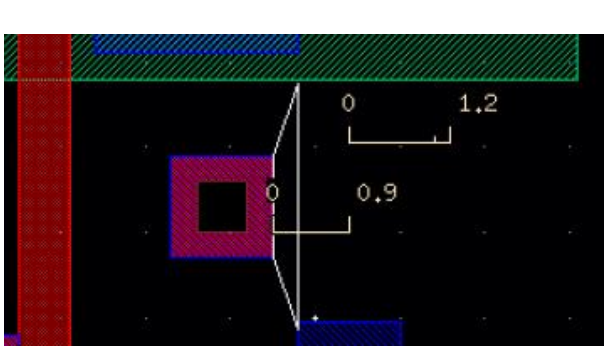


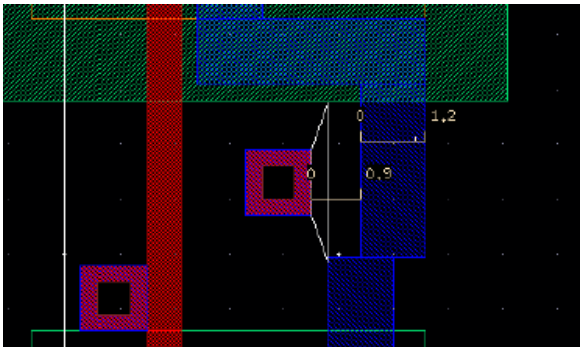
So we move the pad to the right another 0.3µm and run DRC again, but encounter the following error:

```
*********  Summary of rule violations for cell "NAND2X1 layout"
 # errors  Violated Rules
       1   (SCMOS Rule 7.2) metal1 spacing: 0.90 um
       1   Total errors found
```



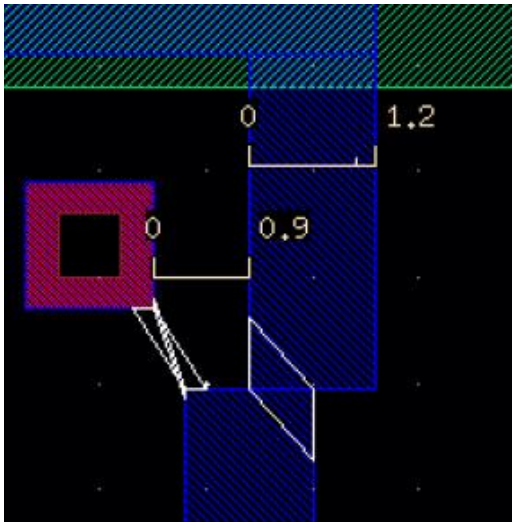
So, we push the output metal1 strip to the right by 2λ more so that we are done placing the pad for the B input.





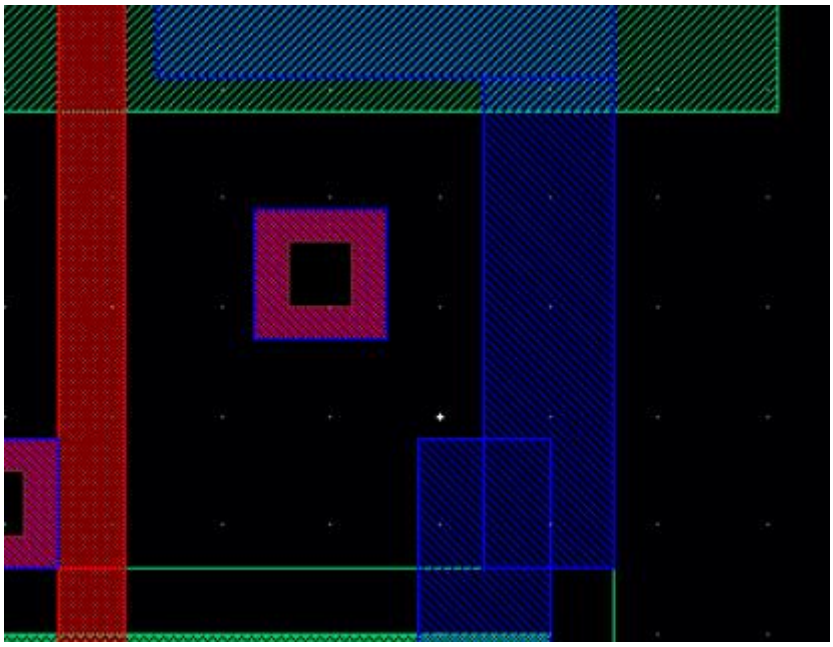
Running DRC again on this final version, we get the following 3 errors:

```
*********  Summary of rule violations for cell "NAND2X1 layout"
 # errors  Violated Rules
       1   (SCMOS Rule 7.1) metal1 width: 0.90 um
       2   (SCMOS Rule 7.2) metal1 spacing: 0.90 um
       3   Total errors found
```



We simply stretch the bottom metal1 to the downward by 0.5λ this problem will be solved. Additionally, stretch the metal1 strip downwards until it extends into the other metal1 by at least 0.9µm (3λ). We run DRC again and it returns no error.

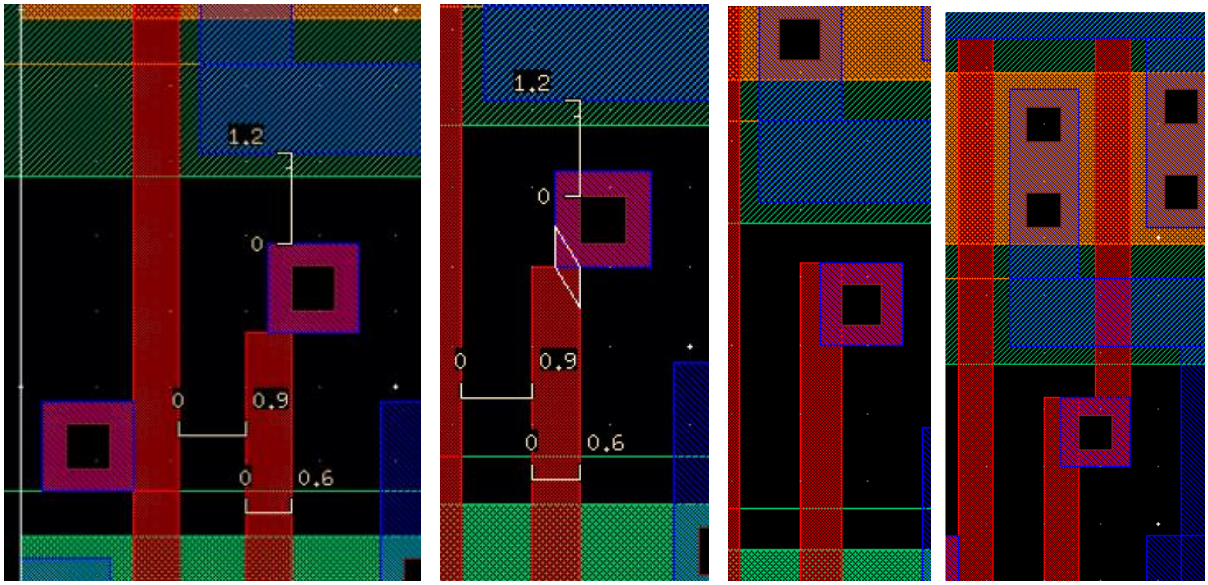
```
*********   Summary of rule violations for cell "NAND2X1 layout"   ****
   Total errors found: 0
```



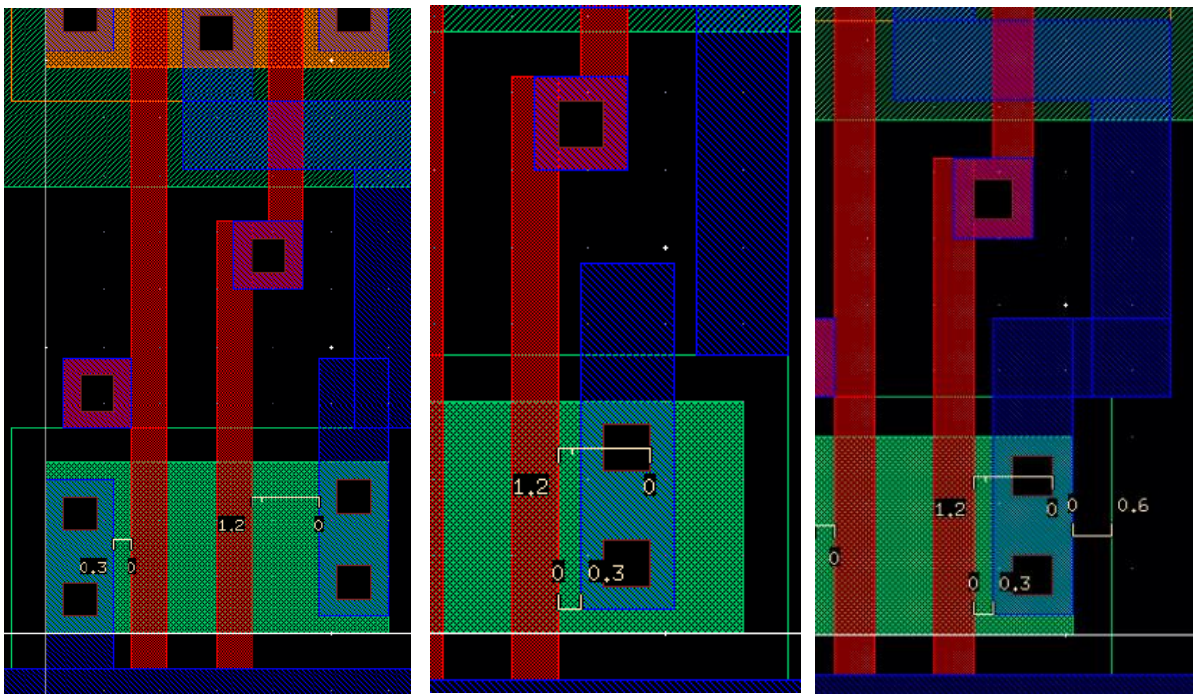
We need a second nmos transistor that is serial to the first one without any contacts in the middle. So we draw a second 2λ-thick poly line that is 3λ away from the other and run DRC again.

```
*********  Summary of rule violations for cell "NAND2X1 layout"
 # errors  Violated Rules
       1   (SCMOS Rule 3.1) poly width: 0.60 um
       1   Total errors found
```

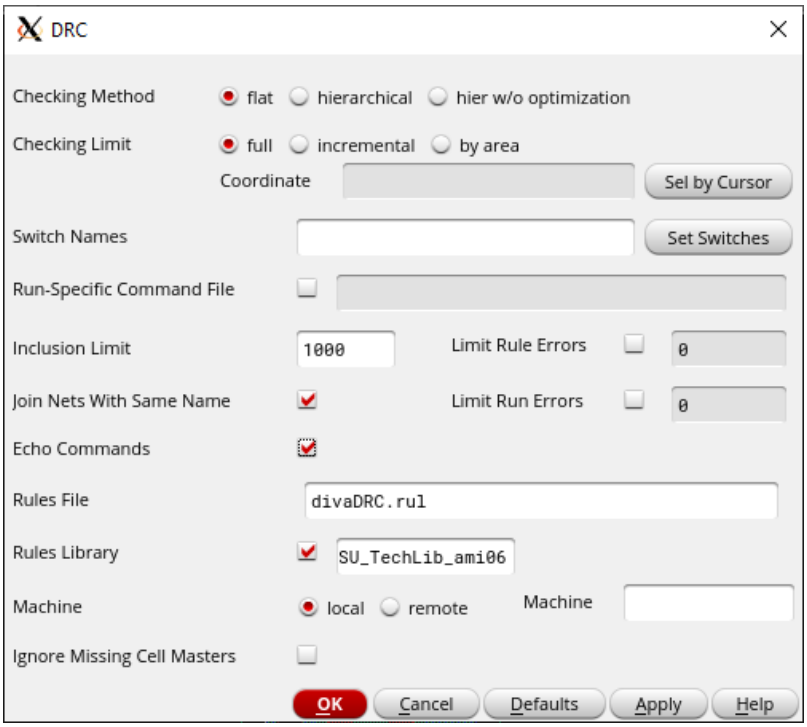
This error says that there is a point in my poly line that is less than 2λ, so we extend the lower poly line until the top of the input pad B. We also create the poly for the pmos above, which will connect to the same B input pad.



There is an excessive nactive (Diffusion) area on the right of the nmos that will create unnecessary diffusion capacitance. Hence we can move the contacts and metal1 area on the right side towards the left by 3λ. After moving the Drain (D) connection of the top transistor, we can also shrink the nactive and nselect areas accordingly and connect the broken metal1.

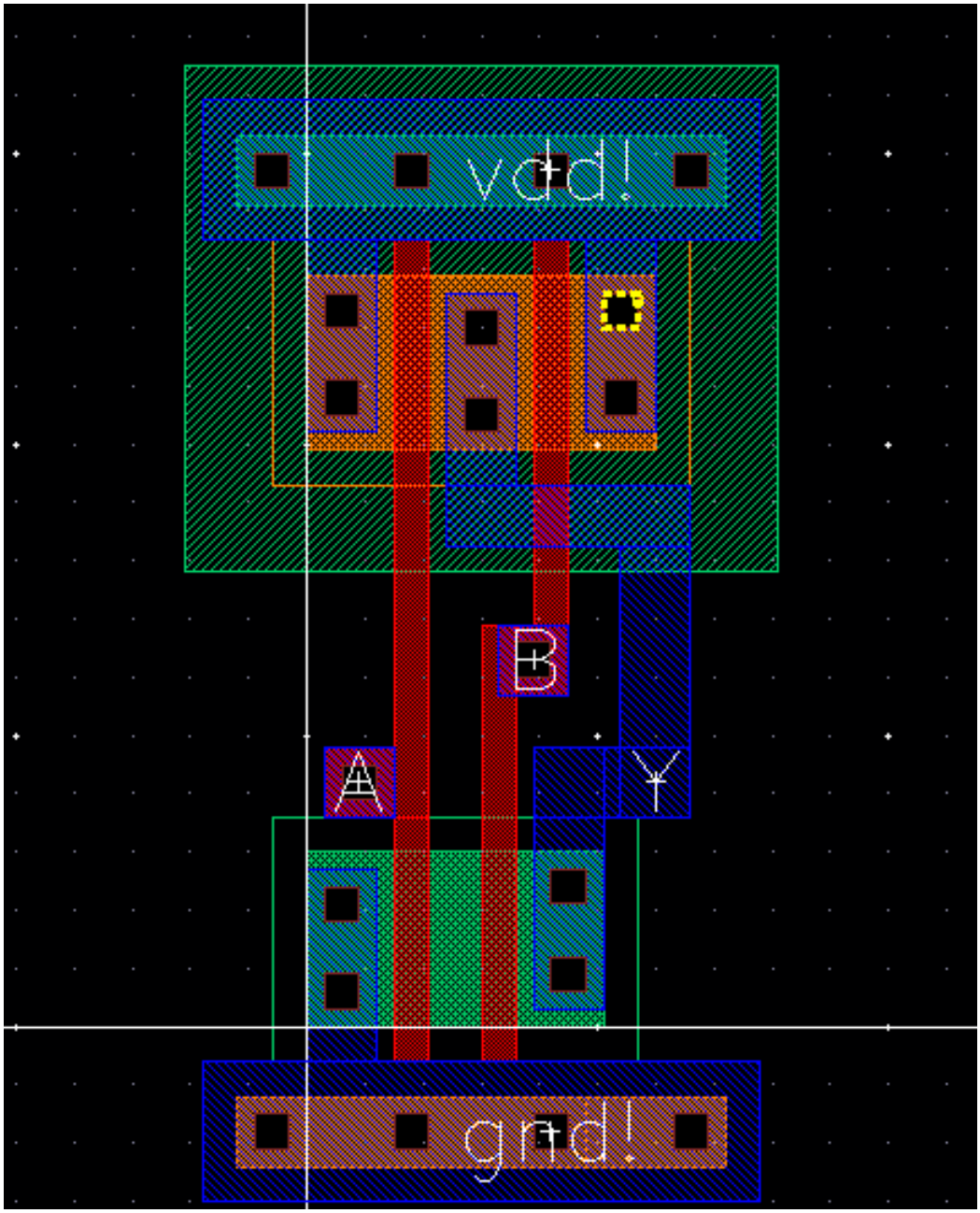


We add an output pin to the output of the NANDX1 on the right and add a label Y. We run DRC again.

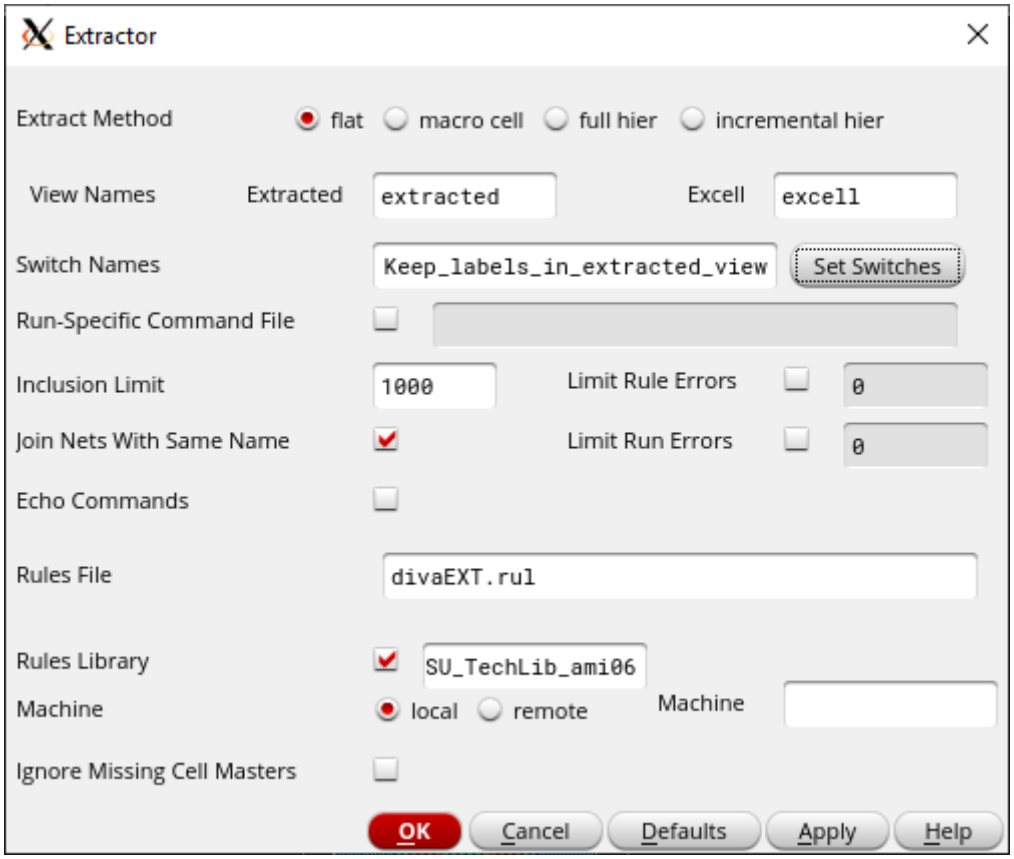



```
*********   Summary of rule violations for cell "NAND2X1 layout"   *********
   Total errors found: 0
```

The final NAND2X1 layout design looks like the following:



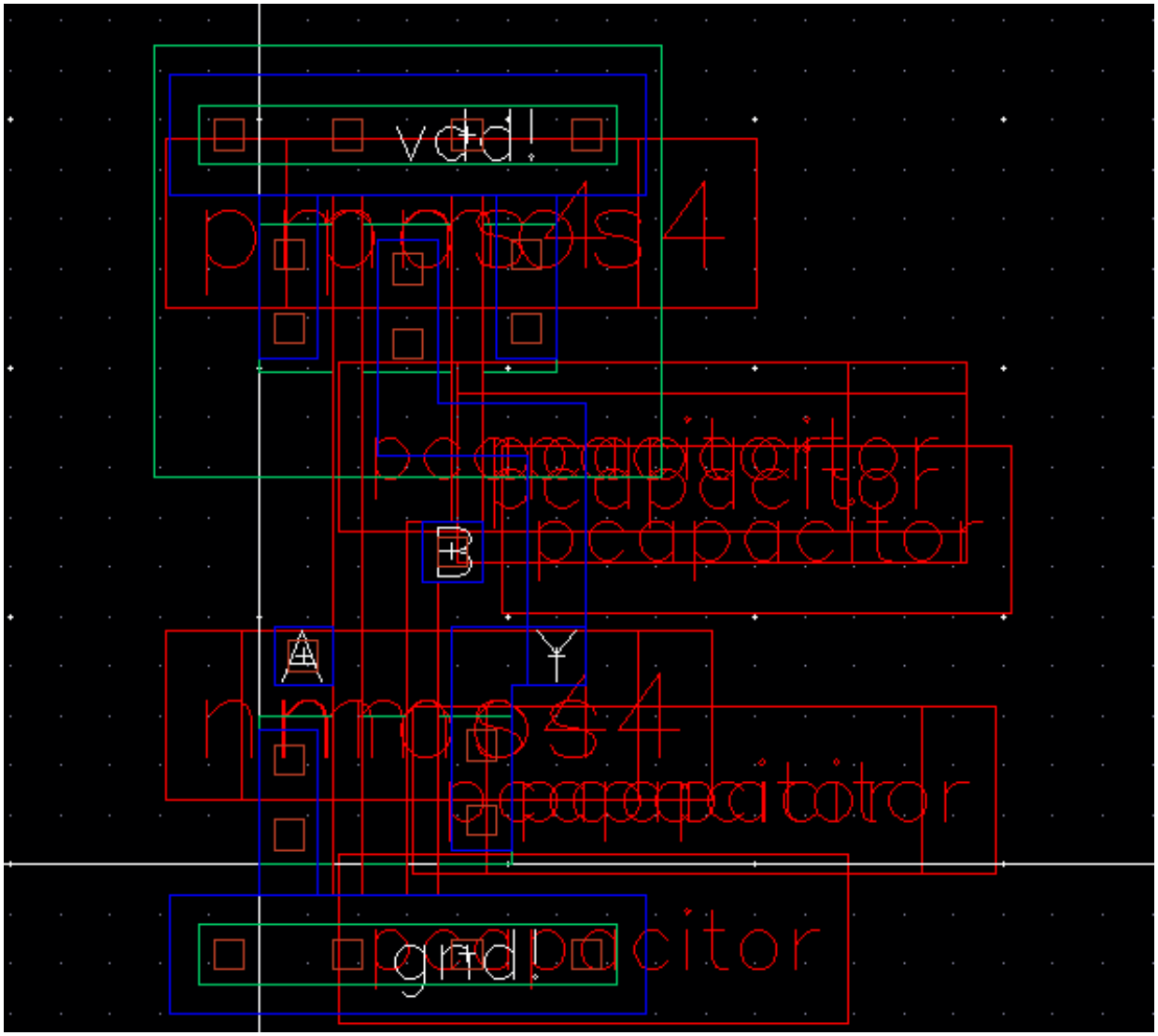
Now, we do Extract and LVS for the NAND2X1.



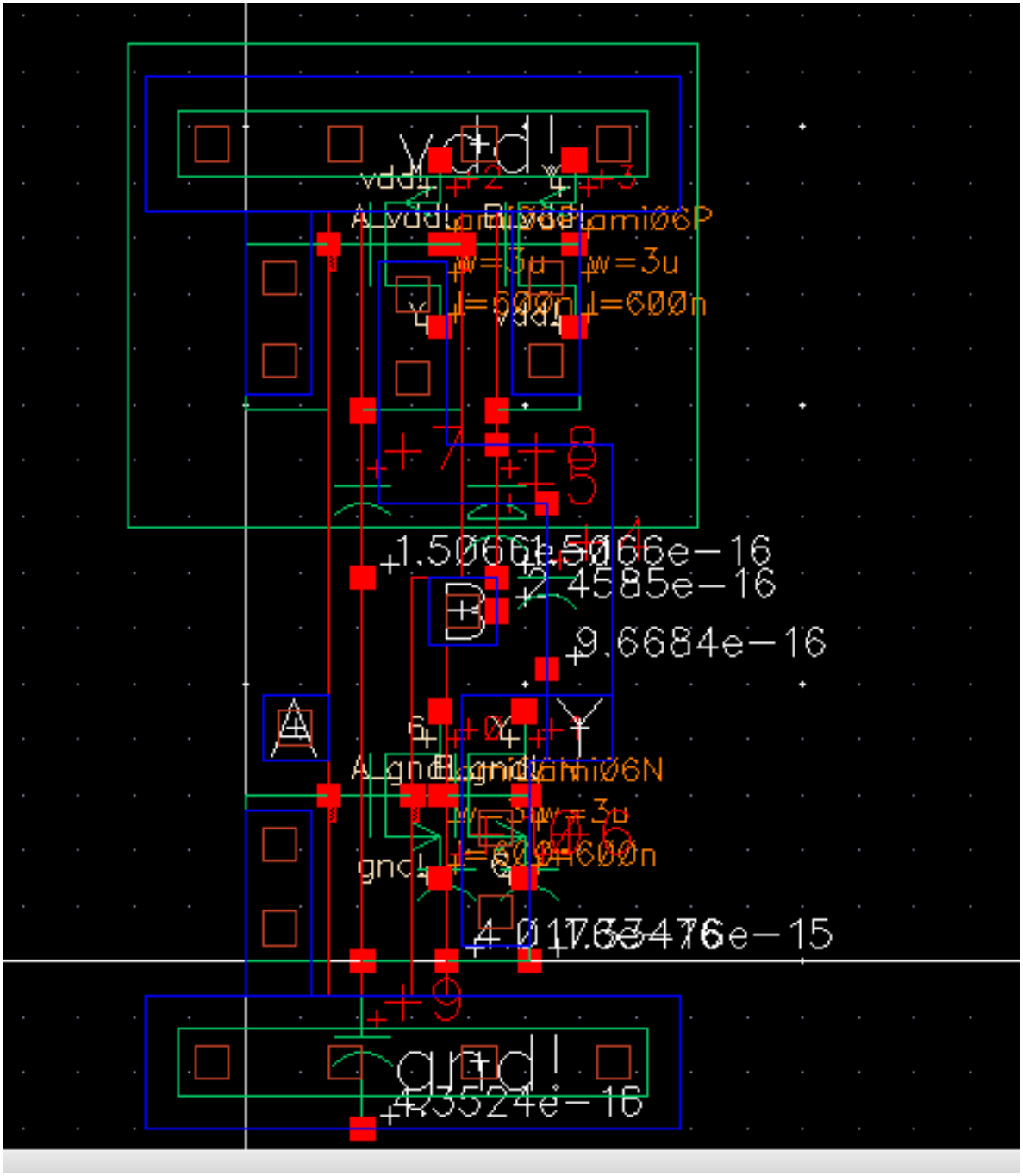
We make sure to select the following switches:

```
saving rep LAB9/NAND2X1/extracted
Getting layout propert bagGetting layout propert bagLoading techComp.cxt
```

The extracted view looks like the following:

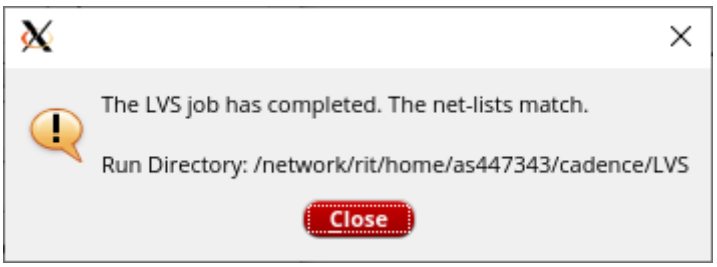


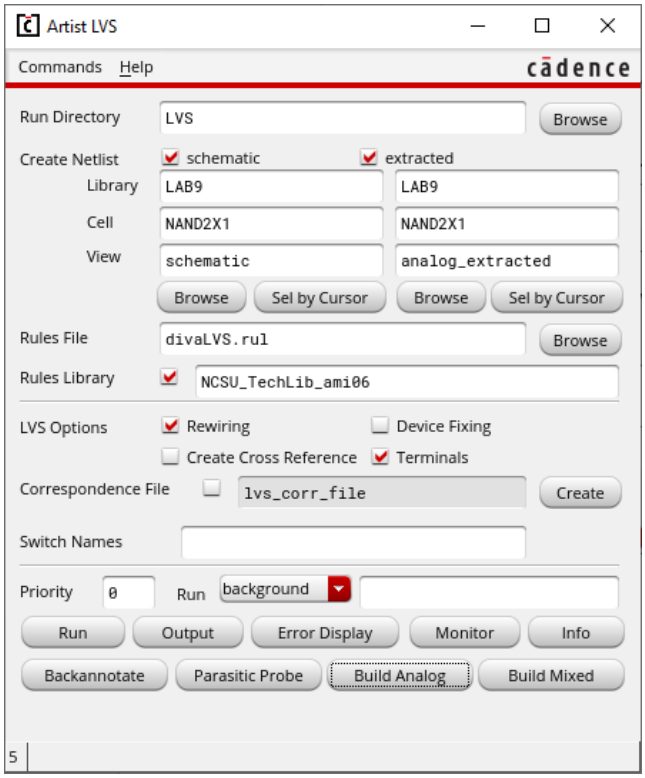
NAND2X1 Extracted view (Top level)



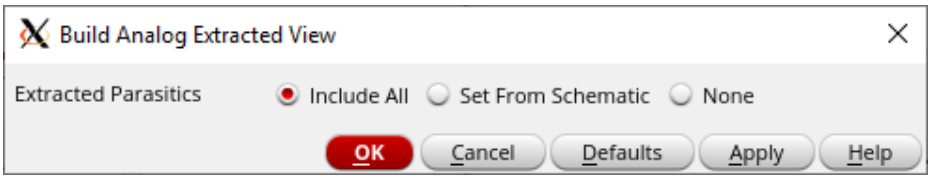
NAND2X1 Extracted view (Lower level)

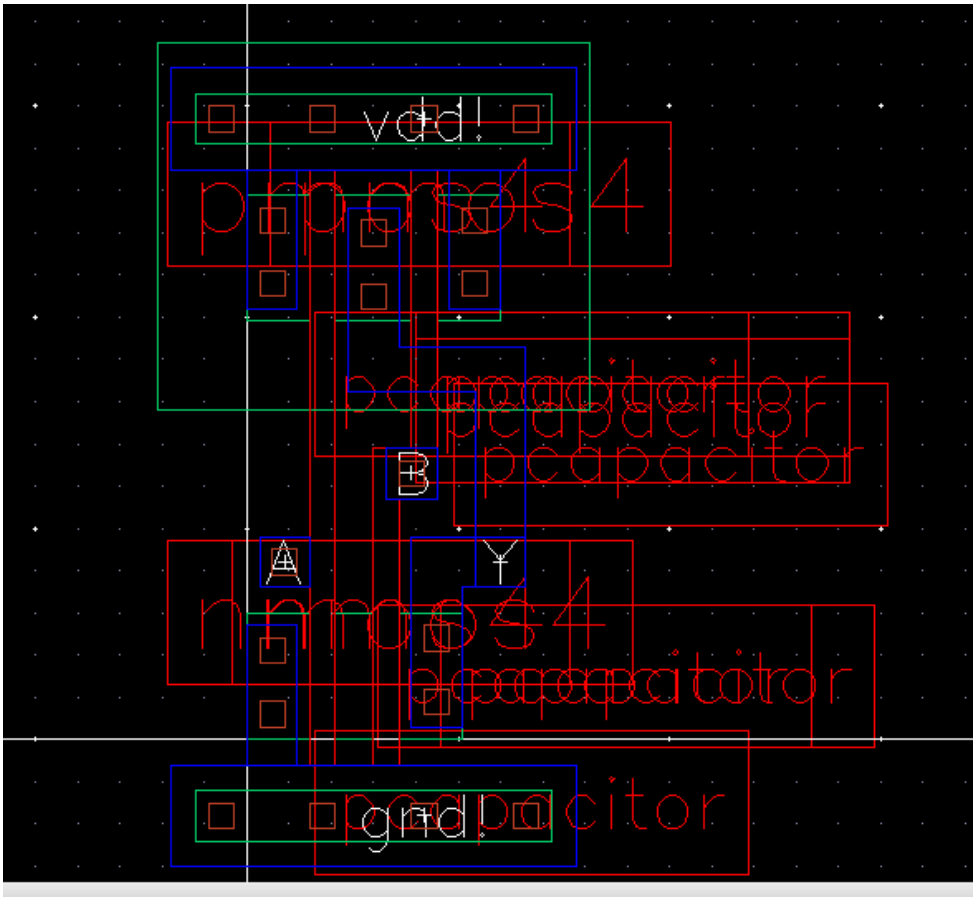
Running LVS, we get the success message! Hence we move forward and create the analog_extracted view of NAND2X1.





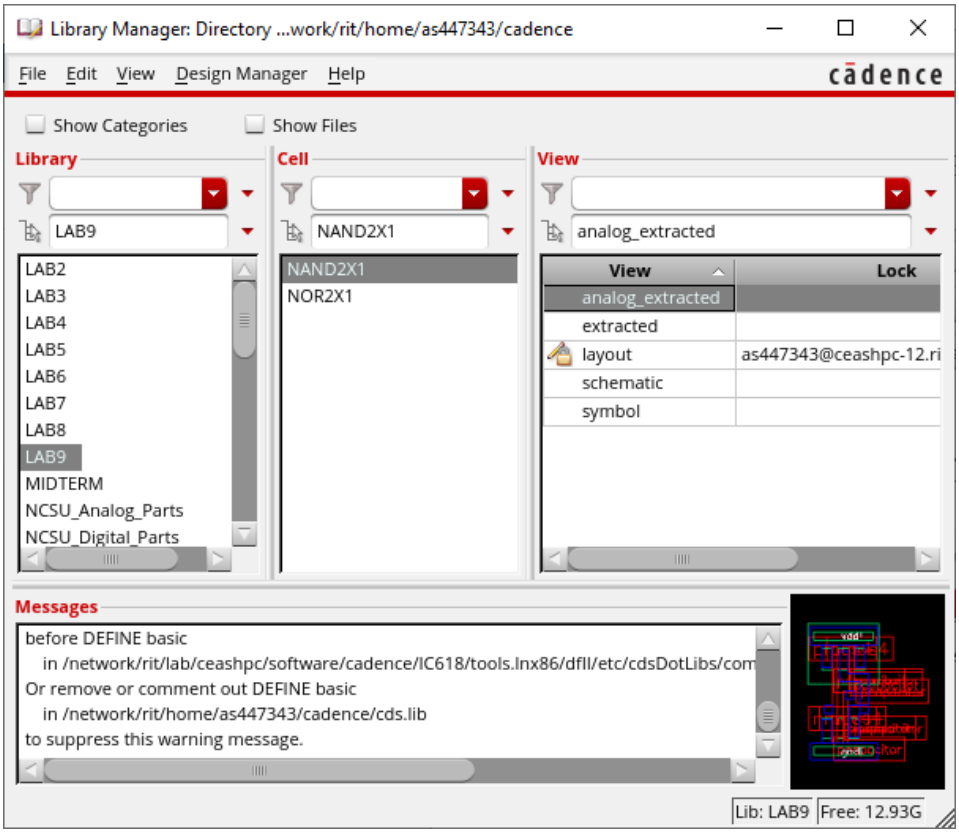
We include all the parasitic components in our design to be later used for config view.



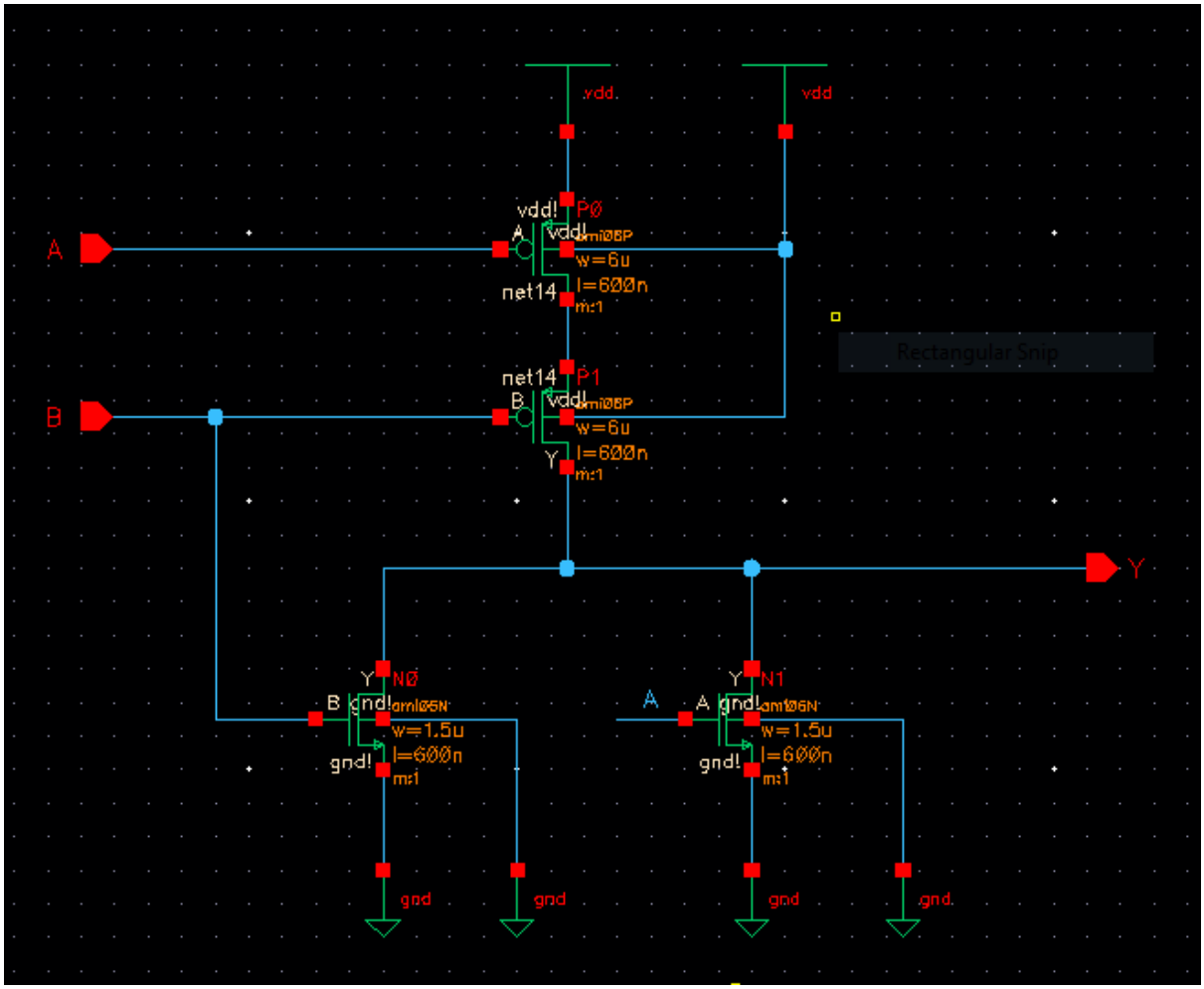


NAND2X1 analog_extracted view

Hence, we have successfully created all five views for NAND2X1.



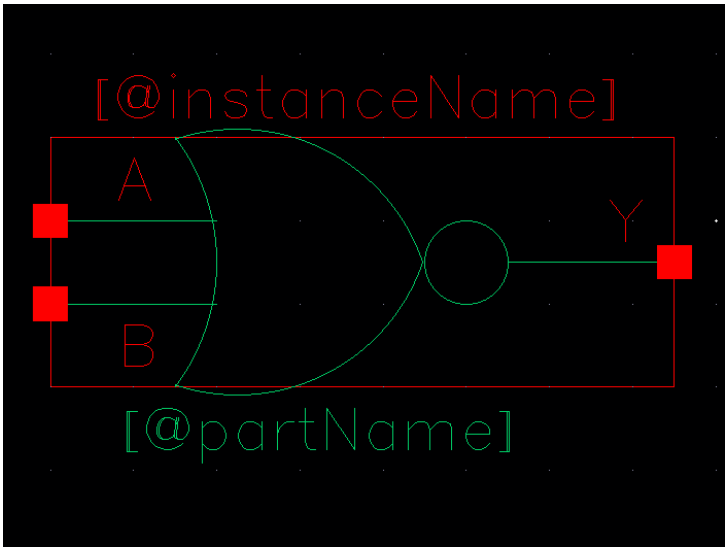
2) Designing a NOR2X1 cell



NOR2X1 Schematic

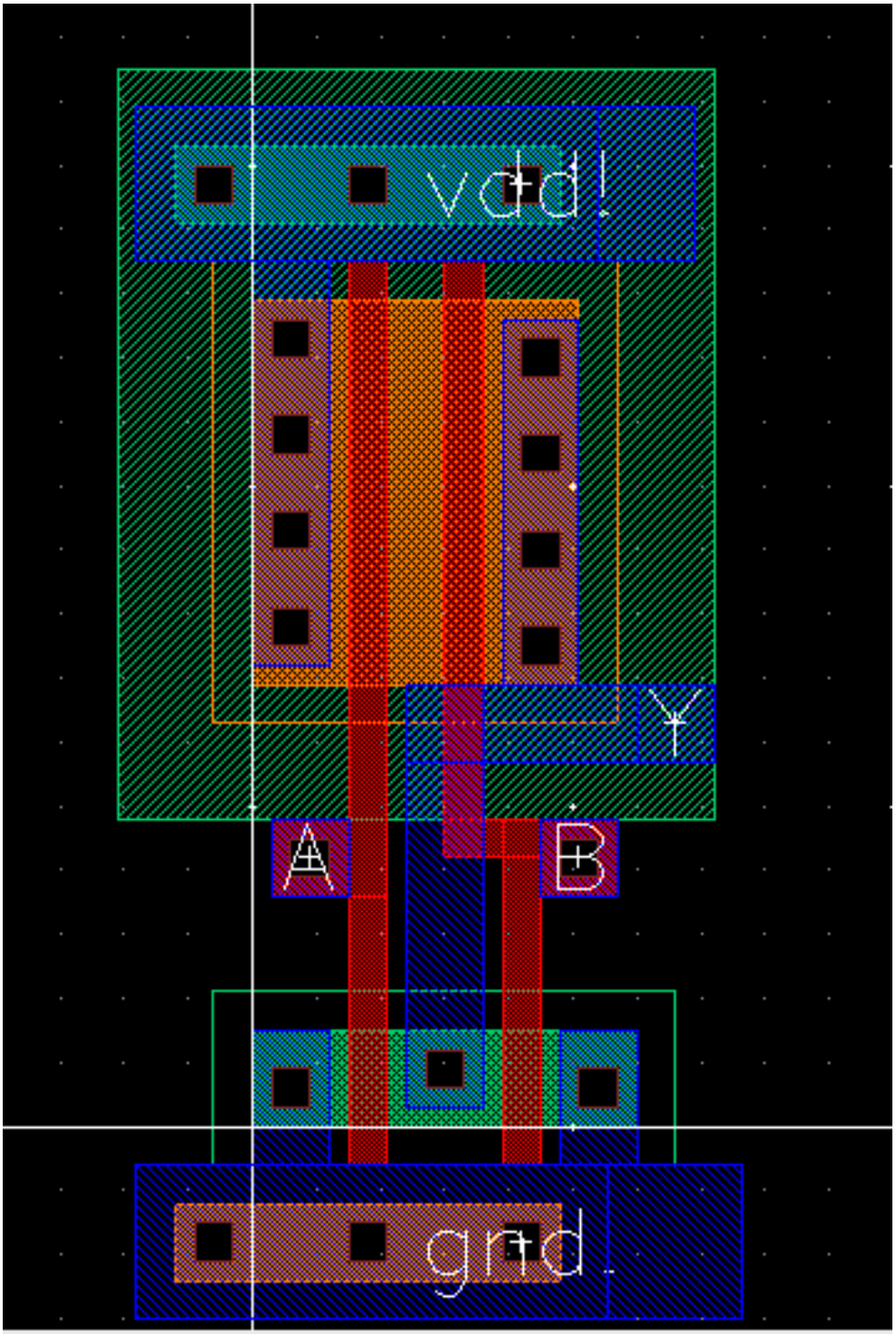
pmos W/L = (6.0µm) / (0.6µm) = 10 W/L=10. This is a size 4 pmos.

nmos W/L = (1.5µm) / (0.6µm) = 2.5 W/L=2.5. This is a size 1 nmos.



NOR2X1 Symbol

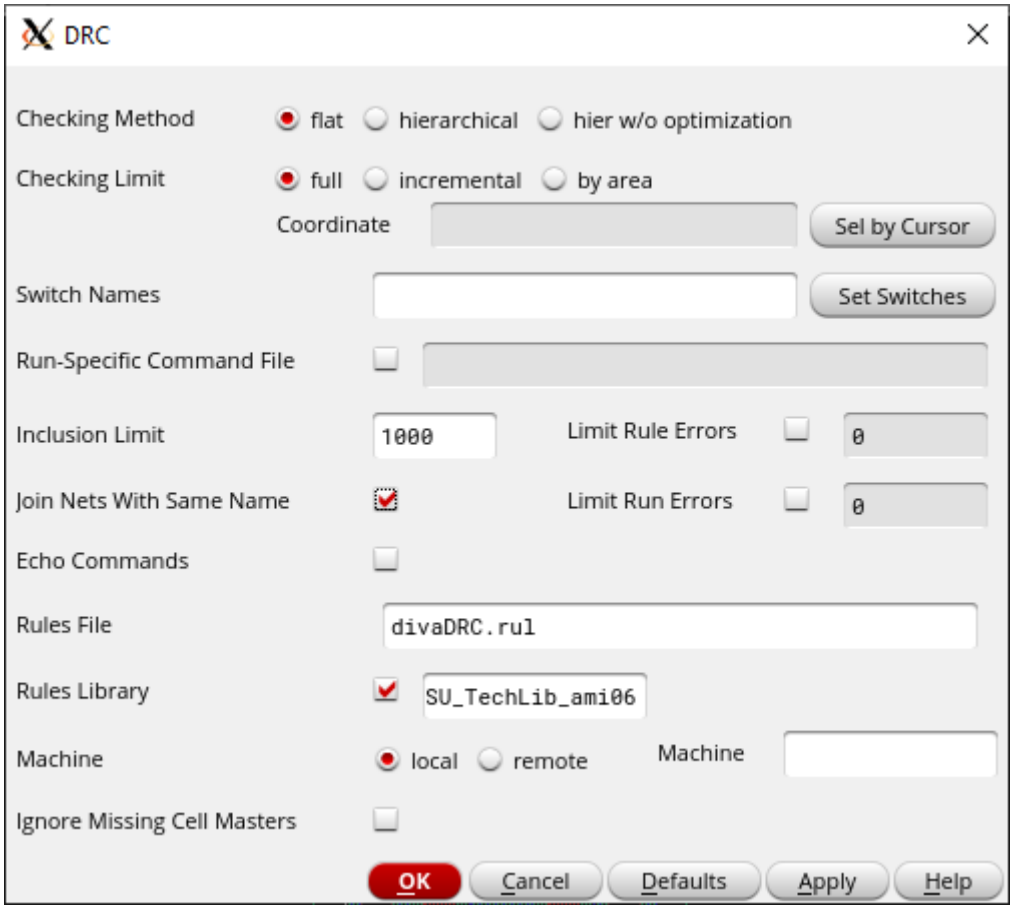
We create the layout of NOR2X1 similar to how we created from NAND2X1.



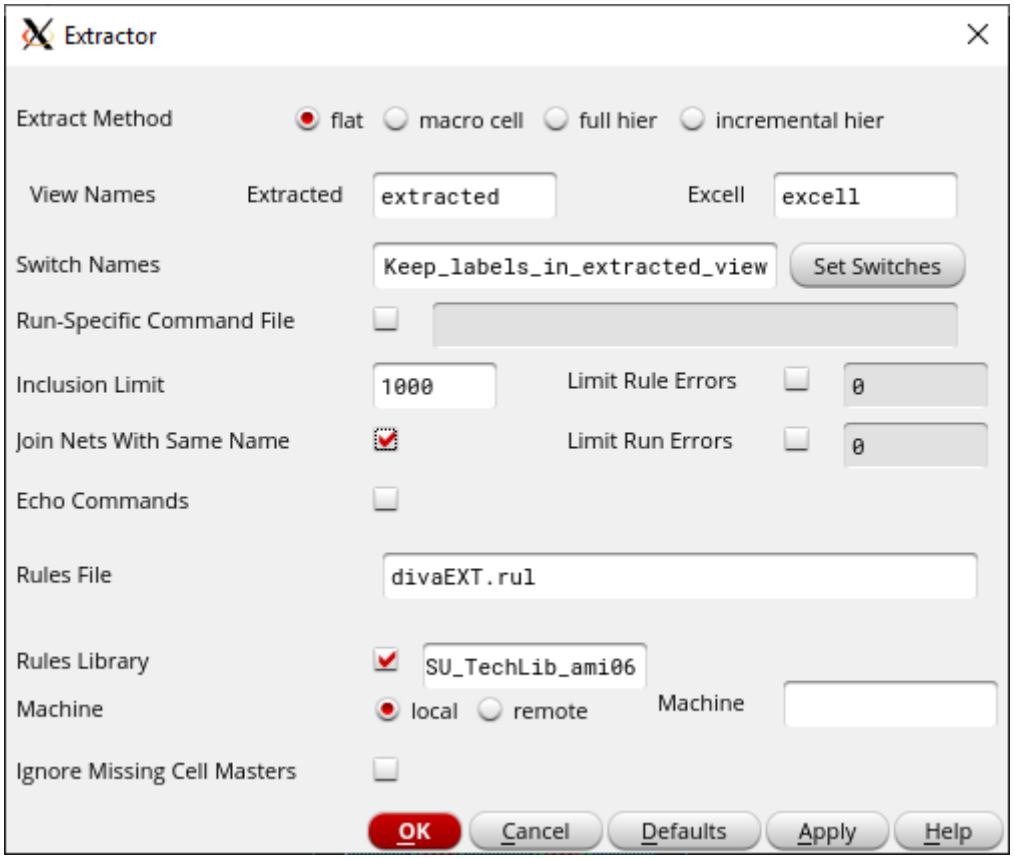
NOR2X1 Layout

Running DRC, we get no errors.

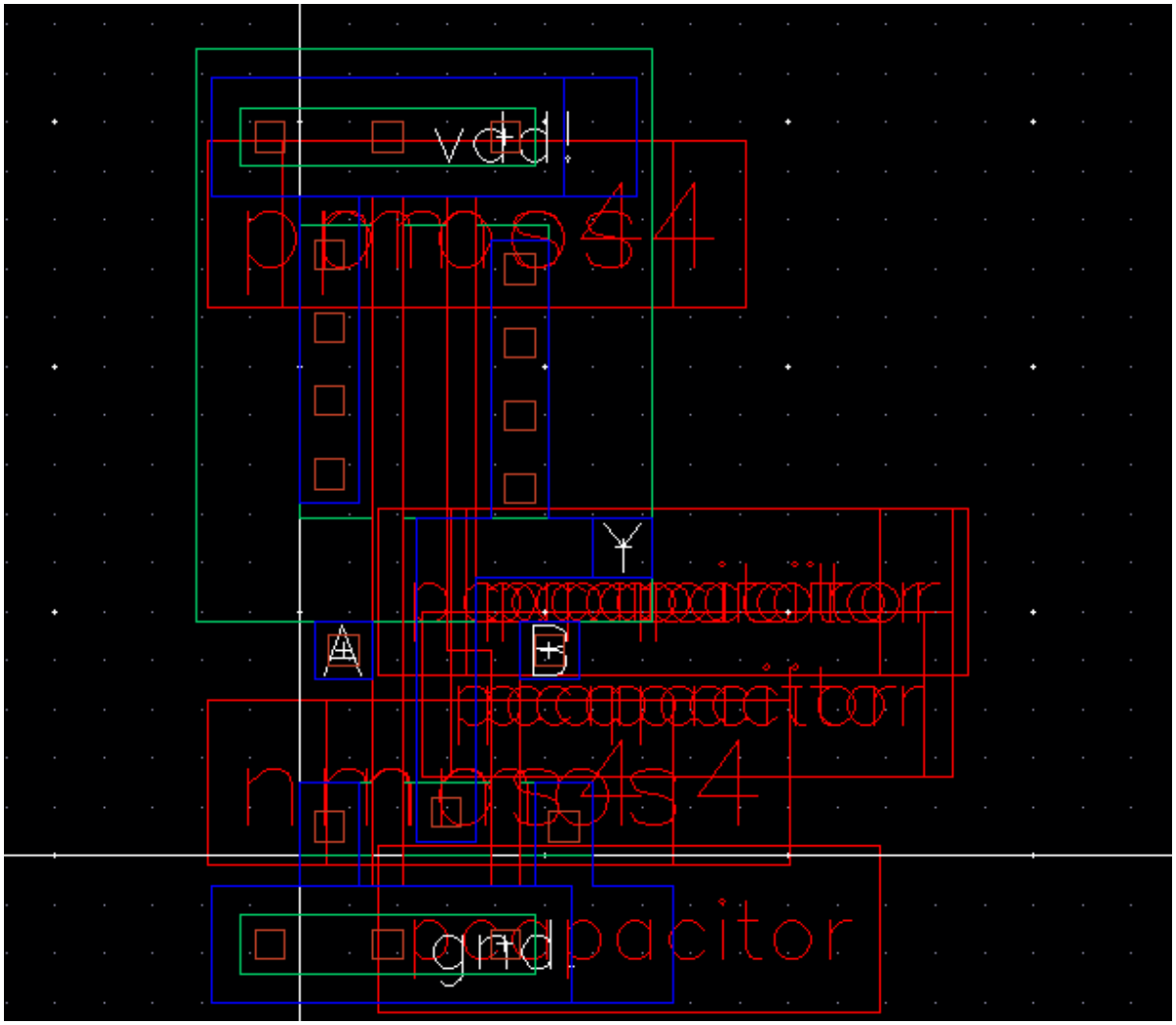
```
*********   Summary of rule violations for cell "NOR2X1 layout"   *********
   Total errors found: 0
```



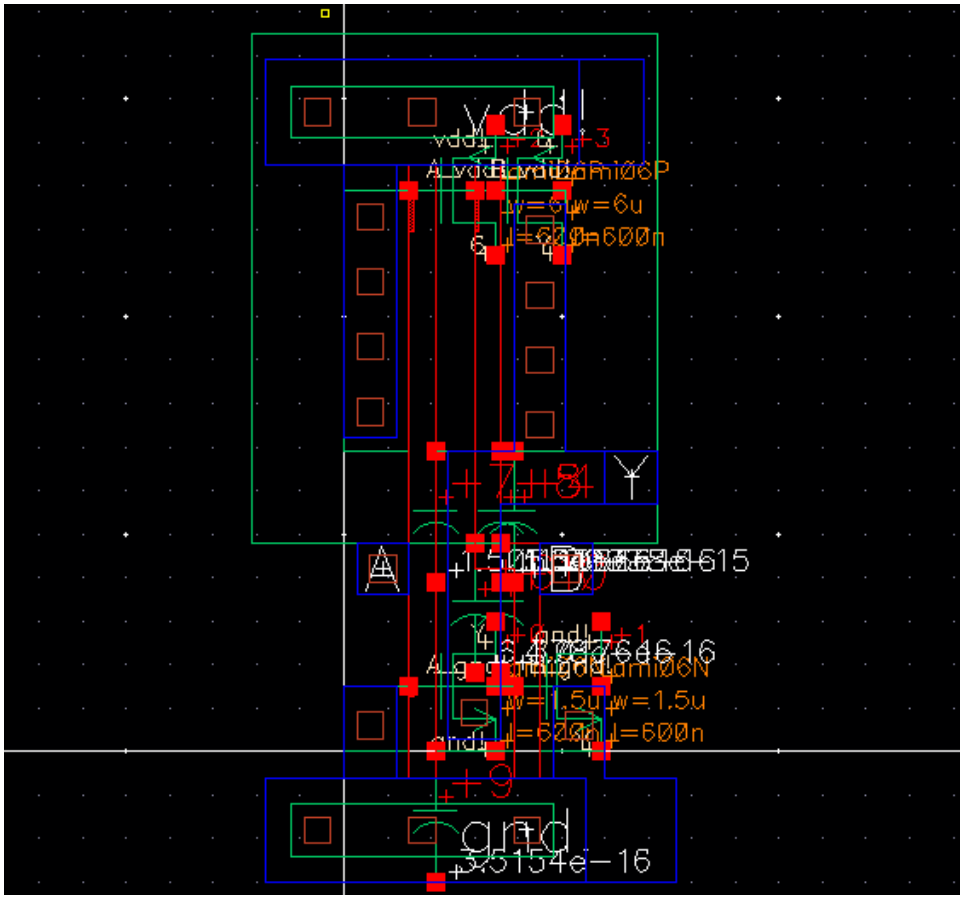
Now, we do Extract and LVS for the NOR2X1.



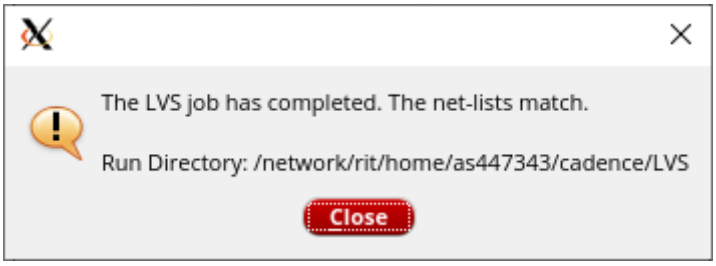
```
saving rep LAB9/NOR2X1/extracted
Getting layout propert bagGetting layout propert bagLoading techComp.cxt
```

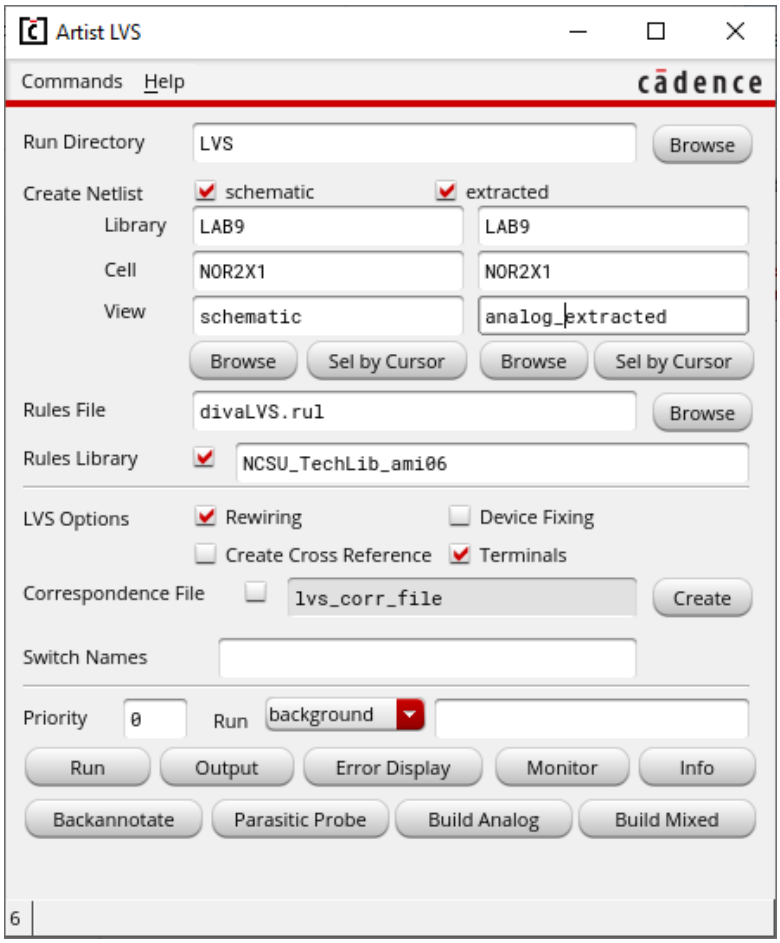


NOR2X1 Extracted view (Top level)

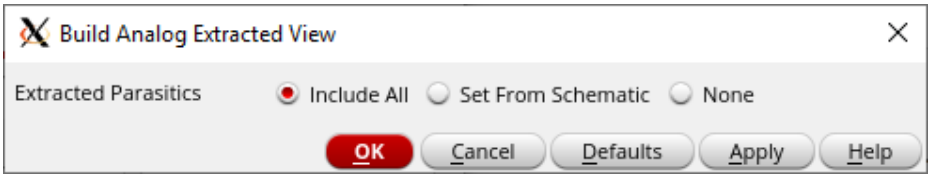


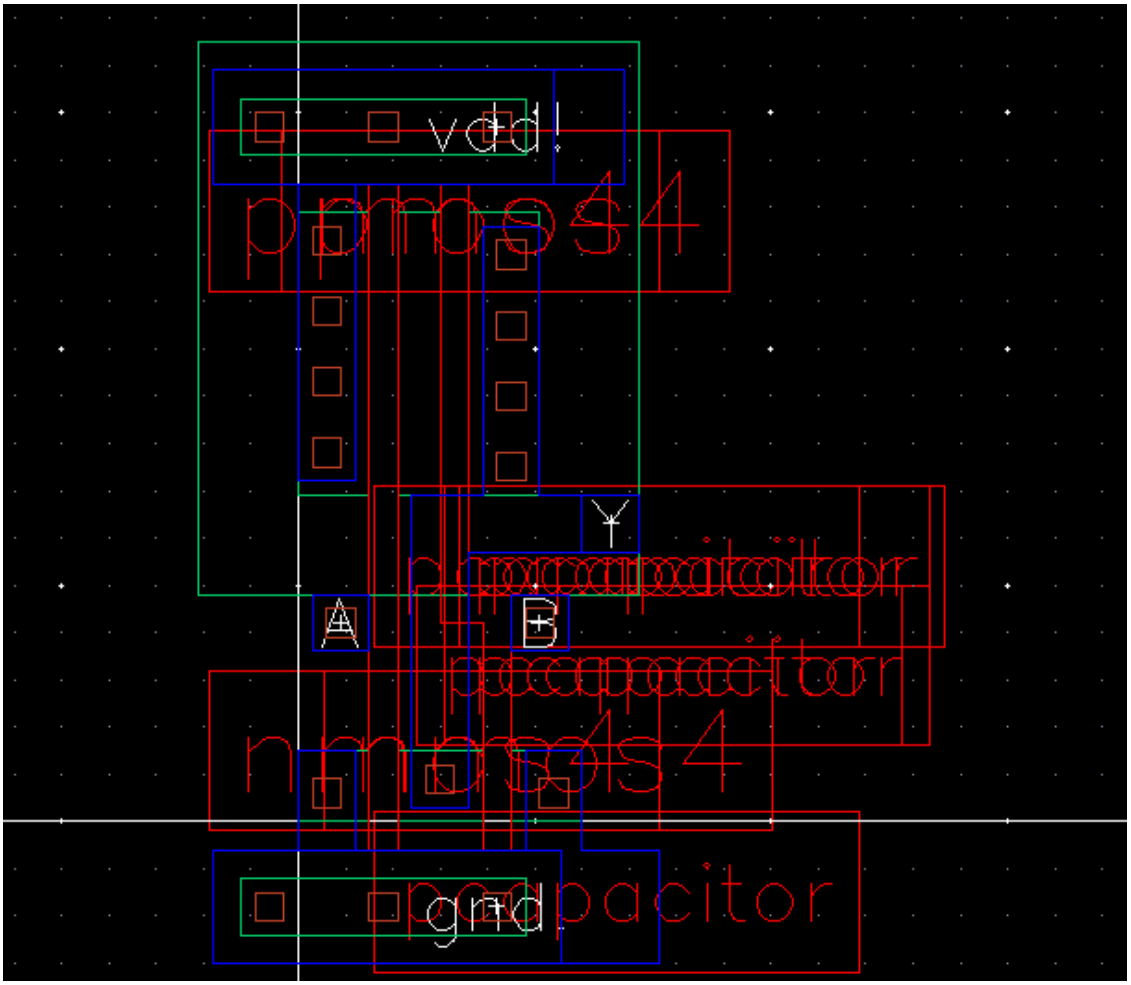
NOR2X1 Extracted view (Lower level)





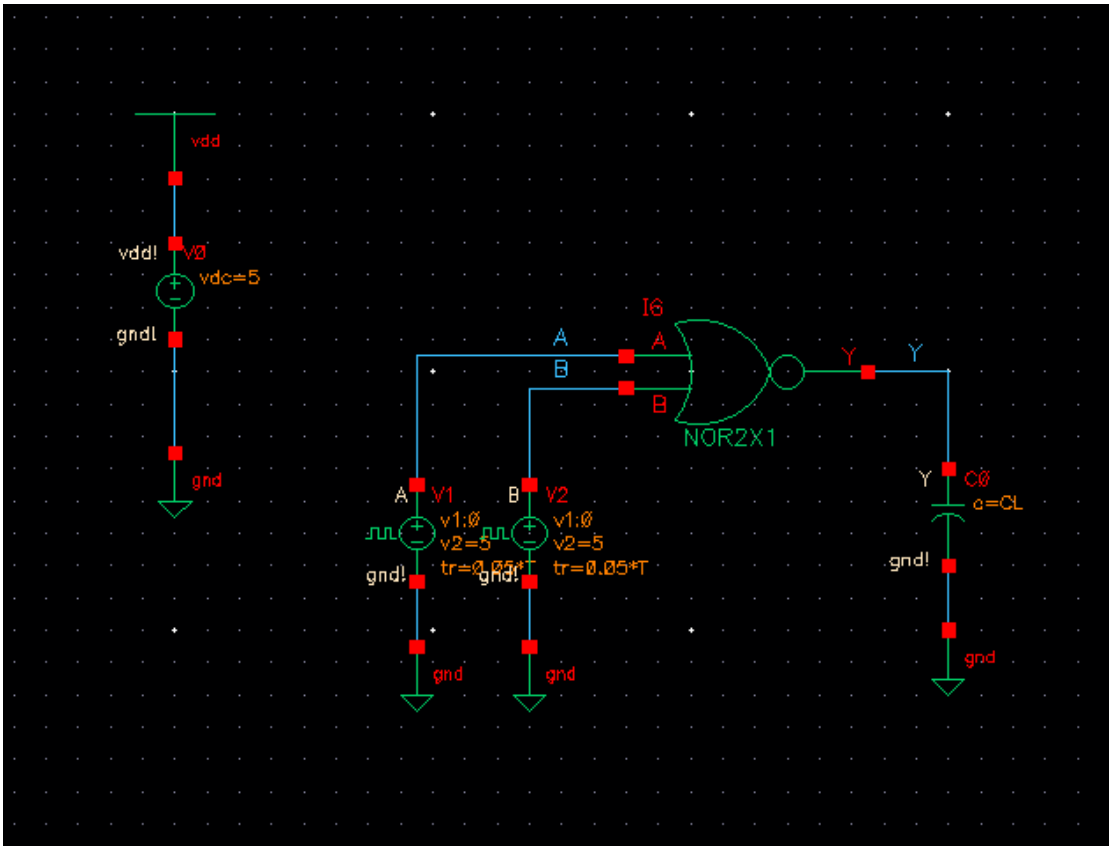
We include all the parasitic components in our design to be later used for config view.



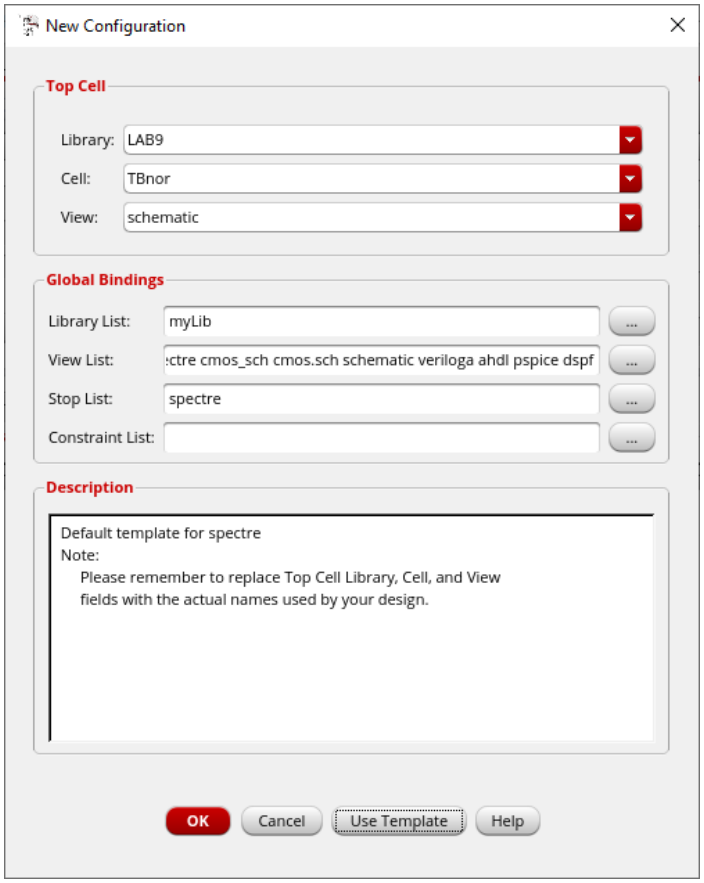


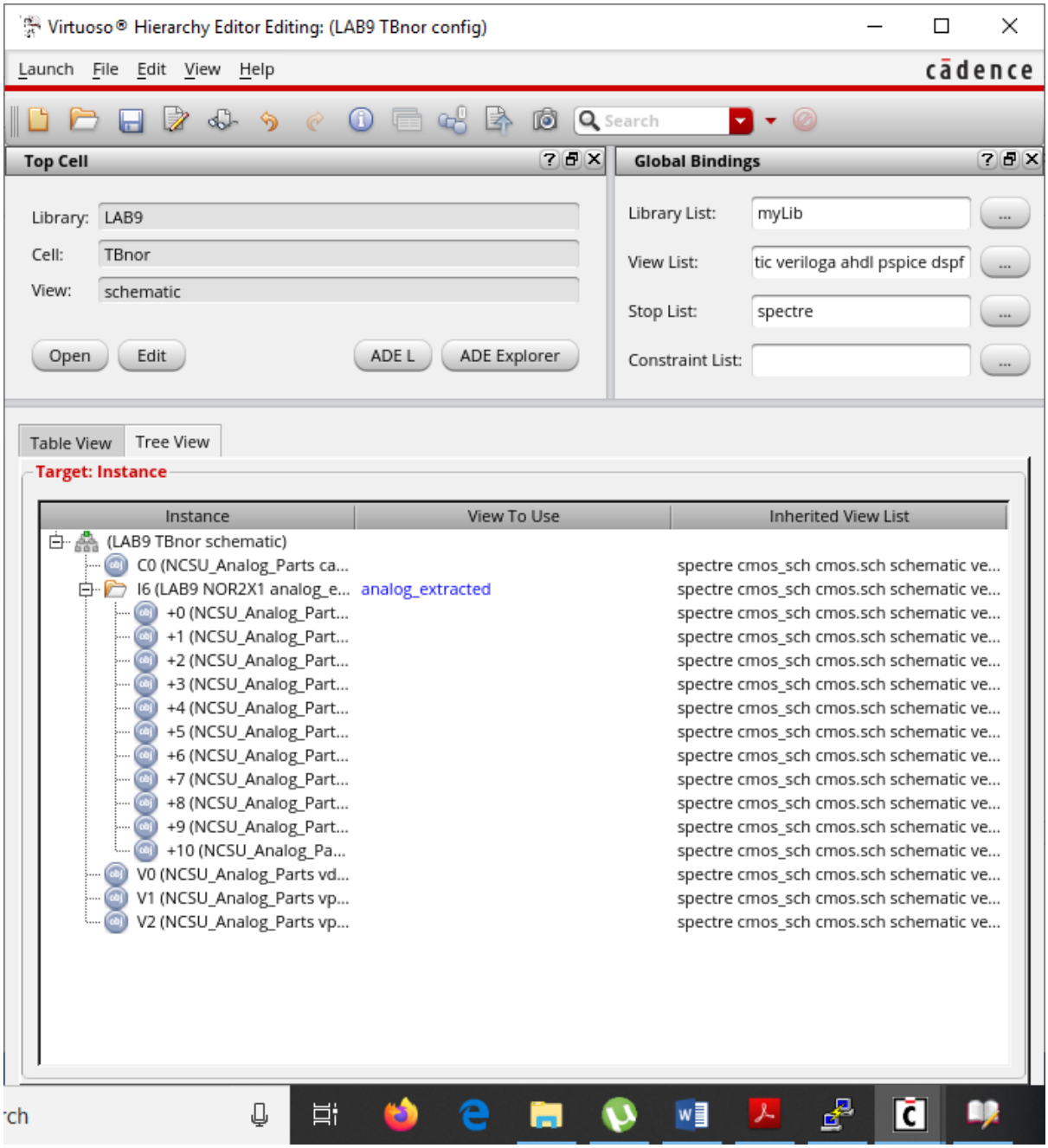
NOR2X1 analog_extracted view

3) Testing the TBnor and TBnand cells in config view



TBnor schematic





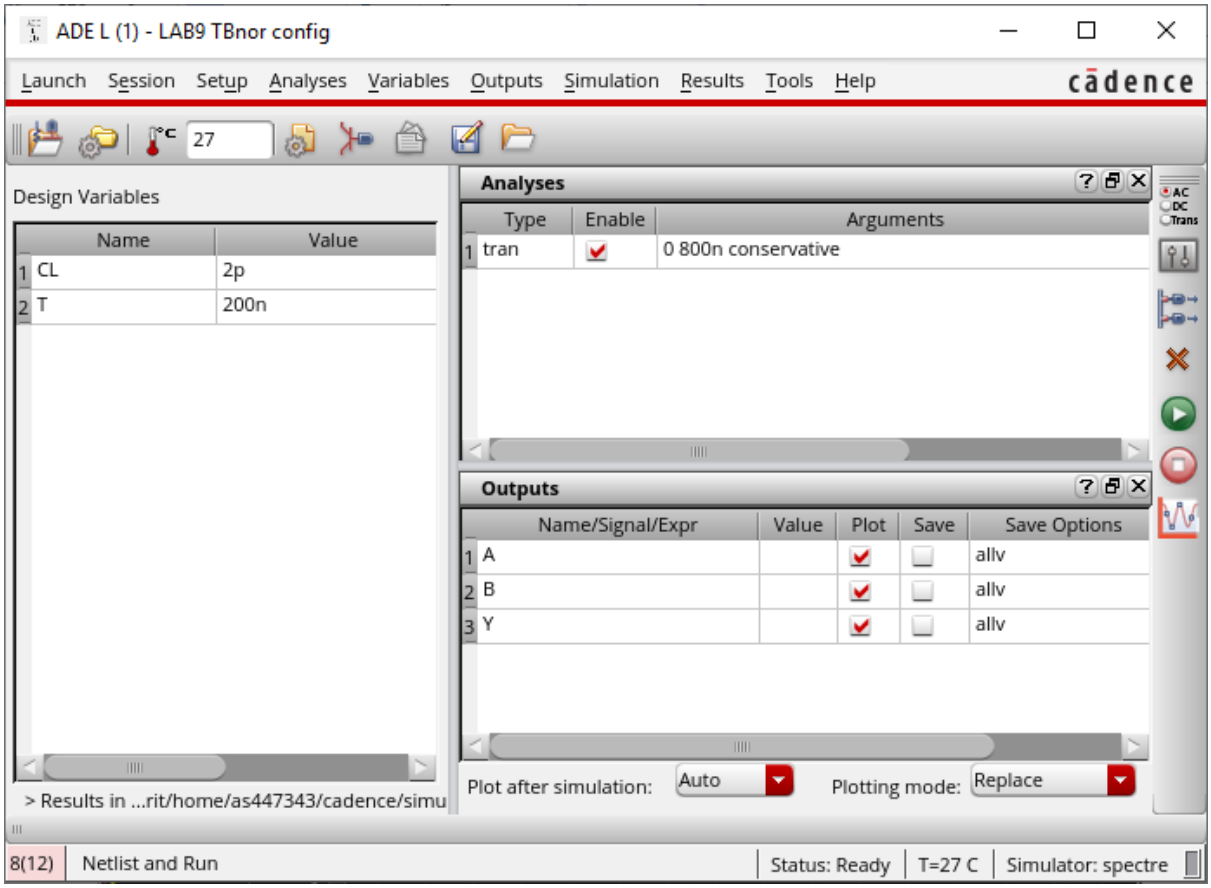
TBnor tree view

Now, we simulate the circuit with **CL = 2p** and **T = 200n**. I did trial runs for CL values from **1p to 10p** and T values from **50n to 500n**. This values seemed the perfect fit, where there is a noticeable propagation delay as well as the output reaching the final value comfortably.

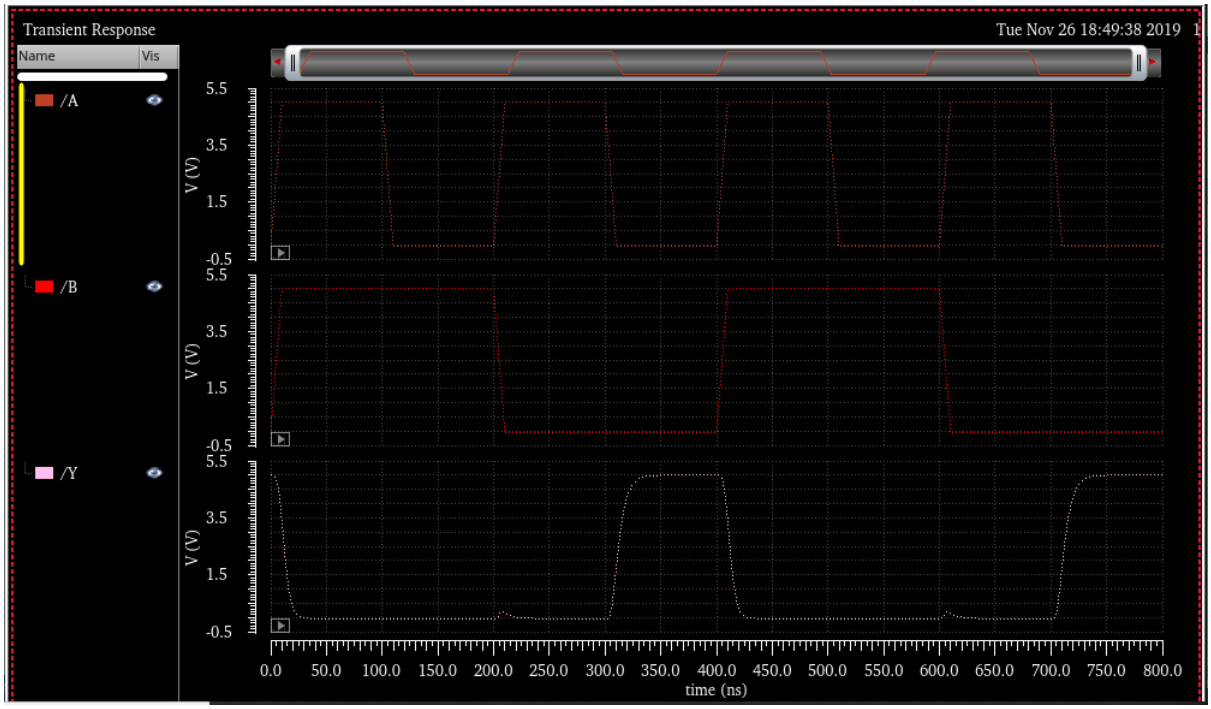
The input pulse signals are as follows:

A = delay – 0, fall time – 0.05*T, rise time – 0.05*T, pulse width – 0.45*T, period – T

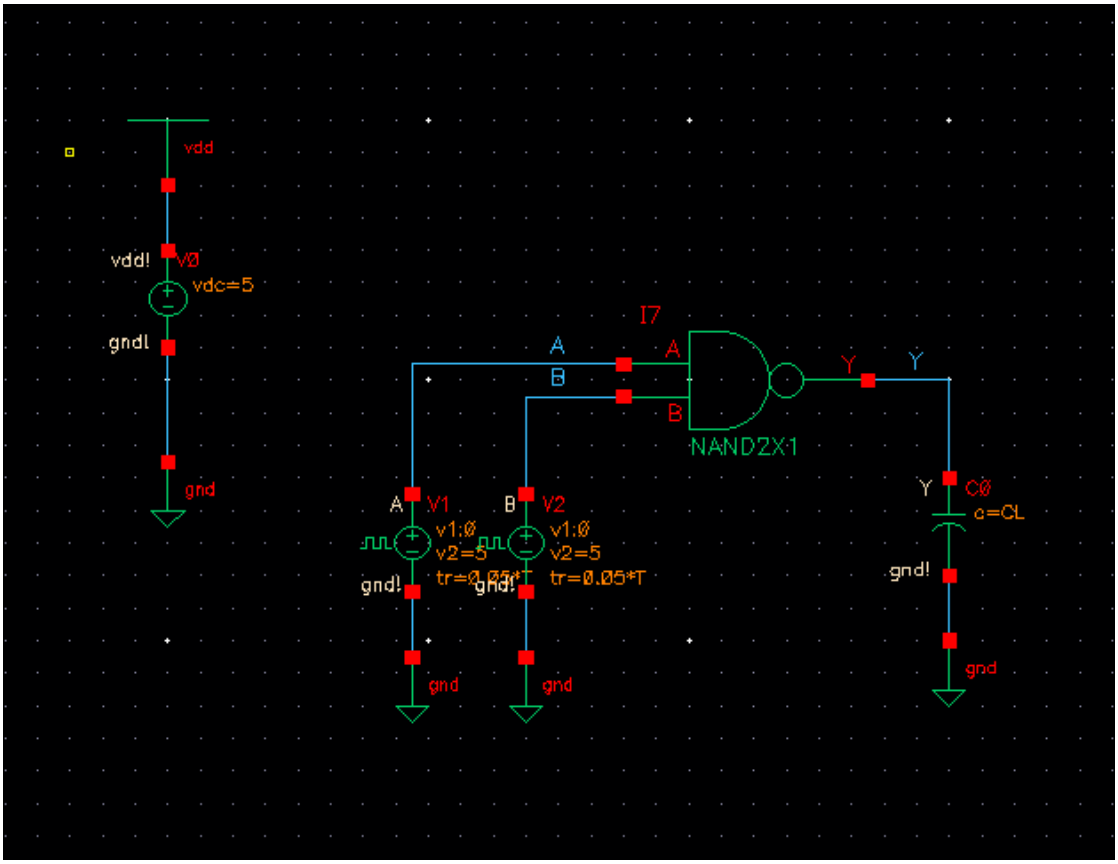
B = delay – 0, fall time – 0.05*T, rise time – 0.05*T, pulse width – 0.95*T, period – 2*T



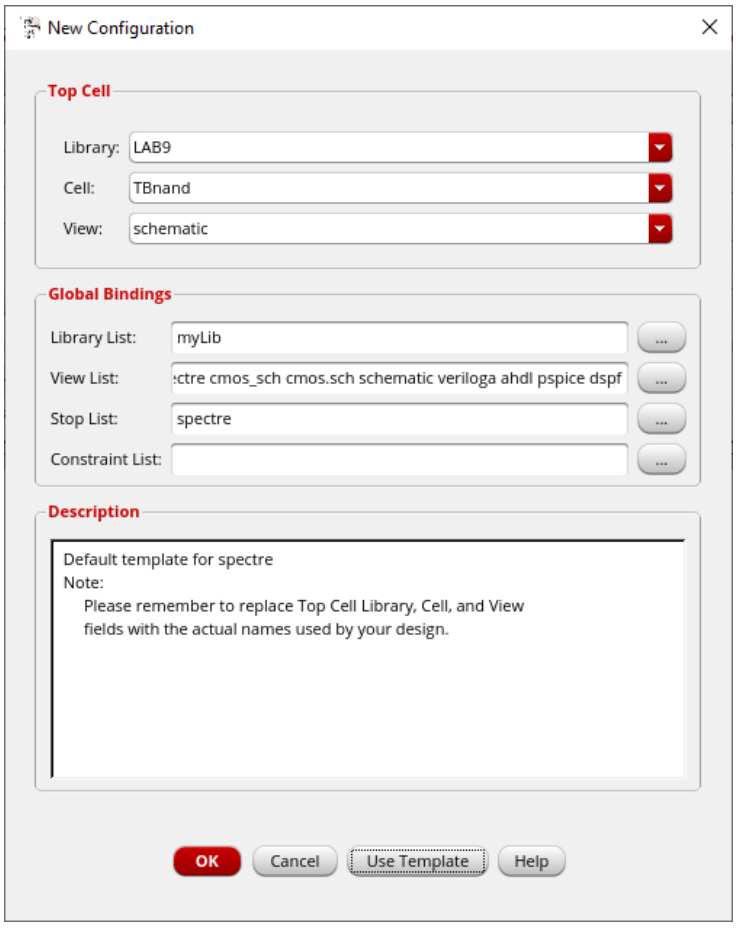
TBnor ADE L

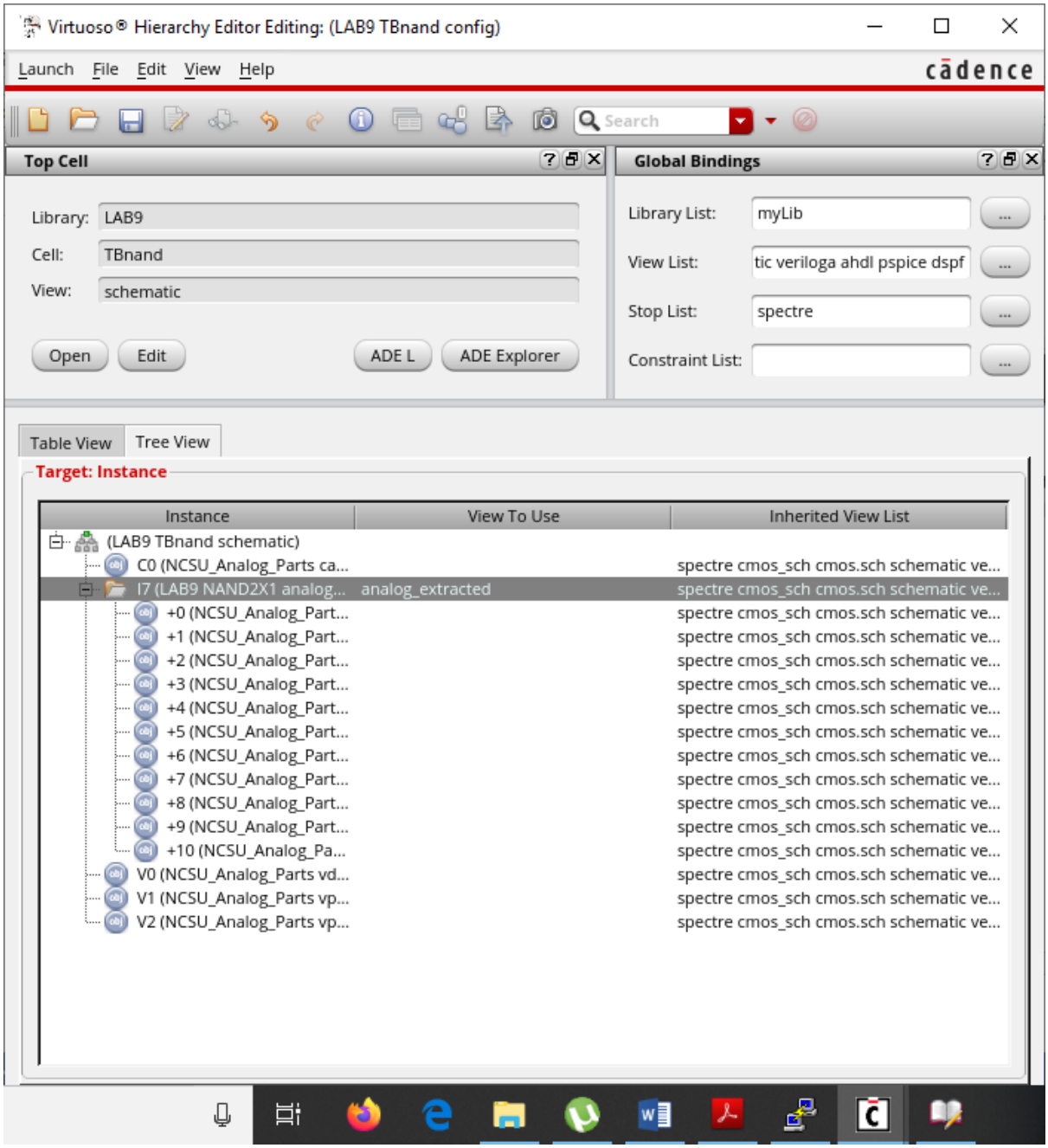


TBnor output waveform



TBnand schematic view





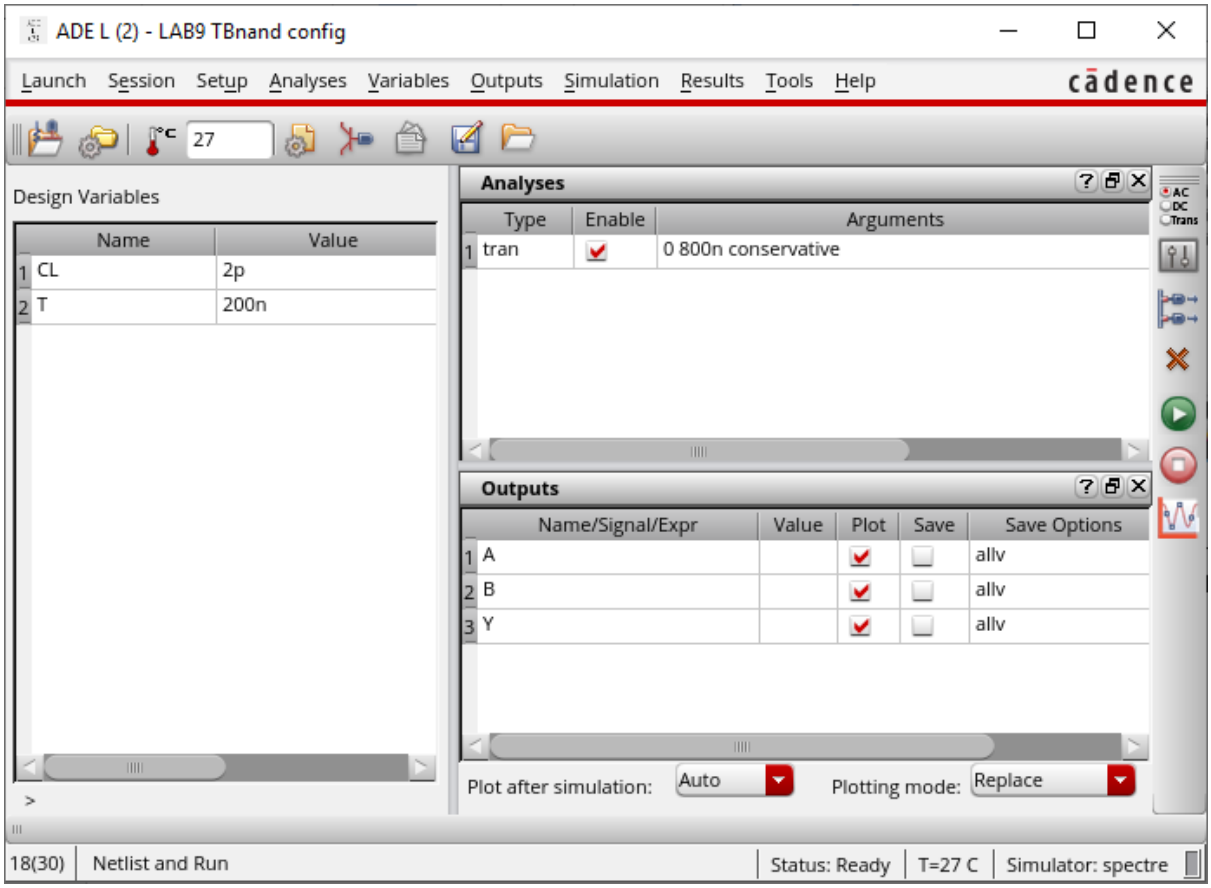
TBnand tree view

Now, we simulate the circuit with **CL = 2p** and **T = 200n**. I did trial runs for CL values from **1p to 10p** and T values from **50n to 500n**. This values seemed the perfect fit, where there is a noticeable propagation delay as well as the output reaching the final value comfortably.

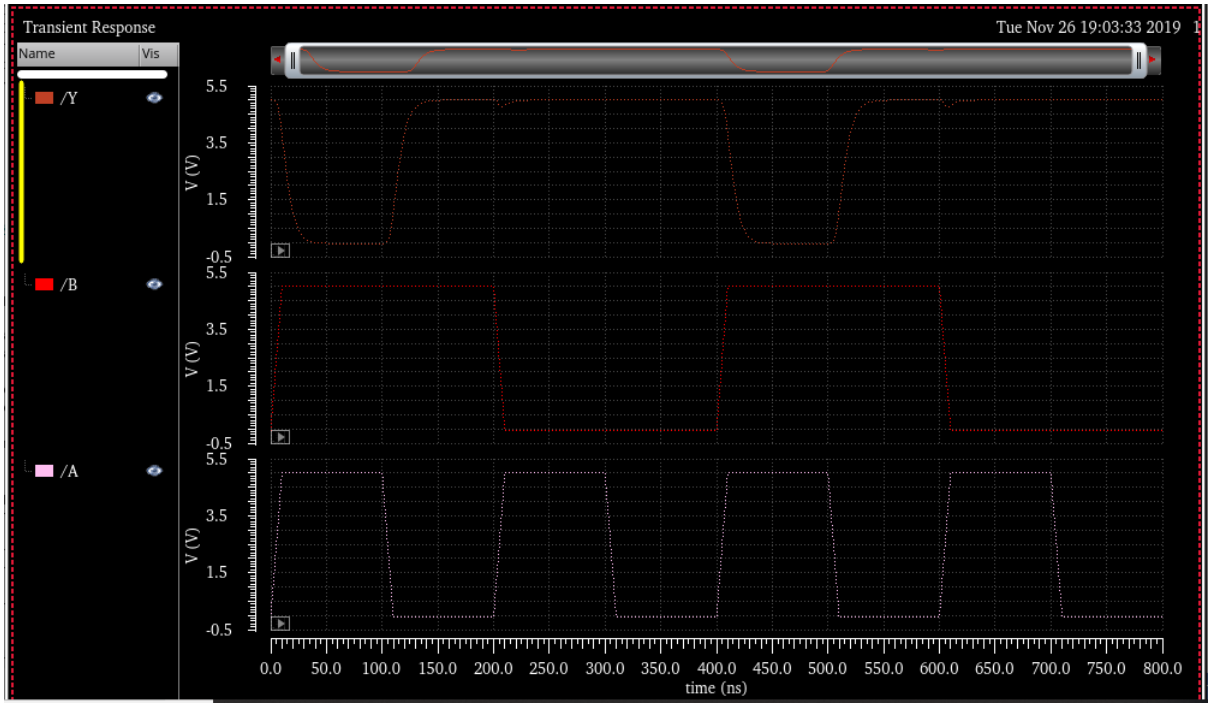
The input pulse signals are as follows:

A = delay – 0, fall time – 0.05*T, rise time – 0.05*T, pulse width – 0.45*T, period – T

B = delay – 0, fall time – 0.05*T, rise time – 0.05*T, pulse width – 0.95*T, period – 2*T



TBnand ADE L



TBnand output waveform