ECE520: Lab 6 Inverter layout and DRC

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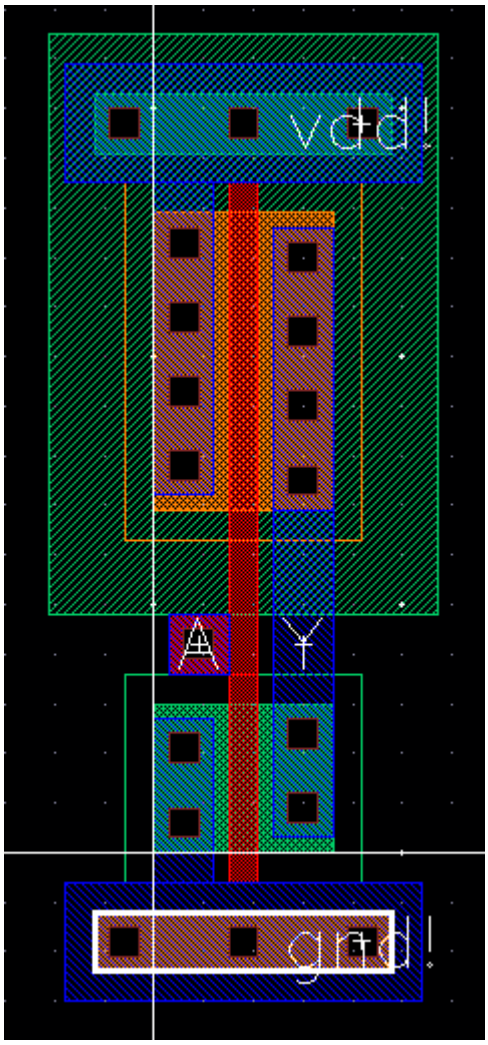
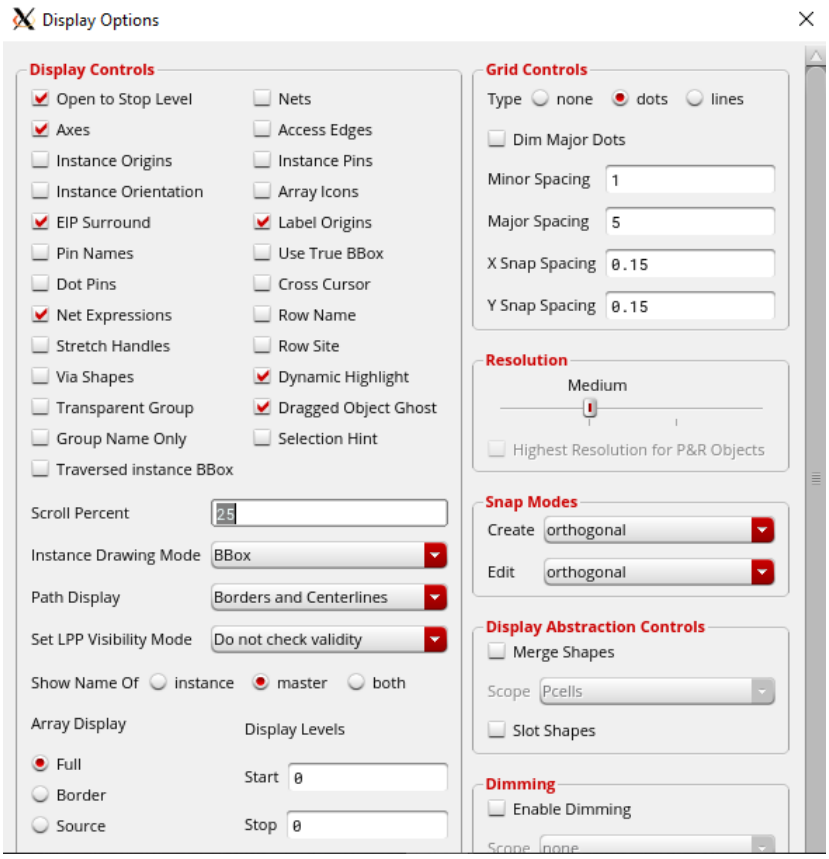
1) Drawing an inverter layout



This is what the final inverter layout should look like.

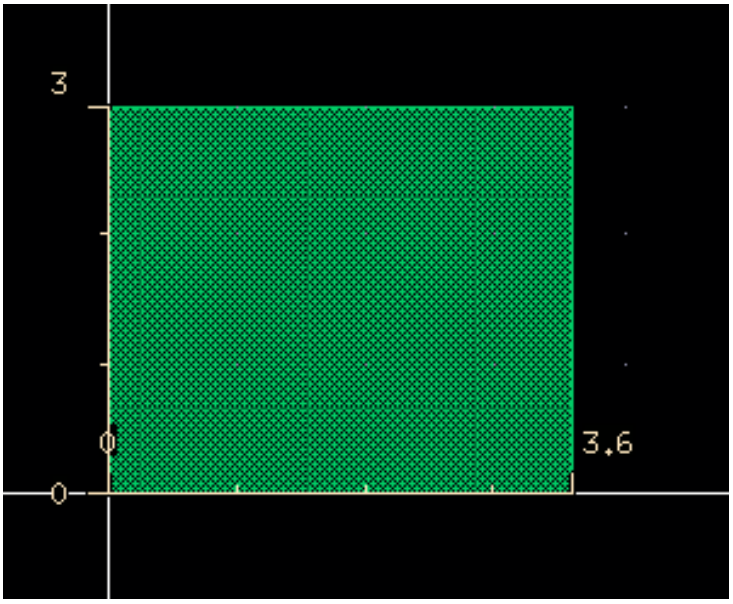
Step 1: Setting the display options (in terms of λ)



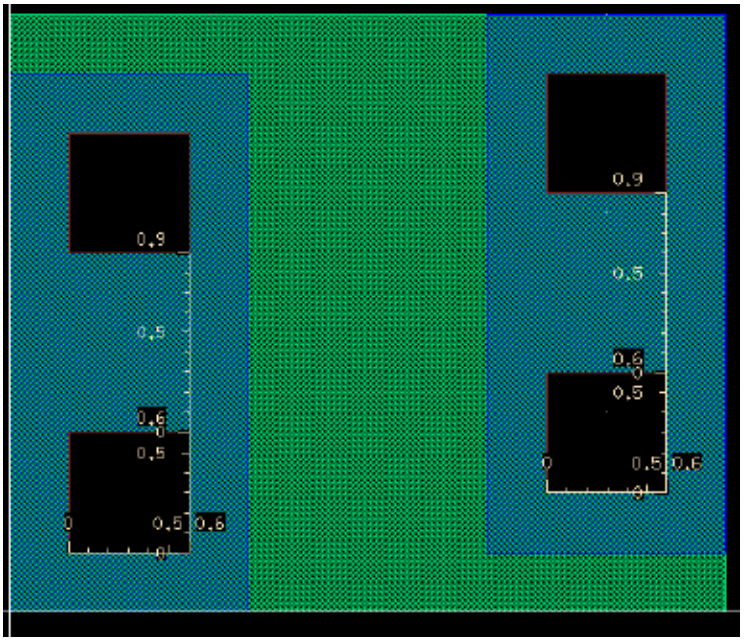
Step 2: Creating the nmos transistor

The dimensions are as follows: W = 3µm = 10λ L = 0.6µm = 2λ

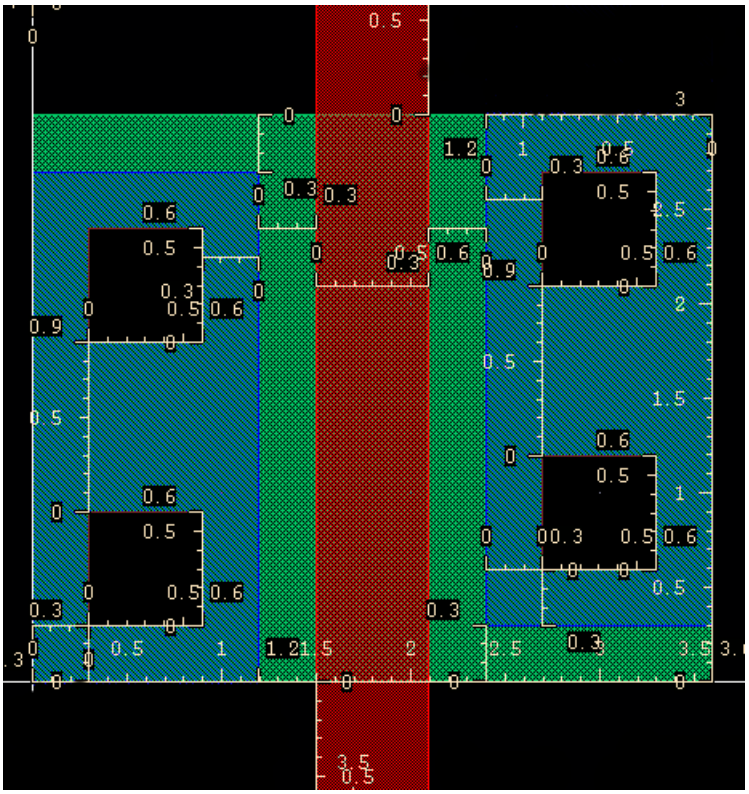
nactive layer: the sizes of the nactive layer should be 10λ x 12λ = 3.0µm x 3.6µm



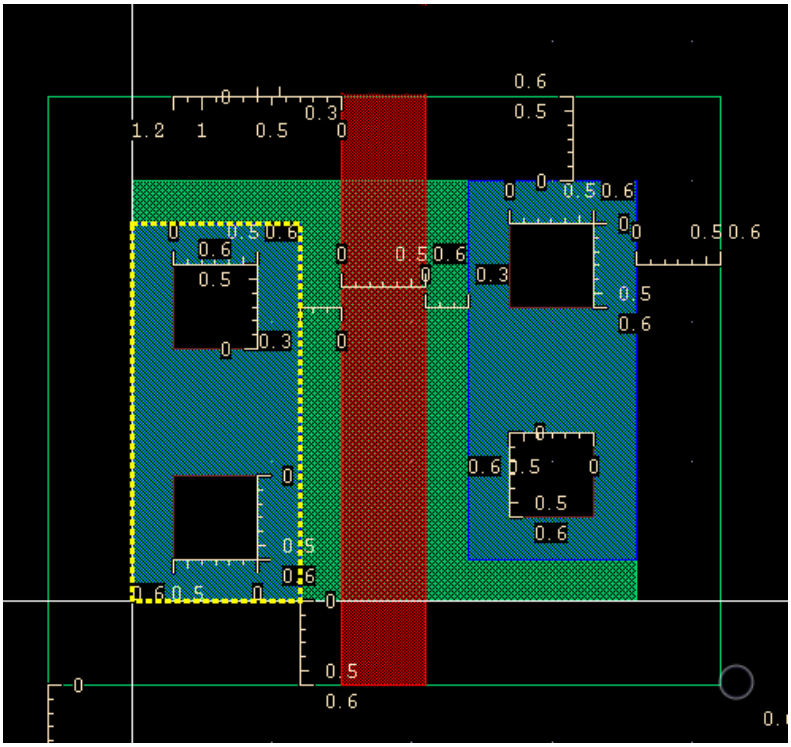
metal1 layer for Source (S) and Drain (D): As per the design rules, metal1 min. width is 4λ (1.2µm) and metal1-metal1 min. distance is also 4λ (1.2µm). Contacts inside the metal1 layer is 2λ x 2λ (0.6µm x 0.6µm).



poly layer: the sizes of the poly layer should be 2λ x 14λ = 0.6µm x 4.2µm



nselect layer: Because nactive is 10λ x 12λ, the nselect layer will be 14λ x 16λ.



Step 3: Creating the pmos transistor

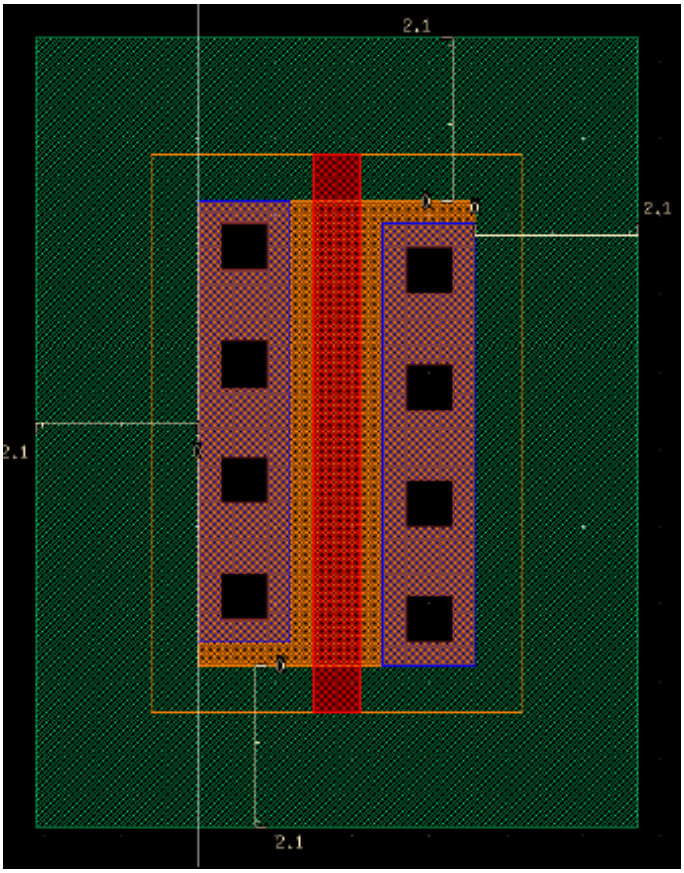
pactive dimensions are: 20λ x 12λ = 6.0µm x 3.6µm,

metal1: The distance between two metal1 layers is 4λ minimum, while each metal1 is 4 λ wide: source (S) and drain (D). While both the S and D connection metal1 layers will be 19λ x 4λ, the pactive is 20λ.

poly: The rules for poly are identical. It should be 2λ wide and 1λ away from both metal1 layers.

pselect: rules for this are identical. A 2λ overhang from both sides of the pactive is necessary.

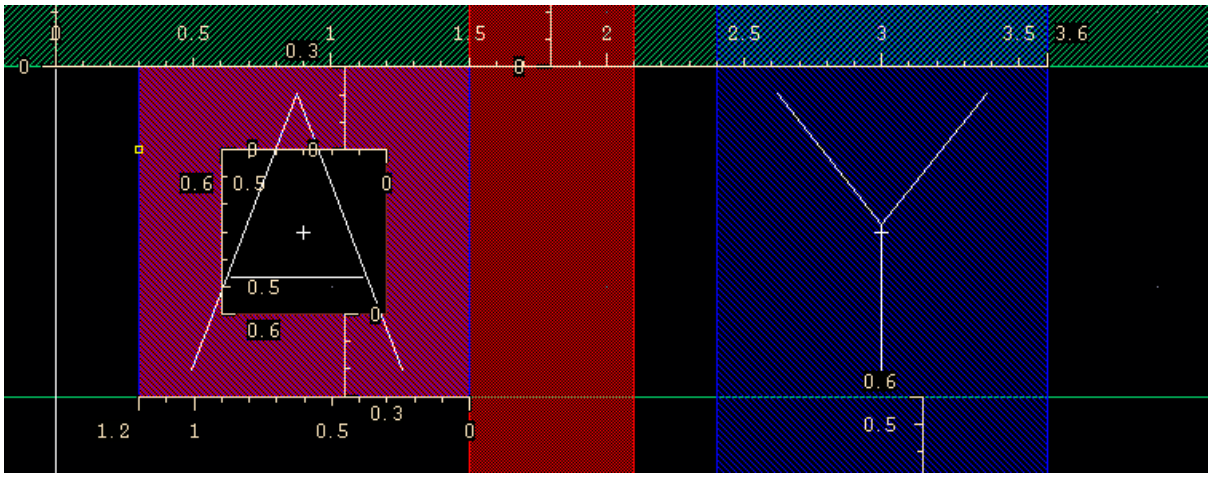
nwell: The nwell should cover the pactive by 7λ (2.1 µm). So, the nwell will be 34λ x 26λ = 10.2µm x 7.8µm.



Step 4: Creating the input (A) and output (Y) pins

Creating the input (A) pin - a 4λ x 4λ poly layer, connected to the up-down long poly; a 4λ x 4λ metal1 layer, which is occupying exactly the same area as the poly; and a 2λ x 2λ contact (cc) that is exactly in the middle of this 4λ x 4λ.

Creating the output (Y) pin - The output pin is the metal1 on the right side of both transistors, which is made by stretching the metal1 above and shorting it to the one below.

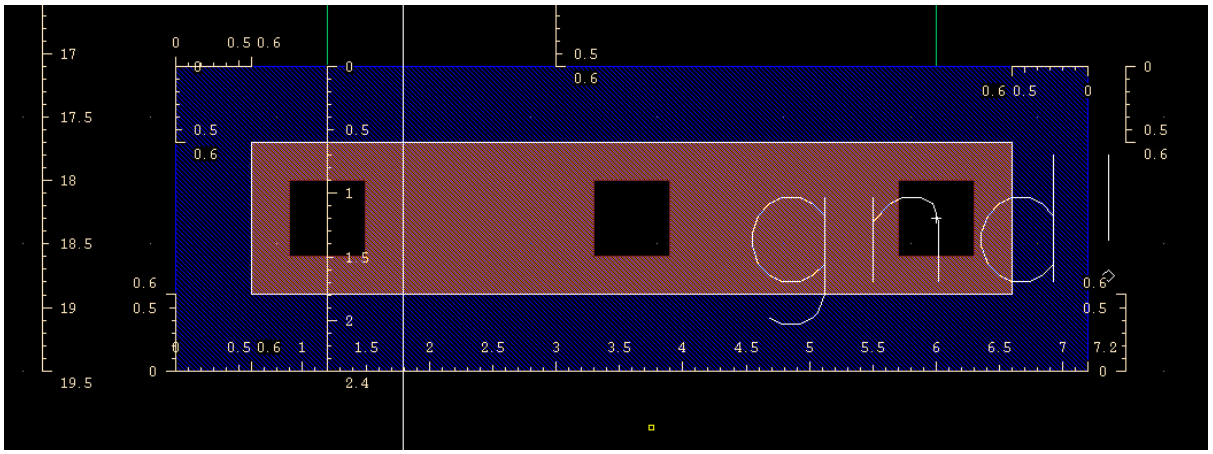


Input A

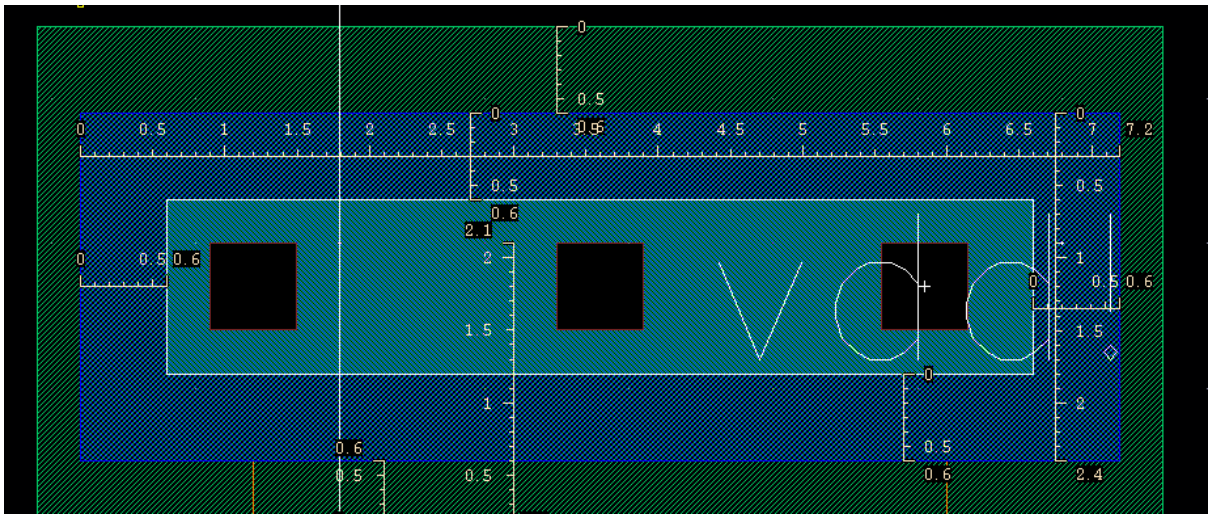
Output Y

Step 5: Creating the vdd! And gnd! for the transistors

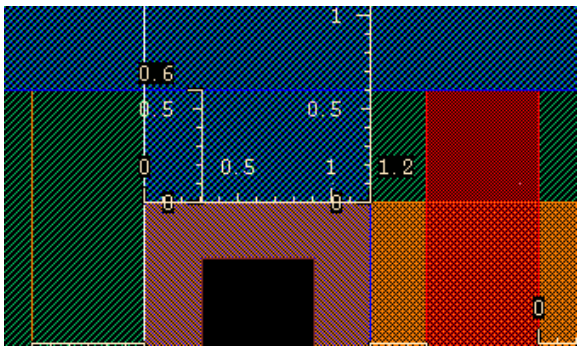
Creating the gnd! - metal1 layer on the bottom to create the gnd! rail, 24λ x 8λ = 7.2µm x 2.4µm with pactive layer of 20λ x 4λ (6µm x 1.2µm) inside it and 3 contacts to connect metal1 (gnd!) and pactive.

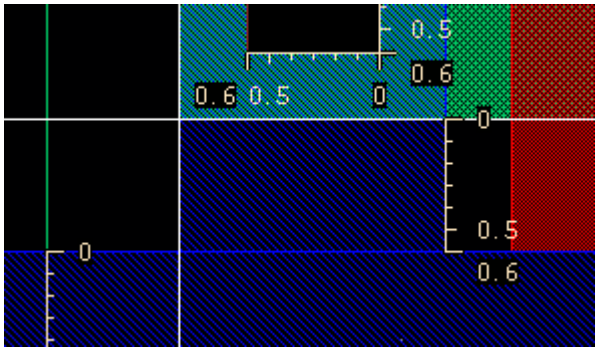


Creating the vdd! - metal1 layer on top to create the vdd! rail also 24λ x 8λ = 7.2µm x 2.4µm with nactive layer of 20λ x 4λ (6µm x 1.2µm) inside it and 3 contacts to connect metal1 (vddd!) and nactive.



Making the connections - Stretching the metal1, connected to the source (S) of pmos above to connect to the vdd! rail and the same for the source (S) connection of the nmos on the bottom, stretching it to touch the gnd! rail.





vdd! connection

gnd! connection

Step 6: Labelling the layout -

- vdd! -upper supply rail
- gnd! - lower supply rail
- A - inverter input
- Y - inverter output

2) DRC: Design Rule Checking

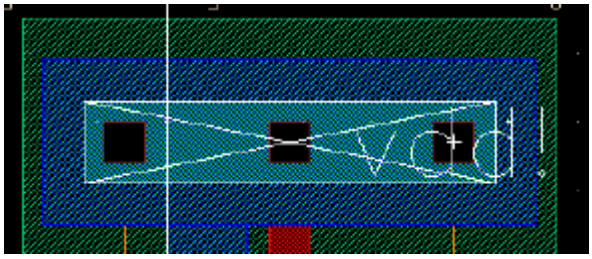
The design rule files are copied into the working directory:

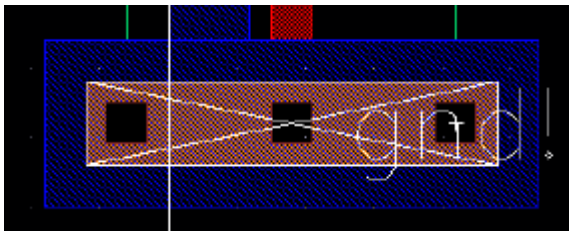
~/cadence/TechLibs/ncsu-cdk-1.6.0.beta/lib/NCSU_TechLib_ami06

The bash commands used to do the same are:

```
-bash-4.2$ cp /network/rit/home/as447343/cadence/TechLibs/ncsu-cdk-1.6.0.beta/techfile/divaDRC.rul /network/rit/home/as447343/cadence/TechLibs/ncsu-cdk-1.6.0.beta/lib/N
CSU_TechLib_ami06
-bash-4.2$ cp /network/rit/home/as447343/cadence/TechLibs/ncsu-cdk-1.6.0.beta/techfile/divaEXT.rul /network/rit/home/as447343/cadence/TechLibs/ncsu-cdk-1.6.0.beta/lib/N
CSU_TechLib_ami06
-bash-4.2$ cp /network/rit/home/as447343/cadence/TechLibs/ncsu-cdk-1.6.0.beta/techfile/divaLVS.rul /network/rit/home/as447343/cadence/TechLibs/ncsu-cdk-1.6.0.beta/lib/N
CSU_TechLib_ami06
-bash-4.2$ cd ~/cadence/TechLibs/ncsu-cdk-1.6.0.beta/lib/NCSU_TechLib_ami06
-bash-4.2$ LS
-bash: LS: command not found
-bash-4.2$ ls
active       divaDRC.rul  elec             M1_ELEC  m1_p     M1_POLY  m3_m2   metal2   NCSU_TechLib_ami06.layermap  nmos  nwell    poly            sym_pins.Cat
cdsinfo.tag  divaEXT.rul  layout_macros.Cat  m1_n     M1_P     m2_m1    M3_M2   metal3   NCSU_TechLib_ami06.TopCat    ntap  pactive  ptap            tech.db
data.dm      divaLVS.rul  m1_elec          M1_N     m1_poly  M2_M1    metal1  nactive  NCSU_TechLib_ami06.TopCat%   NTAP  pmos     sym_contacts.Cat
-bash-4.2$
```

The design is verified by Verify->DRC. It returns 2 errors as follows:



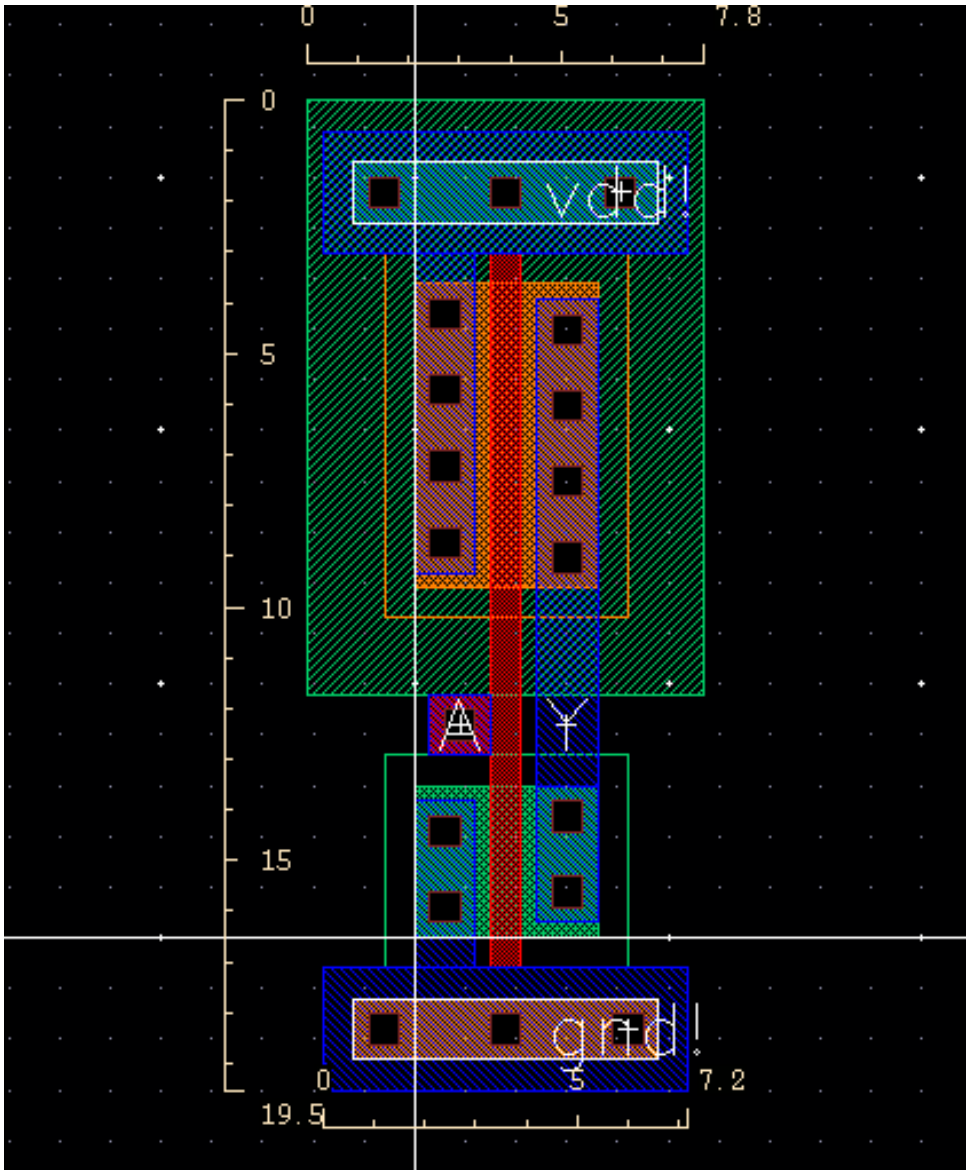


```
DRC started.......Sat Nov  2 16:03:16 2019
    completed ....Sat Nov  2 16:03:16 2019
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********  Summary of rule violations for cell "inverter layout"  *********
 # errors  Violated Rules
        2  (DBM Rule 1.1) Active must be inside select
        2  Total errors found
```

These errors tell us that the active regions must be surrounded by select regions.

- The pactive below (in the nmos) must be surrounded by pselect.
- The nactive below (in the pmos) must be surrounded by nselect.

After drawing the select regions, DRC is run again and returns no error. Hence the design is successful.




```
DRC started.......Sat Nov  2 16:14:48 2019
    completed ....Sat Nov  2 16:14:48 2019
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "inverter layout"   *********
   Total errors found: 0
```