ECE520 Introduction to VLSI, Project 3

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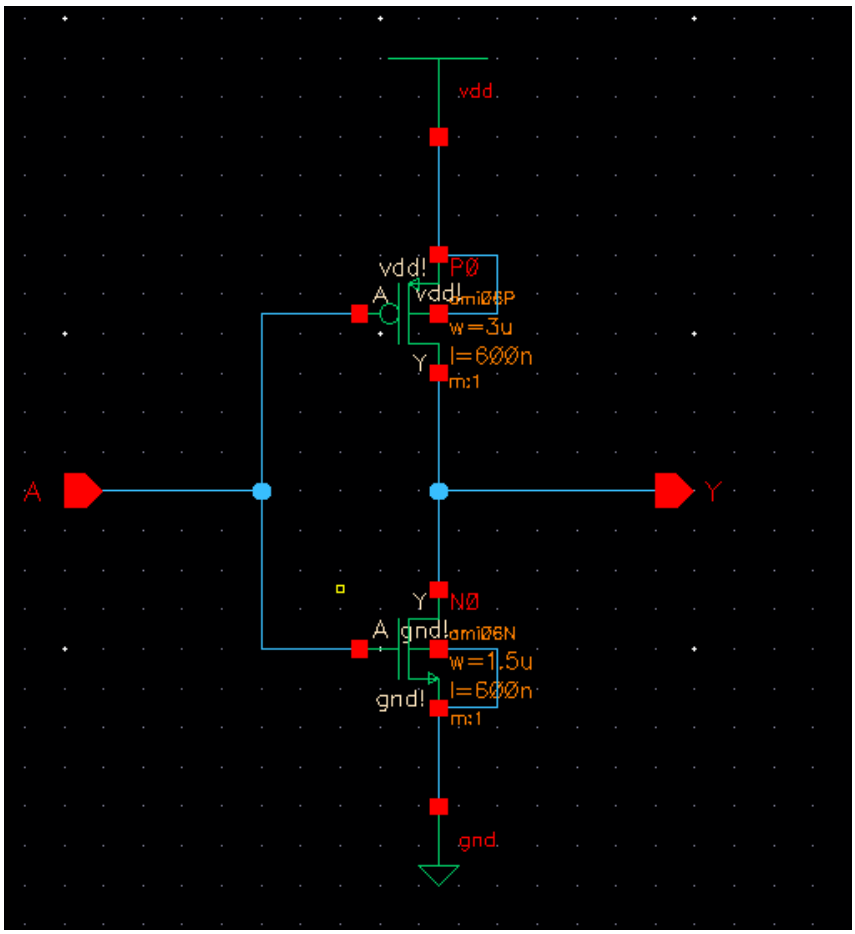
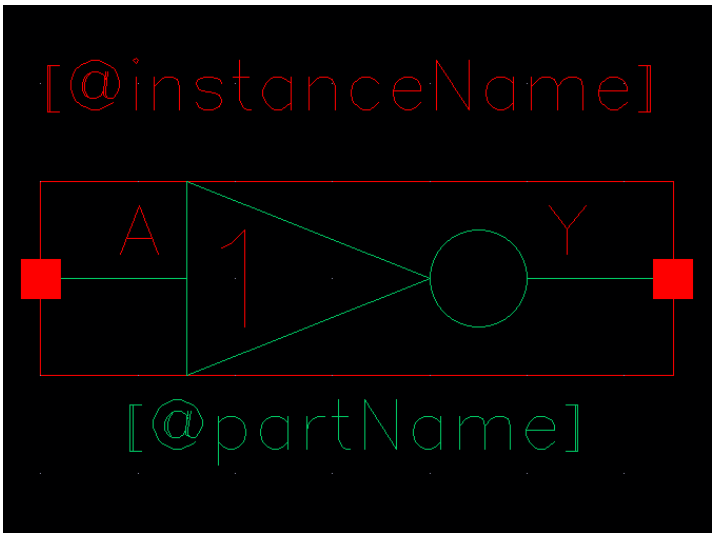
PART A

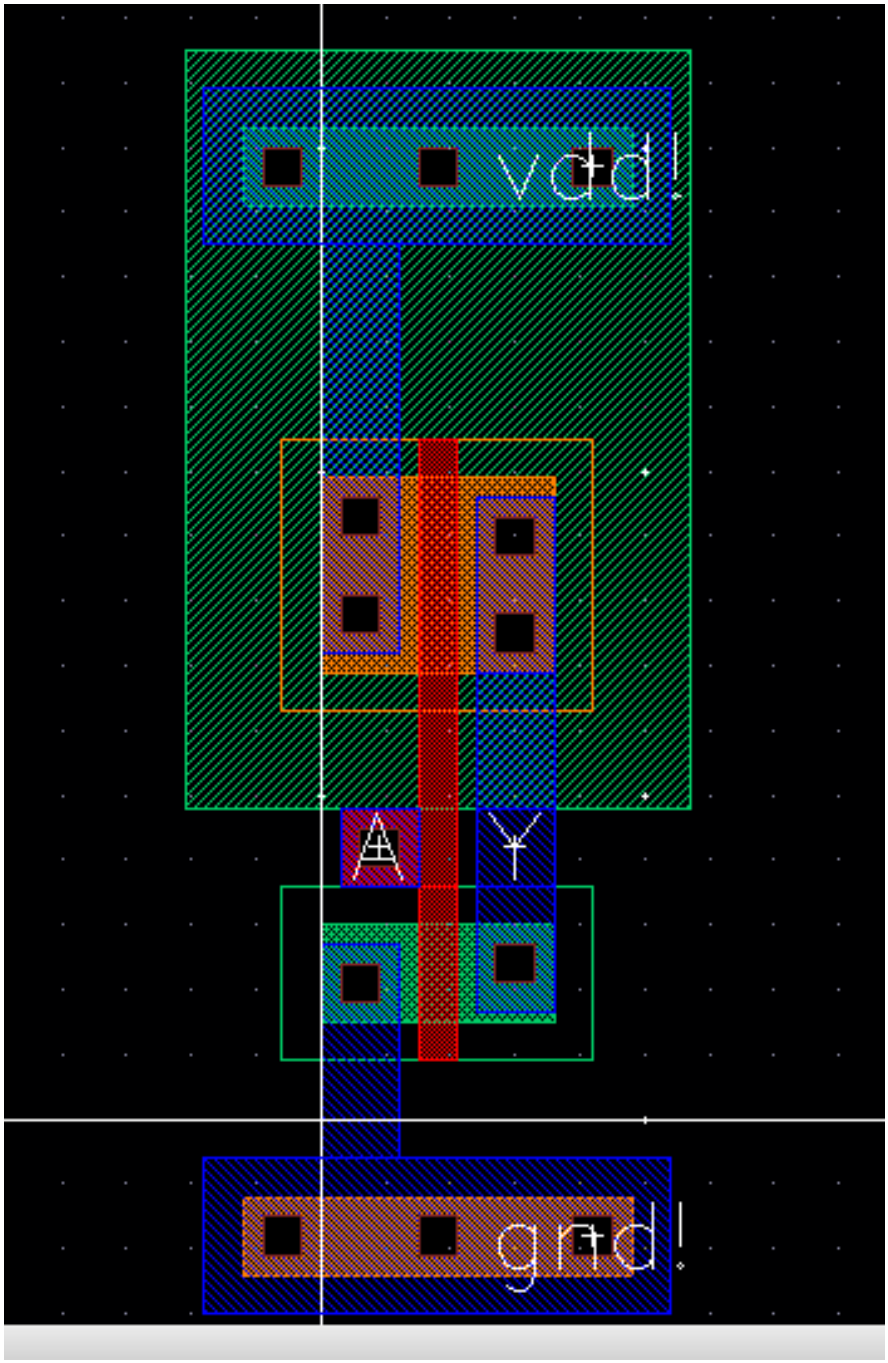
INVX1:



INVX1 Schematic

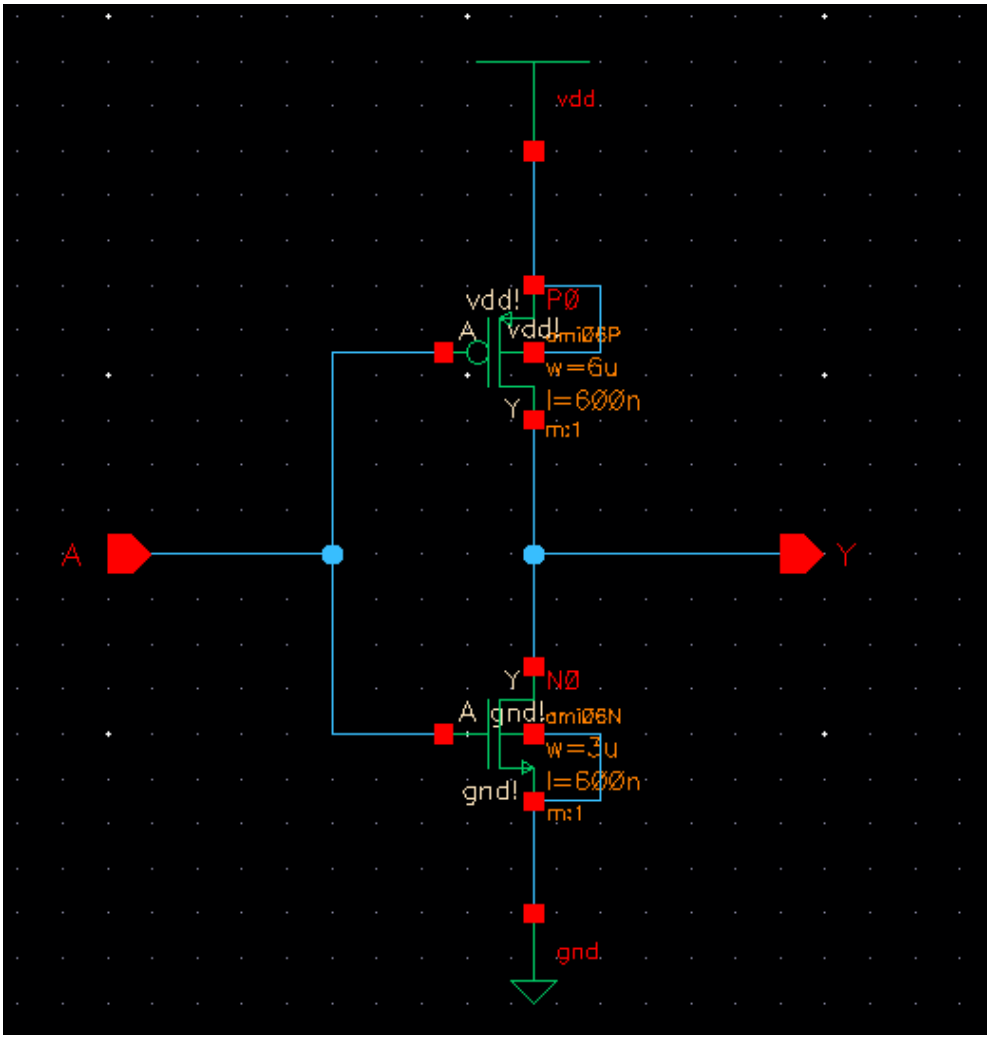


INVX1 Symbol

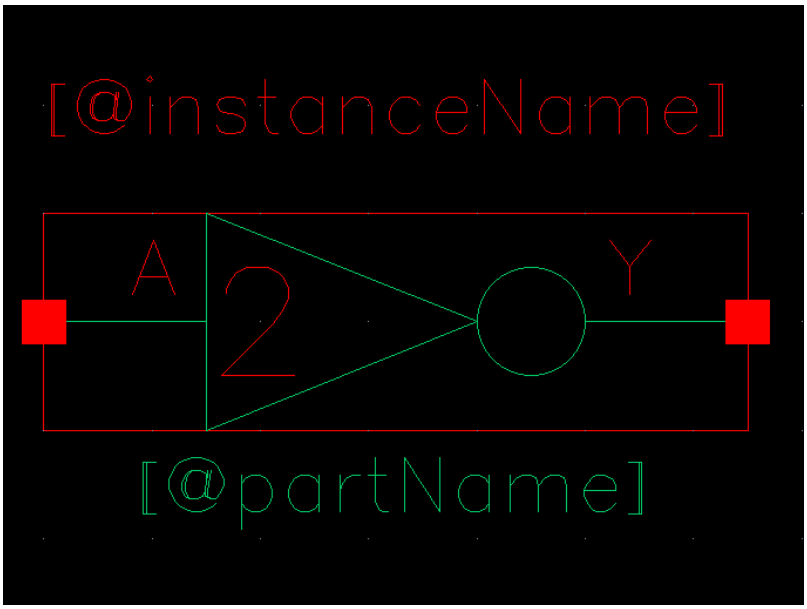


INVX1 Layout

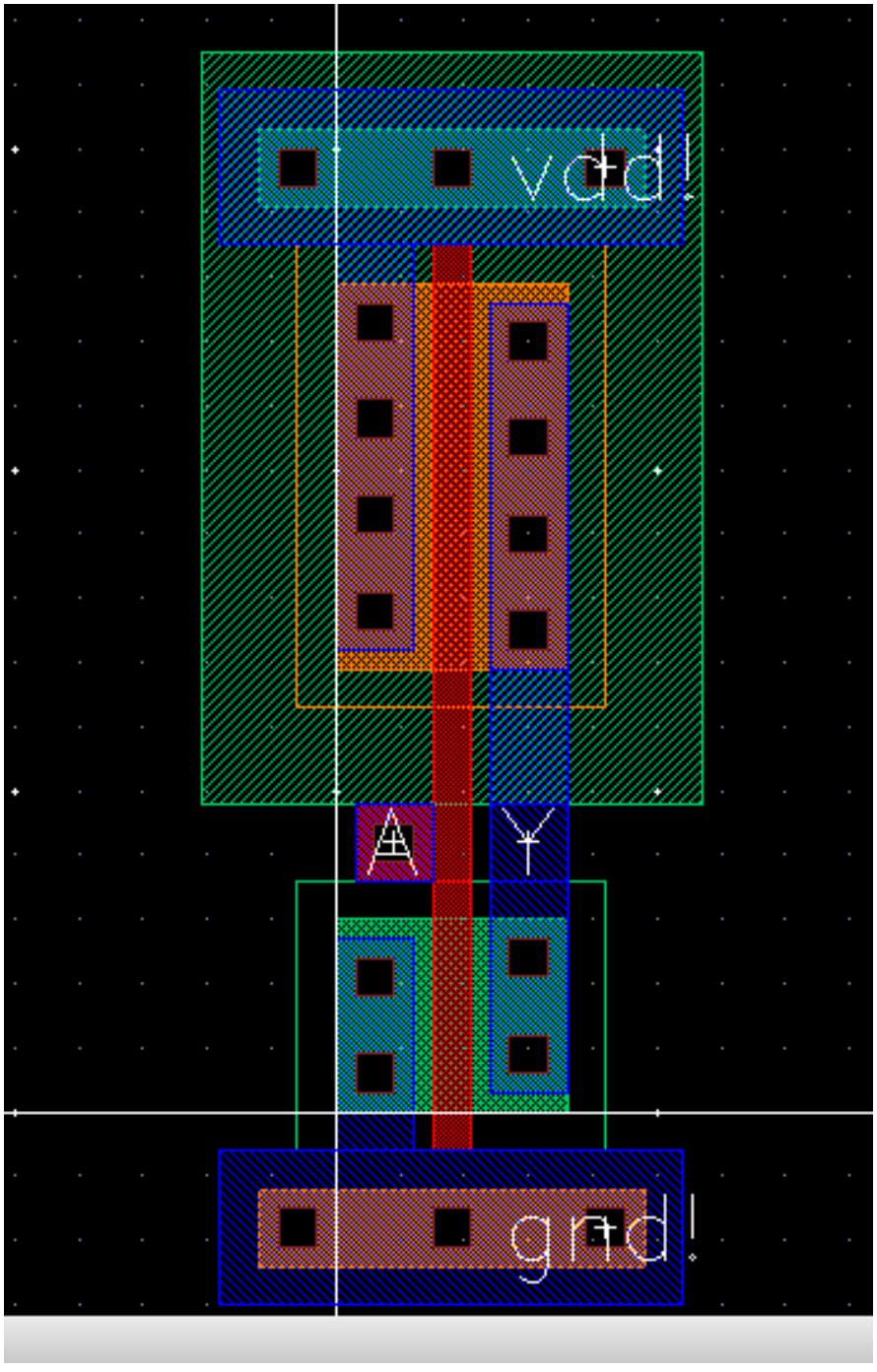
INVX2:



INVX2 Schematic

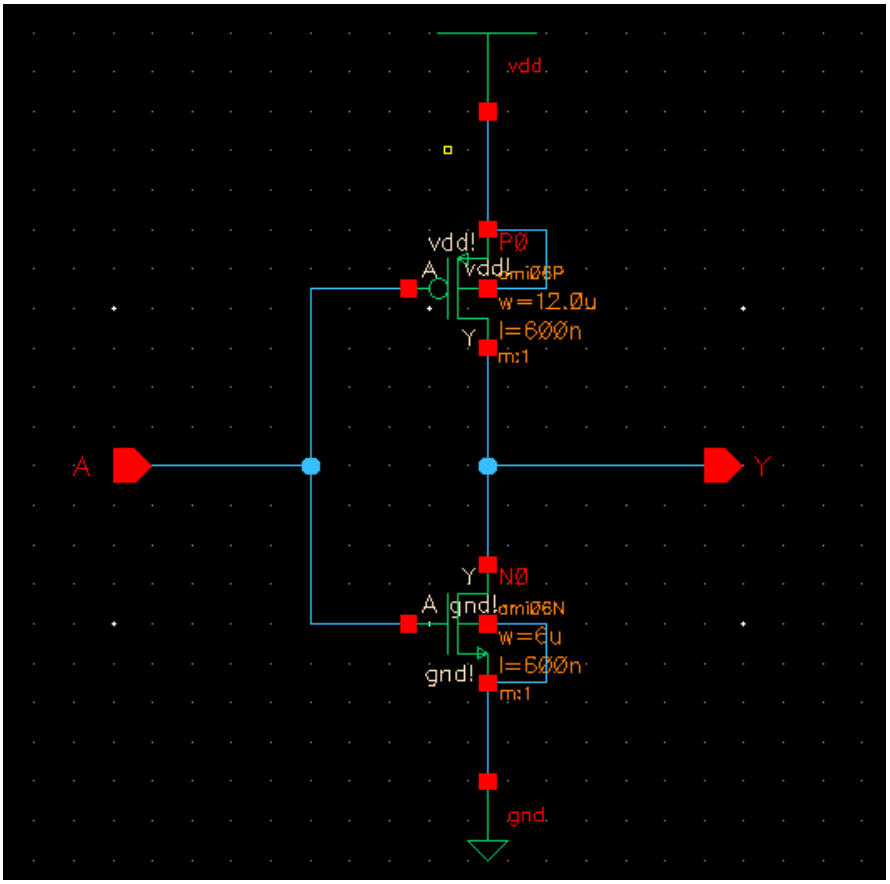


INVX2 Symbol

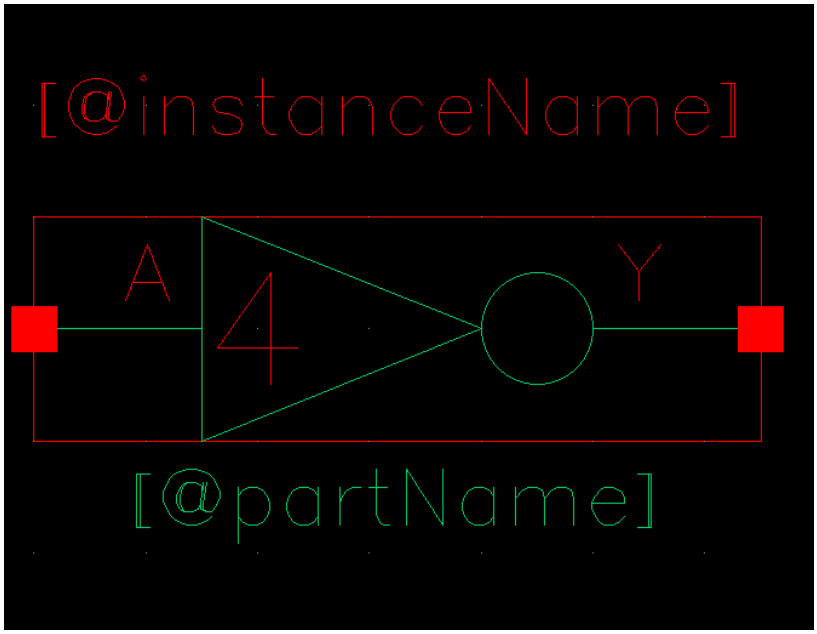


INVX2 Layout

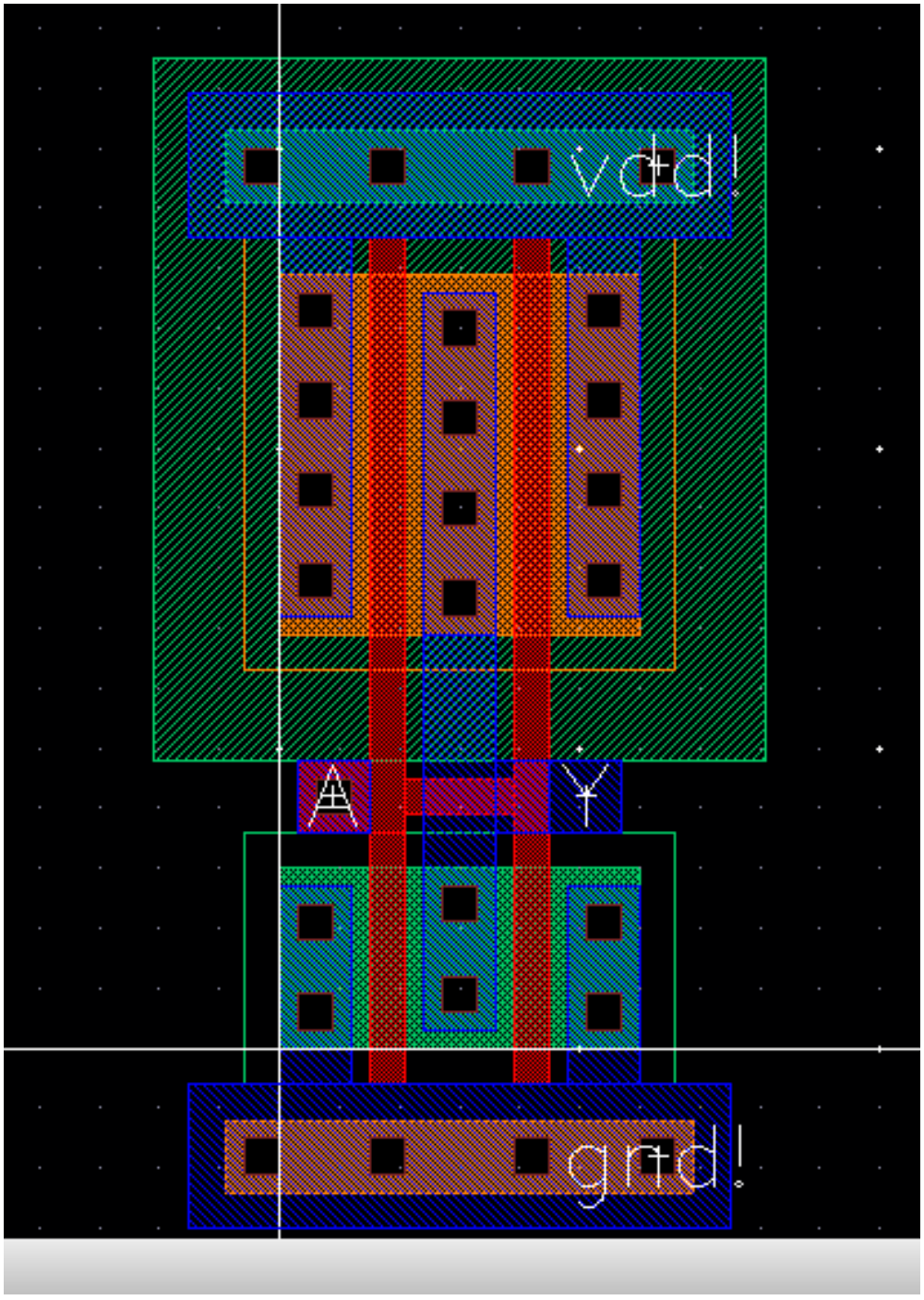
INVX4:



INVX4 Schematic



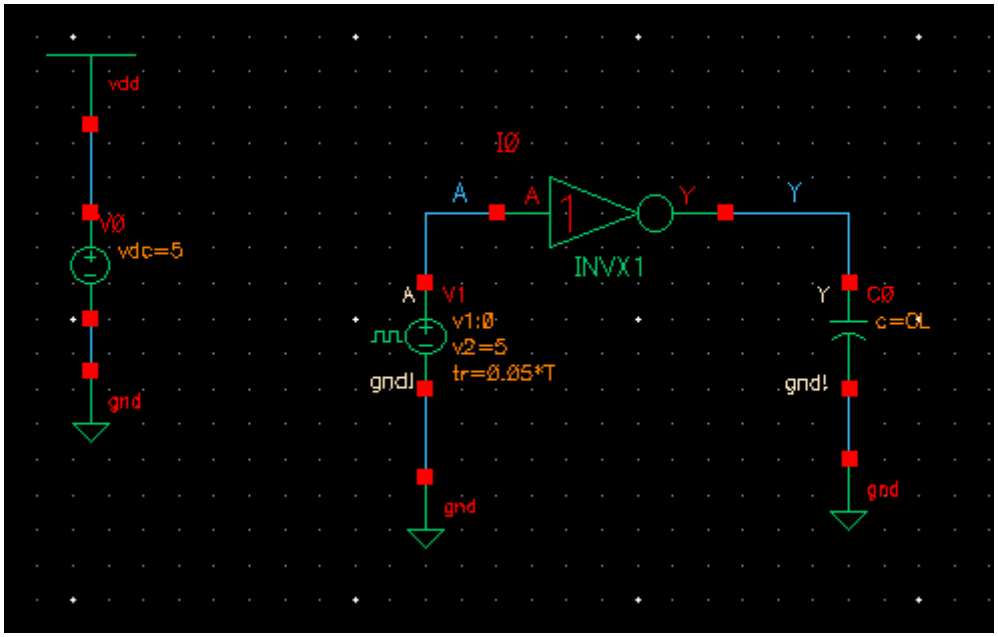
INVX4 Symbol



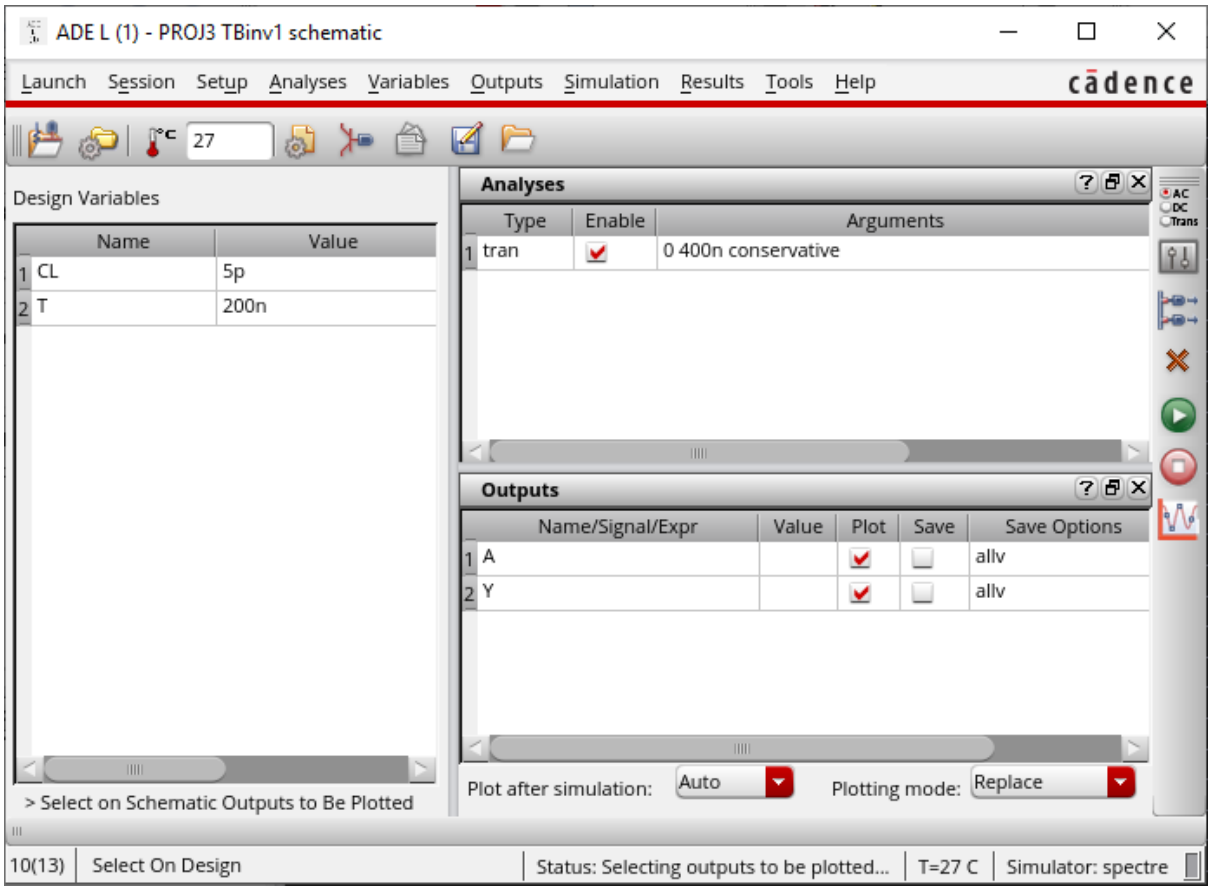
INVX4 Layout

PART B

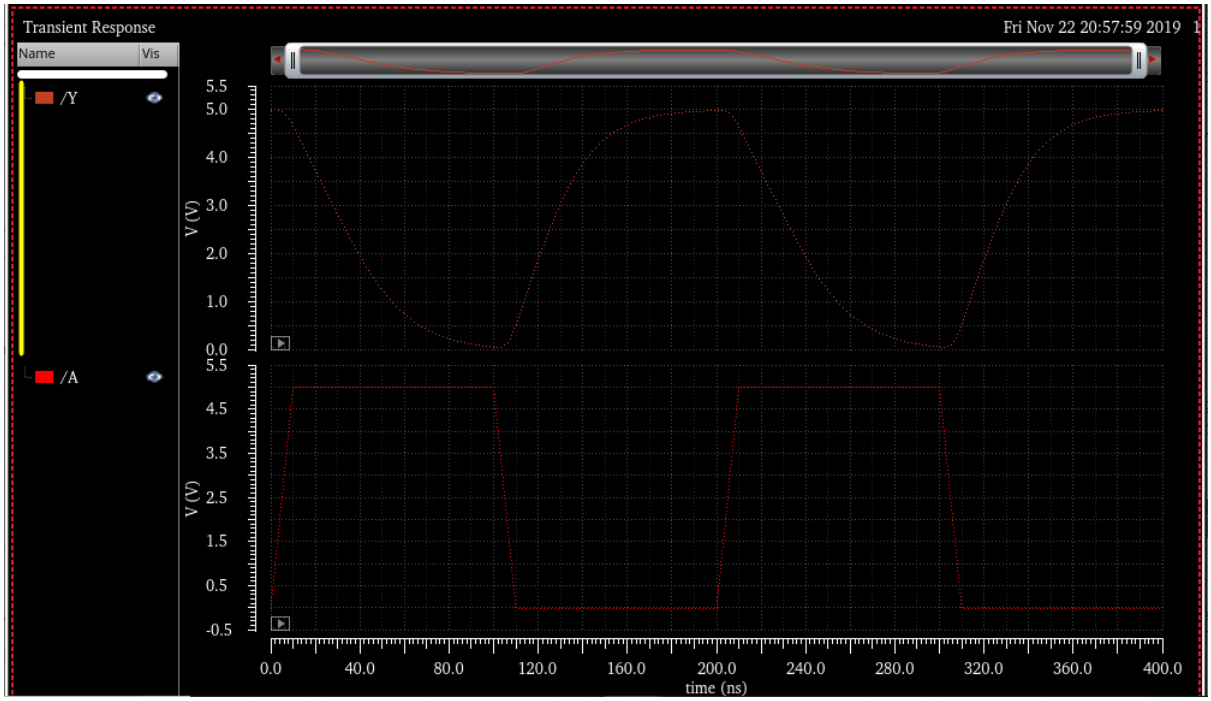
TBinv1:



TBinv1 schematic



TBinv1 ADE L

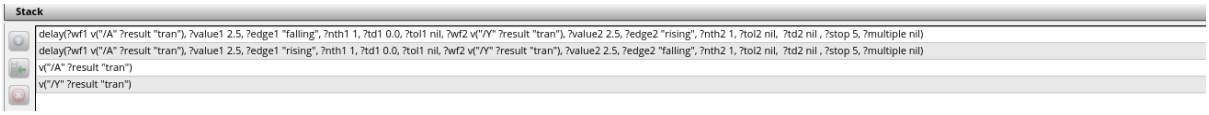


TBinv1 output

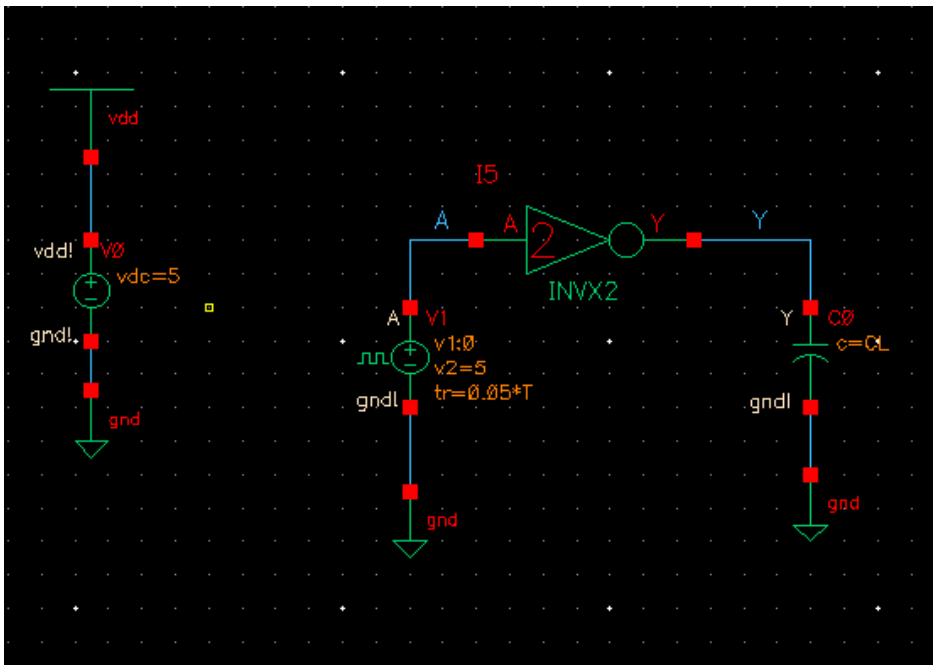
Propagation delays:

t_{pdr} (A -> Y) = 28.7E-9 = **28.7ns**

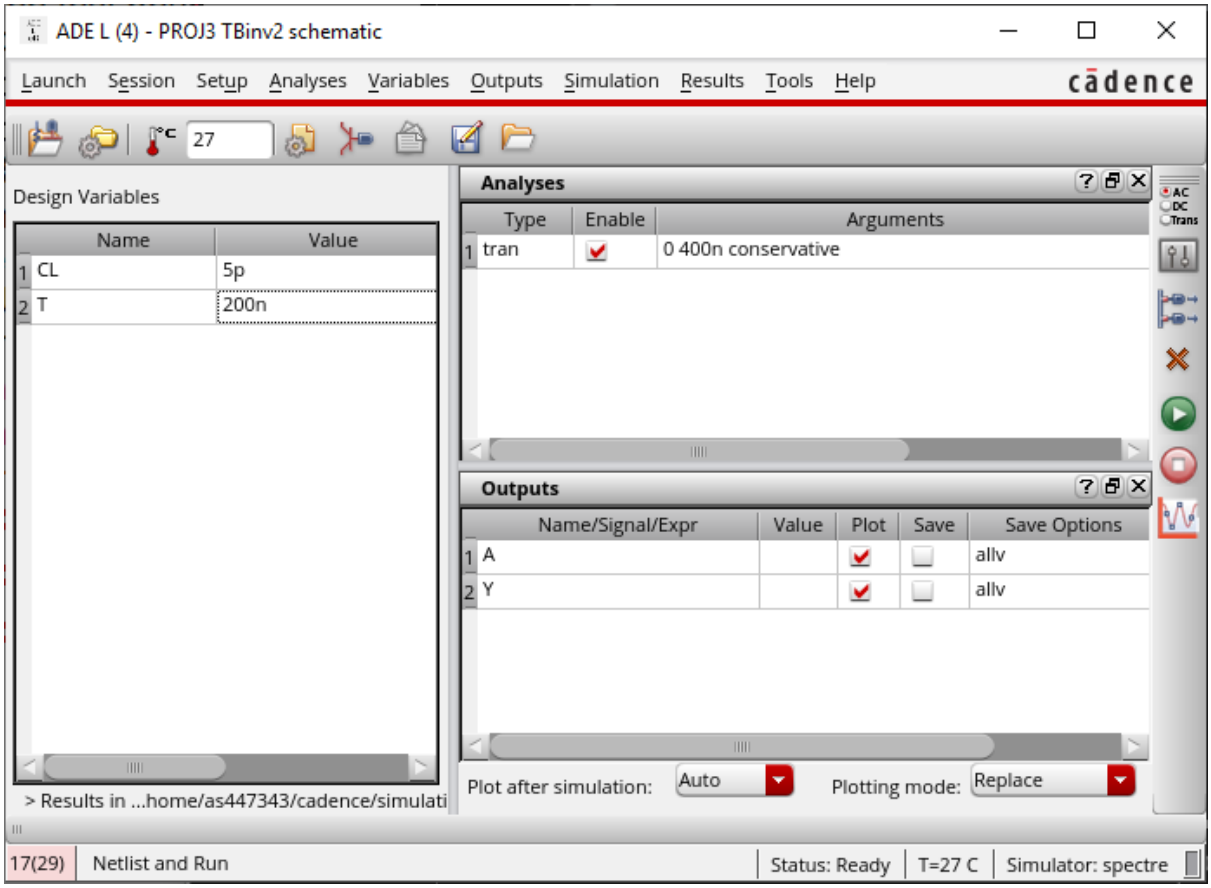
t_{pdf} (A -> Y) = 19.94E-9 = **19.94ns**



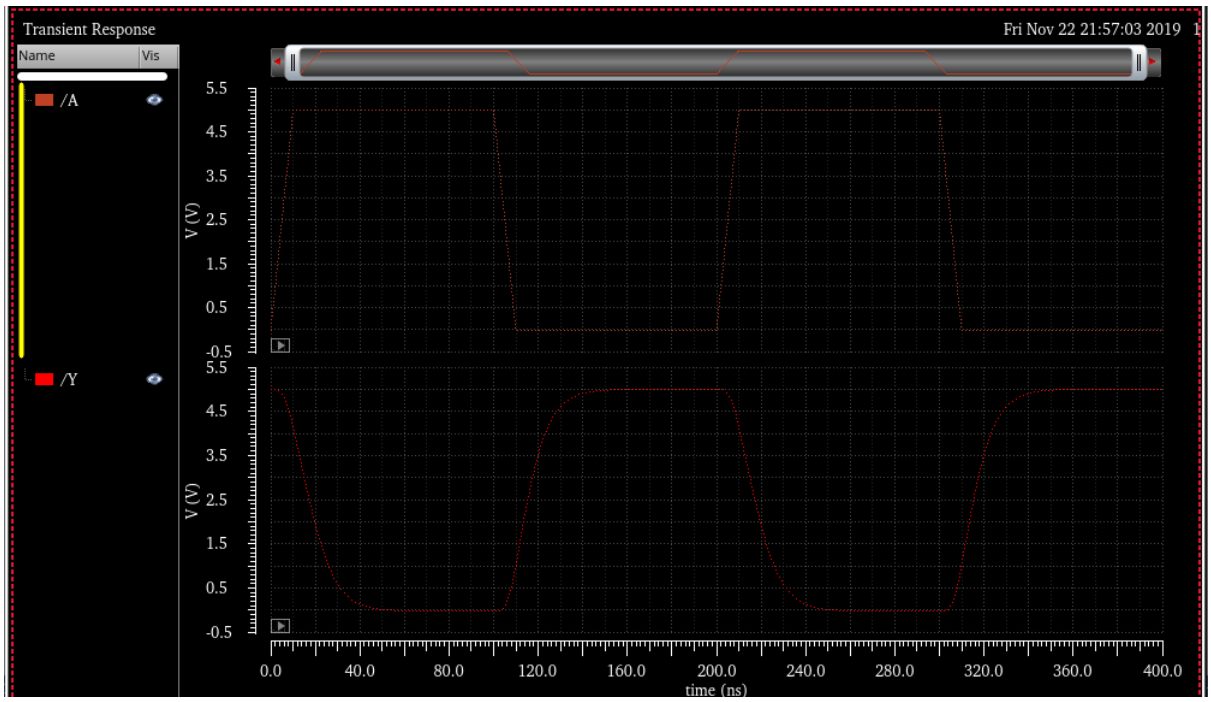
TBinv2:



TBinv2 schematic



TBinv2 ADE L

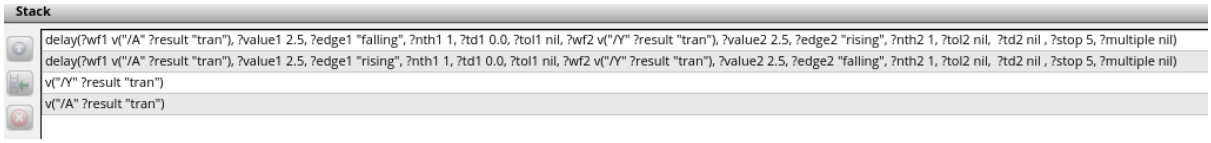


TBinv2 output

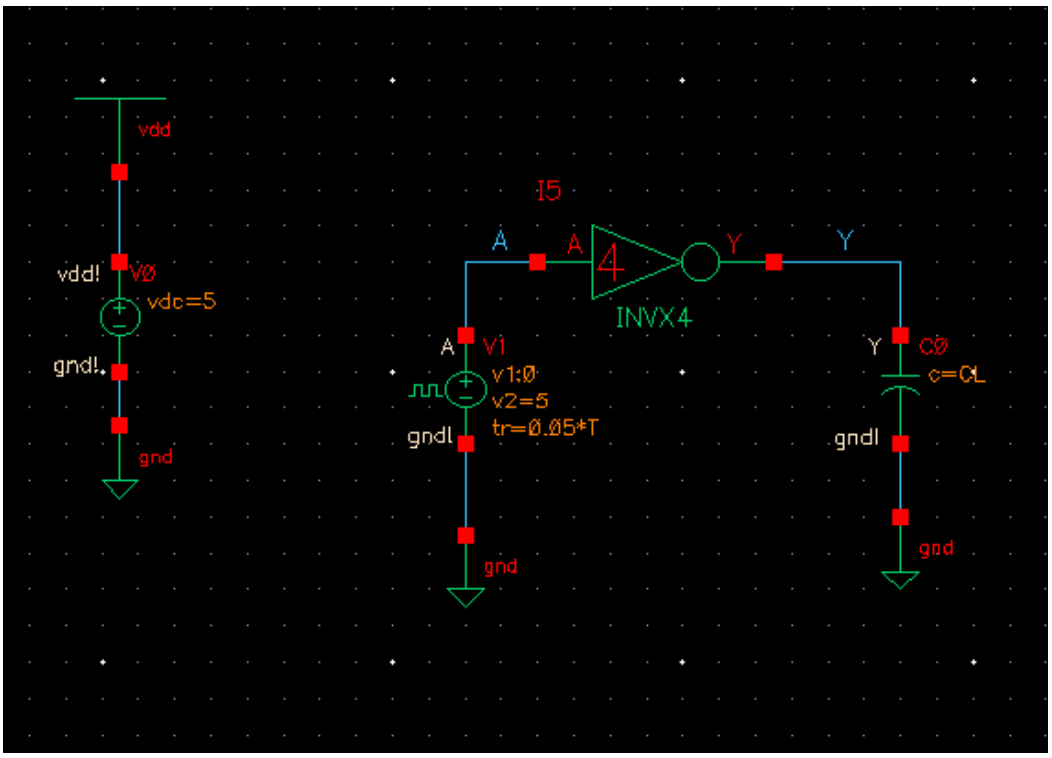
Propagation delays:

t_{pdr} (A -> Y) = 12.34E-9 = **12.34ns**

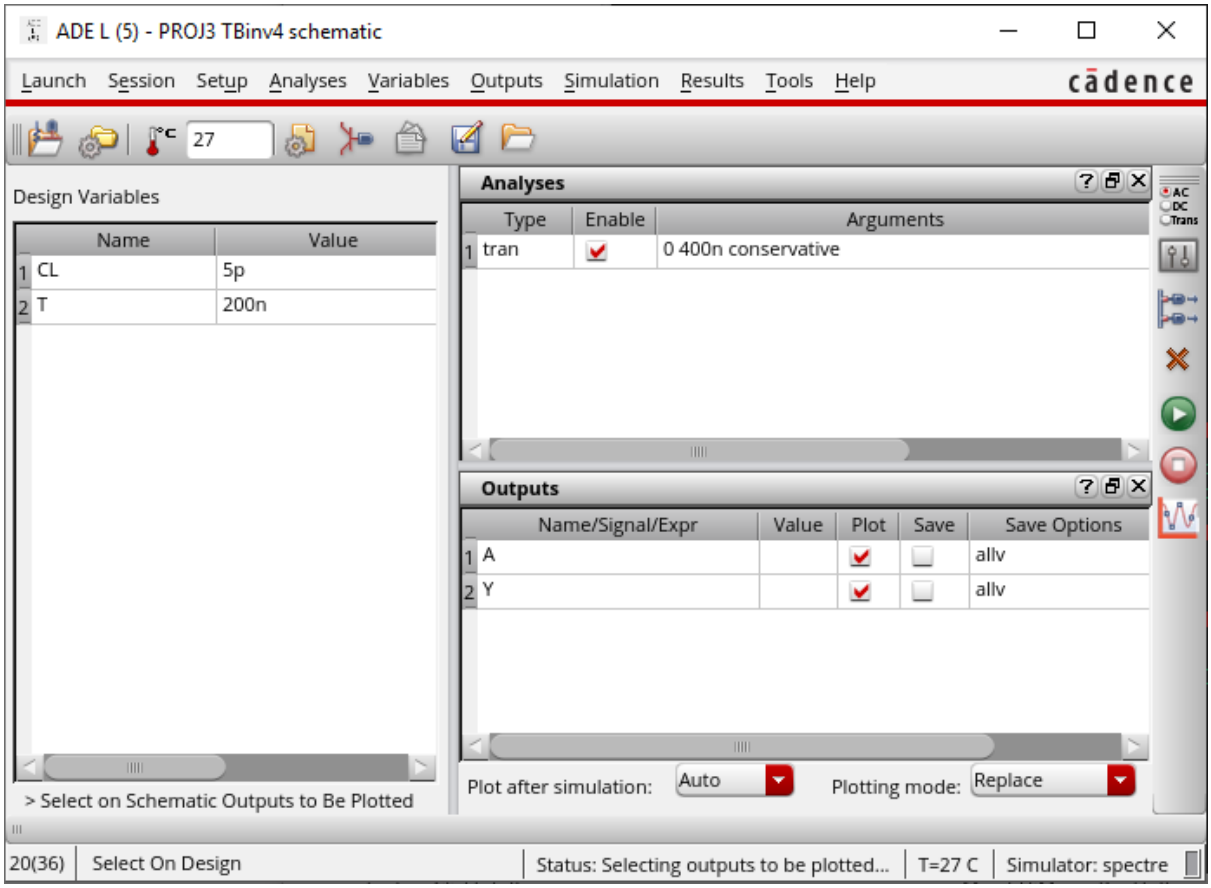
t_{pdf} (A -> Y) = 10.22E-9 = **10.22ns**



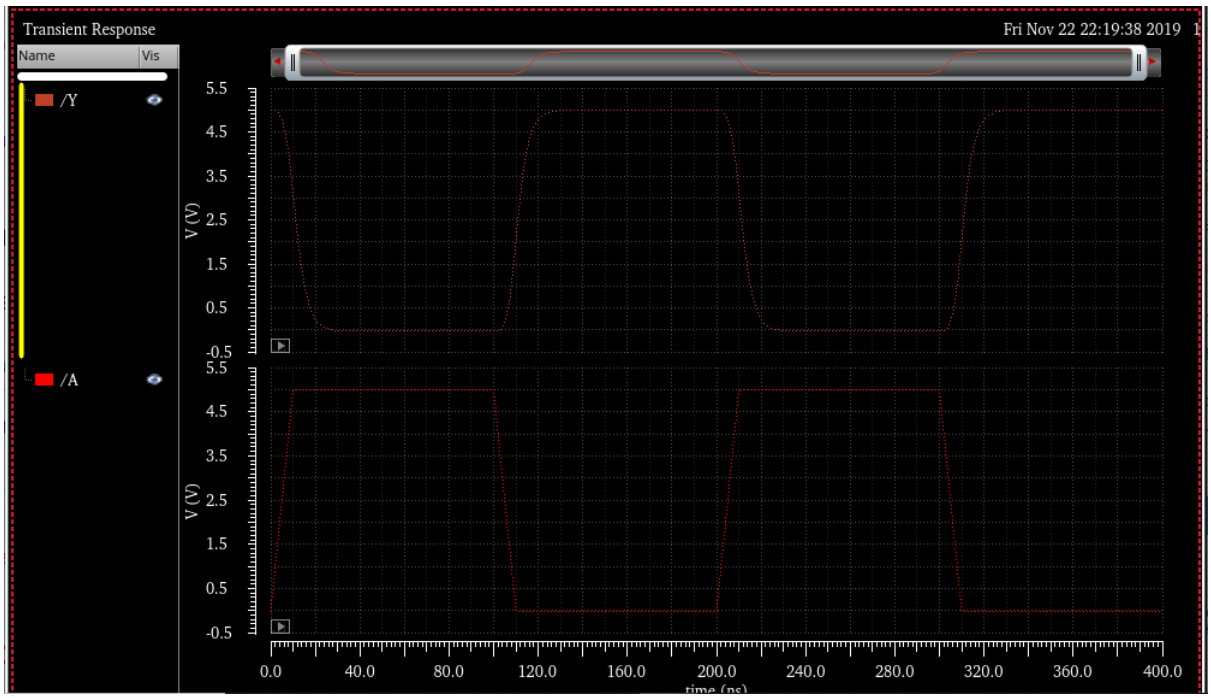
TBinv4:



TBinv4 schematic



TBinv4 ADE L

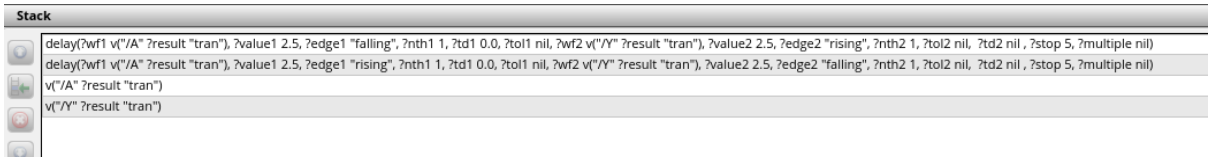


TBinv4 output

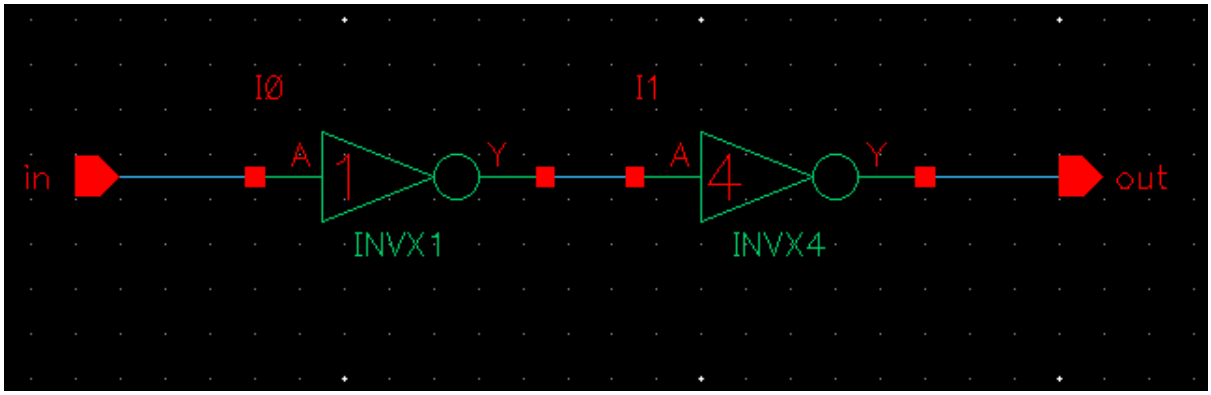
Propagation delays:

t_{pdr} (A -> Y) = 6.296E-9 = **6.296ns**

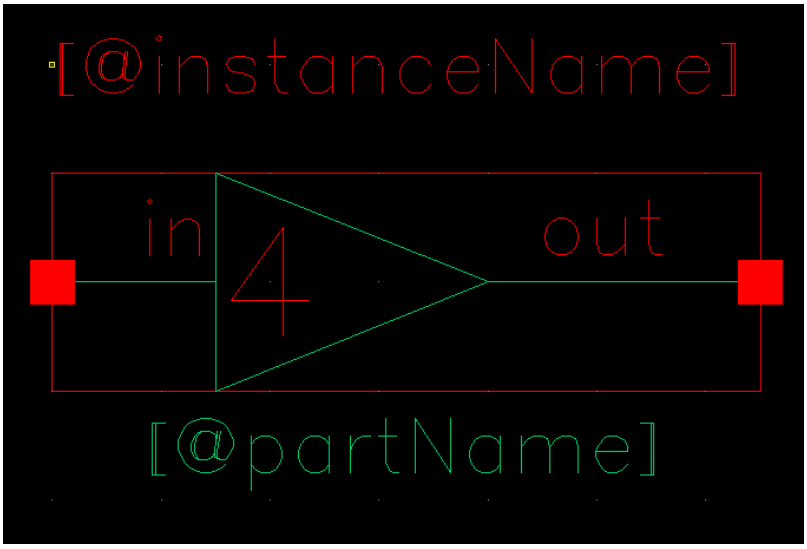
t_{pdf} (A -> Y) = 5.795E-9 = **5.795ns**



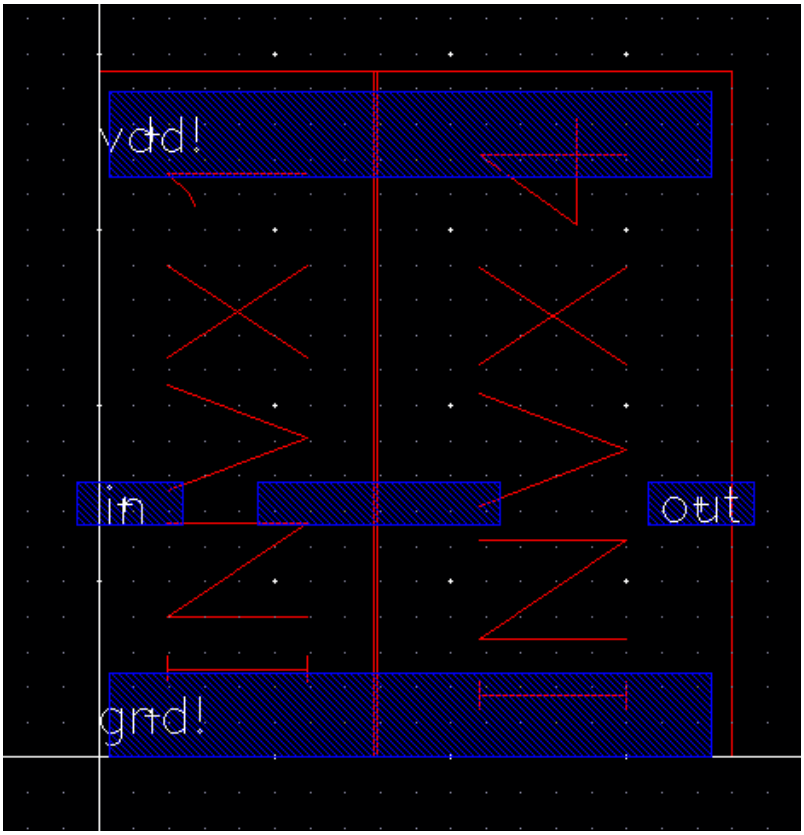
PART C



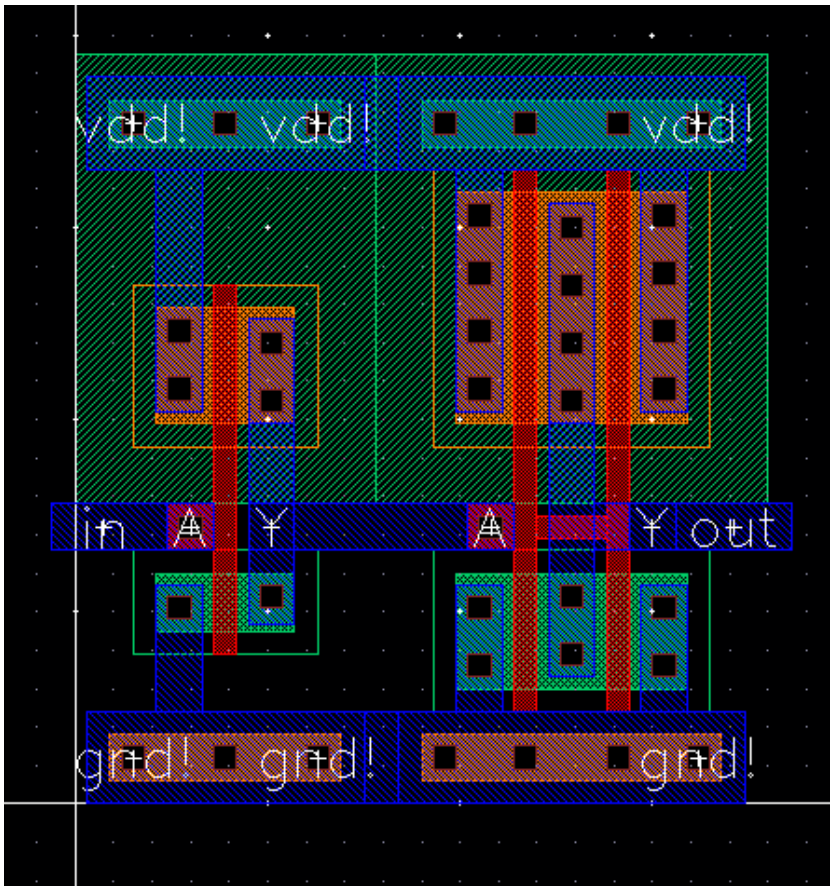
bufX14 schematic



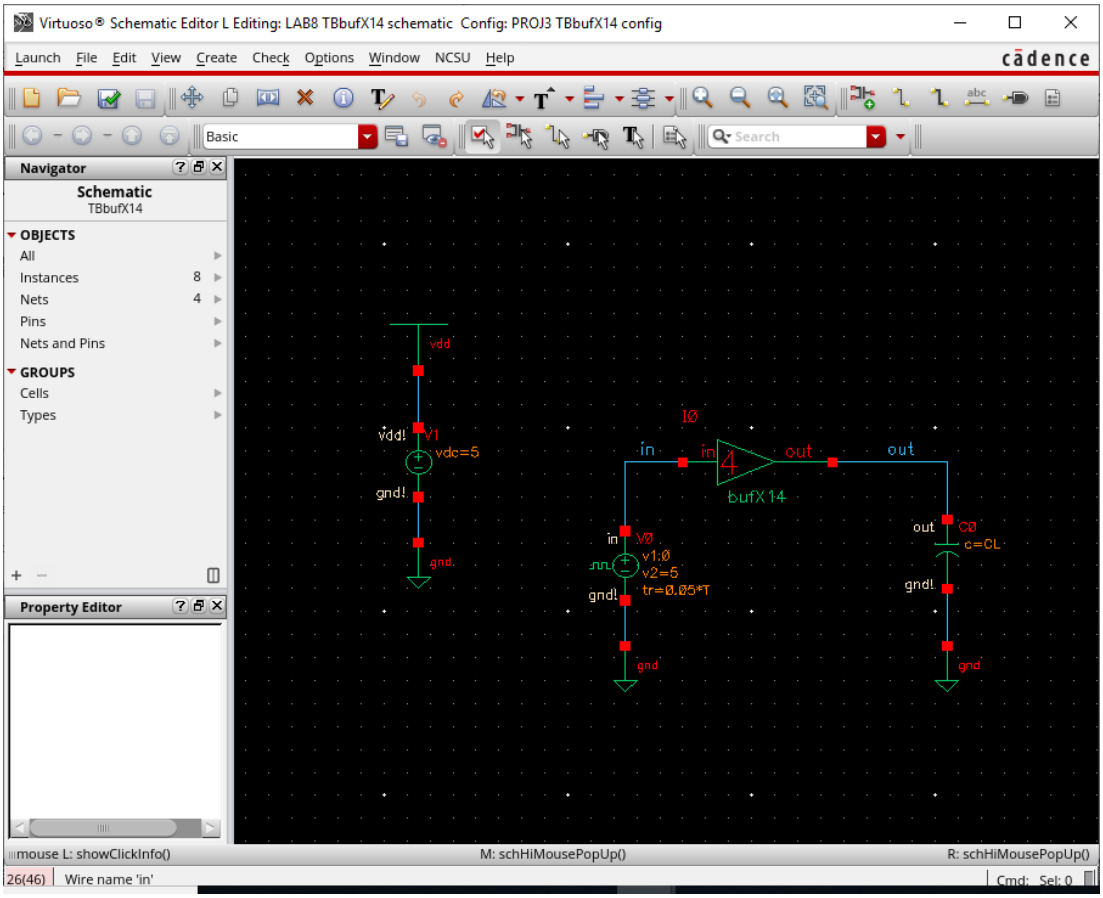
bufX14 symbol



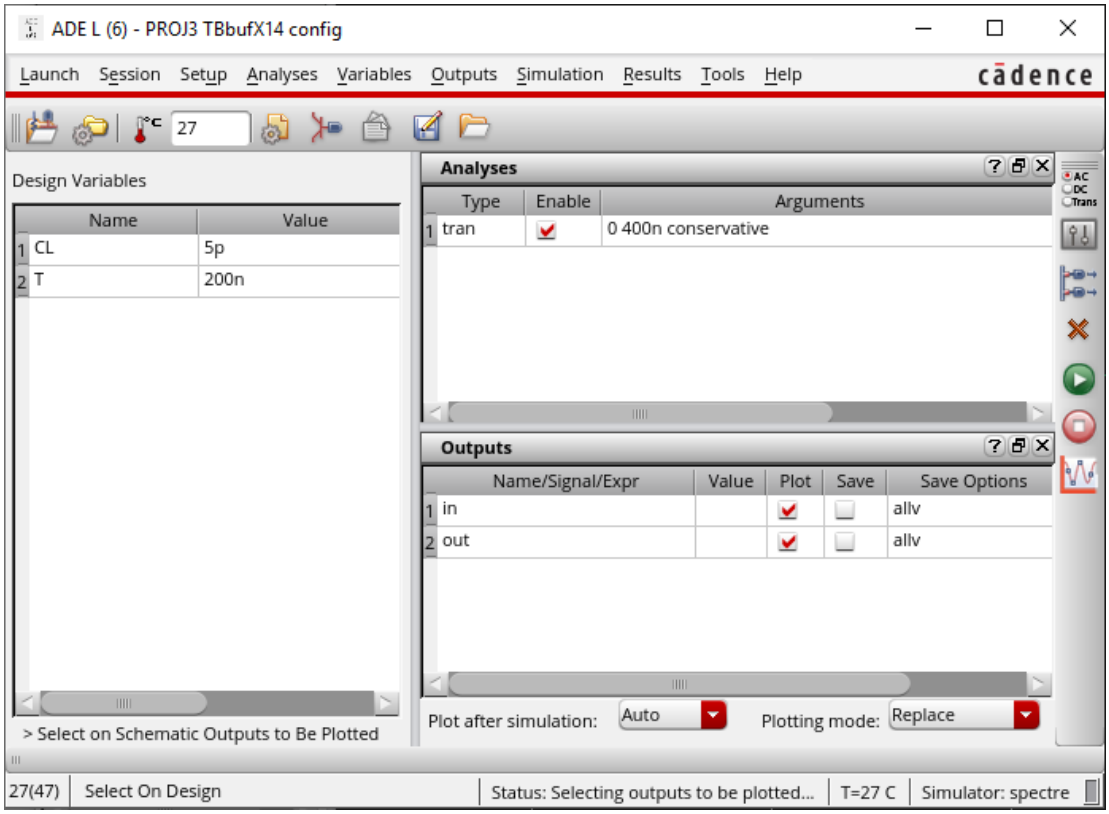
bufX14 Layout (Top Level)



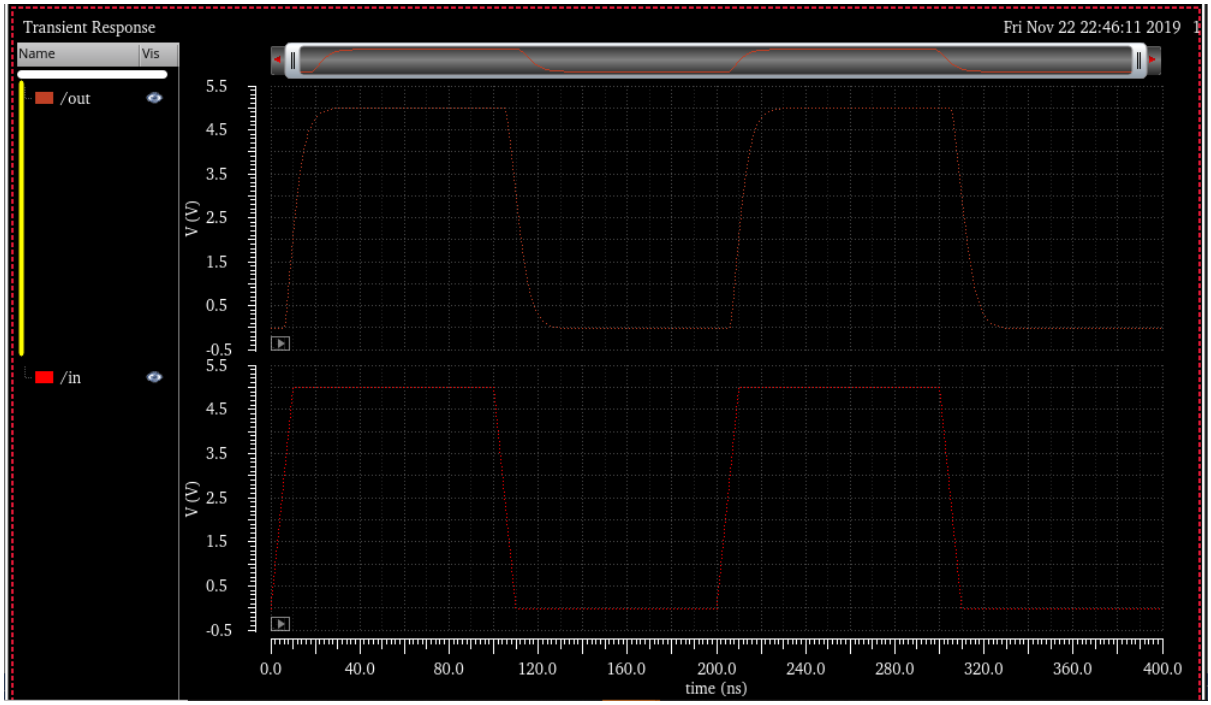
bufX14 layout (Lower Level)



TBbufX14 schematic view (config)



TBbufX14 ADE L

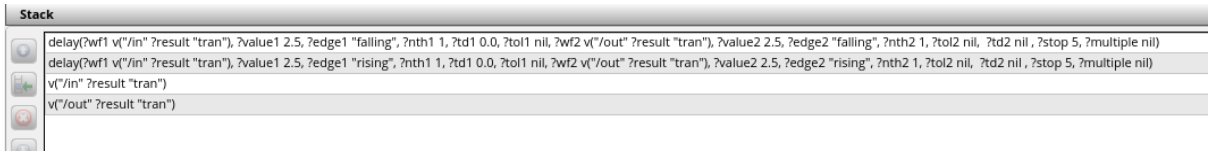


TBbufX14 output

Propagation delays:

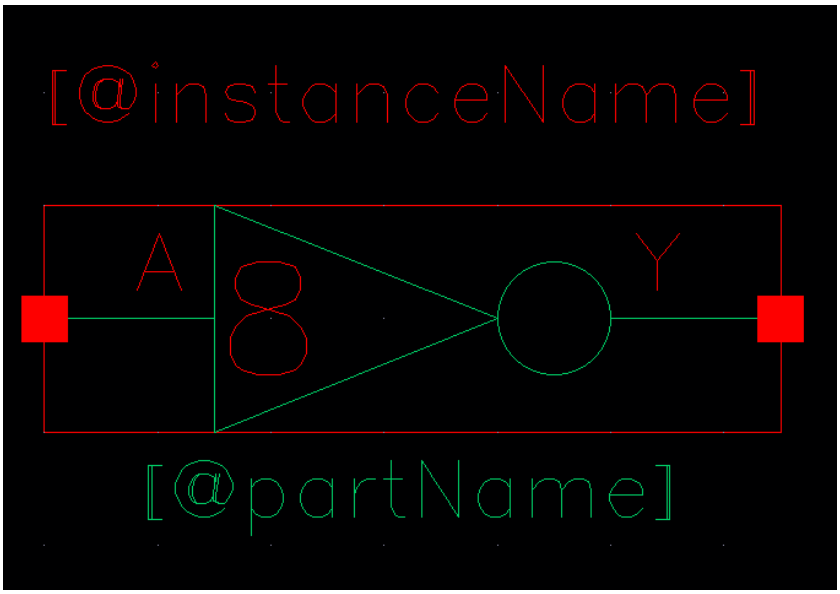
t_{pdr} (in -> out) = 5.803E-9 = **5.803ns**

t_{pdf} (in -> out) = 6.183E-9 = **6.183ns**

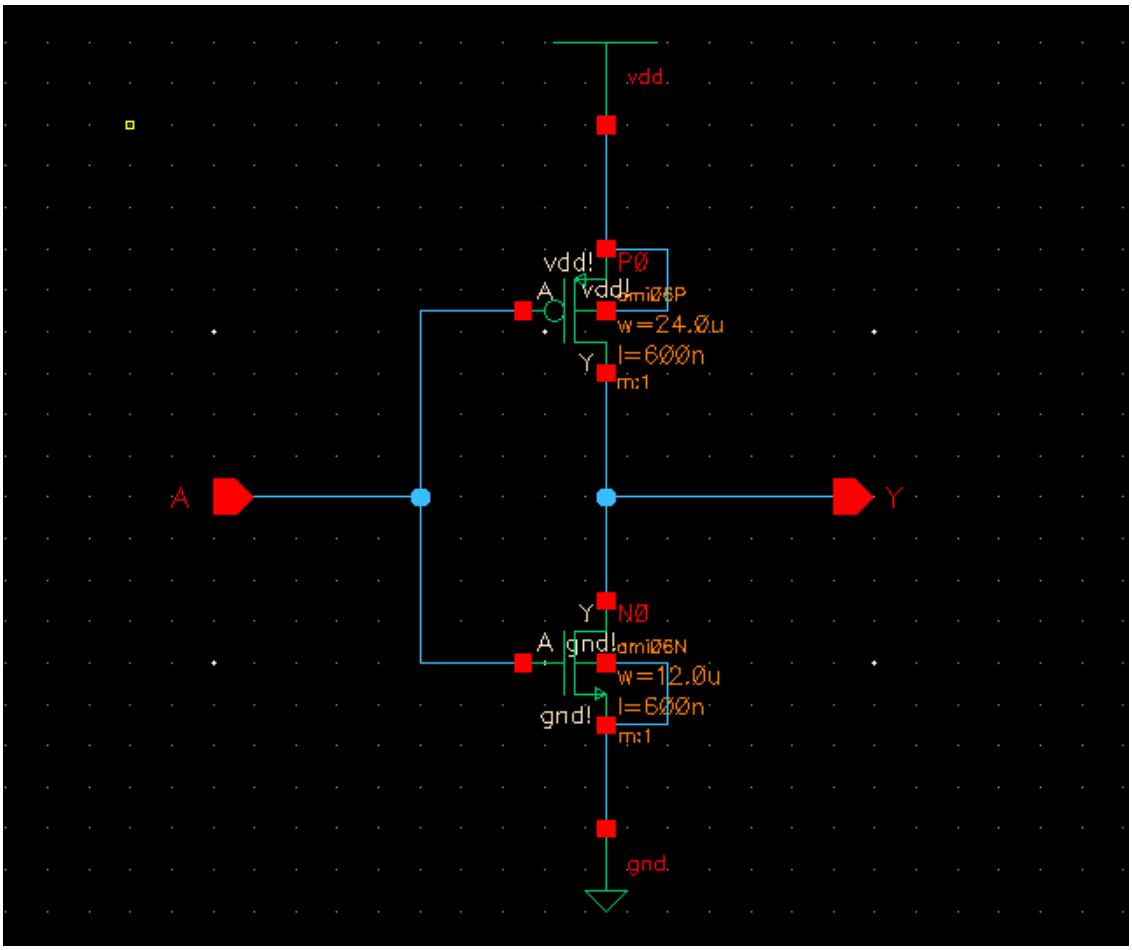


PART D

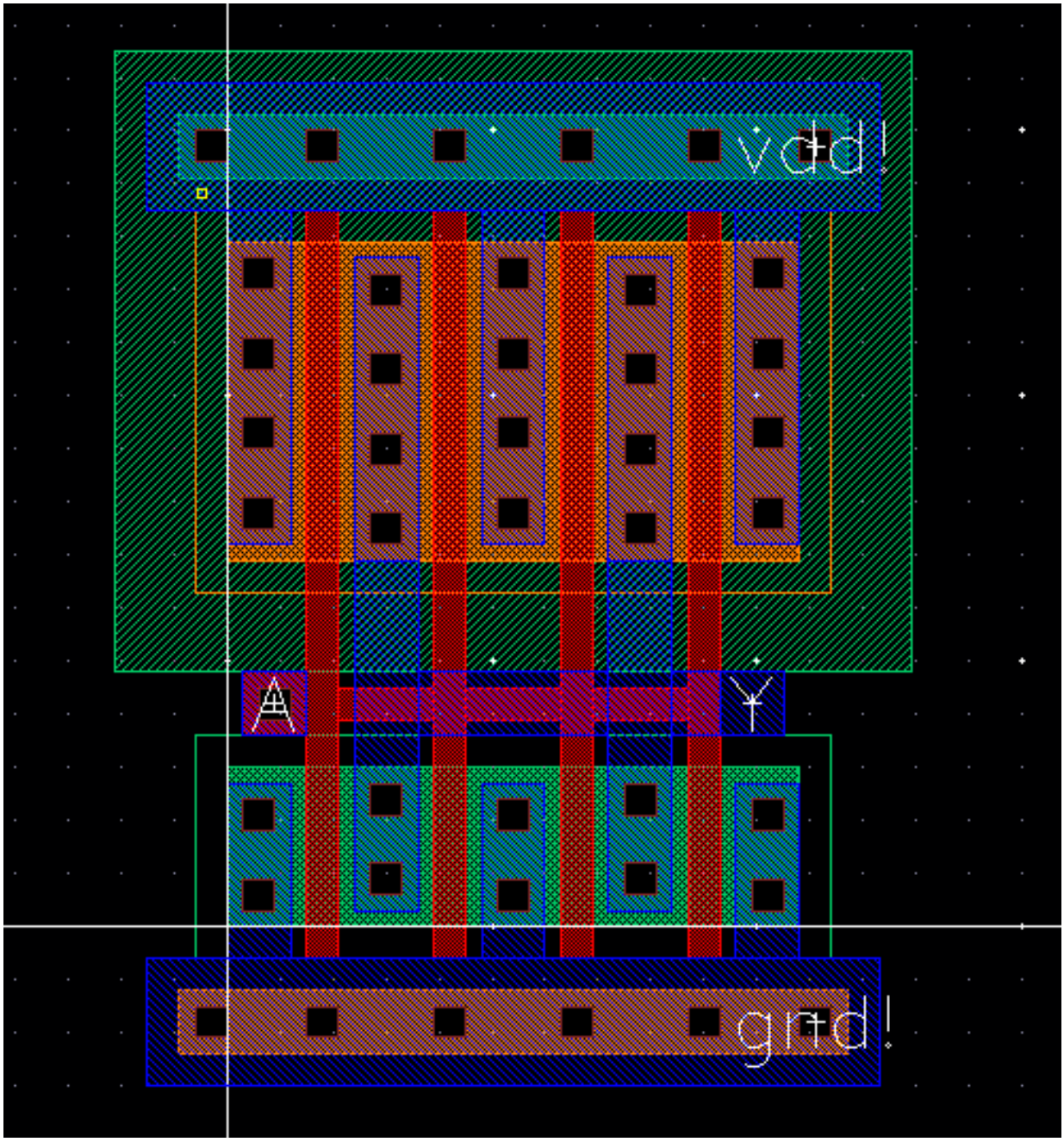
INVX8:



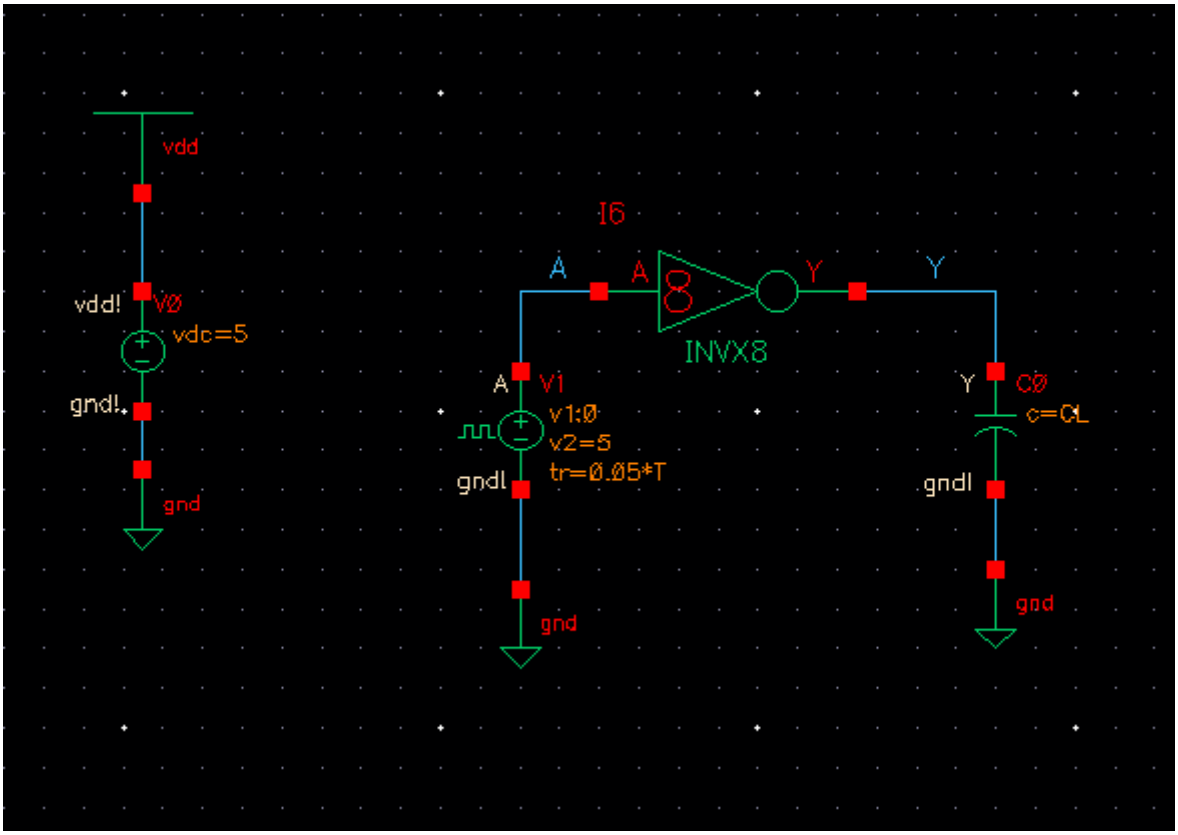
INVX8 Symbol



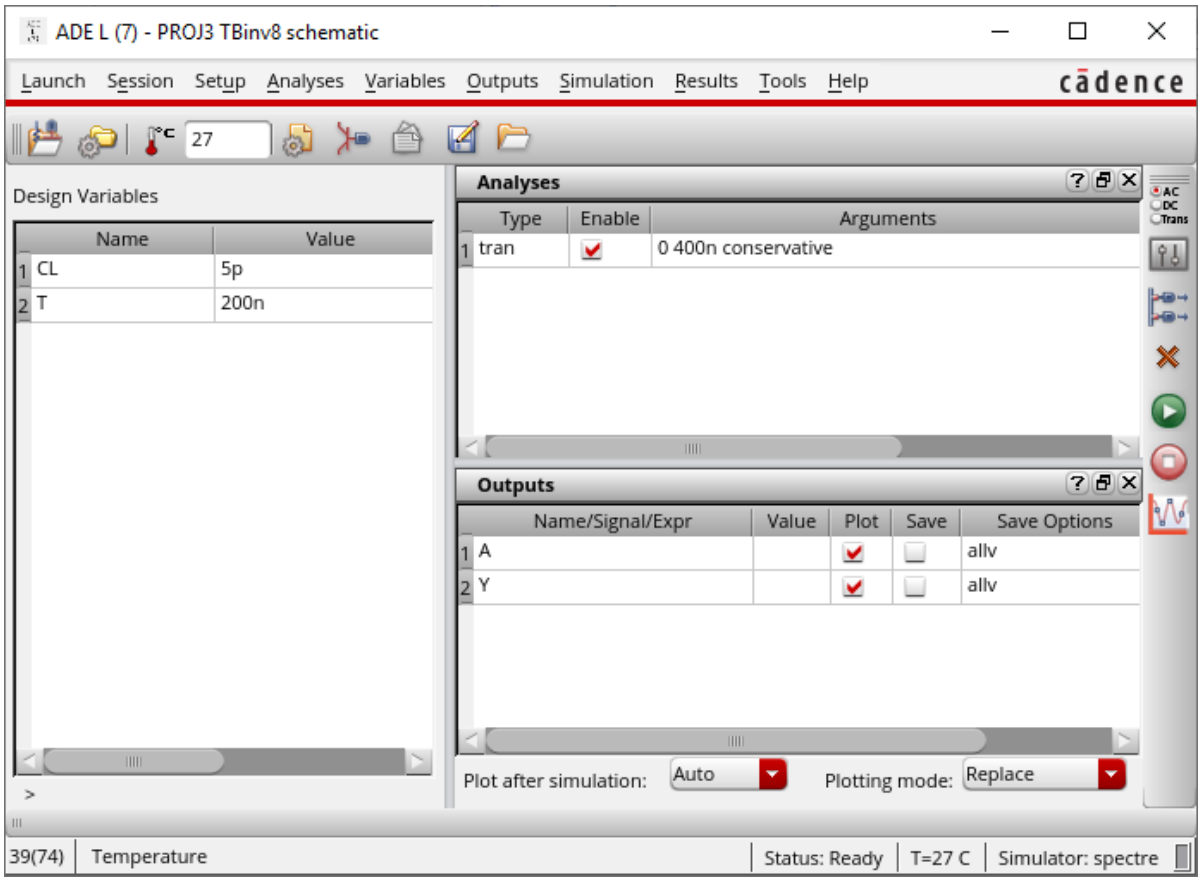
INVX8 Schematic



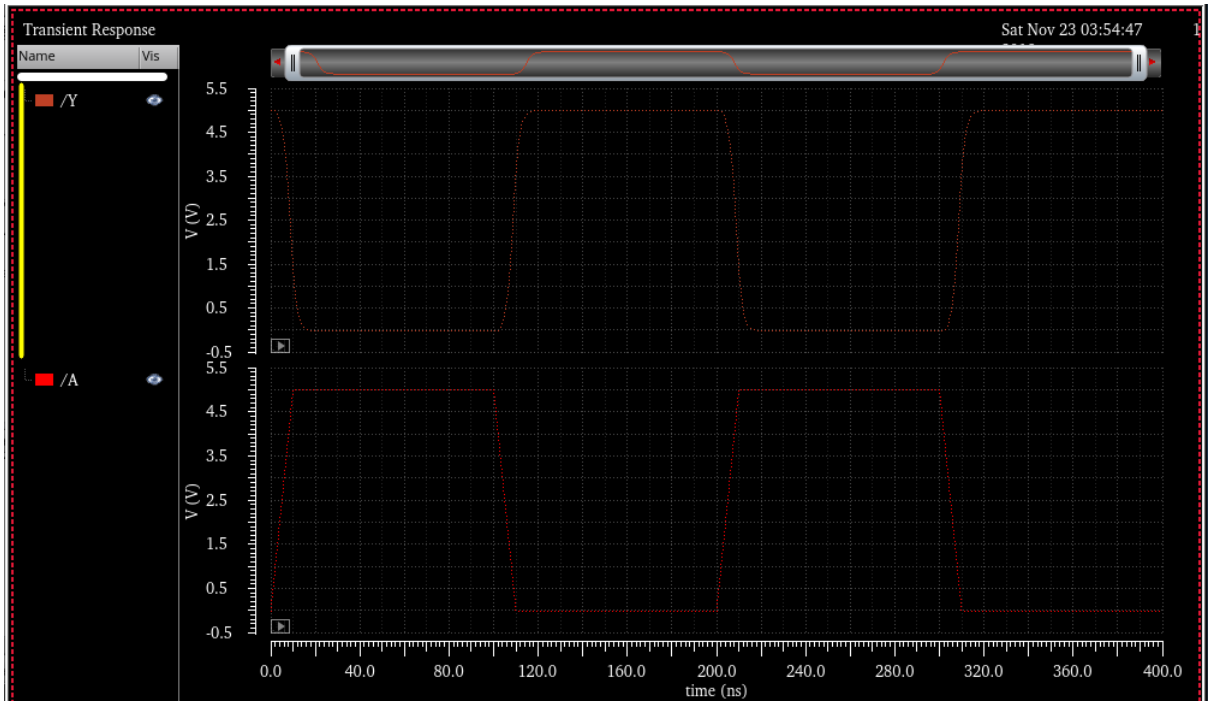
INVX8 Layout



TBinv8 schematic



TBinv8 ADE L



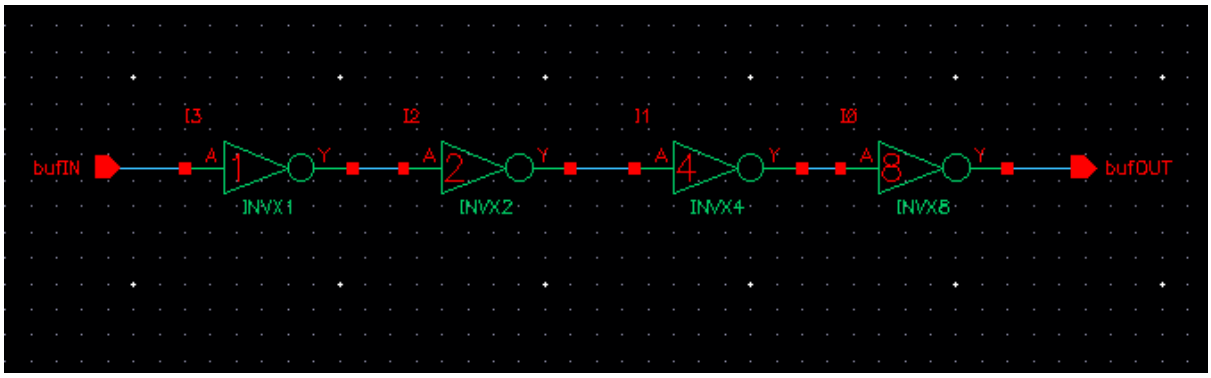
TBinv8 output

Propagation delays:

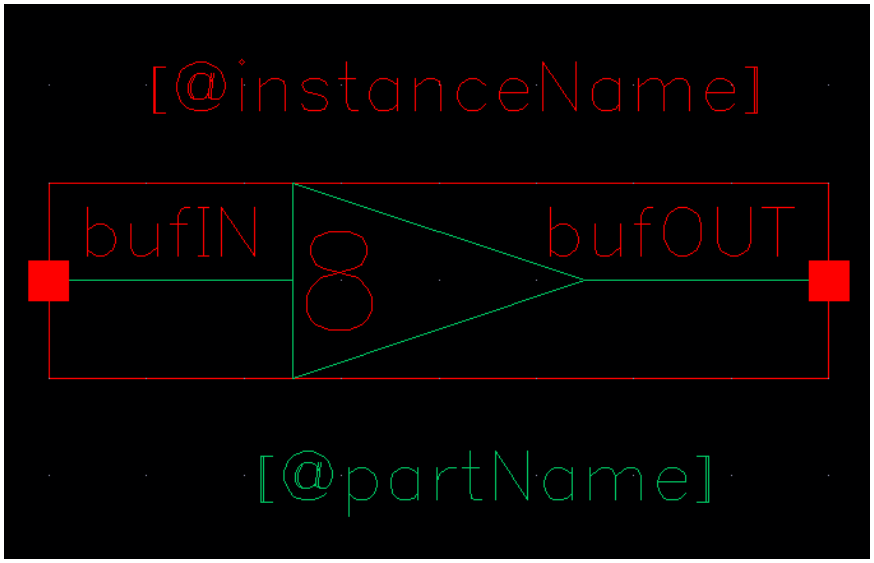
t_{pdr} (A -> Y) = 3.725E-9 = **3.725ns**

t_{pdf} (A -> Y) = 3.681E-9 = **3.681ns**

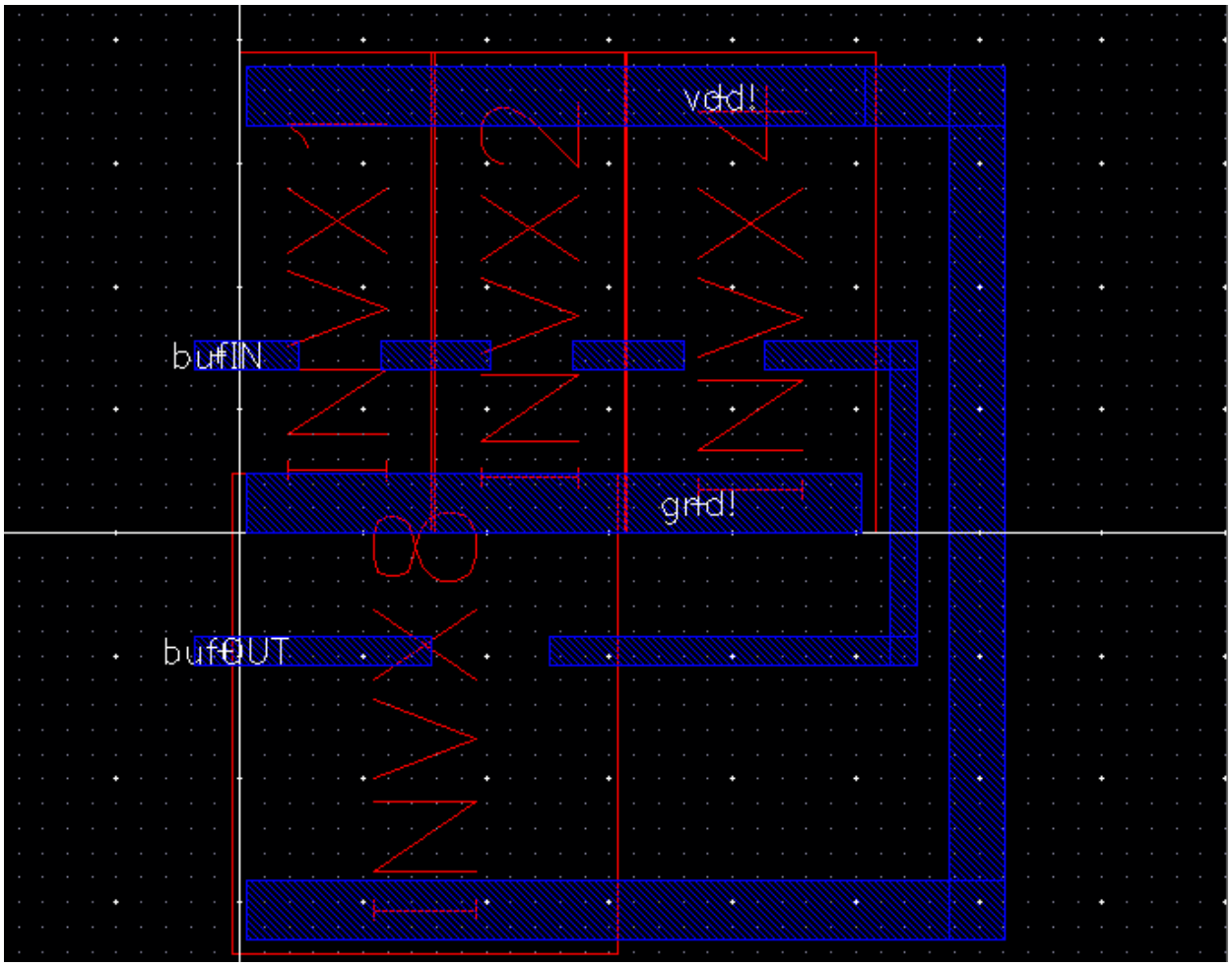
PART E



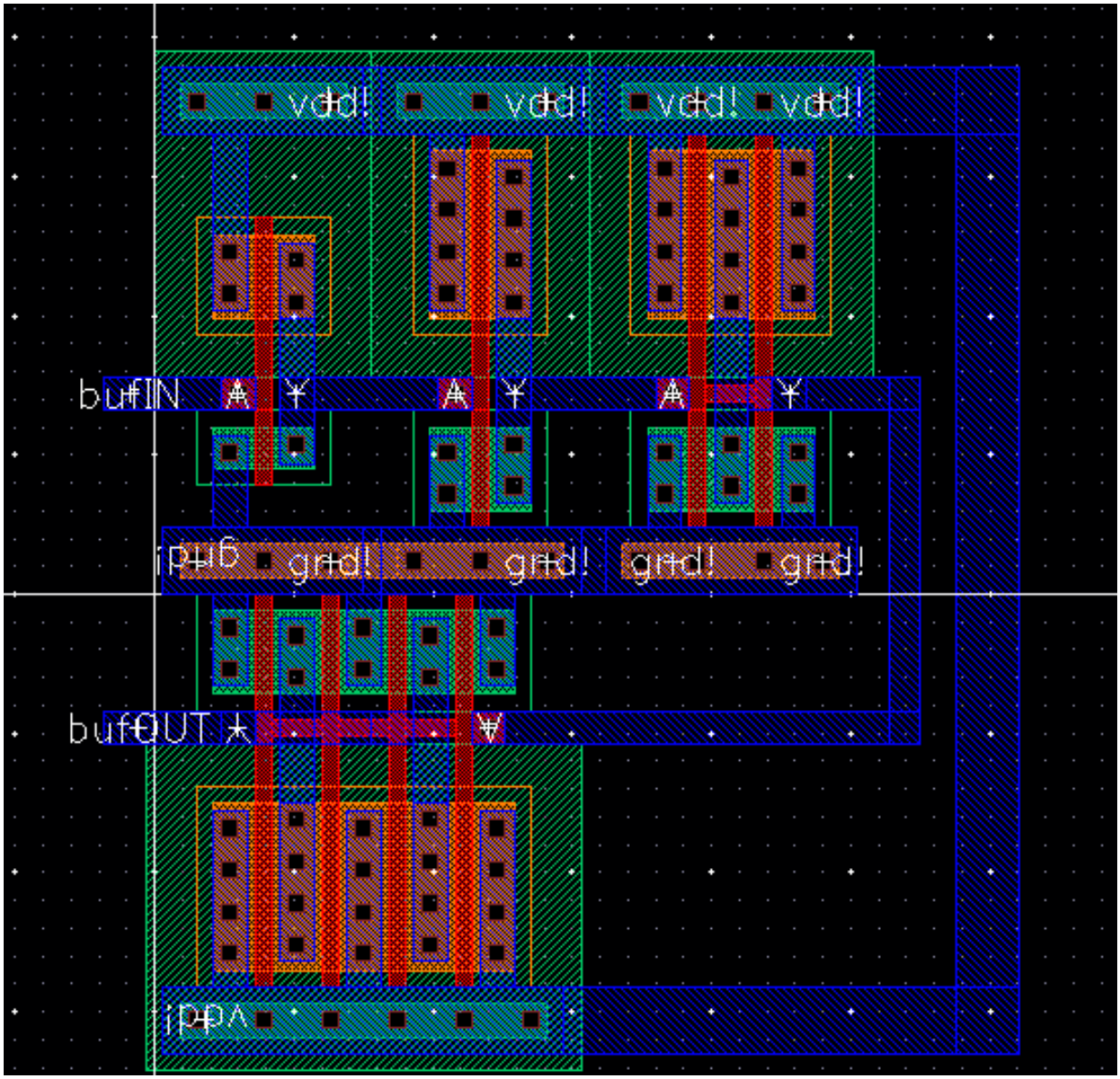
bufX1248 schematic



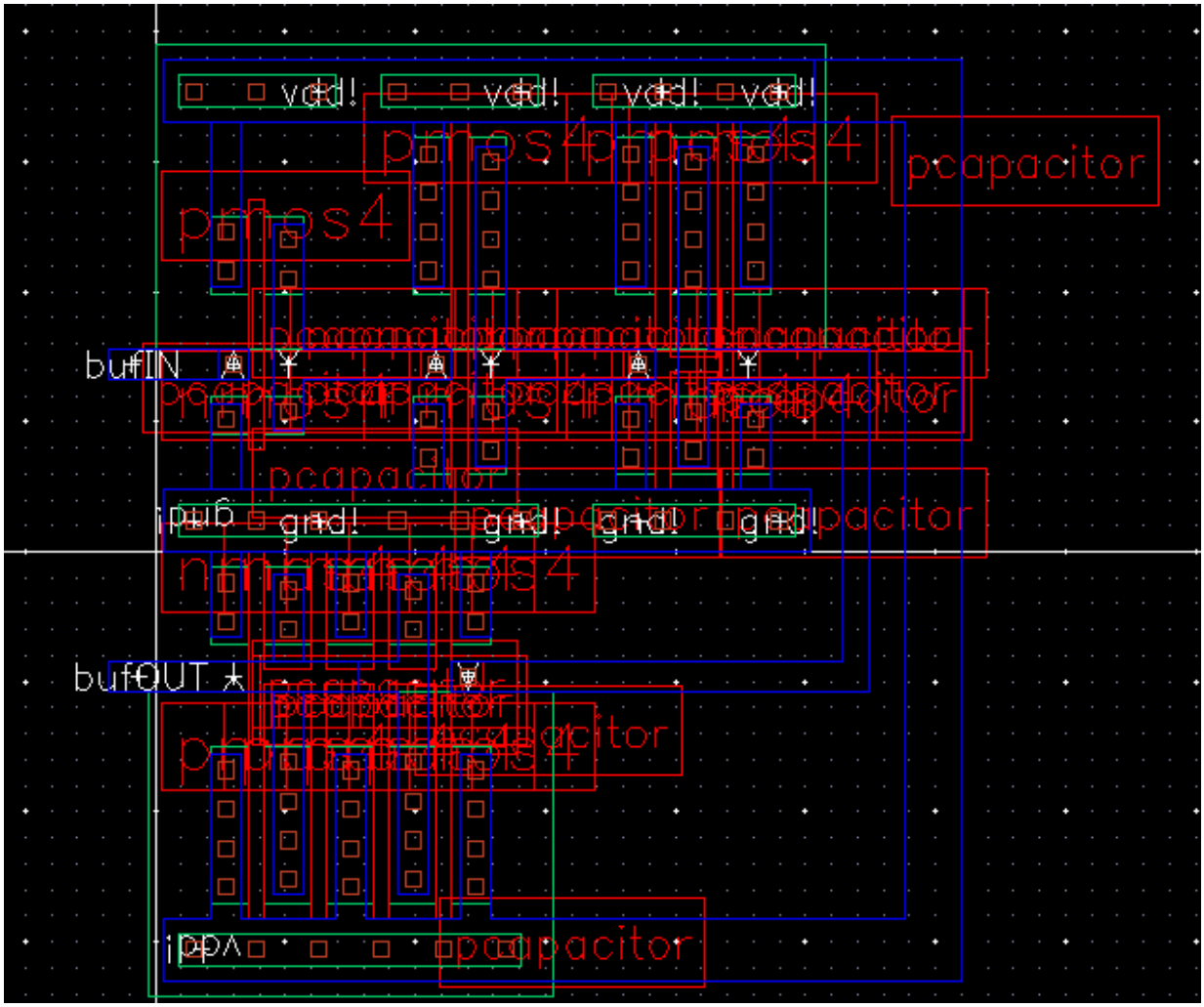
bufX1248 symbol



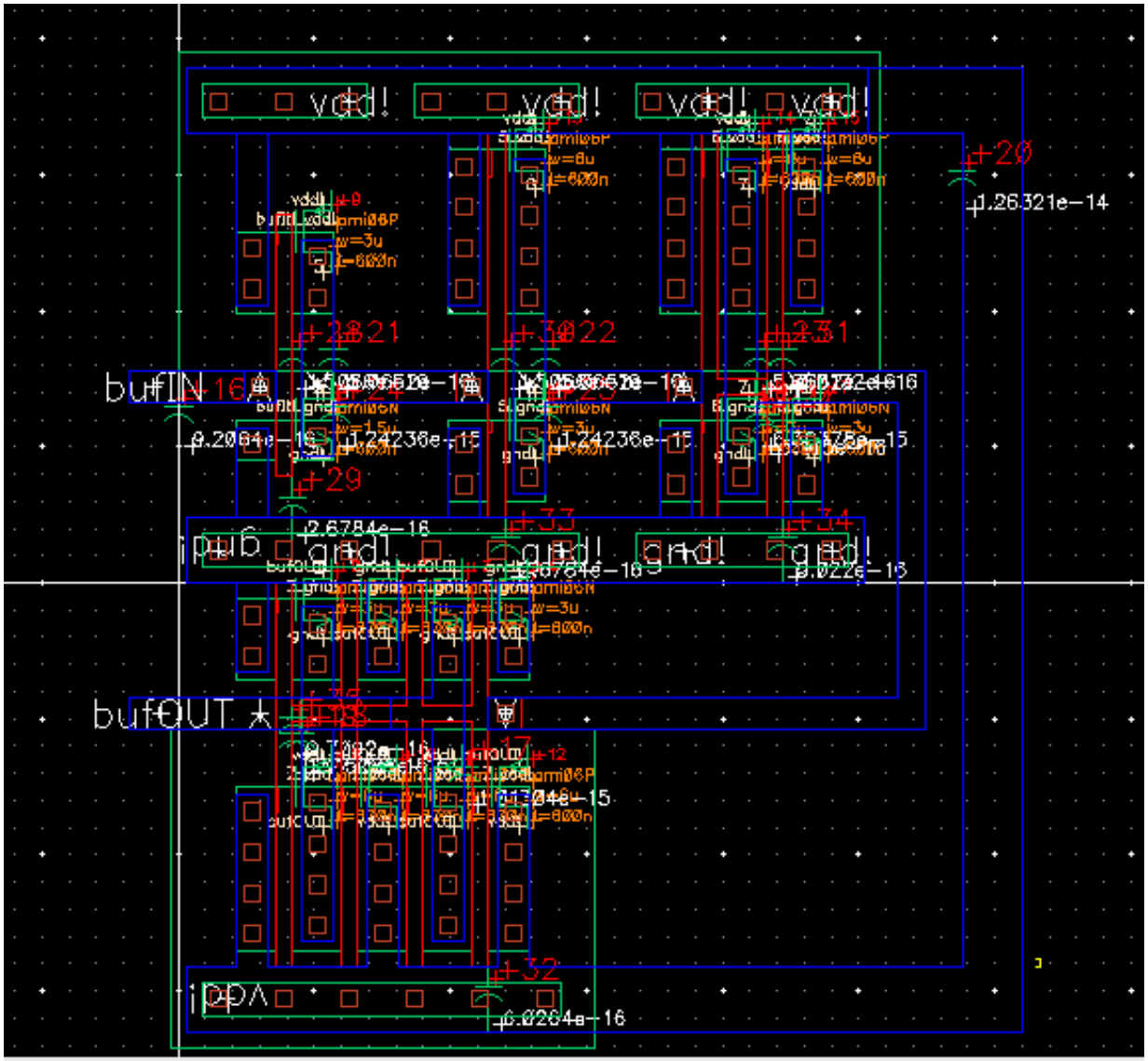
bufX1248 layout (Top Level)



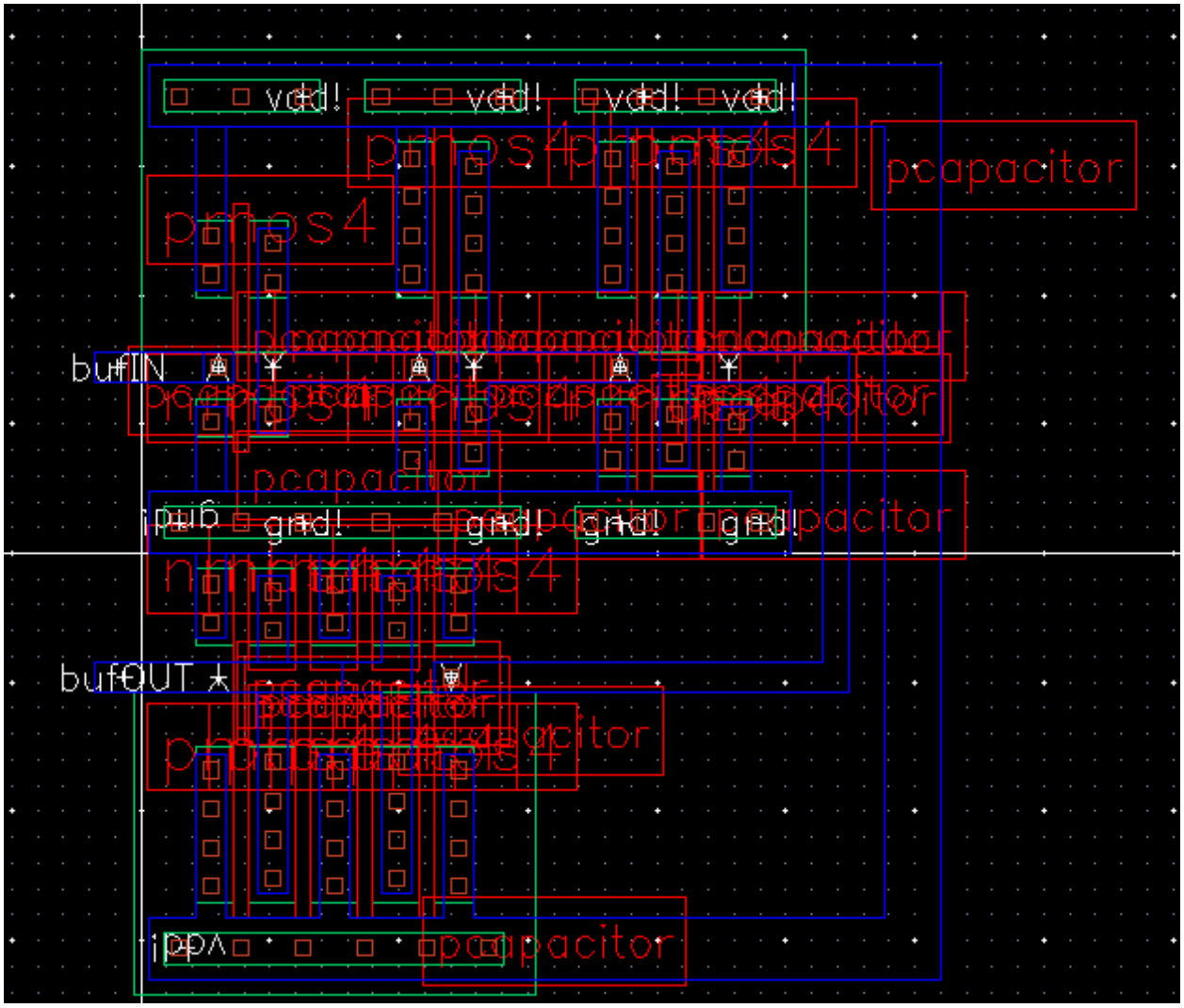
bufX1248 layout (Lower Level)



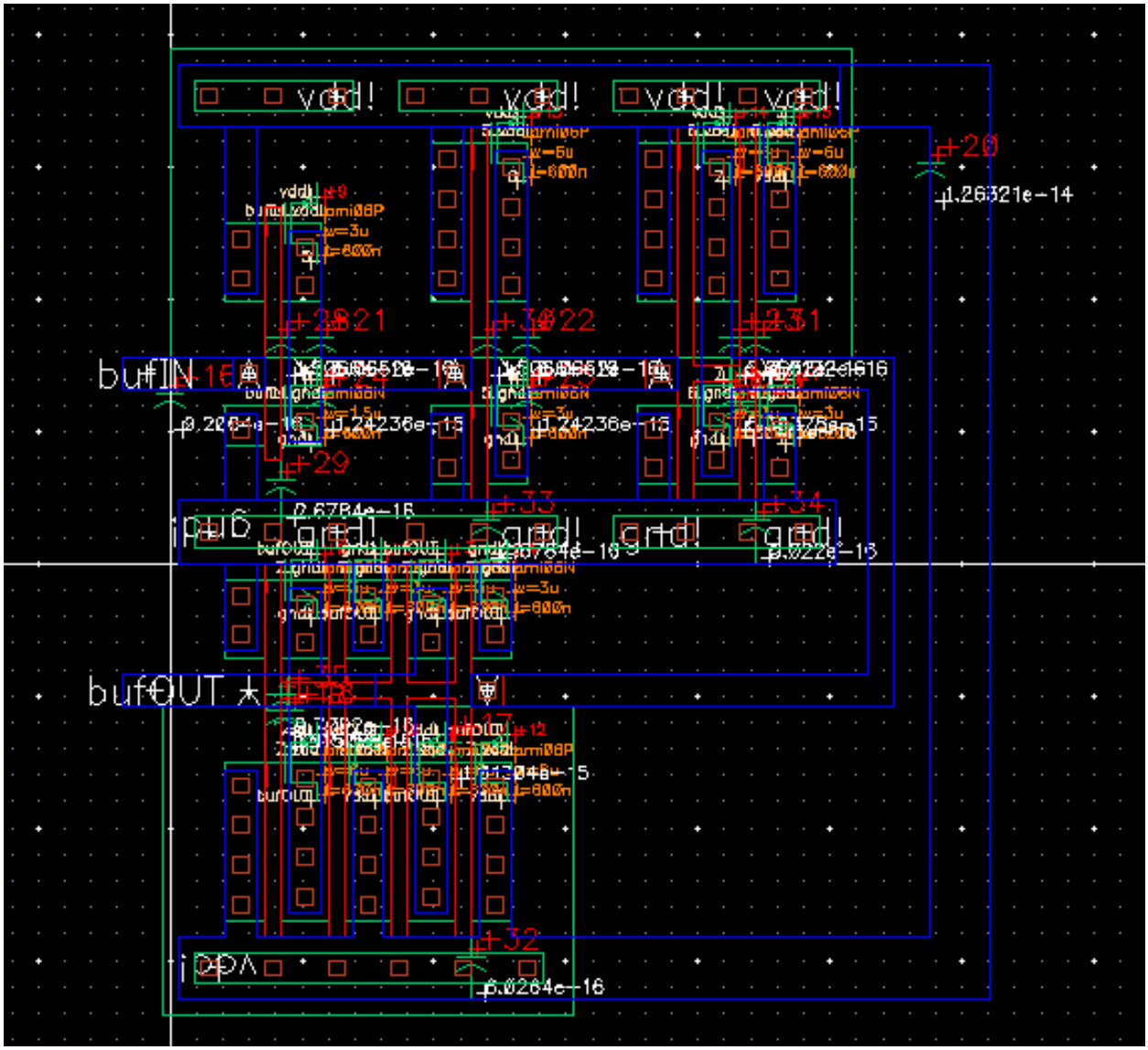
bufX1248 extracted (Top Level)



bufX1248 extracted (Lower Level)

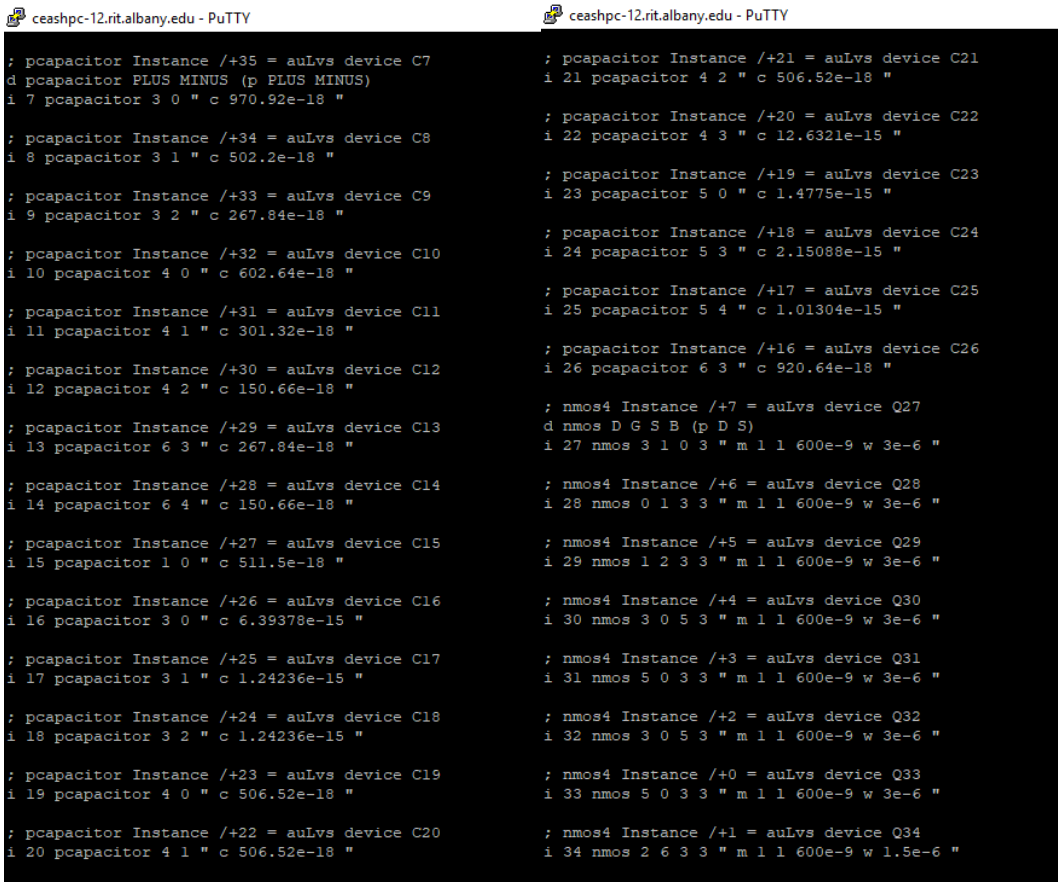


bufX1248 analog extracted (Top Level)



bufX1248 analog extracted (Lower Level)

Parasitic capacitor values:



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```
; pcapacitor Instance /+35 = auLvs device C7
d pcapacitor PLUS MINUS (p PLUS MINUS)
i 7 pcapacitor 3 0 " c 970.92e-18 "

; pcapacitor Instance /+34 = auLvs device C8
i 8 pcapacitor 3 1 " c 502.2e-18 "

; pcapacitor Instance /+33 = auLvs device C9
i 9 pcapacitor 3 2 " c 267.84e-18 "

; pcapacitor Instance /+32 = auLvs device C10
i 10 pcapacitor 4 0 " c 602.64e-18 "

; pcapacitor Instance /+31 = auLvs device C11
i 11 pcapacitor 4 1 " c 301.32e-18 "

; pcapacitor Instance /+30 = auLvs device C12
i 12 pcapacitor 4 2 " c 150.66e-18 "

; pcapacitor Instance /+29 = auLvs device C13
i 13 pcapacitor 6 3 " c 267.84e-18 "

; pcapacitor Instance /+28 = auLvs device C14
i 14 pcapacitor 6 4 " c 150.66e-18 "

; pcapacitor Instance /+27 = auLvs device C15
i 15 pcapacitor 1 0 " c 511.5e-18 "

; pcapacitor Instance /+26 = auLvs device C16
i 16 pcapacitor 3 0 " c 6.39378e-15 "

; pcapacitor Instance /+25 = auLvs device C17
i 17 pcapacitor 3 1 " c 1.24236e-15 "

; pcapacitor Instance /+24 = auLvs device C18
i 18 pcapacitor 3 2 " c 1.24236e-15 "

; pcapacitor Instance /+23 = auLvs device C19
i 19 pcapacitor 4 0 " c 506.52e-18 "

; pcapacitor Instance /+22 = auLvs device C20
i 20 pcapacitor 4 1 " c 506.52e-18 "
```

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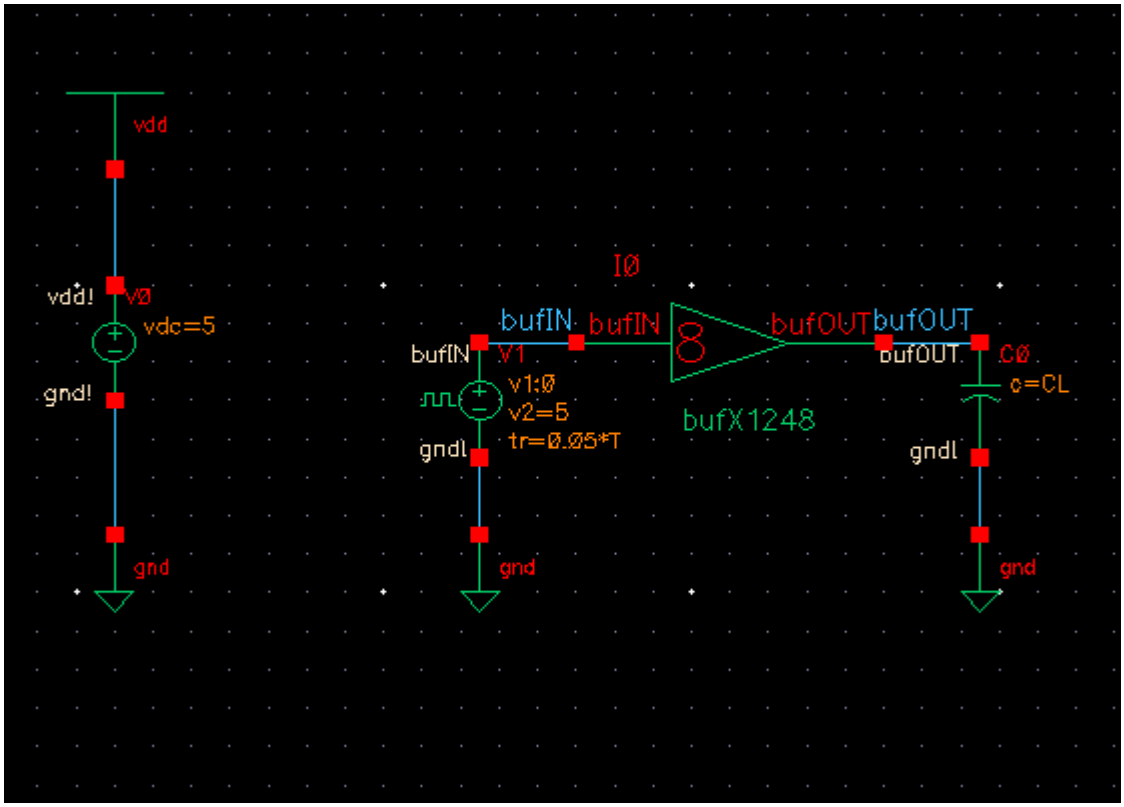
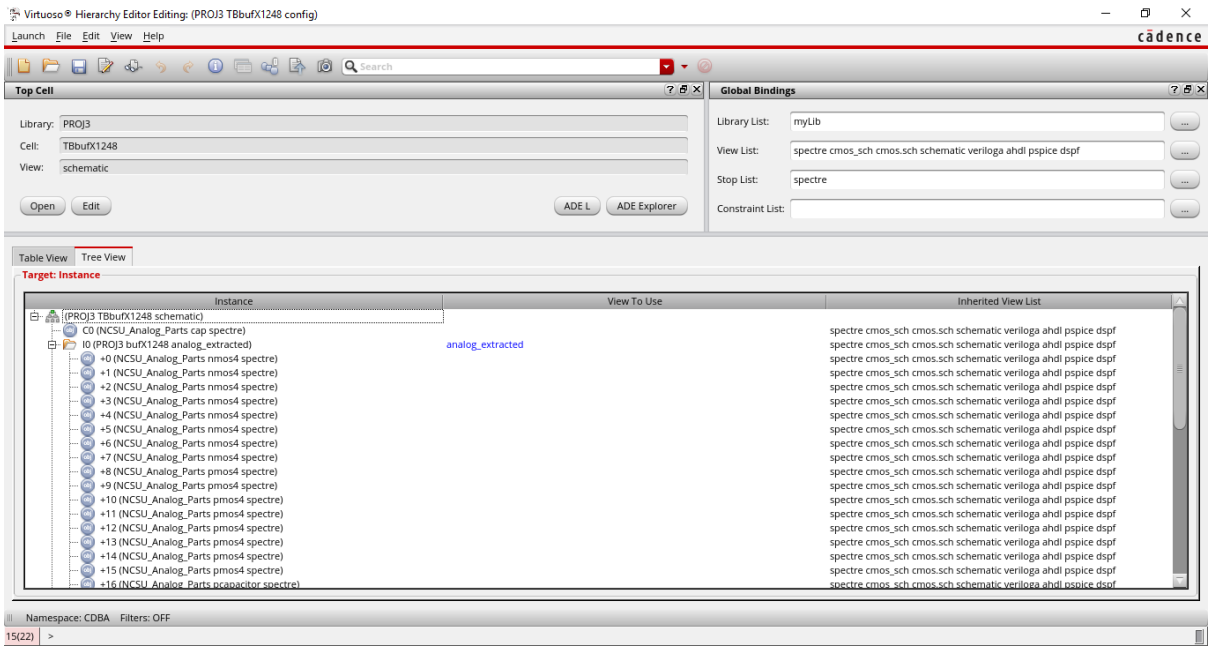
```
; pcapacitor Instance /+21 = auLvs device C21
i 21 pcapacitor 4 2 " c 506.52e-18 "

; pcapacitor Instance /+20 = auLvs device C22
i 22 pcapacitor 4 3 " c 12.6321e-15 "

; pcapacitor Instance /+19 = auLvs device C23
i 23 pcapacitor 5 0 " c 1.4775e-15 "

; pcapacitor Instance /+18 = auLvs device C24
i 24 pcapacitor 5 3 " c 2.15088e-15 "

; pcapacitor Instance /+17 = auLvs device C25
i 25 pcapacitor 5 4 " c 1.01304e-15 "

; pcapacitor Instance /+16 = auLvs device C26
i 26 pcapacitor 6 3 " c 920.64e-18 "

; nmos4 Instance /+7 = auLvs device Q27
d nmos D G S B (p D S)
i 27 nmos 3 1 0 3 " m 1 l 600e-9 w 3e-6 "

; nmos4 Instance /+6 = auLvs device Q28
i 28 nmos 0 1 3 3 " m 1 l 600e-9 w 3e-6 "

; nmos4 Instance /+5 = auLvs device Q29
i 29 nmos 1 2 3 3 " m 1 l 600e-9 w 3e-6 "

; nmos4 Instance /+4 = auLvs device Q30
i 30 nmos 3 0 5 3 " m 1 l 600e-9 w 3e-6 "

; nmos4 Instance /+3 = auLvs device Q31
i 31 nmos 5 0 3 3 " m 1 l 600e-9 w 3e-6 "

; nmos4 Instance /+2 = auLvs device Q32
i 32 nmos 3 0 5 3 " m 1 l 600e-9 w 3e-6 "

; nmos4 Instance /+0 = auLvs device Q33
i 33 nmos 5 0 3 3 " m 1 l 600e-9 w 3e-6 "

; nmos4 Instance /+1 = auLvs device Q34
i 34 nmos 2 6 3 3 " m 1 l 600e-9 w 1.5e-6 "
```

Capacitor Instance ID	Value (F)	From net name	To net name
16	920.64aF	bufIN	A (INVX1)
17	1.01304fF	metal1 connection (Y, INVX4)	A (INVX8)
18	2.15088fF	A (INVX8)	nmos4 (INVX8)
19	1.4775fF	pmos4 (INVX8)	Y (INVX8)
20	12.6321fF	vdd! (top)	vdd! (bottom)
21	506.52aF	pmos4 (INVX1)	Y (INVX1)
22	506.52aF	pmos4 (INVX2)	Y (INVX2)
23	506.52aF	pmos4 (INVX4)	Y (INVX4)
24	1.24236fF	Y (INVX1)	A (INVX2)
25	1.24236fF	Y (INVX2)	A (INVX4)
26	6.39378fF	Y (INVX4)	metal1 connection (A, INVX8)
27	511.5aF	A (INVX4)	nmos4 (INVX4)
28	150.66aF	pmos4 (INVX1)	Y (INVX1)
29	267.84aF	nmos4 (INVX1)	gnd!
30	150.66aF	pmos4 (INVX2)	Y (INVX2)
31	301.32aF	pmos4 (INVX4)	Y (INVX4)
32	602.64aF	vdd! (bottom)	pmos4 (INVX8)
33	267.84aF	nmos4 (INVX2)	gnd!
34	502.2aF	nmos4 (INVX4)	gnd!
35	970.92aF	Y (INVX8)	bufOUT

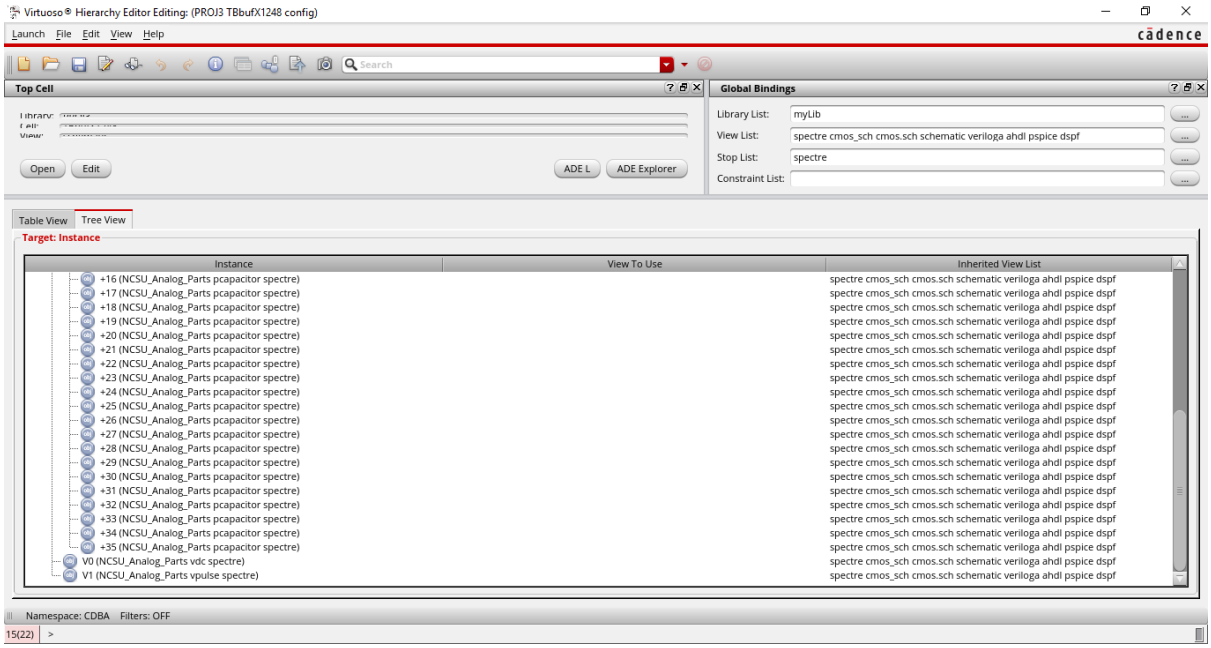
TBbufX1248:

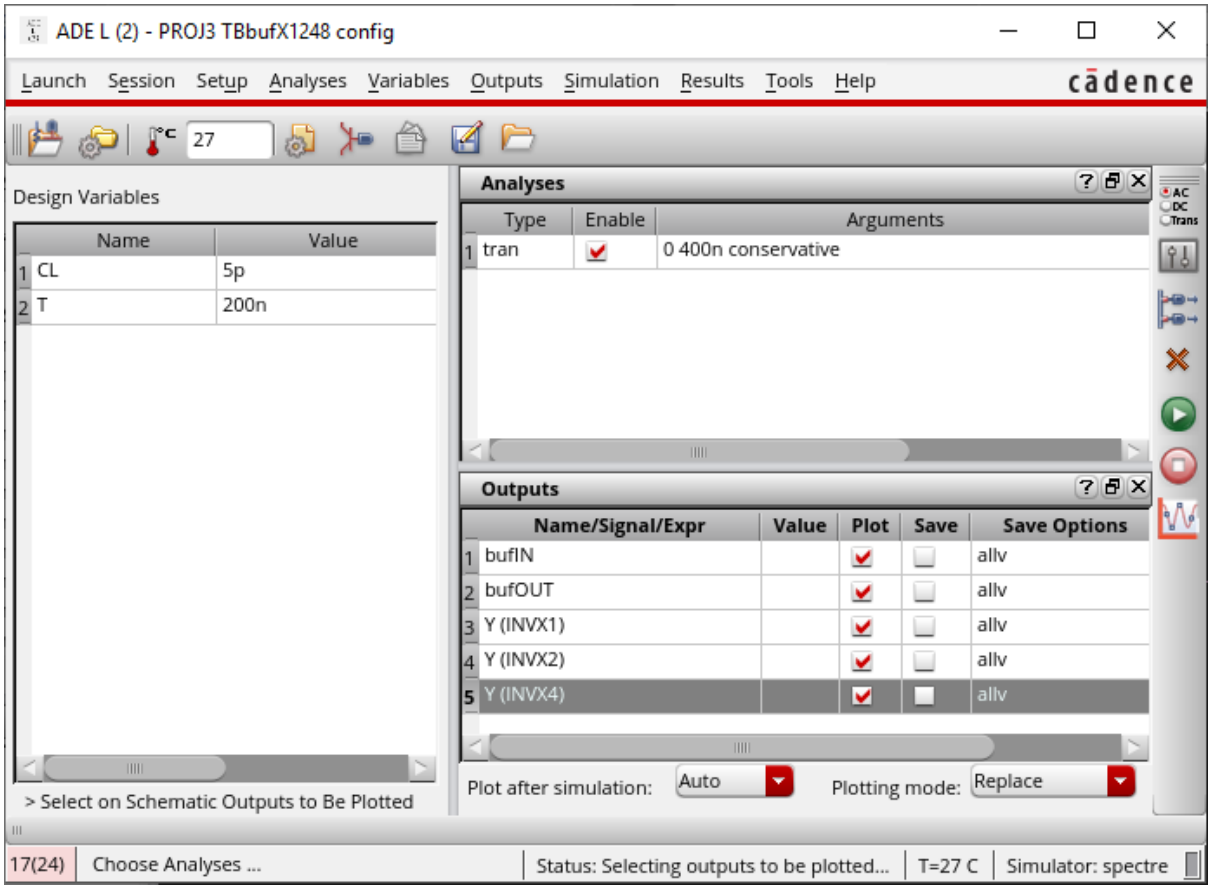


TBbufX1248 schematic



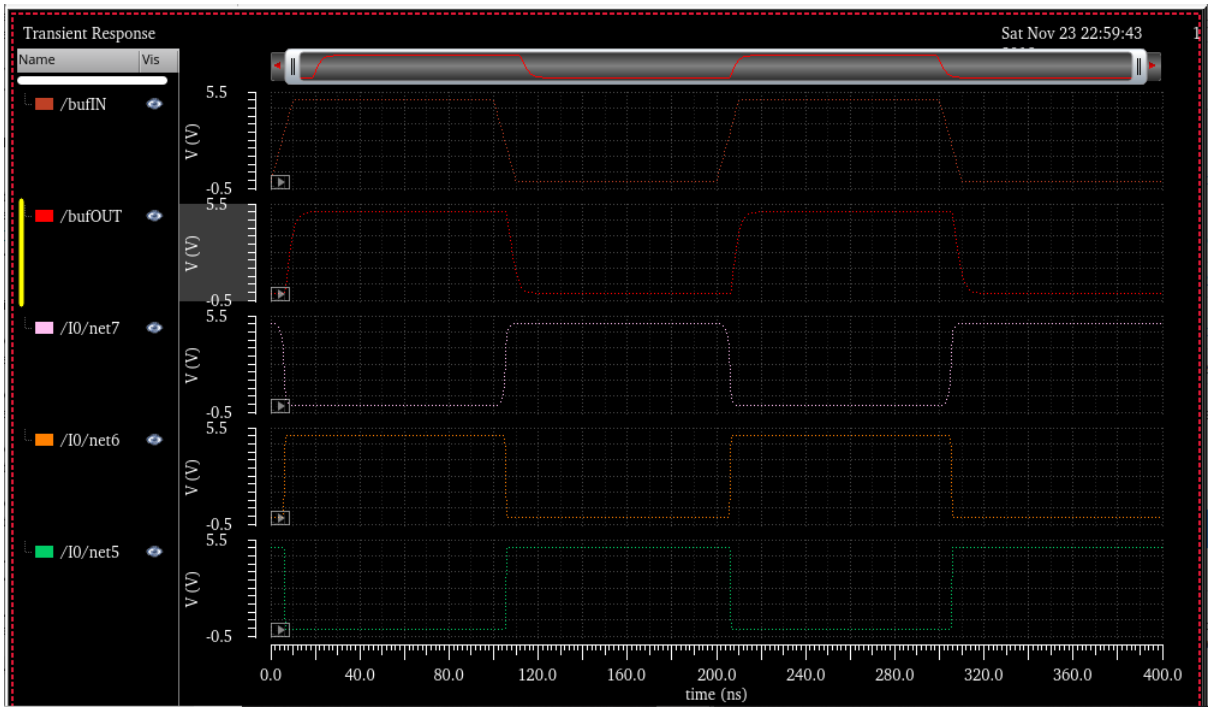
TBbufX1248 config (tree view)





TBbufX1248 ADE L

For the buffer bufX1248, bufIN ≡ A (INVX1), Y (INVX1) ≡ A (INVX2), Y (INVX2) ≡ A (INVX4), Y (INVX4) ≡ A (INVX8) and Y (INVX8) ≡ bufOUT since they are fed directly and hence not re-plotted. In the output below, net7 represents Y (INVX1), net 6 represents Y (INVX2) and net 5 represents Y (INVX4) respectively. The propagation delays are calculated accordingly.



TBbufX1248 output

Device Name	Expression	Value	Delay (s)
INVX1	t_{pdr} (A -> Y)	1.336E-9	1.336ns
	t_{pdf} (A -> Y)	632.5E-12	632.5ps
INVX2	t_{pdr} (A -> Y)	140.9E-12	140.9ps
	t_{pdf} (A -> Y)	161.0E-12	161.0ps
INVX4	t_{pdr} (A -> Y)	229.2E-12	229.2ps
	t_{pdf} (A -> Y)	268.0E-12	268.0ps
INVX8	t_{pdr} (A -> Y)	3.219E-9	3.219ns
	t_{pdf} (A -> Y)	2.646E-9	2.646ns
bufX1248	t_{pdr} (bufIN -> bufOUT)	3.592E-9	3.592ns
	t_{pdf} (bufIN -> bufOUT)	3.443E-9	3.443ns