

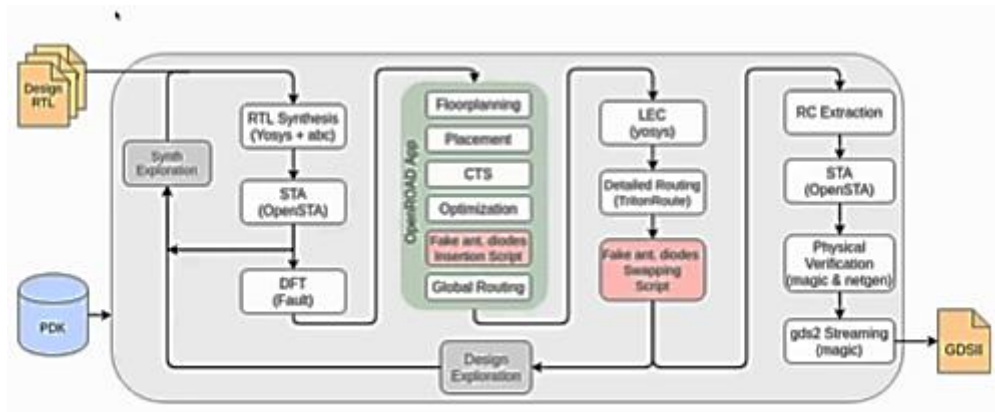
SoC Design Using OpenLANE Report

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Steps covered in the workshop:

1. Macro Hardening
2. SoC Integration

Macro Hardening steps:



First, we clone OpenLANE from Github:

```
Terminal - @db02684dc7...
Terminal - @db02684dc741:/openLANE_flow/openlane_master
File Edit View Terminal Go Help
[root@db02684dc741 openLANE_flow]# git clone https://github.com/efabless/openlane openlane_master
Initialized empty Git repository in /openLANE_flow/openlane_master/.git/
remote: Enumerating objects: 486, done.
remote: Counting objects: 100% (486/486), done.
remote: Compressing objects: 100% (261/261), done.
remote: Total 5142 (delta 306), reused 315 (delta 222), pack-reused 4656
Receiving objects: 100% (5142/5142), 207.47 MiB | 17.76 MiB/s, done.
Resolving deltas: 100% (3446/3446), done.
[root@db02684dc741 openLANE_flow]# ls
AUTHORS.md      configuration  designs      flow.tcl     openlane_master  regression_results  scripts
clean_runs.tcl  CONTRIBUTING.md  doc          LICENSE      README.md        run_designs.py
[root@db02684dc741 openLANE_flow]# cd openlane_master
[root@db02684dc741 openlane_master]# ls
AUTHORS.md      CONTRIBUTING.md  docker_build  Makefile      run_designs.py
clean_runs.tcl  designs          flow.tcl      README.md     scripts
configuration  doc              LICENSE       regression_results  travisCI
[root@db02684dc741 openlane_master]#
```

We are not going to explore this in the labs so I will not proceed with the next commands to set up OpenLANE tool which are:

```
export PDK_ROOT=<absolute path to where skywater-pdk and open_pdk will reside>
make
make test # This is to test that the flow and the pdk were properly installed
```

Steps to implement the lab:

Go to below folder

```
cd work/tools/openlane_working_dir/openLANE_flow
```

Now run below steps

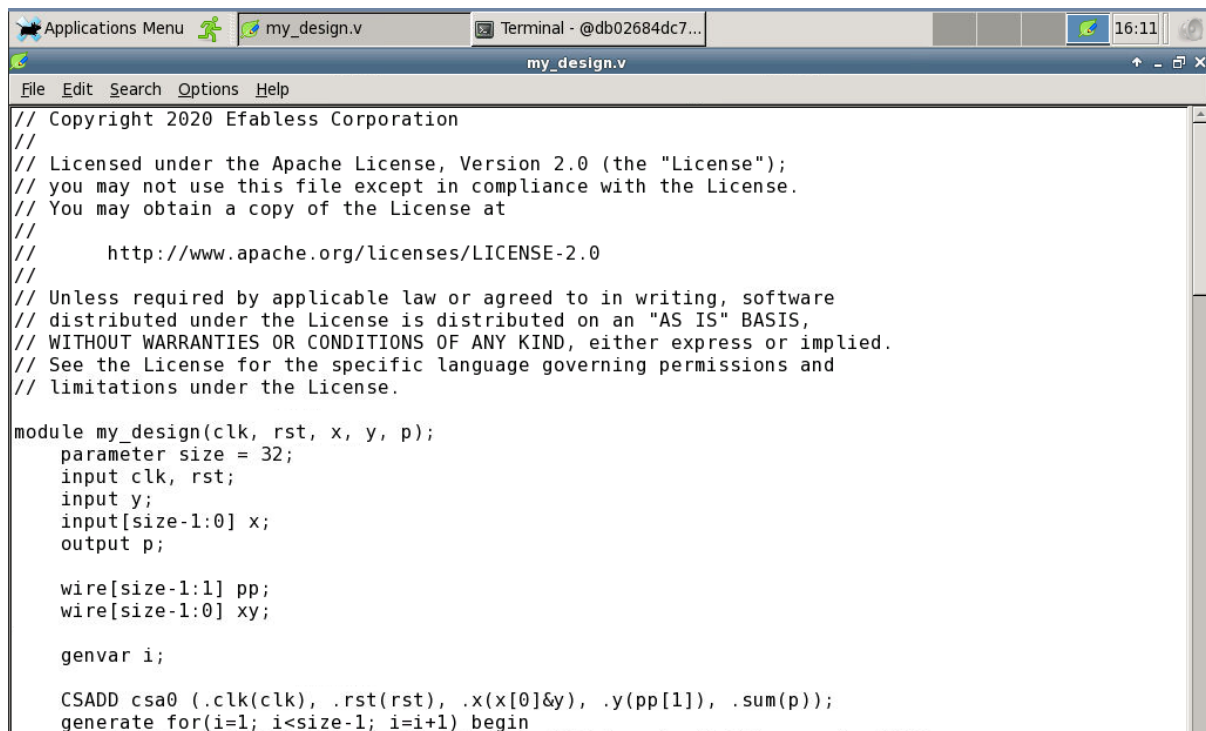
```
mkdir my_sources  
cp designs/spm/src/spm.v my_sources/my_design.v
```

Open my_design.v using below command

```
leafpad my_sources/my_design.v
```

Change top level module name from spm to my_design. Now run below command

```
./flow.tcl -design my_design -src my_sources/my_design.v -  
init_design_config
```



```
// Copyright 2020 Efabless Corporation  
//  
// Licensed under the Apache License, Version 2.0 (the "License");  
// you may not use this file except in compliance with the License.  
// You may obtain a copy of the License at  
//  
//     http://www.apache.org/licenses/LICENSE-2.0  
//  
// Unless required by applicable law or agreed to in writing, software  
// distributed under the License is distributed on an "AS IS" BASIS,  
// WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.  
// See the License for the specific language governing permissions and  
// limitations under the License.  
  
module my_design(clk, rst, x, y, p);  
    parameter size = 32;  
    input clk, rst;  
    input y;  
    input[size-1:0] x;  
    output p;  
  
    wire[size-1:1] pp;  
    wire[size-1:0] xy;  
  
    genvar i;  
  
    CSADD csa0 (.clk(clk), .rst(rst), .x(x[0]&y), .y(pp[1]), .sum(p));  
    generate for(i=1; i<size-1; i=i+1) begin
```



```
Connected (encrypted) to: db02684dc741:20 ()
Terminal - @db02684dc741:/openLANE_flow
File Edit View Terminal Go Help
LEF read, Line 224 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 225 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 227 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 228 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 229 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 265 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 266 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read: Processed 772 lines.
Reading DEF data from file /openLANE_flow/designs/my_design/runs/first_run//results/routing/my_design.n.def.
This action cannot be undone.
  Processed 4 vias total.
  Processed 3307 subcell instances total.
  Processed 38 pins total.
  Processed 2 special nets total.
  Processed 414 nets total.
DEF read: Processed 12304 lines.
[INFO]: Loading my_design

Loading DRC CIF style.
No errors found.
[INFO]: COUNT: 0
[INFO]: Should be divided by 3 or 4
[INFO]: DRC Checking DONE (/openLANE_flow/designs/my_design/runs/first_run//logs/magic/magic.drc)
[INFO]: Saving mag view with DRC errors(/openLANE_flow/designs/my_design/runs/first_run//results/magic/my_design.drc.mag)
[INFO]: Saved
[INFO]: Running LVS...
[INFO]: /openLANE_flow/designs/my_design/runs/first_run//results/magic/my_design.spice against /openLANE_flow/designs/my_design/runs/first_run//results/synthesis/my_design.synthesis preroute.v
```

```
Connected (encrypted) to: db02684dc741:20 ()
Terminal - @db02684dc741:/openLANE_flow
File Edit View Terminal Go Help
Class: skyl130_fd_sc_hd_inv_8 instances: 63
Class: skyl130_fd_sc_hd_clkbuf_1 instances: 8
Class: skyl130_fd_sc_hd_a2lboi_4 instances: 1
Class: skyl130_fd_sc_hd_or2_4 instances: 1
Class: skyl130_fd_sc_hd_and2_4 instances: 32
Class: skyl130_fd_sc_hd_o22a_4 instances: 31
Class: skyl130_fd_sc_hd_diode_2 instances: 759
Class: skyl130_fd_sc_hd_tapvpwrvgn_1 instances: 229
Circuit contains 416 nets.

Circuit 1 contains 1367 devices, Circuit 2 contains 1367 devices.
Circuit 1 contains 416 nets, Circuit 2 contains 416 nets.

Circuits match with 223 symmetries.
Netlists match with 223 symmetries.
Circuits match correctly.
Result: Circuits match uniquely.
Logging to file "/openLANE_flow/designs/my_design/runs/first_run//results/lvs/my_design.lvs.log" disabled
LVS Done.
LVS reports no net, device, pin, or property mismatches.

Total errors = 0

Magic 8.3 revision 37 - Compiled on Mon Jul 20 03:07:05 UTC 2020.
Starting magic under Tcl interpreter
Using the terminal as the console.
Using NULL graphics device.
Processing system .magicrc file
Sourcing design .magicrc for technology skyl130A ...
```

No DRC or LVS errors! That is a good sign.

```
Connected (encrypted) to: db02684dc741:20 ()
Terminal - @db02684dc741:/openLANE_flow
File Edit View Terminal Go Help
skyl30_fd_sc_hd_decap_6: 2 warnings
Extracting skyl30_fd_sc_hd_xor2_4 into skyl30_fd_sc_hd_xor2_4.ext:
Completed 100%
Extracting skyl30_fd_sc_hd_decap_12 into skyl30_fd_sc_hd_decap_12.ext:
skyl30_fd_sc_hd_decap_12: 2 warnings
Extracting skyl30_fd_sc_hd_decap_3 into skyl30_fd_sc_hd_decap_3.ext:
skyl30_fd_sc_hd_decap_3: 2 warnings
Extracting skyl30_fd_sc_hd_diode_2 into skyl30_fd_sc_hd_diode_2.ext:
Extracting skyl30_fd_sc_hd_fill_2 into skyl30_fd_sc_hd_fill_2.ext:
Extracting my_design into my_design.ext:
Completed 5%
Completed 10%
Completed 16%
Completed 21%
Completed 26%
Completed 31%
Completed 36%
Completed 41%
Completed 47%
Completed 52%
Completed 57%
Completed 62%
Completed 67%
Completed 72%
Completed 78%
Completed 83%
Completed 88%
Completed 93%
Completed 98%
Completed 100%
```

Debugging completed.

```
Connected (encrypted) to: db02684dc741:20 ()
Applications Menu yosys_2.stat.rpt Terminal - @db02684dc7... 16:56
yosys_2.stat.rpt
File Edit Search Options Help
17. Printing statistics.
=== my_design ===
Number of wires: 374
Number of wire bits: 405
Number of public wires: 39
Number of public wire bits: 70
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 370
  skyl30_fd_sc_hd_a2lboi_4 1
  skyl30_fd_sc_hd_a2bb2o_4 31
  skyl30_fd_sc_hd_and2_4 32
  skyl30_fd_sc_hd_buf_1 116
  skyl30_fd_sc_hd_dfrtp_4 64
  skyl30_fd_sc_hd_inv_8 63
  skyl30_fd_sc_hd_o22a_4 31
  skyl30_fd_sc_hd_or2_4 1
  skyl30_fd_sc_hd_xor2_4 31
Chip area for module '\my_design': 5311.344000
```

Scenario 1 (open config.tcl using leafpad and add below lines):

```
set ::env(FP_ASPECT_RATIO) "1"
set ::env(PL_TARGET_DENSITY) "0.8"
```

Run below command:

```
./flow.tcl -design my_design -tag first_run -overwrite
```

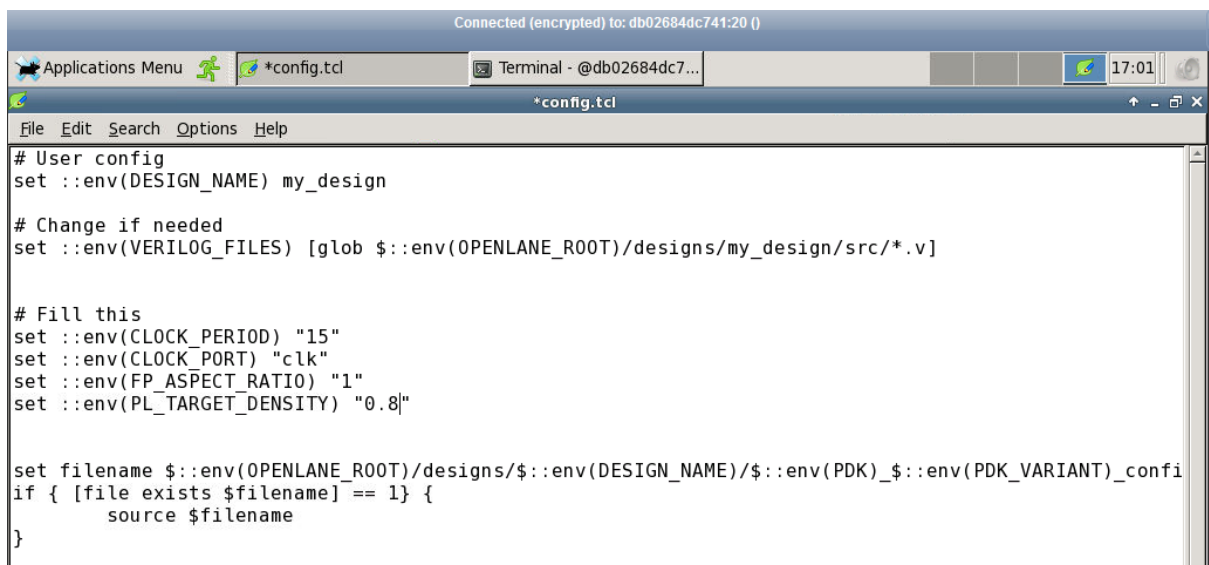
Once the run finishes, type below command

```
cd designs/my_design/runs/first_run/results/magic
magic -T
~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic/sky130A.tech my_design.mag
```

Select whole layout area by left click on bottom left of design and right click on top right of the design and press keypad S

Then on tkcon, type below command:

box

A screenshot of a terminal window titled "Connected (encrypted) to: db02684dc741:20 ()". The window shows a file editor with the file name "*config.tcl". The file contains TCL code for setting environment variables and file paths. The code includes comments and several 'set' commands for variables like DESIGN_NAME, VERILOG_FILES, CLOCK_PERIOD, CLOCK_PORT, FP_ASPECT_RATIO, and PL_TARGET_DENSITY. It also includes a conditional block to source a file if it exists.

```
File Edit Search Options Help
# User config
set ::env(DSIGN_NAME) my_design

# Change if needed
set ::env(VERILOG_FILES) [glob $::env(OPENLANE_ROOT)/designs/my_design/src/*.v]

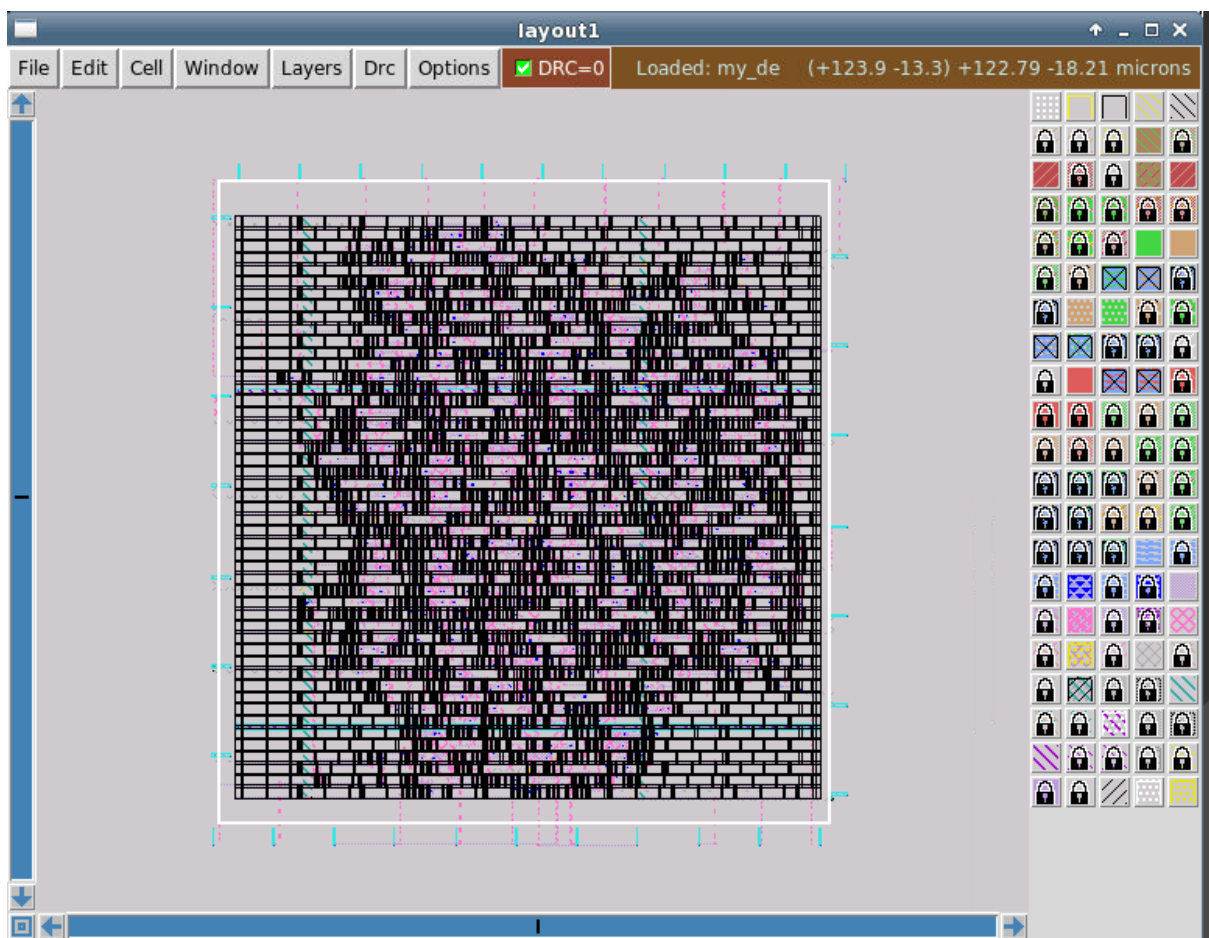
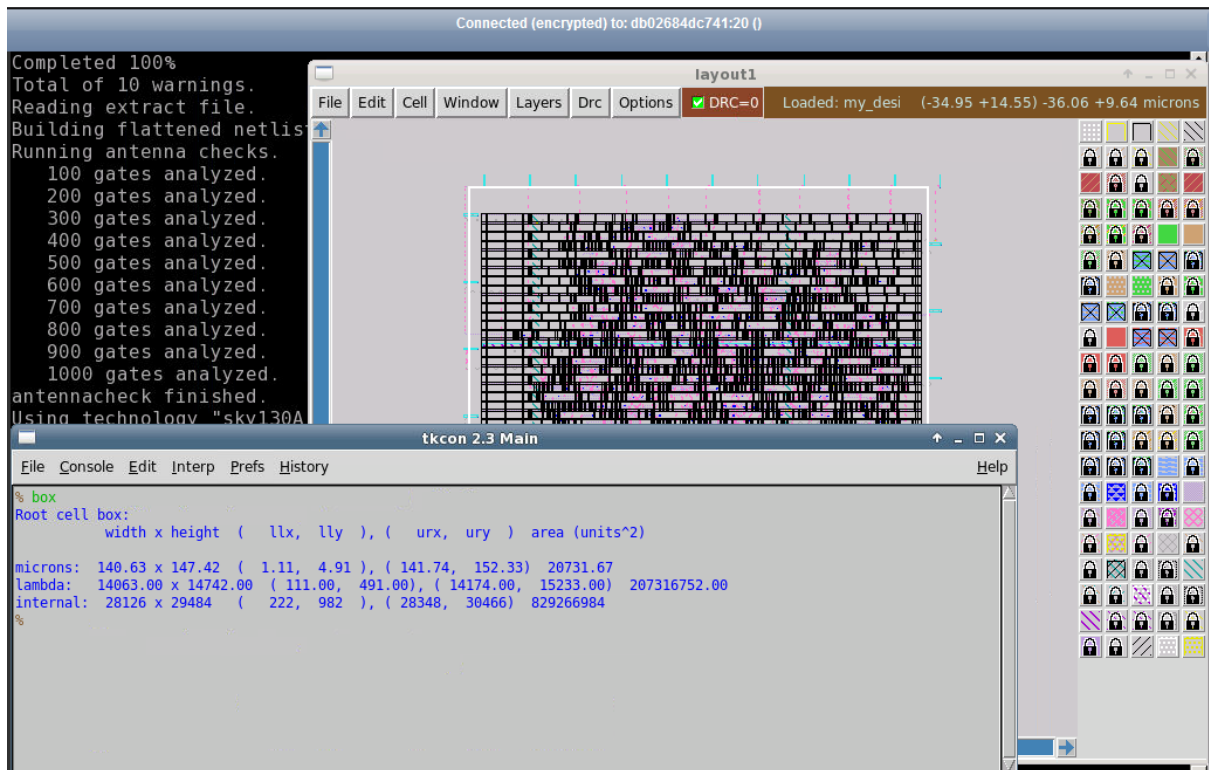
# Fill this
set ::env(CLOCK_PERIOD) "15"
set ::env(CLOCK_PORT) "clk"
set ::env(FP_ASPECT_RATIO) "1"
set ::env(PL_TARGET_DENSITY) "0.8"

set filename $::env(OPENLANE_ROOT)/designs/$::env(DSIGN_NAME)/$::env(PDK)_$::env(PDK_VARIANT)_confi
if { [file exists $filename] == 1 } {
    source $filename
}
```

A screenshot of a terminal window showing the OpenLane logo in a stylized, blocky font. Below the logo, there are several status messages in green text. The messages indicate the version (N/A), the design configuration path, the removal of an existing run, the merging of LEFs, and the matching of sites and macros for the sky130_fd_sc_hd.lef file. The terminal ends with a green cursor.

```

[INFO]: Version: N/A
[INFO]: Using design configuration at /openLANE_flow/designs/my_design/config.tcl
[INFO]: Removing exisiting run /openLANE_flow/designs/my_design/runs/first_run/
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITES matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
mergeLef.py : Merging LEFs complete
```

Done!