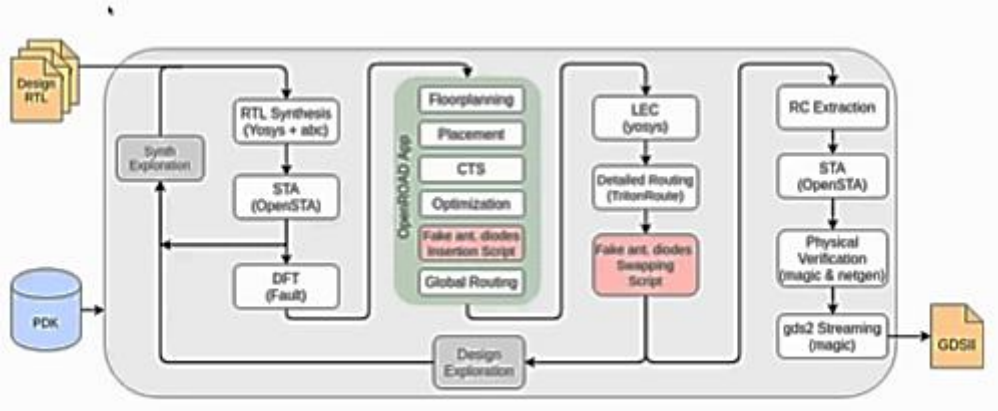
SoC Design Using OpenLANE Report

Arijit Sengupta, 09th October 2020

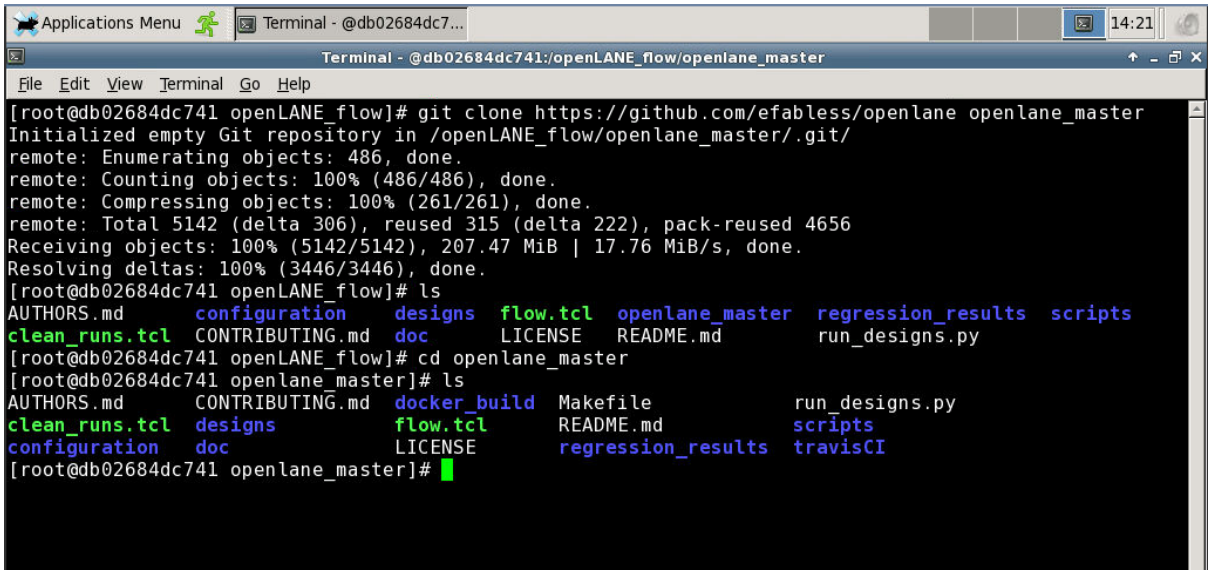
Steps covered in the workshop:

1. Macro Hardening
2. SoC Integration

Macro Hardening steps:



First, we clone OpenLANE from GIthub:



We are not going to explore this in the labs so I will not proceed with the next commands to set up OpenLANE tool which are:

```
export PDK_ROOT=<absolute path to where skywater-pdk and open_pdks will reside>
make
make test # This is to test that the flow and the pdk were properly installed
```

Steps to implement the lab:

Go to below folder

```
cd work/tools/openlane_working_dir/openLANE_flow
```

Now run below steps

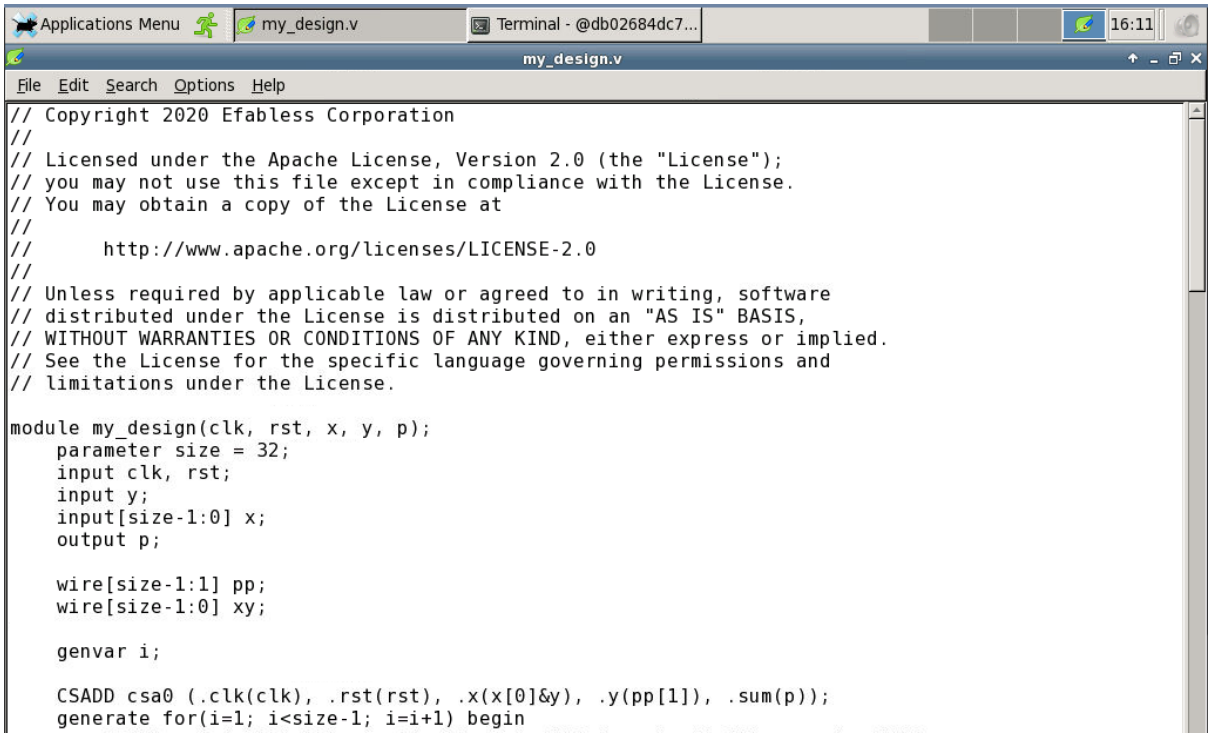
```
mkdir my_sources
cp designs/spm/src/spm.v my_sources/my_design.v
```

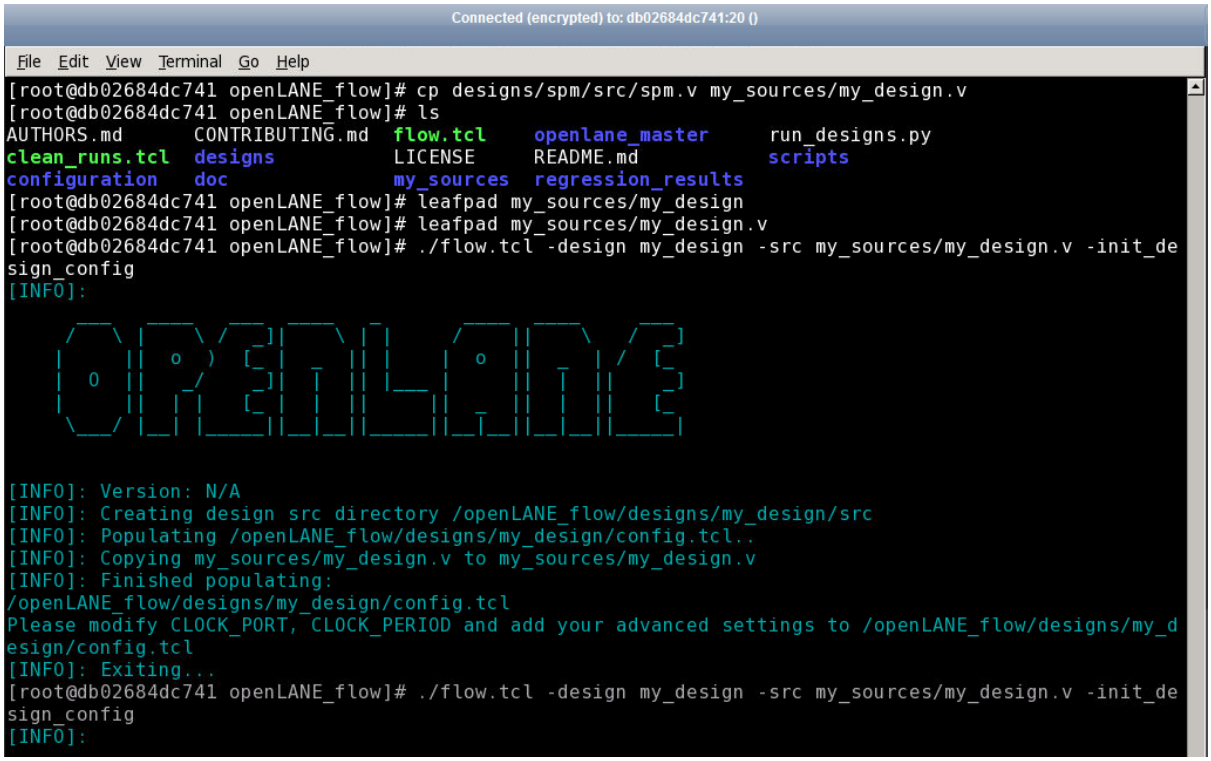
Open my_design.v using below command

```
leafpad my_sources/my_design.v
```

Change top level module name from spm to my_design. Now run below command

```
./flow.tcl -design my_design -src my_sources/my_design.v -
init_design_config
```





Open below file:

```
leafpad designs/my_design/config.tcl
```

Change clock period as shown in video; Save and close. Run below command

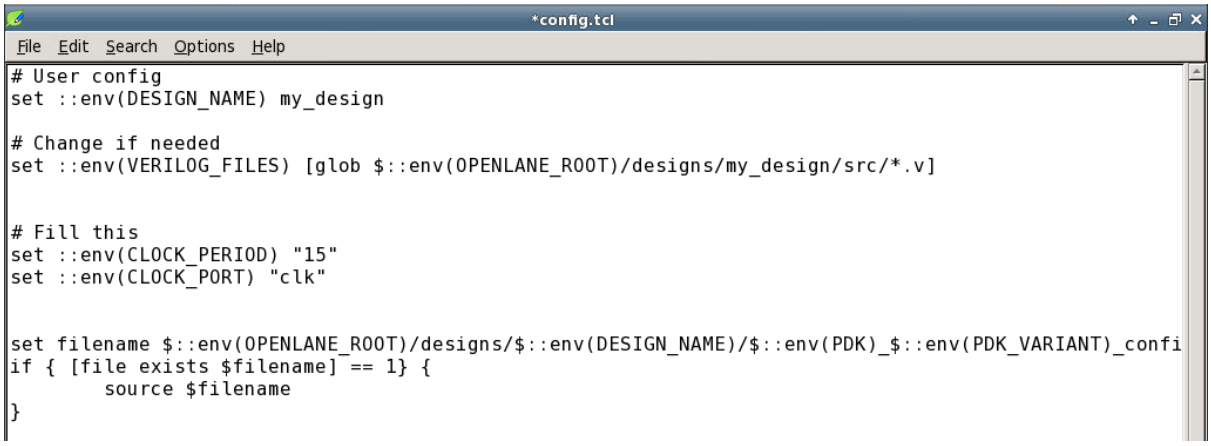
```
./flow.tcl -design my_design -tag first_run
```

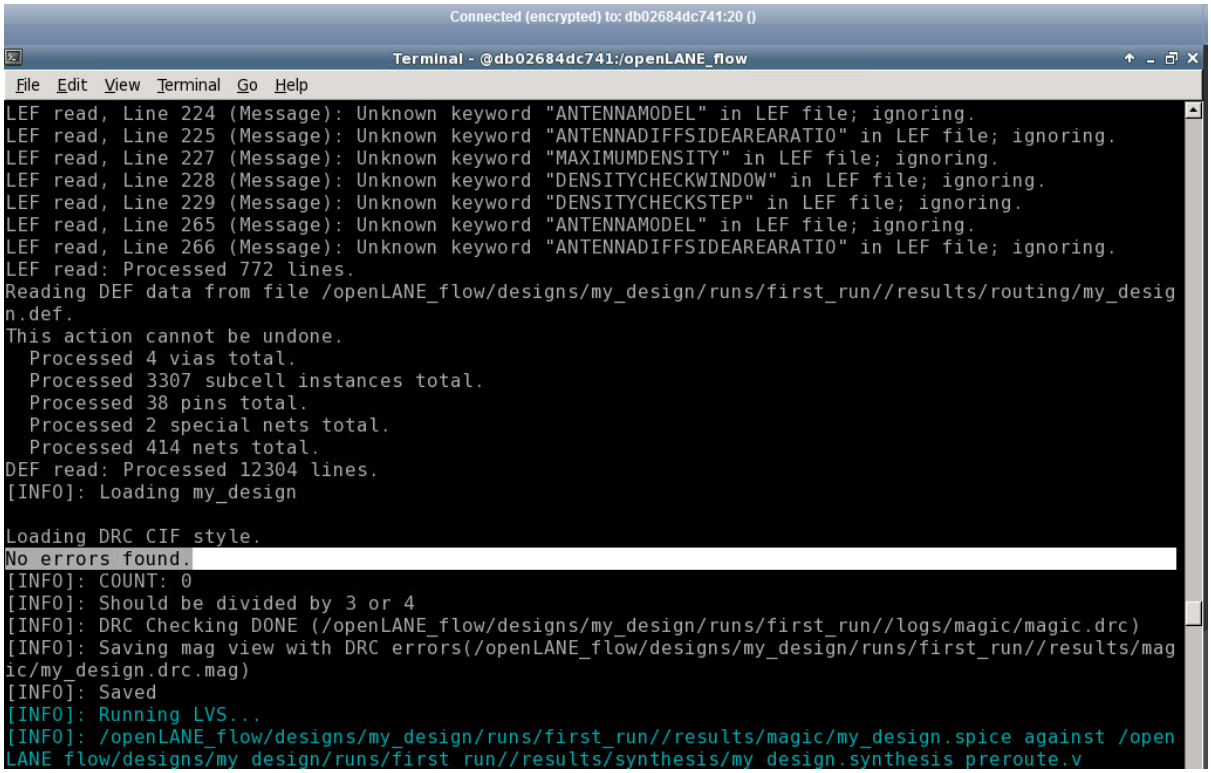
Post synthesis, what is the Flip-Flop (FF) ratio for the design?

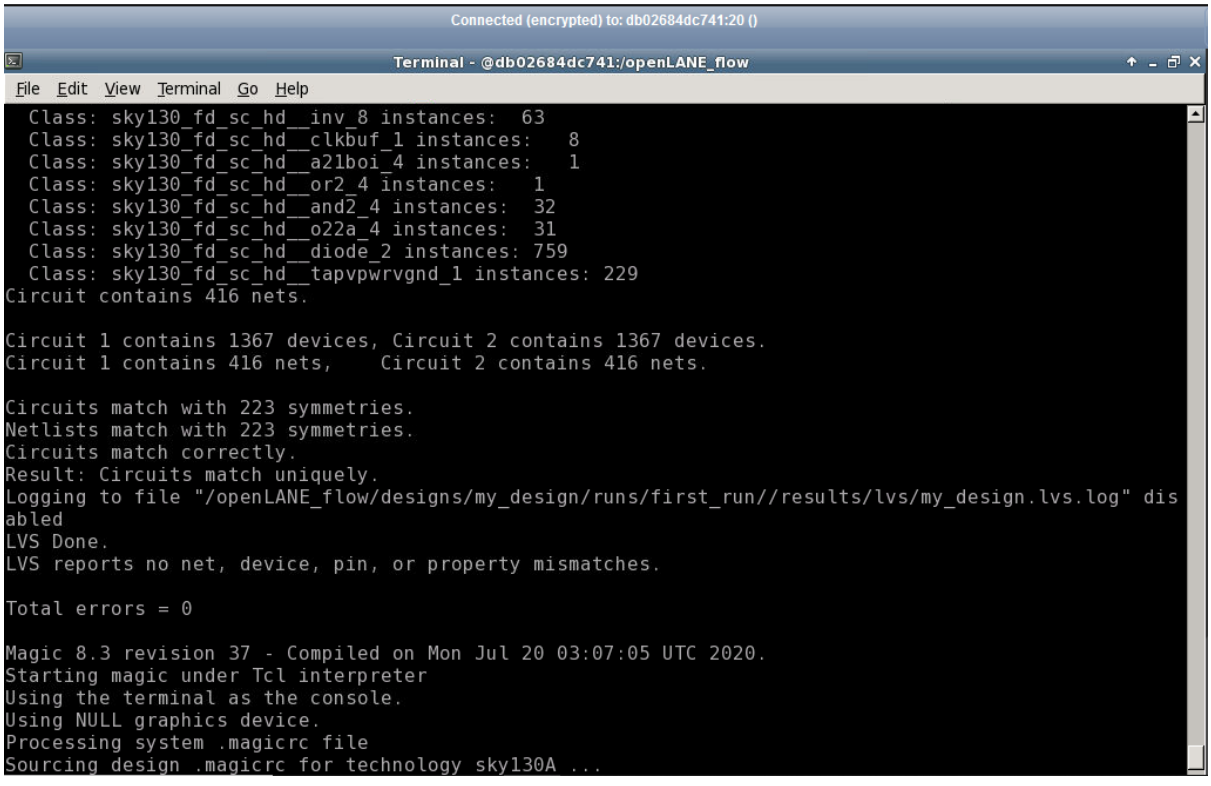
1) Flop ratio = Total no. of FFs / Total number of cells = **0.172**

2) Look for correct yosys stat file in below folder

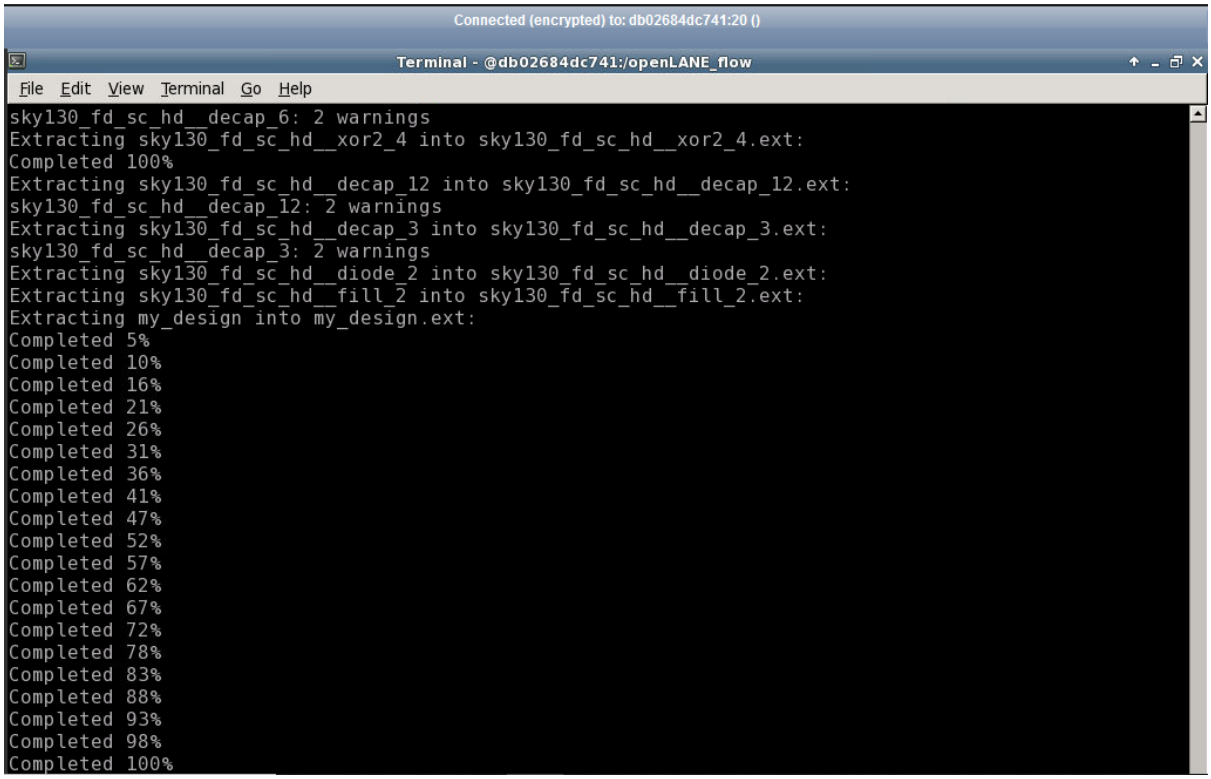
```
leafpad designs/my_design/runs/first_run/reports/synthesis/yosys_2.stat
```



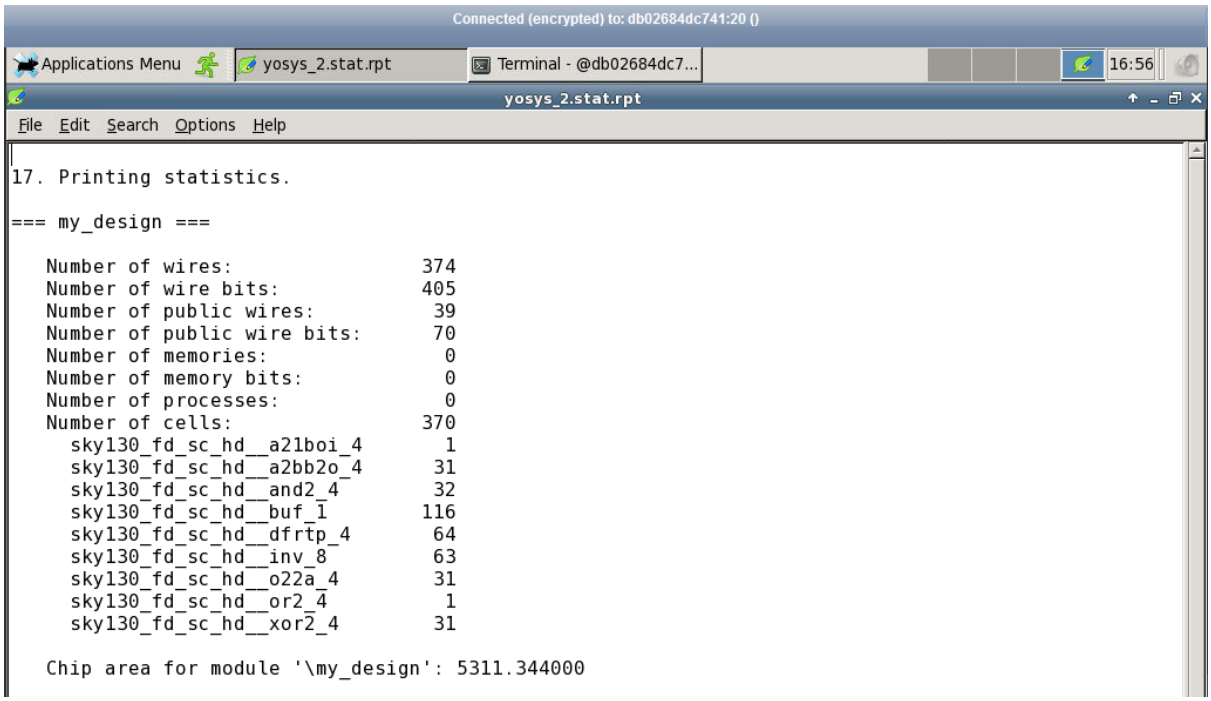




No DRC or LVS errors! That is a good sign.



Debugging completed.



Scenario 1 (open config.tcl using leafpad and add below lines):

```
set ::env(FP_ASPECT_RATIO) “1”
set ::env(PL_TARGET_DENSITY) “0.8”
```

Run below command:

```
./flow.tcl -design my_design -tag first_run -overwrite
```

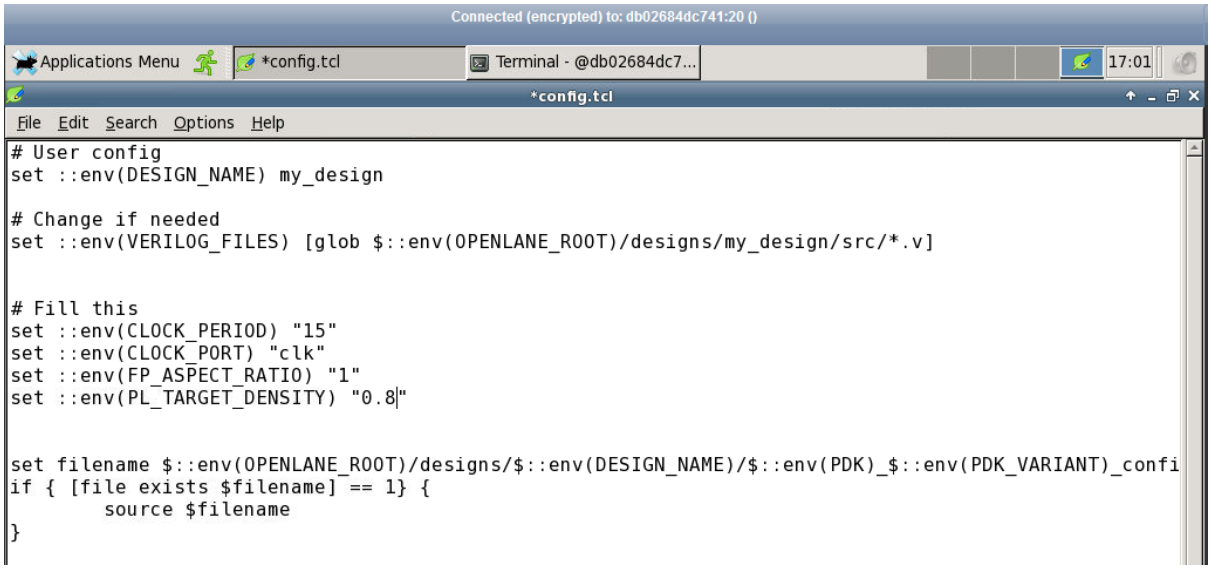
Once the run finishes, type below command

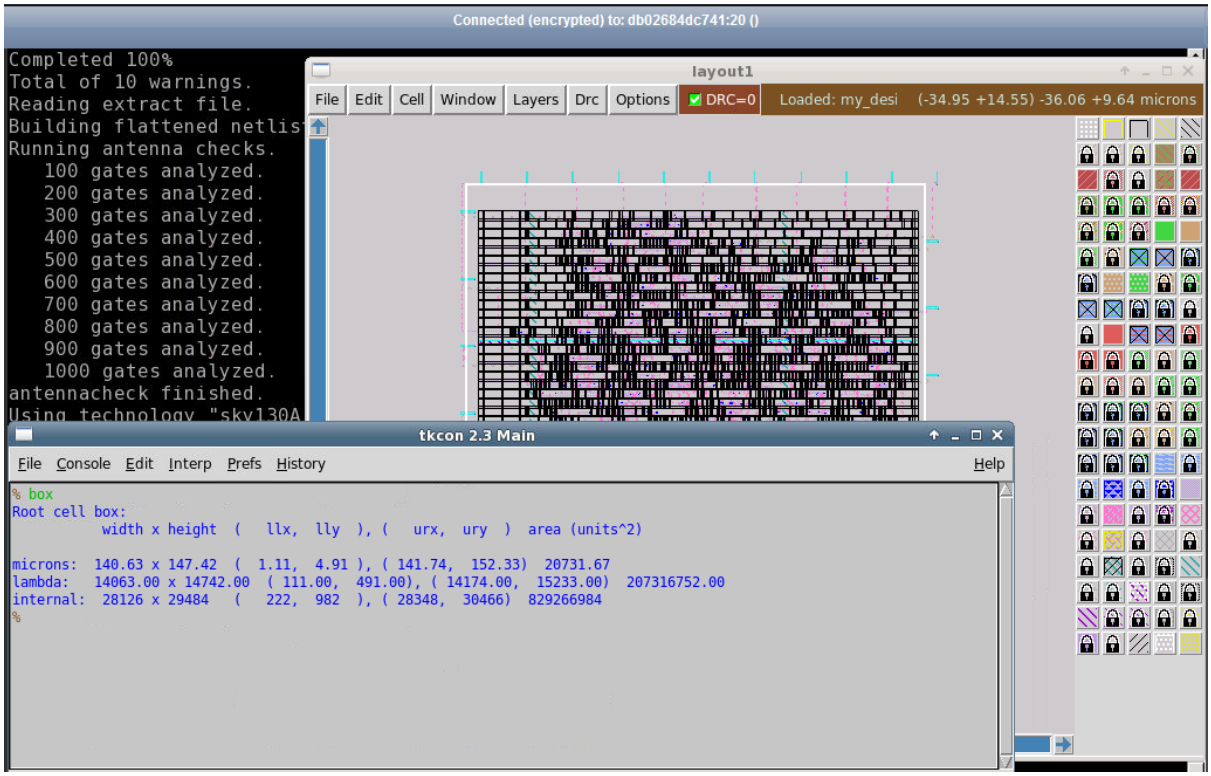
```
cd designs/my_design/runs/first_run/results/magic
magic -T
~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic/sky1
30A.tech   my_design.mag
```

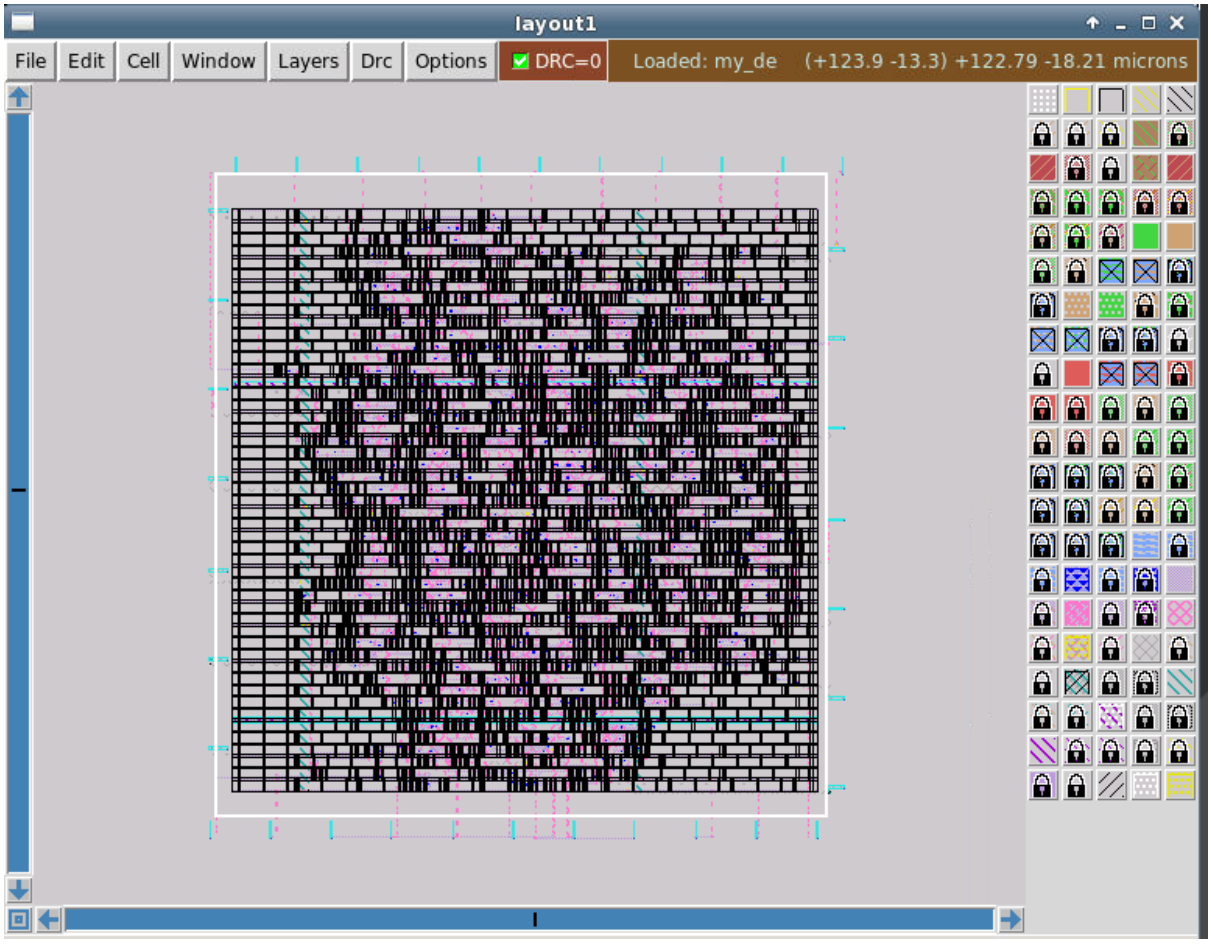
Select whole layout area by left click on bottom left of design and right click on top right of the design and press keypad S

Then on tkcon, type below command:

```
box
```




Connected (encrypted) to: db02684dc741:20 ()
Completed 100%
Total of 10 warnings.
Reading extract file.
Building flattened netlis
Running antenna checks.
100 gates analyzed.
200 gates analyzed.
300 gates analyzed.
400 gates analyzed.
500 gates analyzed.
600 gates analyzed.
700 gates analyzed.
800 gates analyzed.
900 gates analyzed.
1000 gates analyzed.
antennacheck finished.
Using technology "sky130A
layout1
File Edit Cell Window Layers Drc Options DRC=0 Loaded: my_desi (-34.95 +14.55) -36.06 +9.64 microns
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
% box
Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)
microns: 140.63 x 147.42 (1.11, 4.91), (141.74, 152.33) 20731.67
lambda: 14063.00 x 14742.00 (111.00, 491.00), (14174.00, 15233.00) 207316752.00
internal: 28126 x 29484 (222, 982), (28348, 30466) 829266984
%


layout1
File Edit Cell Window Layers Drc Options DRC=0 Loaded: my_de (+123.9 -13.3) +122.79 -18.21 microns

Done!