

Open Source EDA Tool Development Report

Arijit Sengupta, 07th October 2020

Command to fetch files:

```
 wget http://opencircuitdesign.com/open\_pdks/archive/drc\_tests.tgz
 tar xfz drc_tests.tgz
```

```
Connected (encrypted) to: ed9092bb87e2:20 ()  

File Edit View Terminal Go Help  

[root@ed9092bb87e2 openLANE_flow]# wget http://opencircuitdesign.com/open_pdks/a
rchive/drc_tests.tgz
--2020-10-07 15:27:12-- http://opencircuitdesign.com/open_pdks/archive/drc_test
s.tgz
Resolving opencircuitdesign.com... 69.251.36.209
Connecting to opencircuitdesign.com|69.251.36.209|:80... connected.
HTTP request sent, awaiting response... 200 OK
Length: 41651 (41K) [application/x-gzip]
Saving to: 000drc_tests.tgz000

100%[=====] 41,651      58.0K/s   in 0.7s

2020-10-07 15:27:13 (58.0 KB/s) - 000drc_tests.tgz000 saved [41651/41651]

[root@ed9092bb87e2 openLANE_flow]# ls
AUTHORS.md      CONTRIBUTING.md  drc_tests.tgz  README.md      scripts
clean_runs.tcl  designs        flow.tcl     regression_results
configuration  doc           LICENSE      run_designs.py
[root@ed9092bb87e2 openLANE_flow]# tar xfz drc_tests.tgz
[root@ed9092bb87e2 openLANE_flow]# ls
AUTHORS.md      designs        flow.tcl     run_designs.py
clean_runs.tcl  doc           LICENSE      scripts
configuration  drc_tests     README.md
CONTRIBUTING.md drc_tests.tgz regression_results
[root@ed9092bb87e2 openLANE_flow]# cd drc_tests
[root@ed9092bb87e2 drc_tests]# ls
capm.mag       hvtr.mag     mcon.mag    met4.mag    nwell.mag   rpm.mag    via2.mag
difftap.mag    licon.mag    met1.mag    met5.mag    pad.mag     sky130A.tech via3.mag
dnwell.mag    li.mag       met2.mag    npc.mag    poly.mag    tunn.mag   via4.mag
hvtp.mag       lvtn.mag    met3.mag    nsd.mag    psd.mag    varac.mag  via.mag
[root@ed9092bb87e2 drc_tests]#
```

```
Connected (encrypted) to: ed9092bb87e2:20 ()  

File Edit View Terminal Go Help  

puts stdout "Sourcing design .magicrc for technology sky130A ..."  

# Put grid on 0.005 pitch. This is important, as some commands don't
# rescale the grid automatically (such as lef read?).  

set scalefac [tech lambda]
if {[lindex $scalefac 1] < 2} {
    scalegrid 1 2
}

# drc off
drc euclidean on

# Allow override of PDK path from environment variable PDKPATH
if {[catch {set PDKPATH $env(PDKPATH)}]} {
    set PDKPATH "~/cad/pdks/sky130A"
}

# loading technology
# tech load $PDKPATH/libs.tech/magic/sky130A.tech
tech load sky130A.tech

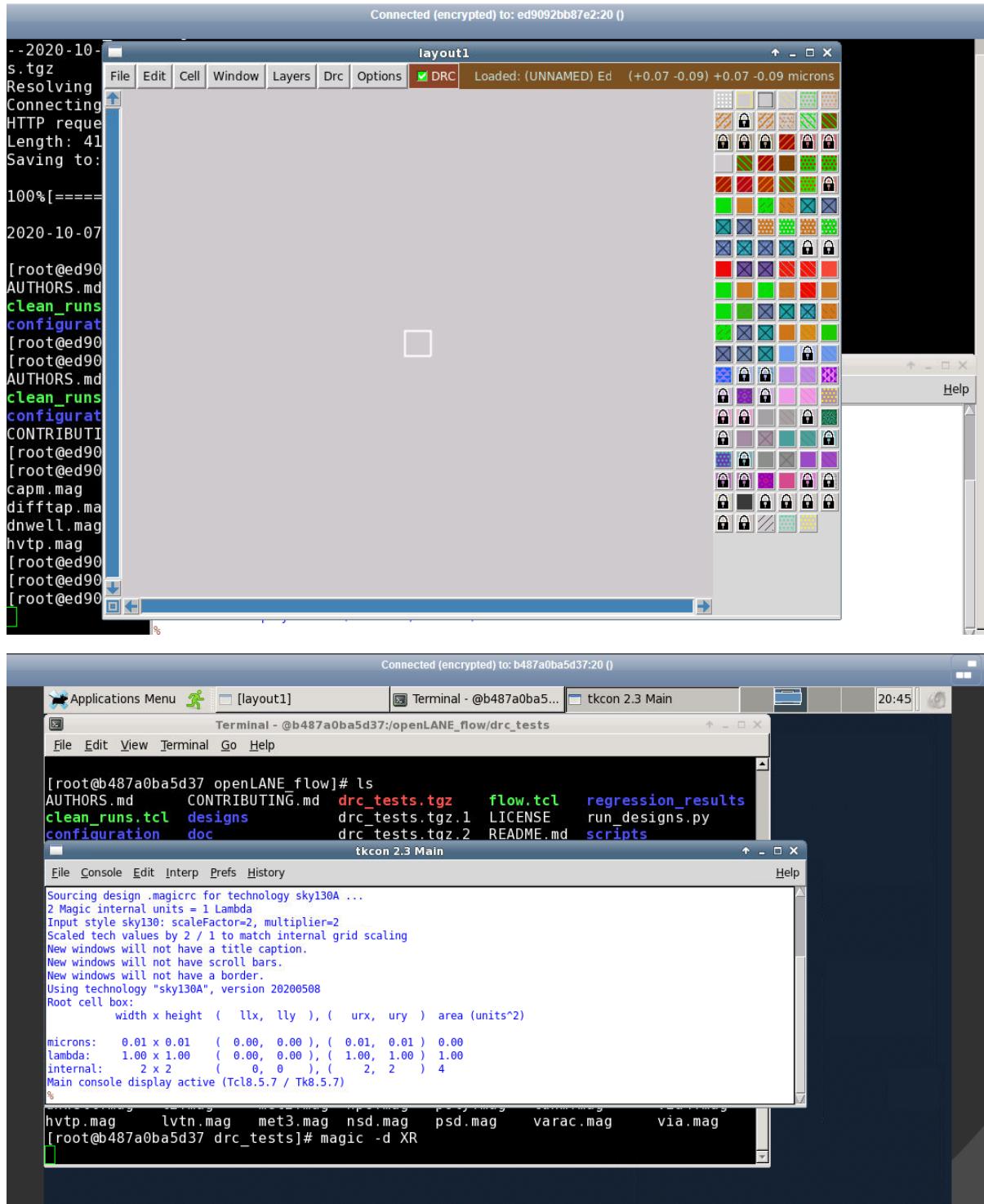
# load device generator
# source $PDKPATH/libs.tech/magic/sky130A.tcl

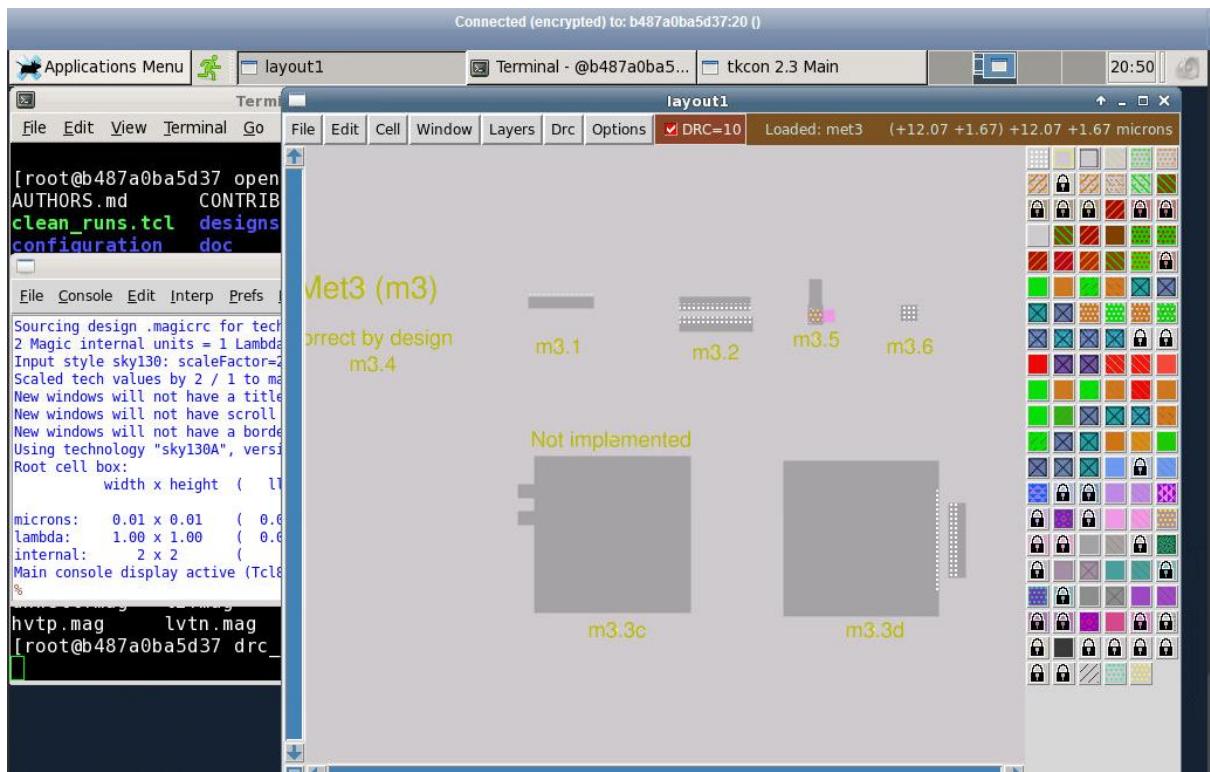
# load bind keys (optional)
# source $PDKPATH/libs.tech/magic/sky130A-BindKeys

# set units to lambda grid
snap lambda
```

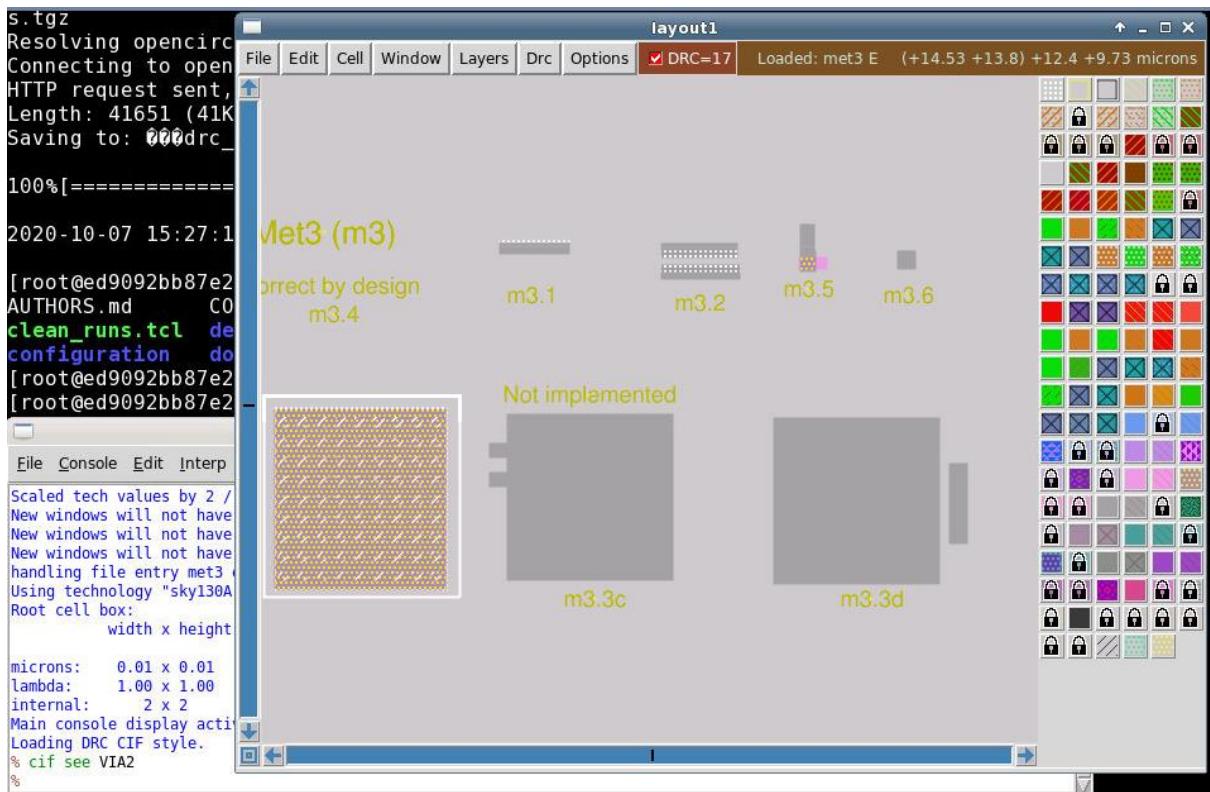
Rules can be found at <https://skywater-pdk.readthedocs.io/en/latest/rules.html>

Command to launch magic: `magic -d XR`

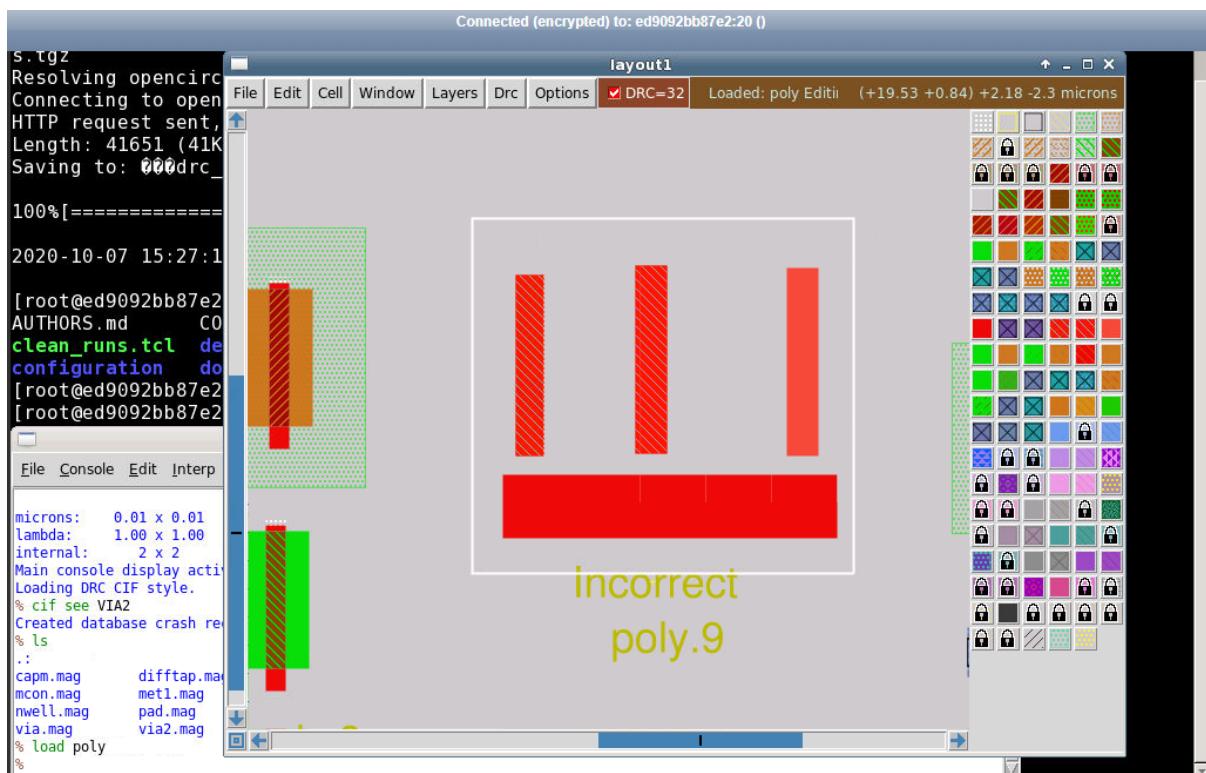


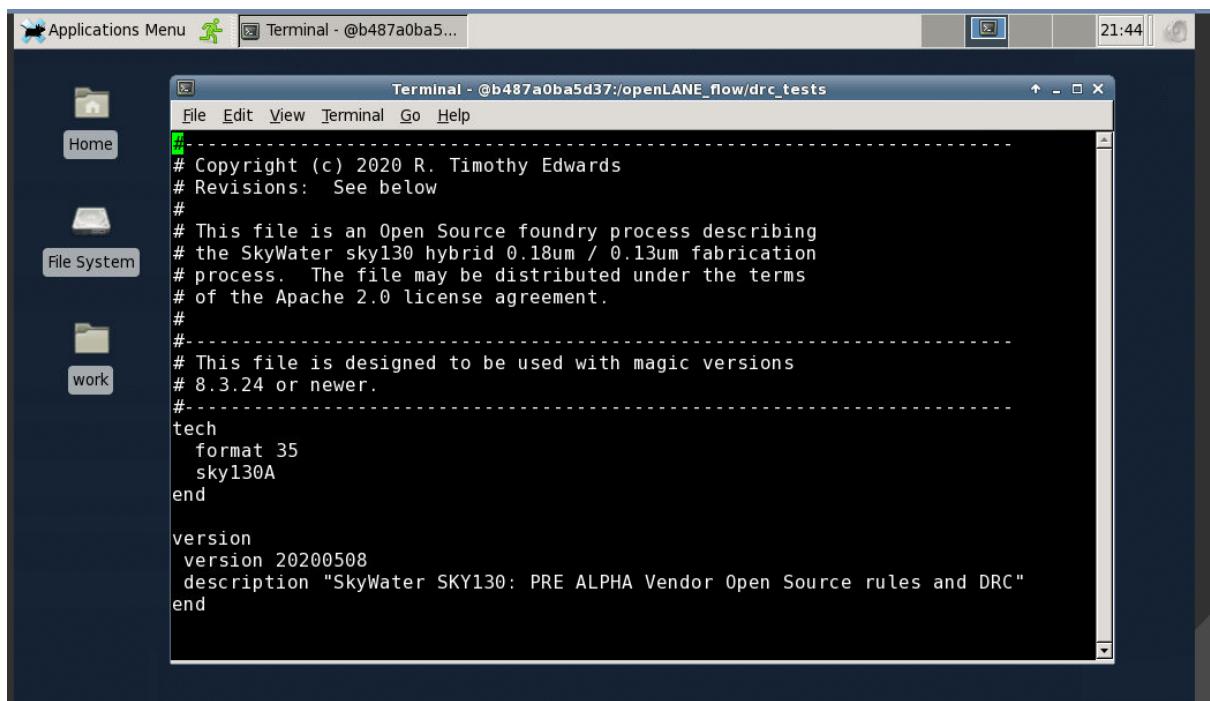
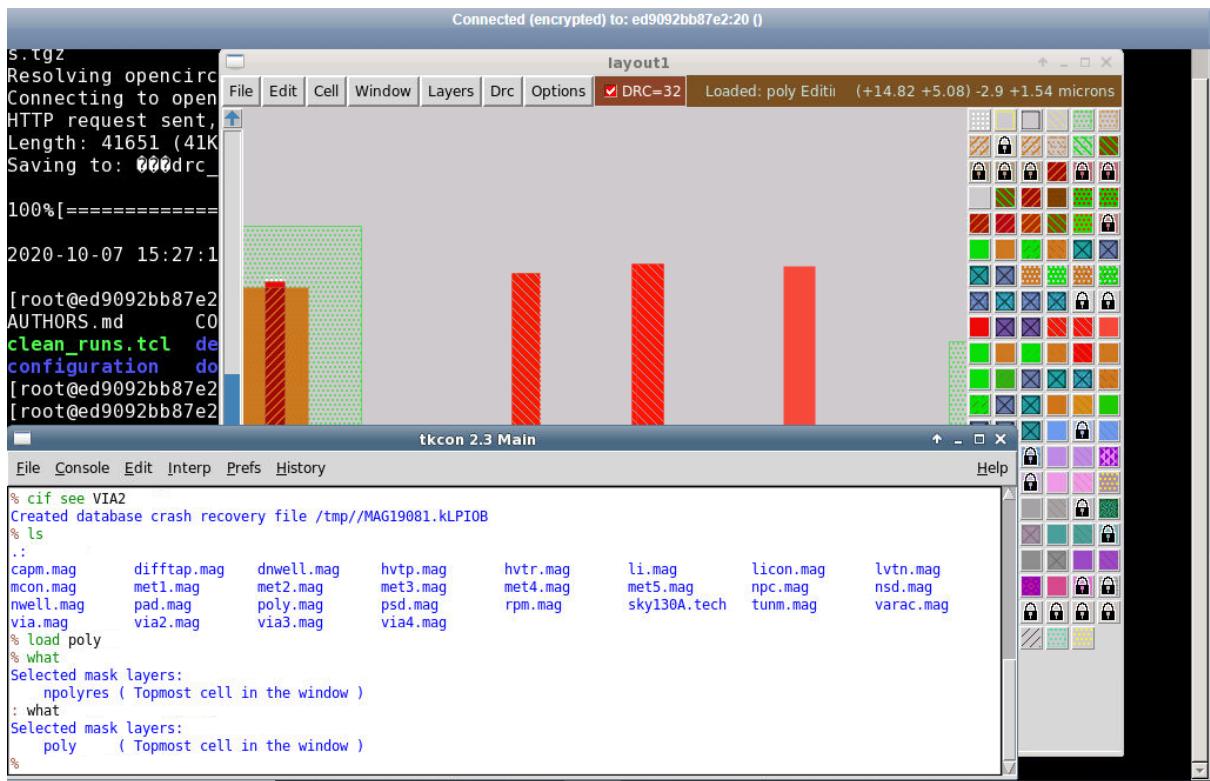


After drawing met3 contact, type *cif see VIA2*



Now, we load poly.





The screenshot shows a Linux desktop environment with a dark theme. A terminal window titled "Terminal - @b487a0ba5d37:/openLANE_flow/drc_tests" is open, displaying a command-line interface for a CAD tool. The terminal window has a menu bar with "File", "Edit", "View", "Terminal", "Go", and "Help". The main area of the terminal shows a configuration file or command script. The text in the terminal includes:

```
width xhrpoly 350 "xhrpoly resistor width < %d (poly.1a)"
# NOTE: xhrpoly resistor requires choice of discrete widths 0.35, 0.69, ... up
to 1.27.

#-----
# uhrpoly (P+ poly resistor, 2kOhm/sq)
#-----

width uhrpoly 350 "uhrpoly resistor width < %d"
spacing xhrpoly,uhrpoly,xpc alldiff 480 touching_illegal \
    "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"

spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
    "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"

#-----
# MOS Varactor device rules
#-----

overhang *nsd var,varhvt 250 \
"N-Tap overhang of Varactor < %d (var.4)"

overhang *mvnsd mvvar 250 \
-- INSERT --
```

The screenshot shows a Linux desktop environment with a dark theme. A terminal window titled "Terminal - @b487a0ba5d37:/openLANE_flow/drc_tests" is open, displaying a command-line interface for a CAD tool. The terminal window has a menu bar with "File", "Edit", "View", "Terminal", "Go", and "Help". The main area of the terminal shows a configuration file or command script. The text in the terminal includes:

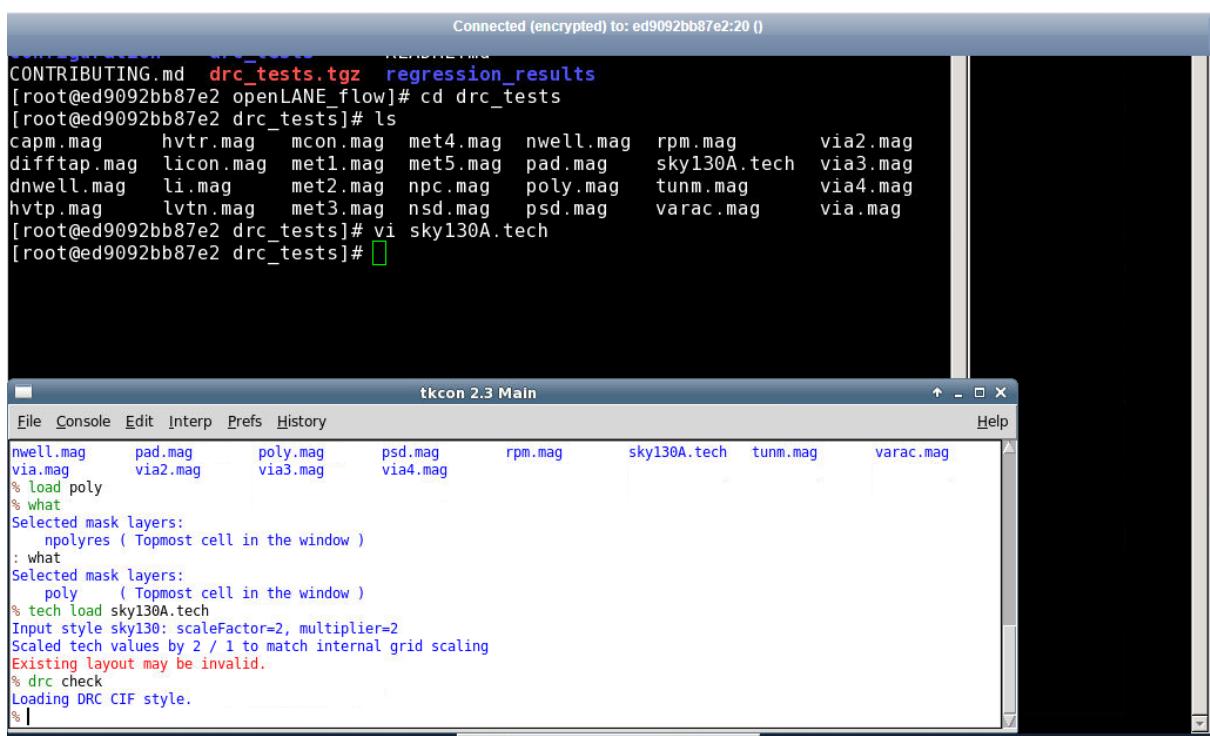
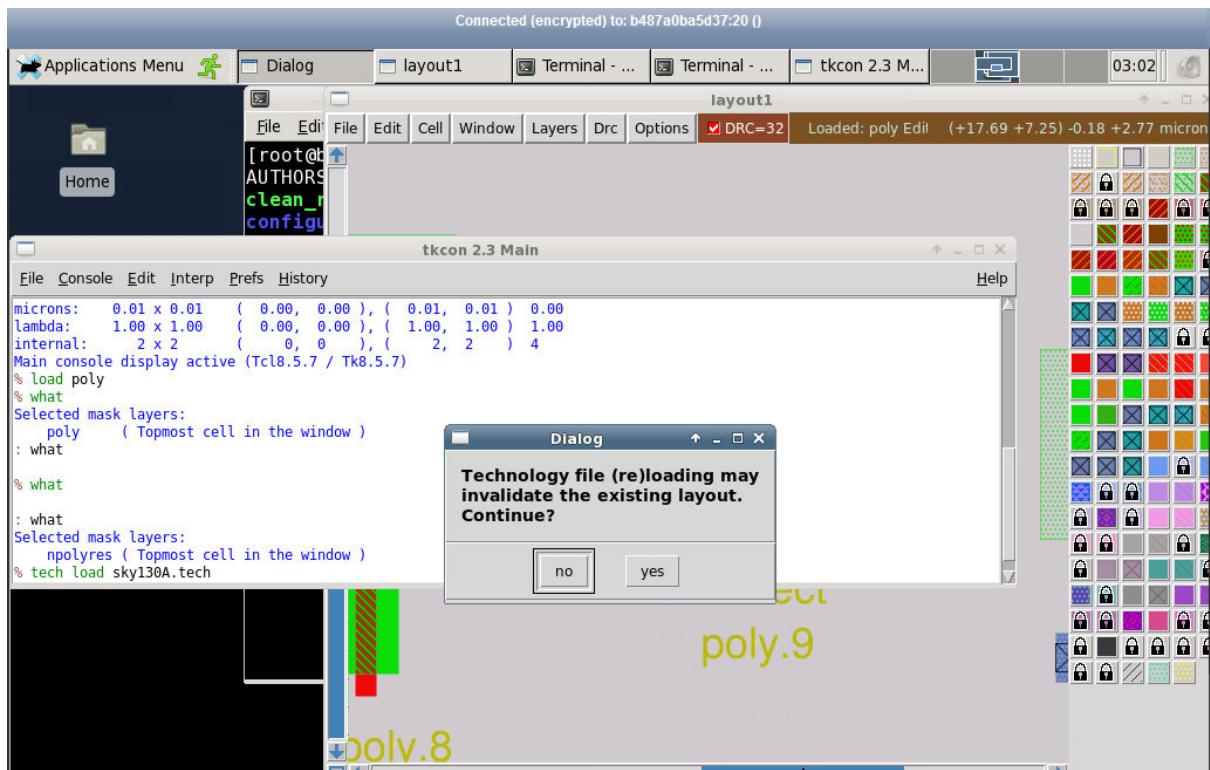
```
variants *

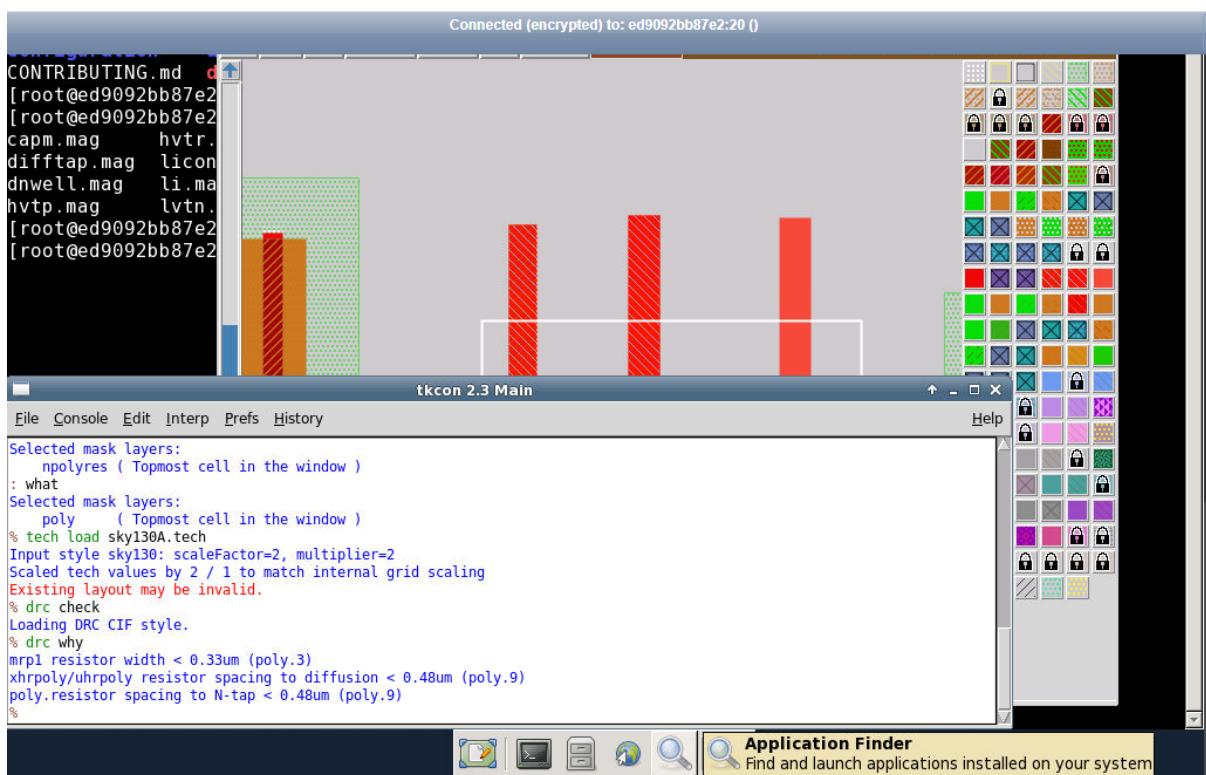
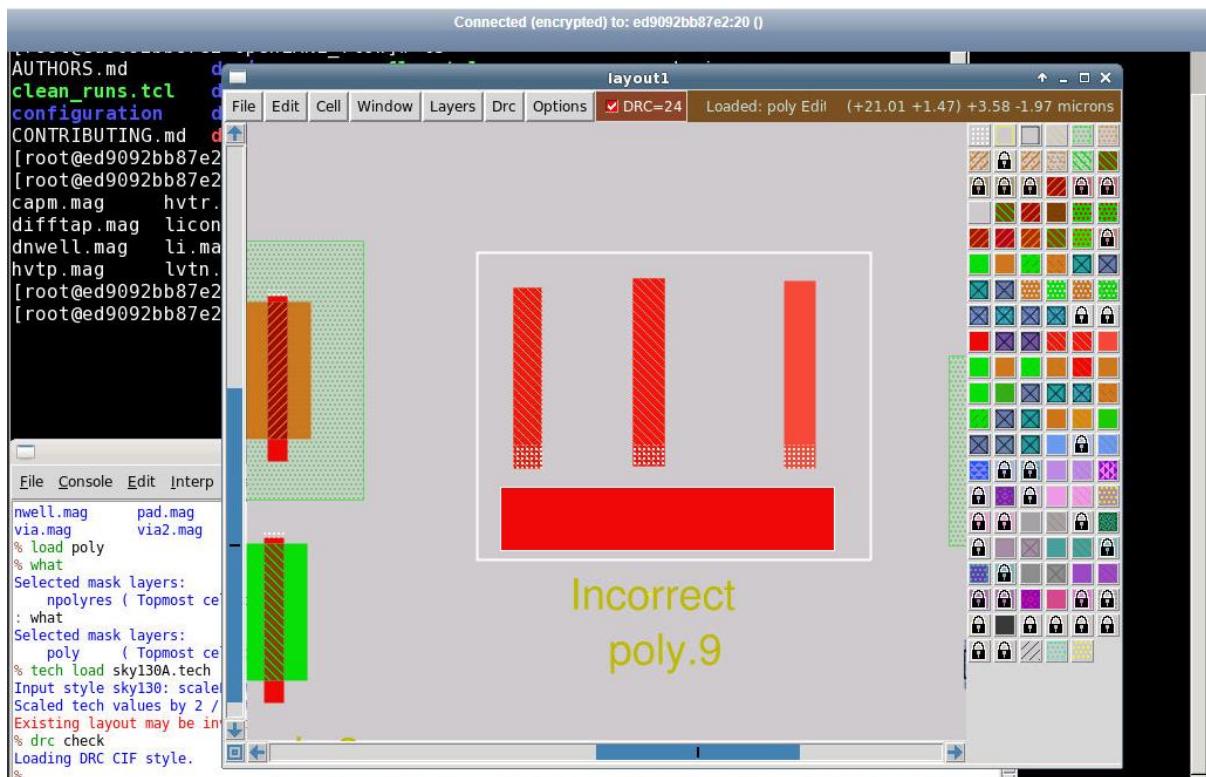
#-----
# POLY
#-----
```

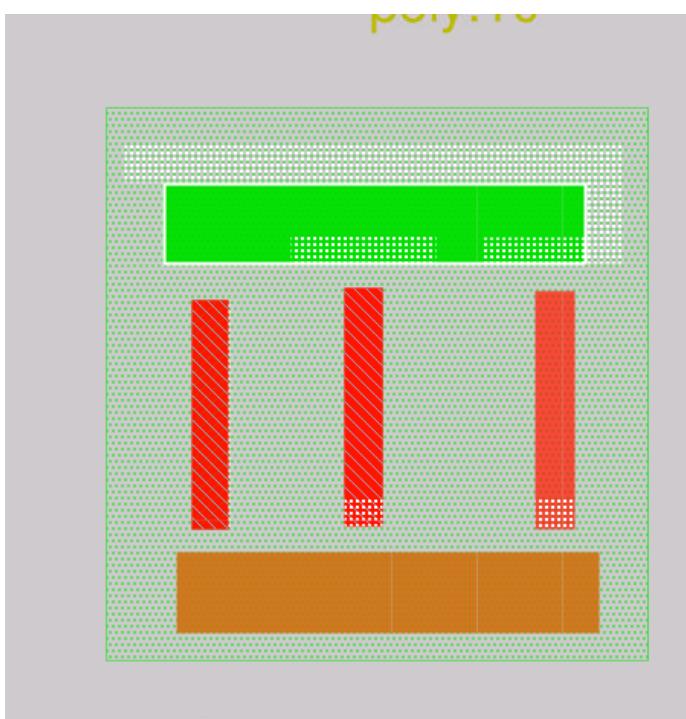
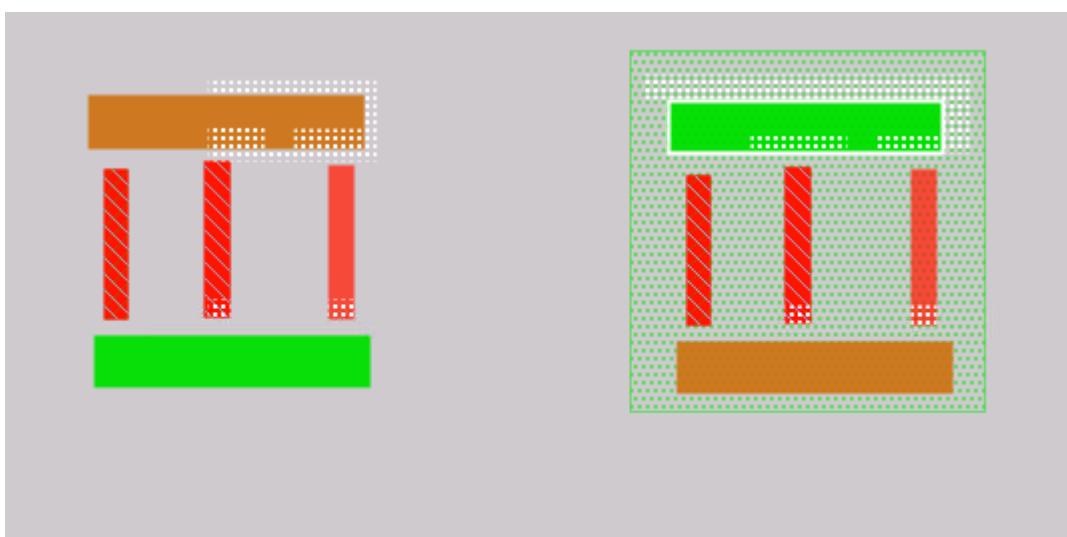
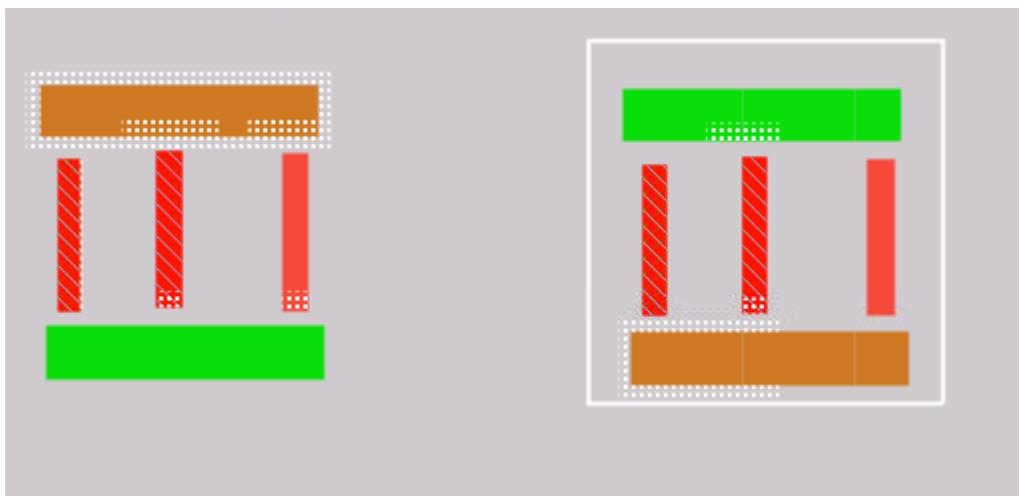
width allpoly 150 "poly.width < %d (poly.1a)"
spacing allpoly alldiff 210 touching_ok "poly.spacing < %d (poly.2)"
spacing allpolynonfet alldifflvnonfet 75 corner_ok allfets \
 "poly.spacing to Diffusion < %d (poly.4a)"
spacing npres *nsd 480 touching_illegal \
 "poly.resistor spacing to N-tap < %d (poly.9)"
spacing npres allpolynonres 480 touching_illegal \
 "poly.resistor spacing to N-tap < %d (poly.9)"

overhang *ndiff,rndiff nfet,scnfet,npd,npass 250 "N-Diffusion overhang of nmos
< %d (poly.7)"
overhang *mvndiff,mvrndiff mvnfet,mvnnfet 250 \
 "N-Diffusion overhang of nmos < %d (poly.7)"
overhang *pdifff,rdifff pfet,scpfet,ppu 250 "P-Diffusion overhang of pmos < %d (
poly.7)"
overhang *mvpdiff,mvrpdiff mvpfet 250 "P-Diffusion overhang of pmos < %d (poly.
7)"

overhang *poly allfets 130 "poly.overhang of transistor < %d (poly.8)"







Terminal - @ed9092bb87e2:/openLANE_flow/drc_tests

```

File Edit View Terminal Go Help
variants *

#-----
# POLY
#-----

width allpoly 150 "poly.width < %d (poly.1a)"
spacing allpoly allpoly 210 touching_ok "poly.spacing < %d (poly.2)"
spacing allpolynonfet alldifflynonfet 75 corner_ok allfets \
    "poly.spacing to Diffusion < %d (poly.4a)"
spacing npres alldiff 480 touching_illegal \
    "poly.resistor spacing to N-tap < %d (poly.9)"
spacing npres allpolynonres 480 touching_illegal \
    "poly.resistor spacing to N-tap < %d (poly.9)"
overhang *ndiff,rndiff nfet,scnfet,npd,npass 250 "N-Diffusion overhang of nmos
< %d (poly.7)"
overhang *mvndiff,mvrndiff mvnfet,mvnnfet 250 \
    "N-Diffusion overhang of nmos < %d (poly.7)"
overhang *pdifff,rpdifff pfet,scpfet,ppu 250 "P-Diffusion overhang of pmos < %d (
poly.7)"
overhang *mvpdiff,mvrpdifff mvpfet 250 "P-Diffusion overhang of pmos < %d (poly.
7)"
overhang *poly allfets 130 "poly.overhang of transistor < %d (poly.8)"
-- INSERT --
Loading DRC CIF style.
% drc why
mrpl resistor width < 0.3
xhrpoly/uhrpoly resistor ...
poly.resistor spacing to ...

```

Connected (encrypted) to: ed9092bb87e2:20 ()

```

CONTRIBUTING.md d
[root@ed9092bb87e2
[root@ed9092bb87e2
cappm.mag hvtr.
difftap.mag licon
dnwell.mag li.ma
hvtp.mag lvtn.
[root@ed9092bb87e2
[root@ed9092bb87e2
[root@ed9092bb87e2
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
% tech load sky130A.tech
Input style sky130: scaleFactor=2, multiplier=2
Scaled tech values by 2 / 1 to match internal grid scaling
Existing layout may be invalid.
% drc check
Loading DRC CIF style.
% drc why
N-Diffusion spacing to N-well < 0.005um (diff/tap.9)
xhrpoly/uhrpoly resistor spacing to diffusion < 0.48um (poly.9)
poly.resistor spacing to N-tap < 0.48um (poly.9)
% drc why
N-Diffusion spacing to N-well < 0.005um (diff/tap.9)
xhrpoly/uhrpoly resistor spacing to diffusion < 0.48um (poly.9)
poly.resistor spacing to N-tap < 0.48um (poly.9)
mrpl resistor width < 0.33um (poly.3)
%
```

Connected (encrypted) to: ed9092bb87e2:20 ()

Applications Menu layout1 Terminal - @ed9... Terminal - @ed9... tkcon 2.3 Main

Terminal - @ed9092bb87e2:/openLANE_flow/drc_tests

File Edit View Terminal Go Help

```

style drc variants (fast),(full),(routing)
scalefactor 10
cifstyle drc

variants (fast),(full)

#-----
# DNWELL
#-----

width dnwell 3000 "Deep N-well width < %d (dnwell.2)"
spacing dnwell dnwell 6300 touching_ok "Deep N-well spacing < %d (dnwell.3)"
spacing dnwell allnwell 4500 surround_ok \
    "Deep N-well spacing to N-well < %d (nwell.7)"
cifmaxwidth nwell_missing 0 bend_illegal \
    "N-well overlap of Deep N-well < 0.4um outside, 1.03um inside (nwell.5a, 7)"
cifmaxwidth dnwell_missing 0 bend_illegal \
    "SONOS nFET must be in Deep N-well (tunm.6a)"

#-----
# NWELL
#-----

```

Connected (encrypted) to: ed9092bb87e2:20 ()

```

scalefactor 10
cifstyle drc

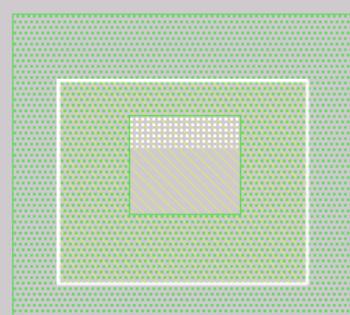
variants (fast),(full)

#-----
# DNWELL
#-----

width dnwell 3000 "Deep N-well width < %d (dnwell.2)"
spacing dnwell dnwell 6300 touching_ok "Deep N-well spacing < %d (dnwell.3)"
spacing dnwell allnwell 4500 surround_ok \
    "Deep N-well spacing to N-well < %d (nwell.7)"
cifmaxwidth nwell_missing 0 bend_illegal \
    "N-well overlap of Deep N-well < 0.4um outside, 1.03um inside (nwell.5a, 7)"
cifmaxwidth dnwell_missing 0 bend_illegal \
    "SONOS nFET must be in Deep N-well (tunm.6a)"

#-----
# NWELL
#-----

```



nwell.6

tkcon 2.3 Main

File Console Edit Interp Prefs History Help

```

xhrpoly/uhrpoly resistor spacing to diffusion < 0.48um (poly.9)
poly.resistor spacing to N-tap < 0.48um (poly.9)
mrpl resistor width < 0.33um (poly.3)
Scaled magic input cell nwell geometry by factor of 2
% drc why
N-well overlap of Deep N-well < 0.4um outside, 1.03um inside (nwell.5a, 7)
% drc why
N-well overlap of Deep N-well < 0.4um outside, 1.03um inside (nwell.5a, 7)
%

```

Connected (encrypted) to: ed9092bb87e2:20 ()

Applications Menu layout1 Terminal - @ed9... Terminal - @ed9... tkcon 2.3 Main 16:32

File Edit View Terminal Go Help

```

#----- style drc
#----- # NOTE: This style is used for DRC only, not for GDS output
#----- scalefactor 10 nanometers
options calma-permissive-labels

# Ensure nwell overlaps dnwell at least 0.4um outside and 1.03um inside
templayer dnwell_shrink dnwell
shrink 1030

templayer nwell_missing dnwell
grow 400
and-not dnwell_shrink
and-not nwell

# SONOS nFET devices must be in deep nwell
templayer dnwell_missing nsonos
and-not dnwell

# Define MiM cap bottom plate for spacing rule
search hit BOTTOM, continuing at TOP

```

xhrpoly/uhrpoly resistor spacing to diffusion < 0.48um (poly.9)
poly.resistor spacing to N-tap < 0.48um (poly.9)

Connected (encrypted) to: ed9092bb87e2:20 ()

tkcon 2.3 Main

```

# NOTE: This style is
#----- scalefactor 10 nanome
options calma-permissi

# Ensure nwell overlap
templayer dnwell_shrin
shrink 1030

templayer nwell_mis
grow 400
and-not dnwell_shr
and-not nwell

# SONOS nFET devices m
templayer dnwell_mis
and-not dnwell

# Define MiM cap botto
search hit BOTTOM, cont

```

mrpl resistor width < 0.33um (poly.3)
Scaled magic input cell nwell geometry by factor of 2
% drc why
N-well overlap of Deep N-well < 0.4um outside, 1.03um inside (nwell.5a, 7)
% drc why
N-well overlap of Deep N-well < 0.4um outside, 1.03um inside (nwell.5a, 7)
% cif ostyle drc
CIF output style is now "drc"
%

Connected (encrypted) to: ed9092bb87e2:20 ()

```

# NOTE: This style is
#-----#
scalefactor 10  nanome
options calma-permissi

# Ensure nwell overlap
templayer dnwell_shrini
shrink 1030

templayer nwell_misssin
grow 400
and-not dnwell_shrink
and-not nwell

# SONOS nFET devices m
templayer dnwell_misssin
and-not dnwell

# Define MiM cap bottom
search hit BOTTOM cont

```

tkcon 2.3 Main

File Console Edit Interp Prefs History Help

```

% cif ostyle drc
CIF output style is now "drc"
% cif see dwell_shrink
CIF name "dwell_shrink" doesn't exist in style "drc".
The valid CIF layer names are: dnwell_shrink, nwell_missing, dnwell_missing, mim_bottom, mim2_bottom, ptap_reach, ptap_m
issing, ntap_reach, ntap_missing, dptap_reach, dptap_missing, m1_small_hole, m1_hole_empty, m2_small_hole, m2_hole_empty
.
% cif see dnwell_shrink
%
```

Connected (encrypted) to: ed9092bb87e2:20 ()

```

# NOTE: This style is
#-----#
scalefactor 10  nanome
options calma-permissi

# Ensure nwell overlap
templayer dnwell_shrini
shrink 1030

templayer nwell_misssin
grow 400
and-not dnwell_shrink
and-not nwell

# SONOS nFET devices m
templayer dnwell_misssin
and-not dnwell

# Define MiM cap bottom
search hit BOTTOM cont

```

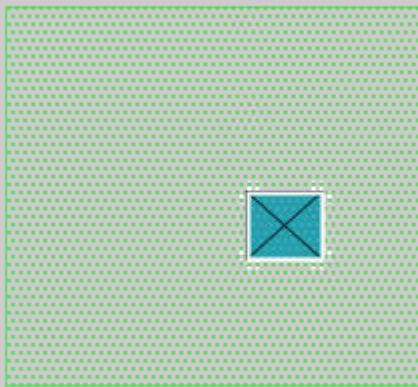
tkcon 2.3 Main

File Console Edit Interp Prefs History Help

```

% cif see dwell_shrink
CIF name "dwell_shrink" doesn't exist in style "drc".
The valid CIF layer names are: dnwell_shrink, nwell_missing, dnwell_missing, mim_bottom, mim2_bottom, ptap_reach, ptap_m
issing, ntap_reach, ntap_missing, dptap_reach, dptap_missing, m1_small_hole, m1_hole_empty, m2_small_hole, m2_hole_empty
.
% cif see dnwell_shrink
% feed clear
% cif see nwell_missing
%
```

ERROR:_Incorrect_Implementation



nwell.4

```
Applications Menu layout1 Terminal - @ed9... Terminal - @ed9... tkcon 2.3 Main
Terminal - @ed9092bb87e2:/openLANE_flow/drc_tests
File Edit View Terminal Go Help
#-----
width dnwell 3000 "Deep N-well width < %d (dnwell.2)"
spacing dnwell dnwell 6300 touching_ok "Deep N-well spacing < %d (dnwell.3)"
spacing dnwell allnwell 4500 surround_ok \
    "Deep N-well spacing to N-well < %d (nwell.7)"
cifmaxwidth nwell_missing 0 bend_illegal \
    "N-well overlap of Deep N-well < 0.4um outside, 1.03um inside (nwell.5a,
7)"
cifmaxwidth dnwell_missing 0 bend_illegal \
    "SONOS nFET must be in Deep N-well (tunm.6a)"

#-----
# NWELL
#-----

width allnwell 840 "N-well width < %d (nwell.1)"
spacing allnwell allnwell 1270 touching_ok "N-well spacing < %d (nwell.2a)"
cifmaxwidth nwell_untapped 0 bend_illegal \
    "N-well missing tap (nwell.4)"

#-----
# DIFF
#-----

-- INSERT --
```

```
Terminal - @ed9092bb87e2:/openLANE_flow/drc_tests
File Edit View Terminal Go Help
templayer dnwell_shrink dnwell
shrink 1030

templayer nwell_missing dnwell
grow 400
and-not dnwell_shrink
and-not nwell

templayer nwell_tapped
bloat-all nsc nwell

templayer nwell_untapped nwell
and-not nwell_tapped

# SONOS nFET devices must be in deep nwell
templayer dnwell_missing nsonos
and-not dnwell

# Define MiM cap bottom plate for spacing rule
templayer mim_bottom
bloat-all *mimcap *metal3

# Define MiM2 cap bottom plate for spacing rule
-- INSERT --
```

```
Applications Menu layout1 Terminal - @ed9... Terminal - @ed9... tkcon 2.3 Main
Terminal - @ed9092bb87e2:/openLANE_flow/drc_tests
File Edit View Terminal Go Help

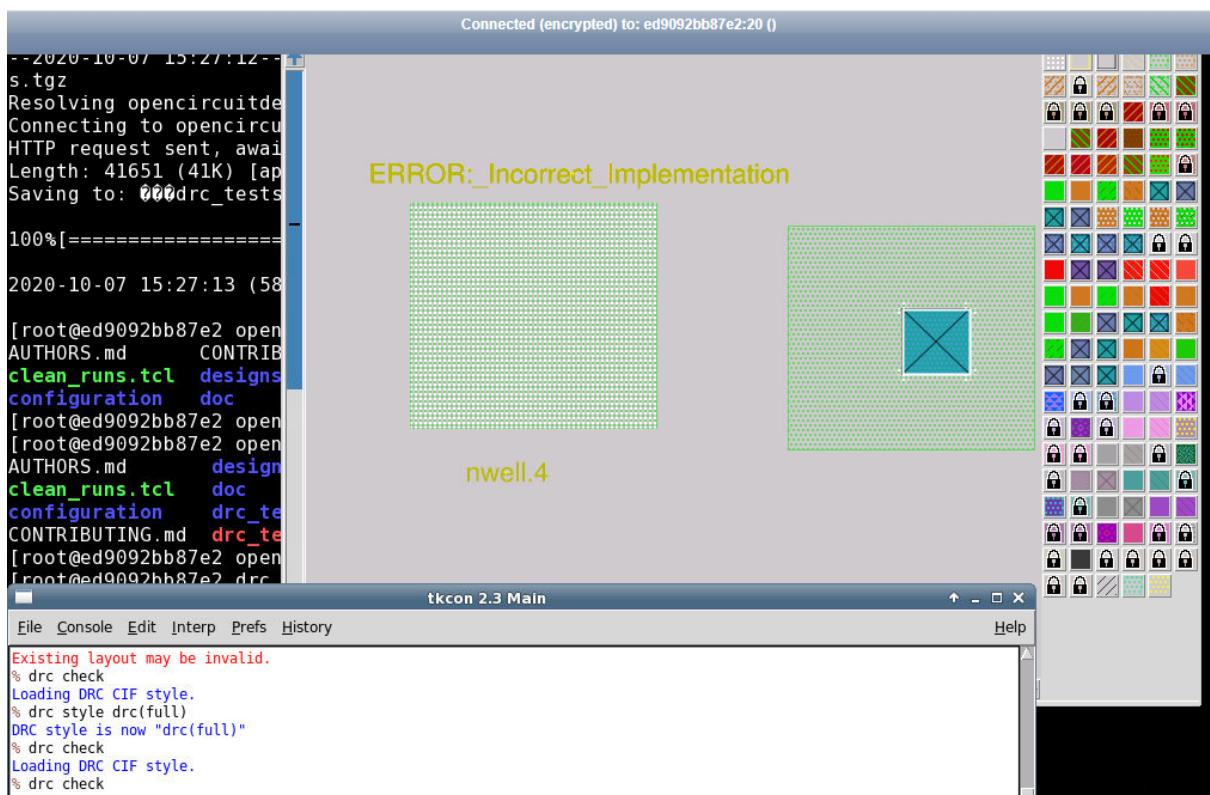
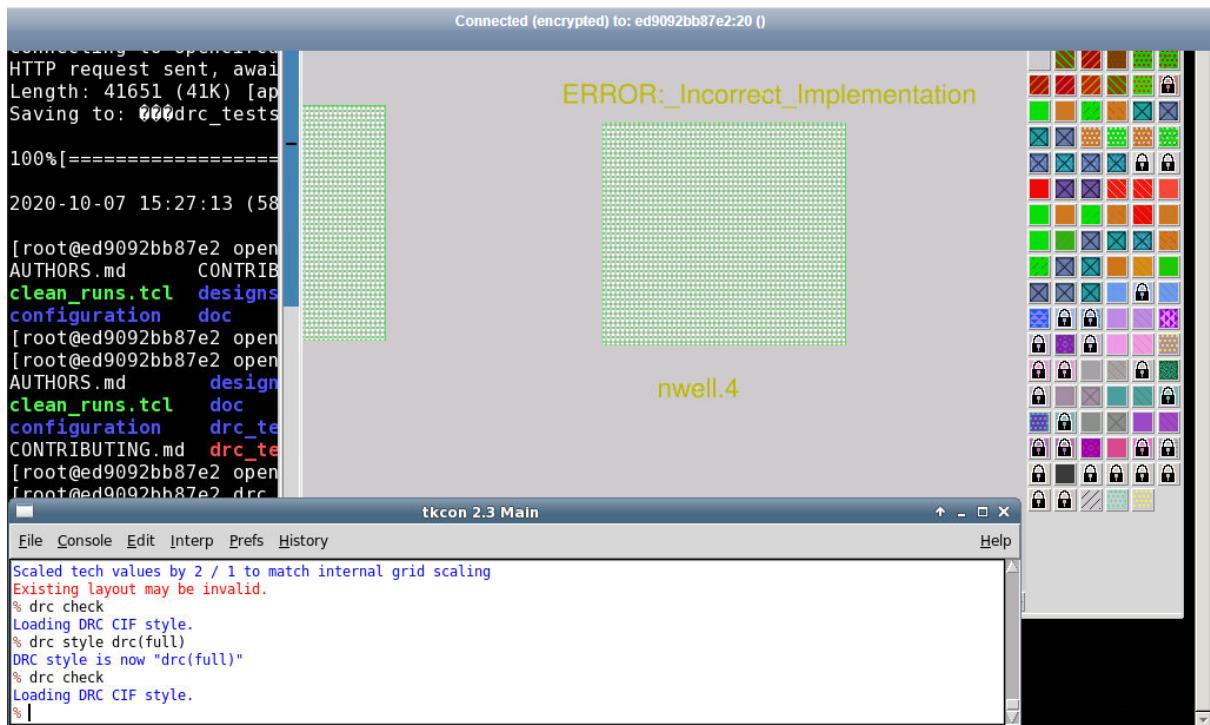
width dnwell 3000 "Deep N-well width < %d (dnwell.2)"
spacing dnwell dnwell 6300 touching_ok "Deep N-well spacing < %d (dnwell.3)"
spacing dnwell allnwell 4500 surround_ok \
    "Deep N-well spacing to N-well < %d (nwell.7)"
cifmaxwidth nwell_missing 0 bend_illegal \
    "N-well overlap of Deep N-well < 0.4um outside, 1.03um inside (nwell.5a,
7)"
cifmaxwidth dnwell_missing 0 bend_illegal \
    "SONOS nFET must be in Deep N-well (tunm.6a)"

#-----
# NWELL
#-----

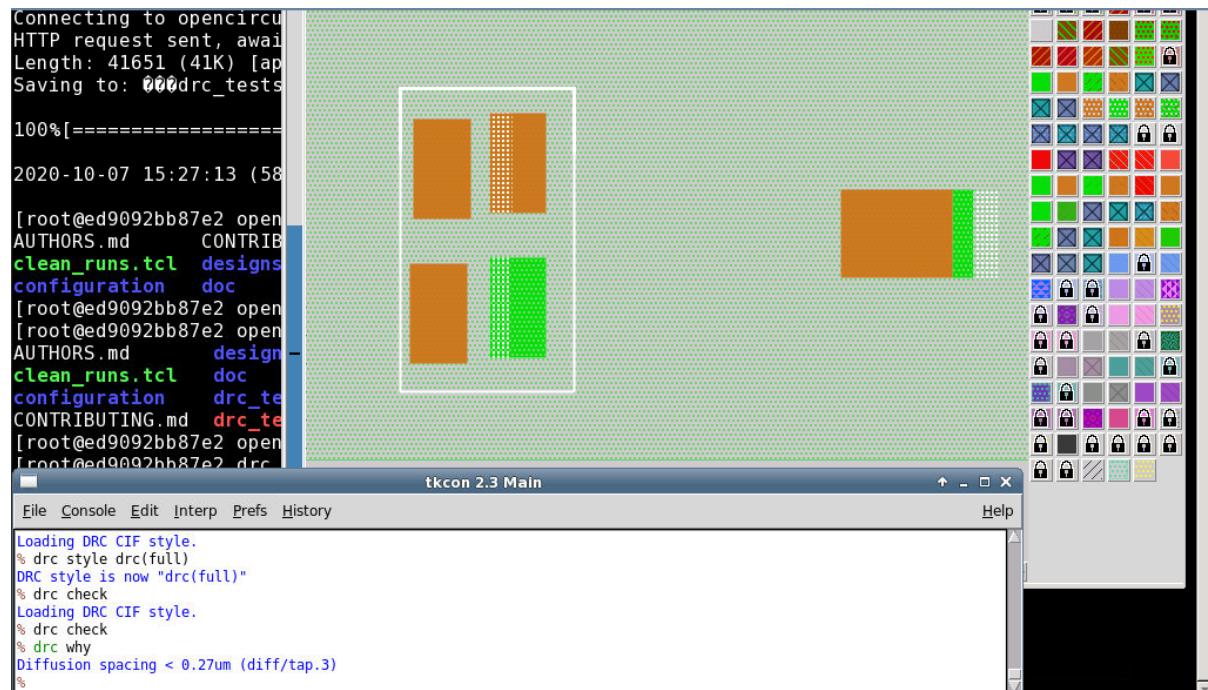
width allnwell 840 "N-well width < %d (nwell.1)"
spacing allnwell allnwell 1270 touching_ok "N-well spacing < %d (nwell.2a)"

variants (full)
cifmaxwidth nwell_untapped 0 bend_illegal \
    "N-well missing tap (nwell.4)"
variants *

-- INSERT --
```



For the Lab challenge, I picked *difftap.mag* and fixed one error on my own.



Fixing the errors by manually placing them at least the minimum specified distance apart:

