

# **8085 DELAYS AND DELAY ROUTINES**

# **DELAYS**

A delay is a time gap between two events. Delays are very useful in computer programs. Something as simple as a traffic light needs delays after every state.

Delays in a computer system can be generated in two ways:

- 1) Hardware delays
- 2) Software delays

	HARDWARE DELAYS	SOFTWARE DELAYS
1	Caused by external hardware (Timer IC like 8254)	Caused by a software delay routine (program)
2	$\mu P$ is not involved in causing the delay and hence is free for other applications.	$\mu P$ is busy as it is executing the delay routine so cannot be used otherwise.
3	Multiple delay routines are possible	Multiple delay routines are not possible
4	Flexibility is low as h/w is involved.	Flexibility is high as delay caused by s/w.
5	External h/w required so circuit becomes more complex	External h/w not required so circuit is simple and less expensive
6	Circuit is More Expensive	Circuit is Less Expensive.

#### Note

In this section we will focus on Software delay routines. After a few lectures, we will learn Timer chips like 8253/54. There we will focus on Hardware delays.

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# **SOFTWARE DELAY ROUTINES**

Software delays are produced in programs by one of the various software "Delay Routines".

As the amount of delay required varies from application-to-application different types of delay routines are present, as follows:

- 1) Using NOP Instruction
- 2) Using One 8-bit register
- 3) Using One 16-bit register

#### **Note**

The above three methods are the most standard ways of producing delays. We can also produce delays using Nested loops or any other user defined method. Though not advisable to be used in college exams, they too are interesting to learn.

## **Nested delay routines: (Not standard)**

- 4) Using Two 8-bit registers
- 5) Using One 8-bit register and One 16-bit register
- 6) Using Two 16-bit registers



## 1) Using NOP Instruction

Eg: NOP;

1-byte instruction

Opcode fetch --- 4 T-states.

 $T_D = 4T$ .

T = 1/(Clk freq)

 $\therefore$  assuming 8085 working at 3 MHz, T = 1/(3 MHz) = 0.333  $\mu$  sec.

∴  $T_D = 4 \times 0.333 = 1.332 \ \mu \ sec.$ 

 $\therefore$  T<sub>D</sub> = 1.332  $\mu$  sec.

This is the maximum delay that can be achieved by writing a NOP instruction.

# 2) Using One 8-bit register

Delay: **MVI B**, 8-bit count 7T Loop: **DCR B** 4T

 DCR B
 4T

 JNZ Loop
 10/7T

 RET
 10T

$$T_D = MT + [(Count)_d \times NT] - 3T$$

**NT** = No of T-states inside the loop {here NT = 10T + 4T = 14T}

MT = No of T-states outside the loop {here MT = 7T + 10T = 17T}

 $Count_{max} = 255 \{8-bit count in decimal\}$ 

$$T_{D \text{ max}} = 17T + [255 \times 14T] - 3T$$

∴  $T_{D \text{ max}} = 3584T$ .

Assuming 8085 working at 3 MHz i.e. T = 333 n sec.

 $\therefore$  T<sub>D max</sub> = 1.18 m sec.

#### **Special Note:**

If you are learning this by piracy, then you are not my student. You are simply a thief! #PoorUpbringing

#### **Very Important:**

8-bit delays are extremely useful for the further topics where we need delays to generate square waves, perform serial communications etc.



## 3) Using One 16-bit register

Delay:	LXI B, 16-bit count	10T		
Loop:	DCX B	6T		
	MOV A, B	4T	Ν	М
	ORA C	4T	Т	Т
	JNZ Loop	10/7T		
	RET	10T		

$$T_D = MT + [(Count)_d \times NT] - 3T$$

Here 
$$NT = 6T + 4T + 4T + 10T = 24T$$

$$MT = 10T + 10T = 20T$$

Count<sub>max</sub> = 65535 {16-bit count in decimal}

$$T_{D \text{ max}} = 20T + [65535 \times 24T] - 3T$$

$$T_{D \text{ max}} = 1572057T.$$

Assuming 8085 working at 3 MHz i.e. T = 333 n sec.

 $\therefore$  T<sub>D max</sub> = 0.525 sec.

### **Note**

In the above method, you have learnt how to decrement a 16-bit register paid and check for zero. Remember this trick for other programs as well – Bharat Acharya.



Non-standard but interesting delay methods to learn just for knowledge...

# 4) Using Two 8-bit registers

Delay:	MVI C, Count2	7T		
Loop2:	MVI B, Count1	7T		
Loop1:	DCR B	4T	NIT	
	JNZ Loop1	10/7T	NT MT P	Γ
	DCR C	4T		
	JNZ Loop2	10/7T		
	RET	10T		

$$T_D = PT + [(Count2)_d \times T_{loop1}] - 3T$$

$$T_{loop1} = MT + [(Count1)_d \times NT] - 3T$$

 $NT = No of T-states inside loop1 {here NT = 4T + 10T = 14T}.$ 

 $\mathbf{MT} = \text{No of T-states outside loop1 but inside loop2} \{ MT = 7T + 4T + 10T = 17T \}$ 

**PT** = No of T-states outside loop2 {here PT = 10T + 7T = 17T }.

 $Count1_{max} = 255 \{8-bit count in decimal\}$ 

 $Count2_{max} = 255 \{8-bit count in decimal\}$ 

 $T_{D \text{ max}} = 914954T.$ 

Assuming 8085 working at 3 MHz i.e. T = 333 n sec.

 $\therefore$  T<sub>D max</sub> = 0.304 sec.



## 5) Using One 8-bit register and One 16-bit register

Delay:	MVI D, Count2	7T			
Loop2:	LXI B, Count1	10T			
Loop1:	DCX B	6T			
·	MOV A, C	4T	NIT		
	ORA B	4T	NT		
	JNZ Loop1	10/7T		MT	PT
	DCR D	4T			
	JNZ Loop2	10/7T			
	RET	10T			

$$T_D = PT + [(Count2)_d \times T_{loop1}] - 3T$$

$$T_{loop1} = MT + [(Count1)_d \times NT] - 3T$$

Here 
$$NT = 6T + 4T + 4T + 10T = 24T$$
.

$$MT = MT = 10T + 4T + 10T = 24T$$
.

$$PT = 7T + 10T = 17T.$$

 $Count1_{max} = 65535 \{16-bit count in decimal\}$ 

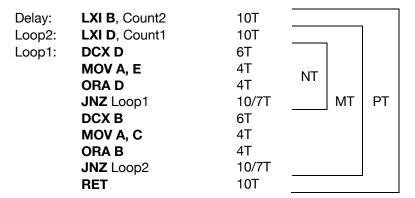
 $Count2_{max} = 255 \{8-bit count in decimal\}$ 

Assuming 8085 working at 3 MHz i.e. T = 333 n sec.

∴  $T_{D \text{ max}} = 133.69 \text{ sec.}$ 



# 6) Using Two 16-bit registers



$$T_D = PT + [(Count2)_d \times T_{loop1}] - 3T$$

$$T_{loop1} = MT + [(Count1)_d \times NT] - 3T$$

Here 
$$NT = 6T + 4T + 4T + 10T = 24T$$
.

$$MT = MT = 10T + 6T + 4T + 4T + 10T = 34T.$$

$$PT = 10T + 10T = 20T$$
.

 $Count1_{max} = 65535 \{16-bit count in decimal\}$ 

 $Count2_{max} = 65535 \{16-bit count in decimal\}$ 

Assuming 8085 working at 3 MHz i.e. T = 333 n sec.

 $\therefore$  T<sub>D max</sub> = 9 hours, 32 min, 24 sec.

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Delay Method	Max Delay
NOP	1.332 μ sec
One 8-bit register	1.18 m sec
One 16-bit register	.525 sec
Two 8-bit registers	.304 sec
One 8-bit / one 16-bit reg	133.69 sec
Two 16-bit register	9 hrs, 32 min, 24 sec

### **Note**

All these calculations are w.r.t. 8085 operating at 3 MHz.

In case in the exam, the frequency is different then calculate 1T = 1/(Clk. freq.), and then calculate the appropriate delay.

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