LOGIC GROUP

Special Note:
In the explanation of every instruction, I have mentioned its machine cycles and T-states. You will understand this part once you watch the two videos of timing diagrams

1) ANA R

Logically AND the contents of the specified register with accumulator, store result in accumulator.
Eg: ANA B ; A ← A AND B

Addr. Mode	Flags Affected	Cycles	T-States
Register	**ALL**	1	**4**

2) ANA M

Logically AND the contents of the memory location pointed by HL pair, with the accumulator.
Eg: ANA M ; A ← A AND M

Addr. Mode	Flags Affected	Cycles	T-States
Indirect	**ALL**	2	**7**

3) ANI 8-bit data

Logically AND the immidiate 8-bit data, with the accumulator.
Eg: ANA 25; A ← A AND 25

Addr. Mode	Flags Affected	Cycles	T-States
Immidiate	**ALL**	2	**7**

Special Note: Use of AND operation
To “Clear any bit”, we must “AND” that bit with “0” and the remaining bits with “1”.
Eg: ANI F0H will Clear the Lower Nibble of A while the Higher Nibble will remain the same.

Simillarly we have the other logic instrctions as follows:

4) ORA R
5) ORA M
6) ORI 8-bit data

Special Note: Use of OR operation
To "Set any bit", we must "OR" that bit with "1" and the remaining bits with "0".
Eg: ORI 0FH will Set the Lower Nibble of A while the Higher Nibble will remain the same.

7) XRA R
8) XRA M
9) XRI 8-bit data

Special Note: Use of XOR operation
To "Complement any bit", we must "XOR" that bit with "1" and the remaining bits with "0".
Eg: XRI 0FH will Complement the Lower Nibble while the Higher Nibble will remain the same.

10) CMP R

Compares the contents of register R and accumulator.
Comparision essntially is subtraction. Hence, this instruction performs A – R.
It is very important to **remember** that the **result** of this comparision is **NOT stored** in **accumulator**, only the Flags are afftected. ☺ In case of doubts, contact Bharat Sir: - 98204 08217.
Eg: CMP B ; Compares A and B i.e. A – B (and not B - A)
We decide which one of the two is greater by checking the flags affected as follows:

Conclusion	Zero Flag 'Z'	Carry Flag 'Cy'
A > B	0	0
A = B	1	0
A < B	0	1

Addr. Mode	Flags Affected	Cycles	T-States
Register	**ALL**	1	**4**

Simillarly we have the other comparision instrctions as follows:

11) CMP M
12) CPI 8-bit data

13) STC

Sets the carry flag.
Cy ← 1.

Addr. Mode	Flags Affected	Cycles	T-States
Implied	**Only Carry**	1	**4**

14) CMC

Complements the carry flag.
Cy ← Cy.

Addr. Mode	Flags Affected	Cycles	T-States
Implied	**Only Carry**	1	**4**

15) CMA

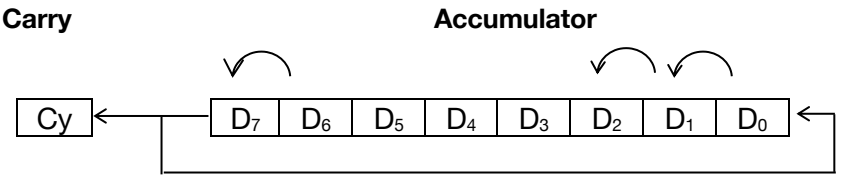
Complements the accumulator.
A ← 1's complement of A.

Addr. Mode	Flags Affected	Cycles	T-States
Implied	**None**	1	**4**

Special Note: Use of CMA operation
It acts as a NOT gate. AND followed by NOT gives a NAND.
Hence using CMA we can derive NAND, NOR and XNOR operations.

16) RLC

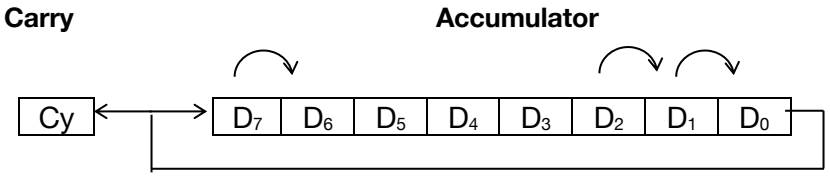
The Contents of accumulator are rotated left by 1.
The MSB goes to the Carry AND the LSB.



Addr. Mode	Flags Affected	Cycles	T-States
Implied	**Carry**	1	**4**

17) RRC

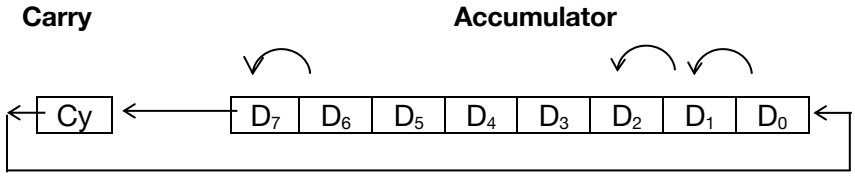
The Contents of accumulator are rotated right by 1.
The LSB goes to the Carry AND the MSB.



Addr. Mode	Flags Affected	Cycles	T-States
Implied	**Carry**	1	**4**

18) RAL

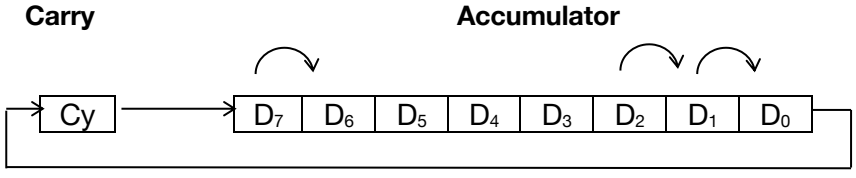
The Contents of accumulator are rotated left by 1.
The MSB goes to the Carry and THE CARRY goes to LSB.



Addr. Mode	Flags Affected	Cycles	T-States
Implied	**Carry**	1	**4**

19) RAR

The Contents of accumulator are rotated right by 1.
The LSB goes to the Carry and the CARRY goes to the MSB.



Addr. Mode	Flags Affected	Cycles	T-States
Implied	**Carry**	1	**4**

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