8085 TIMING DIAGRAMS

Instruction Cycle:
This is the time required by the µP to fetch and execute one complete instruction.
The instruction cycle is in two parts:
1. Fetch Cycle
2. Execute Cycle

Fetch Cycle:
This is the time required by the µP to fetch all bytes of an instruction
The length of the fetch cycle is thus determined by the no of bytes in an instruction.

Execution Cycle:
This is the time required by the µP to execute a fetched instruction.

An Instruction cycle consists of various machine cycles.
The most important and also compulsory machine cycle of every instruction is OPCODE FETCH.
There are other machine cycles such as memory read, memory write, I/O read etc.
Machine cycles contain T-states

T-State:
A T-State is one clock cycle of the µP.
∴T = Clock Period = 1/Clock Frequency
Since 8085 (standard version) works at 3 MHz, one T-state = 1÷3 microseconds = 0.333 microseconds.

MACHINE CYCLES

It is the time required by the μP doing one operation and accessing one byte from the external module (Memory or I/O). As the data bus of 8085 is 8-bit, one machine cycle will transfer one byte (8-bits). Instructions that require to read or write 16-bit data from memory, need multiple machine cycles.

The Machine cycles of 8085 are given below:

Name	IO/M	RD	WR	S1	S0	INTA	T-States
Opcode Fetch	0	0	1	1	1	1	**4/6**
Mem Read	0	0	1	1	0	1	3
Mem Write	0	1	0	0	1	1	3
IO Read	1	0	1	1	0	1	3
IO Write	1	1	0	0	1	1	3
Int. Acknowledge	1	1	1	1	1	0	**3 or 6**
Bus Idle	0	1	1	0	0	1	3

Opcode fetch is compulsory in every instruction and is the first machine cycle of every instruction.

Most instructions are memory based so they may need Memory Reads or Memory Writes after Opcode Fetch.

Only IN and OUT instructions involve IO Read and IO Write respectively.

Only DAD instruction needs Bus Idle

Interrupt Acknowledgment cycle is performed in response to INTR signal. This will be explained much later in the topic of interrupts

Special Note:

Be smart and focus mainly on Opcode Fetch, Memory Read and Memory Write in the beginning as the other machine cycles are used by only a handful of instructions.

OPCODE FETCH

- This cycle is used to **fetch** the **Opcode from** the **memory**.
- This is the **First** Machine Cycle of every instruction.
- It is a **compulsory** Machine Cycle
- It is **generally** of **4 T**-States but **some** instructions require a **6 T**-State Opcode Fetch.

During T1

- **A15-A8** contains the higher byte of the address (**PCH**)
- As **ALE** is **high AD7-AD0** contains the lower byte of the address (**PCL**).
- Since it is an Opcode fetch cycle, **S1** and **S0** go **high**.
- Since it is a memory operation, **IO/M** goes **low**.

During T2

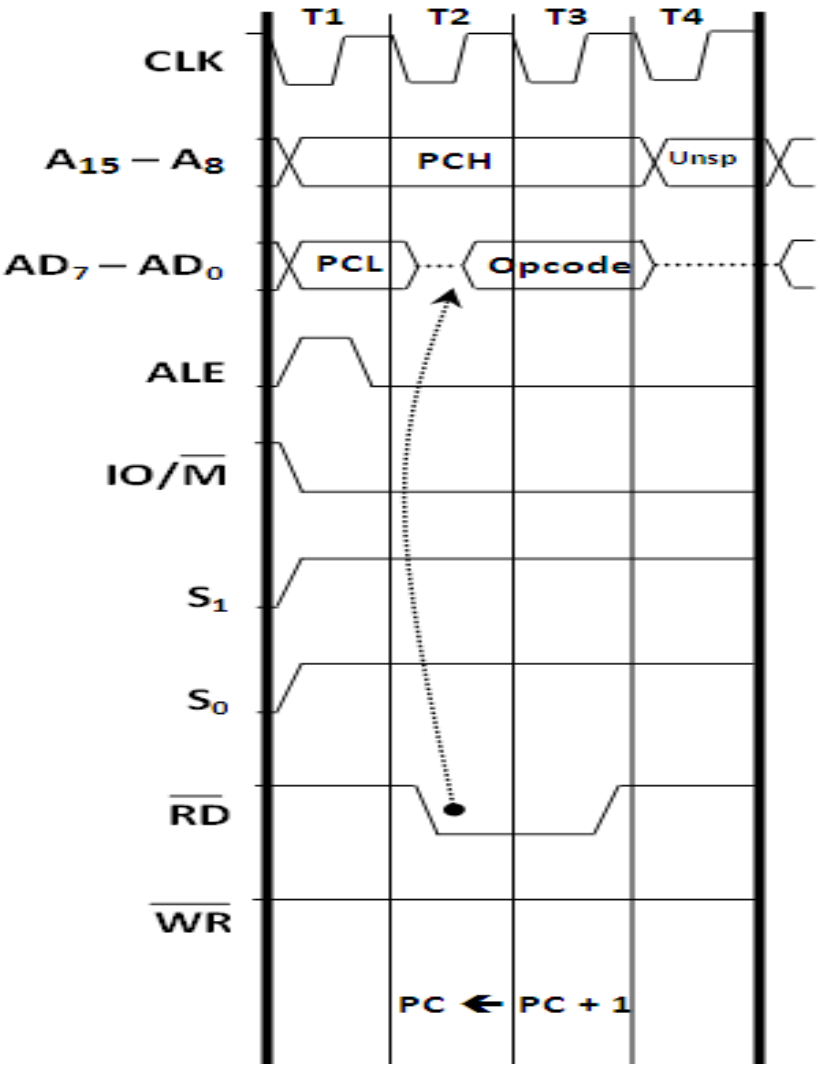
- As **ALE** goes **low** address is removed from AD7-AD0.
- As **RD** goes **low**, **data** appears **on AD7-AD0**. ☺ In case of doubts, contact Bharat Sir: - 98204 08217.
- As µP is reading the data (Opcode) from memory, there is a propagation delay between sending the address and arrival of data. This is the time required for data (Opcode) to travel from memory to µP. {It is shown by dots between address and data}
- The µP examines the state of the READY pin.
  If READY pin is "high", µP will continue, but if it is low, then it means the device is not ready, as it is slow. Hence the µP enters wait-state by executing wait cycles and remains in the wait-state until READY goes high.

During T3

- Data remains on AD7-AD0 till RD is low. This is the time given to µP to capture the data (Opcode) from the data bus.

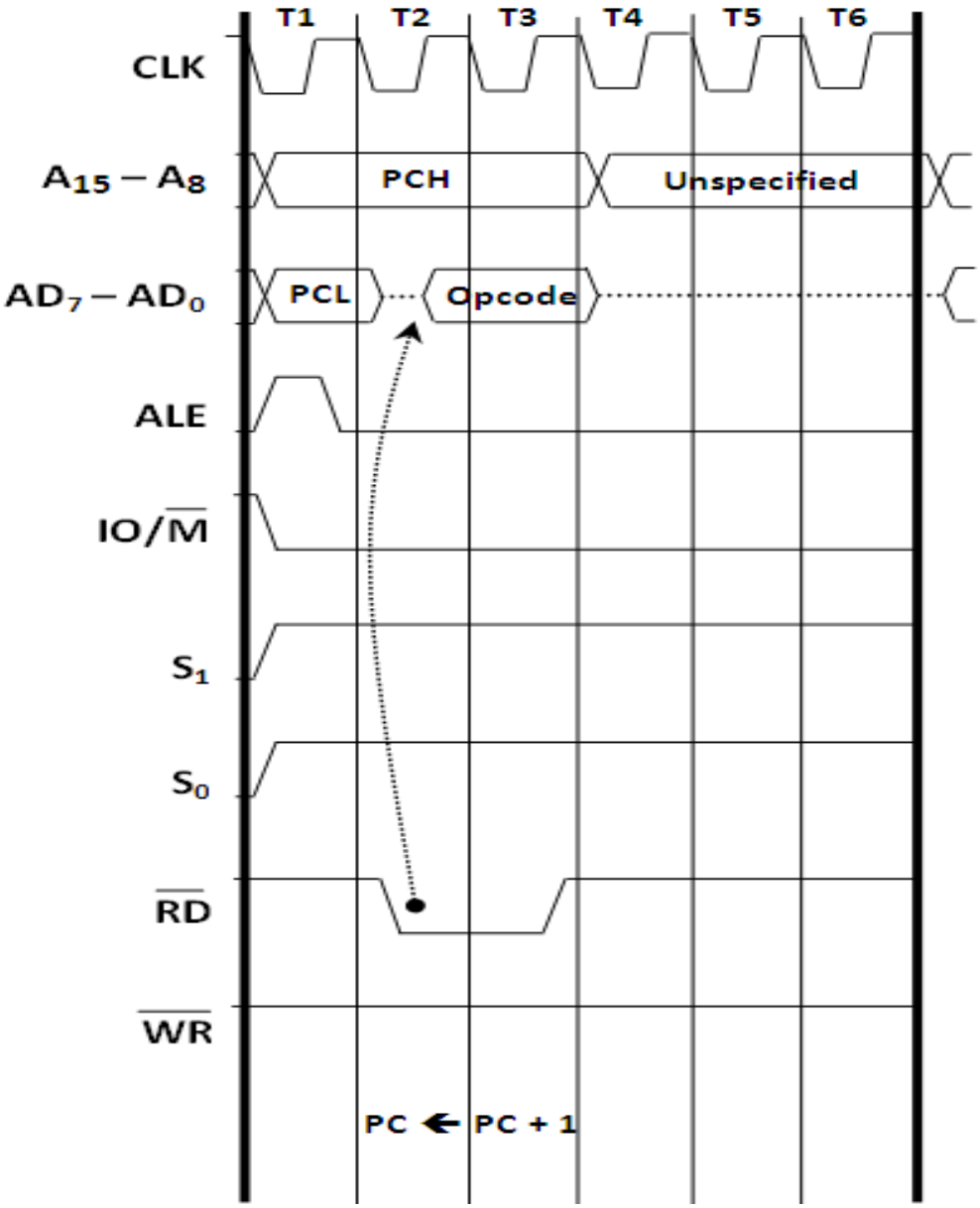
During T4

- T4 state is used by the µP to decode the Opcode.
- This is how an Opcode Fetch cycle is different from a Memory Read cycle.



Special Note:
Timing diagrams show what is happening in the buses. Decoding in an internal operation and hence is not shown in timing diagrams.

OPCODE FETCH OF 6 T-STATES



Instructions that use a 6T Opcode Fetch

PCHL
SPHL
INX
DCX
PUSH
CALL (all types)
RC (Conditional RET)
RSTn

You will of course, understand this later as you learn timing diagrams of instructions.

Special Note:
T5 and T6 are used for internal operation. Nothing happens on the buses during that time hence nothing is shown in the timing diagram.

MEMORY READ

- This cycle is used to **fetch one byte from** the **memory**.
- This cycle can be used to fetch the operand bytes of an instruction or any data from the memory.
- It is a not compulsory Machine Cycle
- It requires **3 T-States**.

During T1

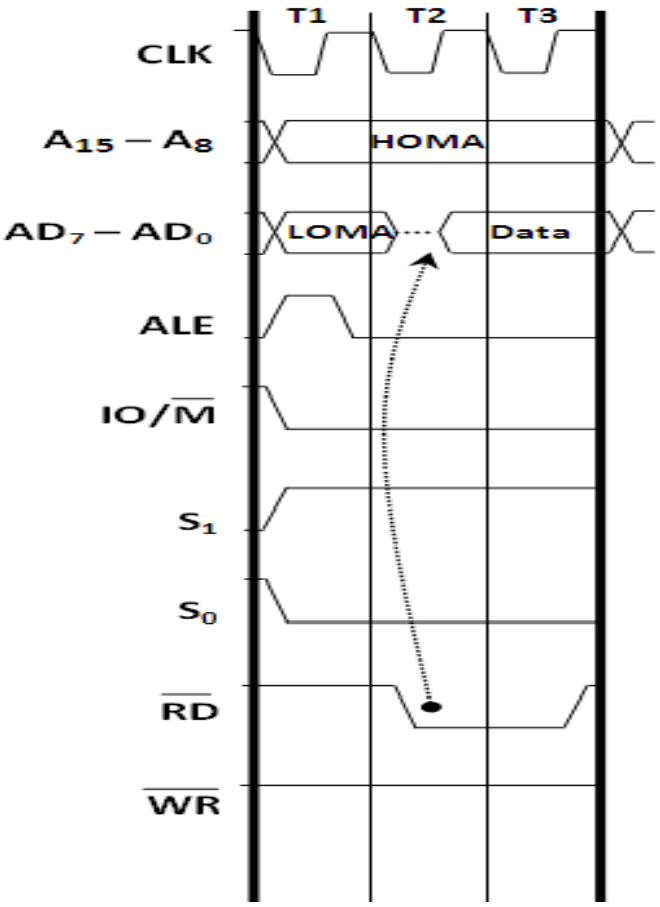
- **A15-A8** contains the higher byte of the address (**PCH**)
- As **ALE** is **high**, **AD7-AD0** contains the lower byte of the address (**PCL**).
- Since it is a Memory Read cycle, **S1** goes **high**.
- Since it is a memory operation, **IO/M** goes **low**.

During T2

- **ALE** goes **low**.
- Address is removed from AD7-AD0.
- As **RD** goes **low, data** appears **on AD7-AD0**.

During T3

- Data remains on AD7-AD0 till RD is low.



Special Note:

Notice the propagation delay, as this is a read operation.

MEMORY WRITE

- This cycle is used to **send** (write) **one byte into** the **memory**.
- It is a not compulsory Machine Cycle
- It requires **3 T-States**.

During T1

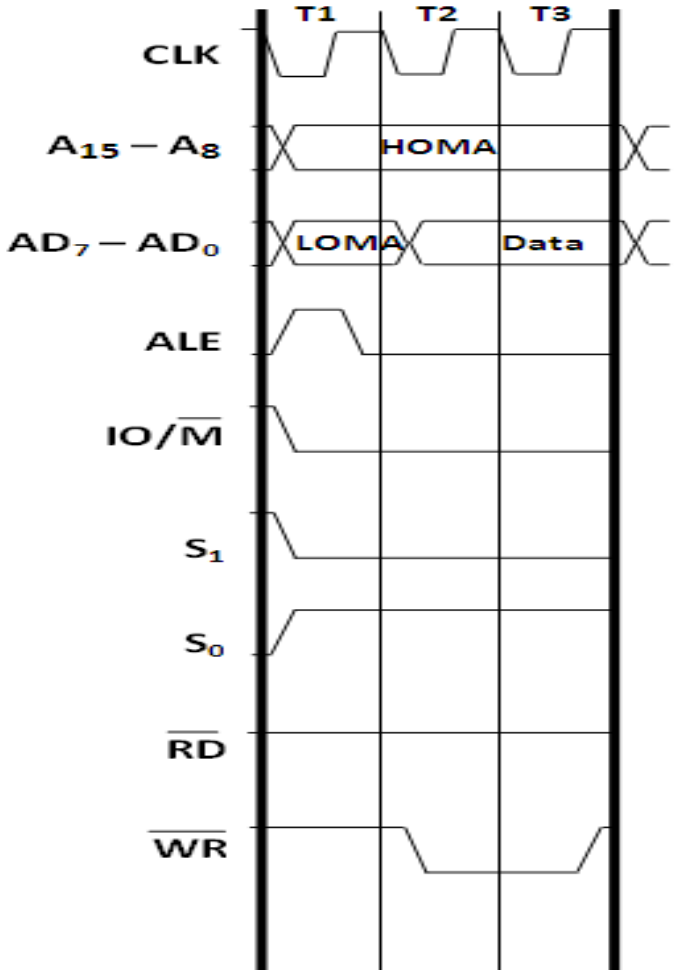
- **A15-A8** contains the higher byte of the address (**PCH**)
- As **ALE** is **high**, **AD7-AD0** contains the lower byte of the address (**PCL**).
- Since it is a Memory Write cycle, **S0** goes **high**.
- Since it is a memory operation, **IO/M** goes **low**.

During T2

- **ALE** goes **low**.
- Address is removed from AD7-AD0.
- **Data** appears **on AD7-AD0** and **WR** goes **low**.

During T3

- Data remains on AD7-AD0 till WR is low.



Special Note:

Notice, NO propagation delay, as this is a write operation.

IO READ

- This cycle is used to **fetch one byte from** an **IO Port**.
- It is a not compulsory Machine Cycle
- It requires **3 T-States**.

During T1

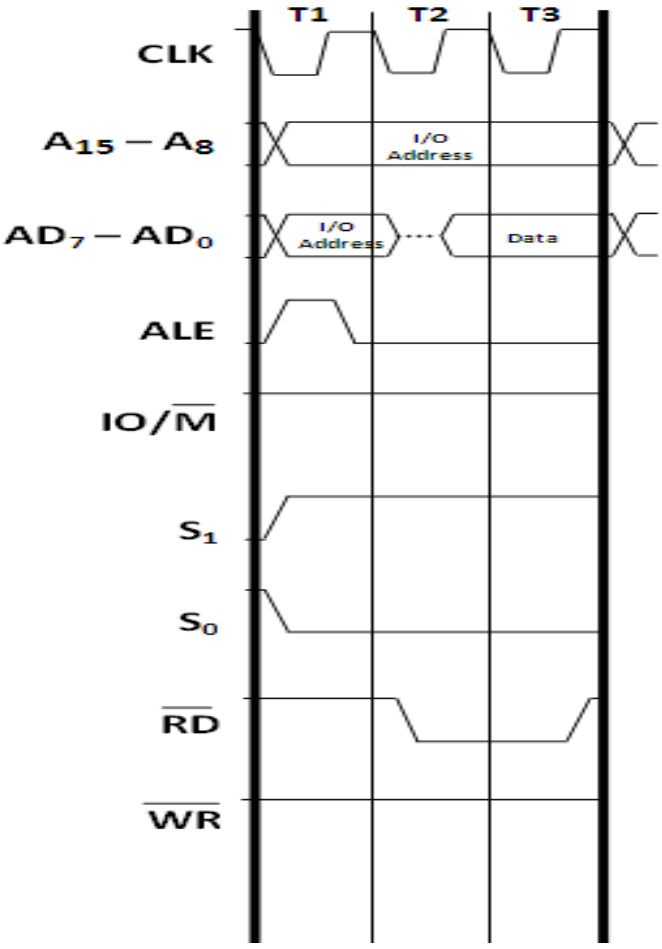
- The **lower 8 bits of the IO Port Address** are **duplicated into** the higher order address bus **A15-A8**.
- As **ALE** is **high AD7-AD0 contains** the **lower byte of** the **address**
- Since it is an IO **Read** cycle **S1** goes **high**.
- Since it is an **IO** operation **IO/M** goes **high**.

During T2

- **ALE** goes **low.**
- Address is removed from AD7-AD0.
- As **RD** goes **low**, **data** appears on **AD7-AD0**.

During T3

- Data remains on AD7-AD0 till RD is low.



Special Note:

Notice the propagation delay, as this is a read operation.

IO WRITE

- This cycle is used to **send** (write) **one byte into** an **IO Port**.
- It is a not compulsory Machine Cycle
- It requires **3 T-States.**

During T1

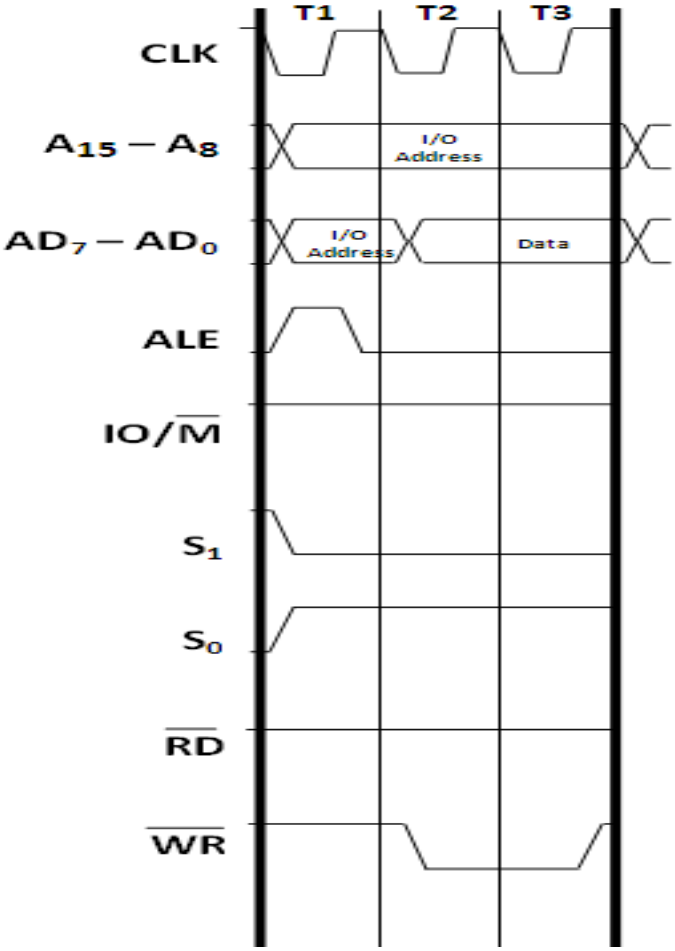
- The **lower 8 bits of the IO Port Address** are **duplicated into** the higher order address bus **A15-A8**.
- As **ALE** is **high AD7-AD0 contains** the **lower byte of** the **address**
- Since it is an IO **Write** cycle, **S0** goes **high**.
- Since it is an **IO** operation, **IO/M** goes **high**.

During T2

- **ALE** goes **low.**
- Address is removed from AD7-AD0.
- **Data** appears **on AD7-AD0** and **WR** goes **low**.

During T3

- Data remains on AD7-AD0 till RD is low.



Special Note:

Notice, NO propagation delay, as this is a write operation.

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