



Khulna University of Engineering & Technology

Department of Computer Science and Engineering

Project Report

Submitted By

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Objectives:

- To develop a minimal computer system using “Logisim” software, along with components like central processing unit (CPU) and a main memory.
- To learn implementation of ALU, registers, instruction set architecture, MAR, MBR, IR, control unit, CPU and main memory (RAM) in minimal computer system.
- To implement various instructions like AND, OR, NOR, BRANCH, LOAD, STORE, ADD, SUB, MUL & HALT.
- To understand how an instruction is fetched to a computer and how it functions internally.

Introduction:

Introducing the small computer system we have: including a wealth of important instructions, like branch, stop, add, sub, load, store, mul, and and. It consists of important parts including the control unit, CPU, main memory, MAR, MBR, IR, ALU, and accumulators in addition to complex algorithms like Booth's Algorithm. Designed with customization and efficiency in mind, it offers powerful features

Component	Description
Word Size	21 bits
OP-Code	4 bits
RAM Address Size	12 bits
Architecture	21-bit architecture with 12-bit RAM addressability

Instruction Format: (21 Bits)

Don't Care	Op-Code	Memory Address
5 bits	4 bits	12 bits

- 0 – AND : perform logical and operation between two operands.
- 1 – ADD : perform addition between two operands.
- 2 – STORE : store the result of the operation in memory.
- 3 – OR : perform logical OR between two operands.
- 4 – SUB : perform subtraction between two operands.
- 5 – BUN : branch unconditionally.
- 6 – LDA : loads data from memory to accumulator.
- 7 – HLT : halt the CPU.

The diagram illustrates a 4x4 crossbar switch and its routing table. The switch has four input lines (A, B, C, D) and four output lines (A, B, C, D). The routing table shows the connection between inputs and outputs for each switch state.

Input	Output	0000	0001	0002	0003
A	A	0000	08000d	02000e	06000c
B	B	0001	08000d	02000e	06000c
C	C	0002	08000d	02000e	06000c
D	D	0003	08000d	02000e	06000c

The routing table shows that the output for each input is determined by the switch state. The output for each input is the same for all switch states, indicating a simple routing scheme.

The CPU stores both data and instructions in the same memory, using the simple Von Neumann architecture. Only a few simple tasks are carried out here. A single clock pulse is used to complete each action. The Logisim simulator has all of these designs implemented. Every arithmetic and logical action on data kept in registers is handled by the CPU's ALU. ALUs that can execute addition, subtraction, AND, OR, and multiplication can be designed with the help of Logisim's tools. The data and instruction flow inside the CPU is regulated by the control unit. Our system provides enough of storage and memory access capabilities with a 12-bit RAM addressability and a 21-bit accumulator. Depending on whatever instruction is being executed at the time, it regulates how other CPU components operate.