

Probability Hardware Assignment

Name -: Arjit Jain
Roll no -: AI22BTECH11002

Abstract—Shift registers were used to create a random number generator for this assignment.

COMPONENTS USED

| Component | Value | Quantity |
|-----------------------|--------------|----------|
| Breadboard | | 1 |
| Seven Segment Display | Common Anode | 1 |
| Decoder | 7447 | 1 |
| Flip Flop | 7474 | 2 |
| X-OR Gate | 7486 | 1 |
| 555 IC | | 1 |
| Resistor | 1 KΩ | 1 |
| Capacitor | 100 nF | 1 |
| Capacitor | 10 nF | 1 |
| Jumper Wires | | |

TABLE 0
COMPONENTS USED

PROCEDURE

- 1) The 555 timer circuit was connected as shown in Figure 7.6
- 2) Next, the clock output of the 555 timer was coupled to the clock signal of the D-flip flops. circuit for shift registers was constructed using four D-flip flops, utilizing two 7474 ICs.
- 3) The XOR gate (7486 IC) was connected according to the configuration depicted in Figure 7.6
- 4) The decoder (7447 IC) was connected, with its A, B, C, and D inputs connected to Q0, Q1, Q2, and Q3, respectively, as indicated in Figure 7.6
- 5) Following the table, the seven-segmented display and the decoder (7447 IC) were interconnected, as depicted in Figure 7.6
- 6) Finally, all the independent components were linked together before connecting the power supply, ensuring proper functionality of the circuit.

OUTPUT

Random numbers are generated on the display.

1.1.1. Generate the CLOCK signal using the 555 timer the figure ??

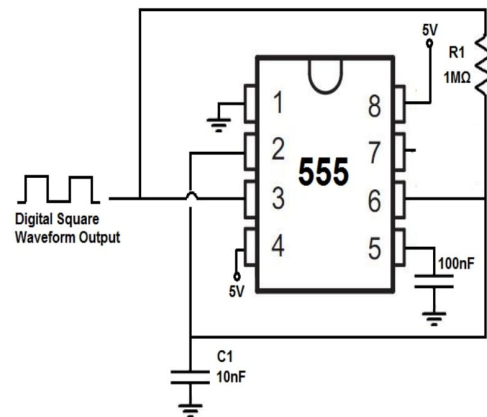


Fig. 6. Connection in 555 timer circuit

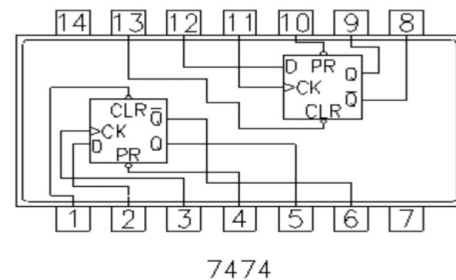


Fig. 6. Connection in 7474 IC

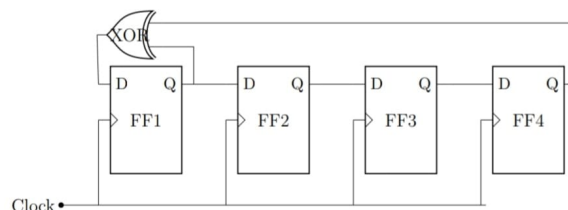


Fig. 6. Connection in XOR gate

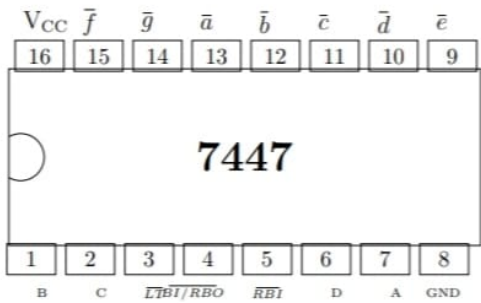


Fig. 6. Connection in Decoder gate

| | | | | | | | |
|----------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 7447 | \bar{a} | \bar{b} | \bar{c} | \bar{d} | \bar{e} | \bar{f} | \bar{g} |
| Display | a | b | c | d | e | f | g |

Table 1.1.6.1

Fig. 6. Connection of seven segmented display with decoder

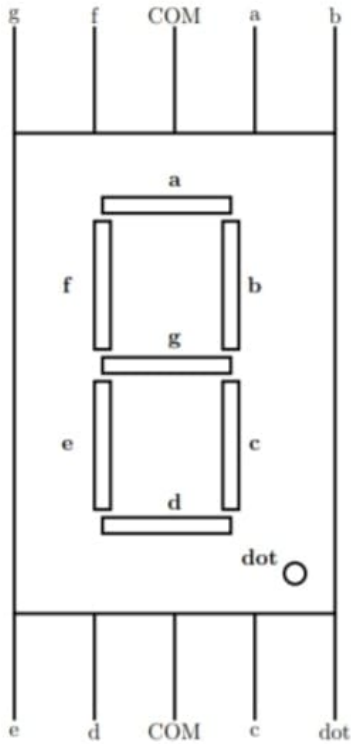


Fig. 6. Seven segmented display

Block Diagram

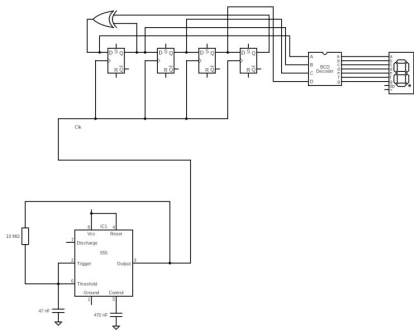


Figure 4: Block Diagram

Fig. 6. Block Diagram

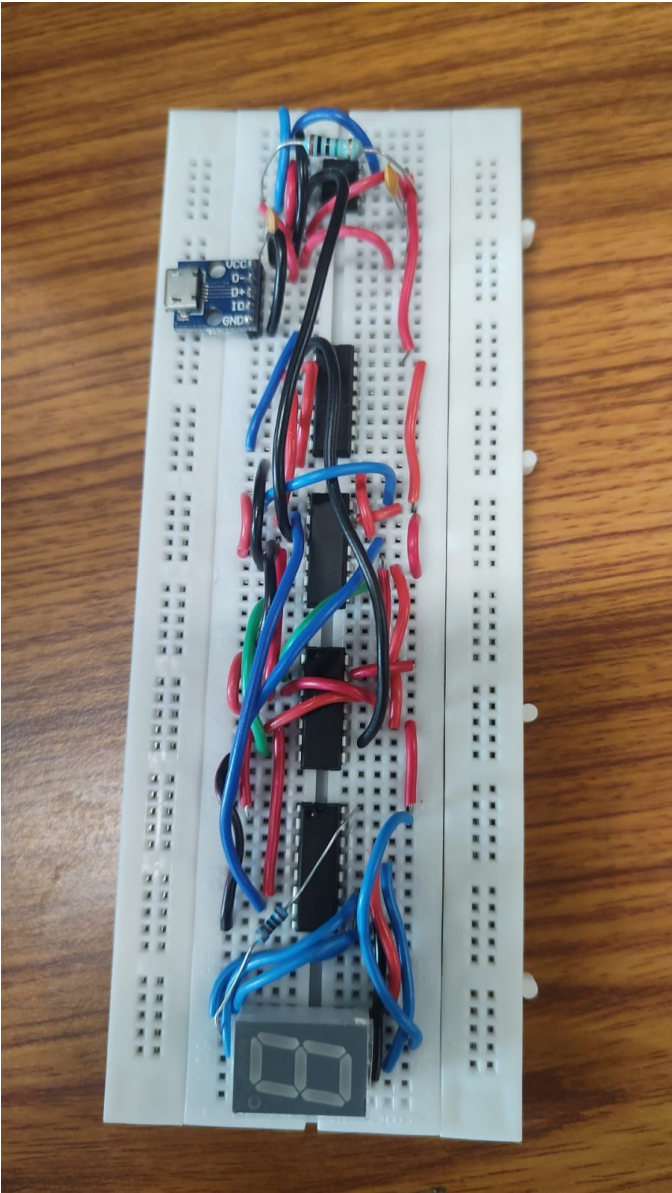


Fig. 6. output

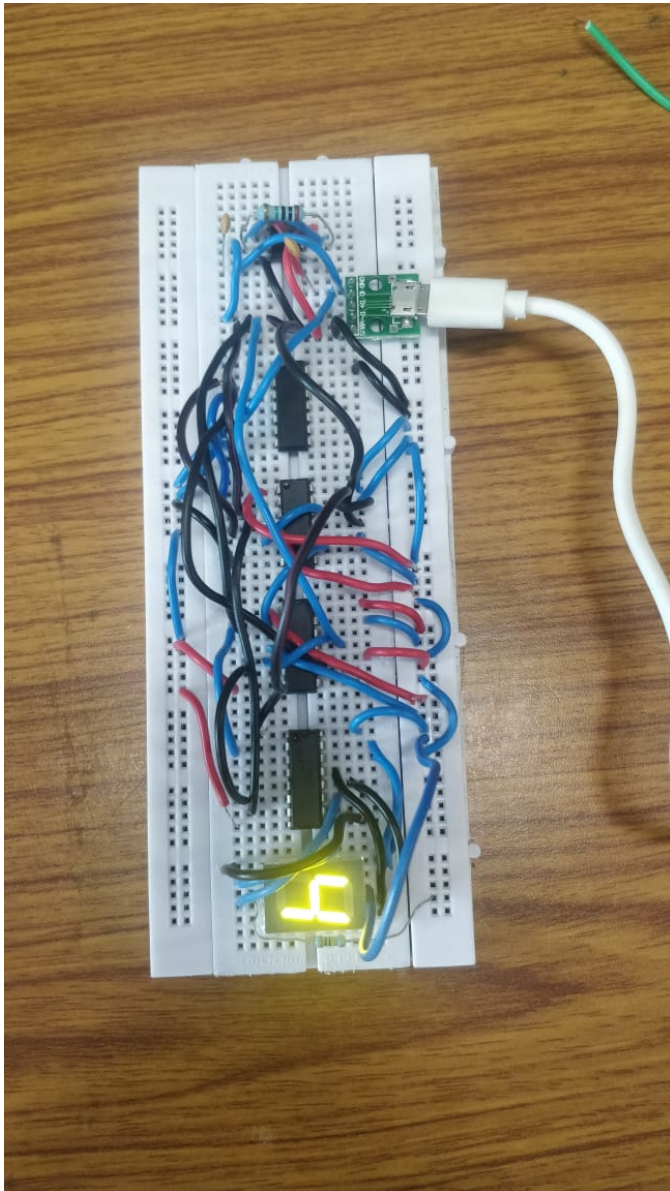


Fig. 6. output

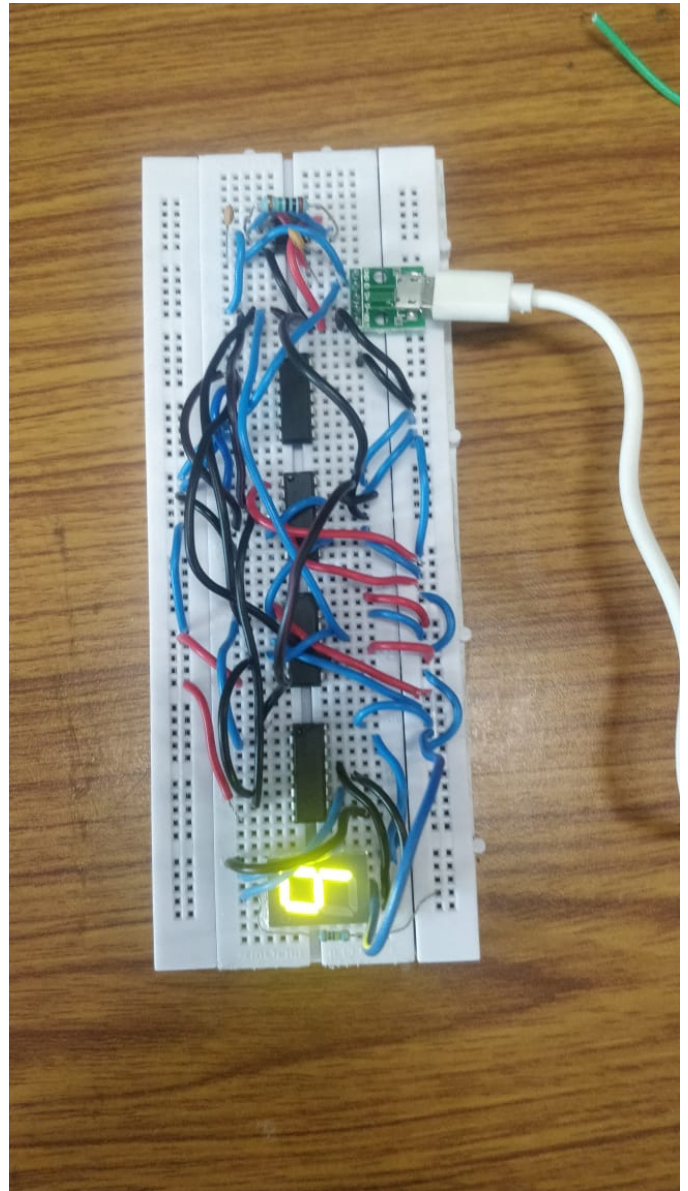


Fig. 6. output