

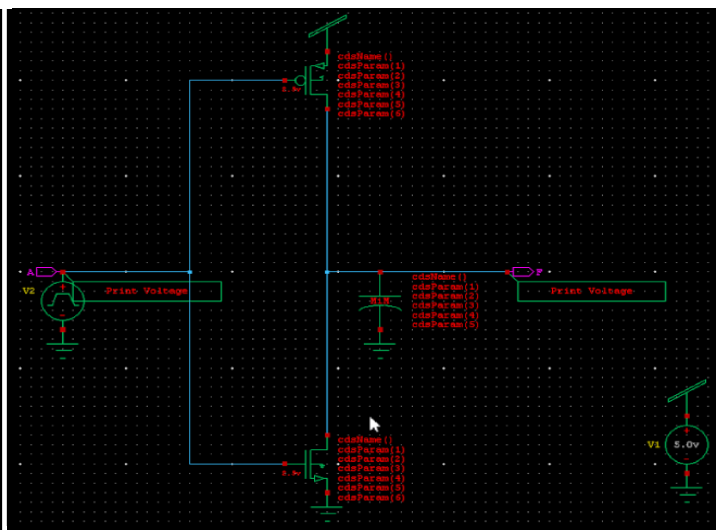
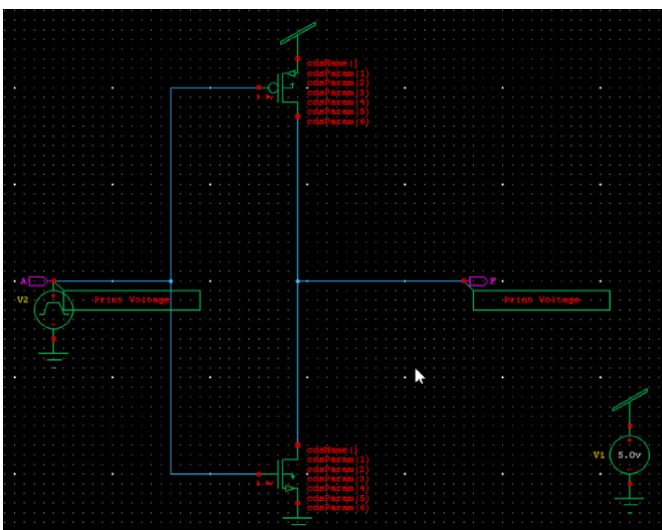
Batch 08- Simulation of circuits in T-SPICE

Objective: Develop accurate and efficient simulation models for electronic circuits using T-Spice to analyse and predict circuit behaviour under varying conditions and optimize circuit performance and reliability

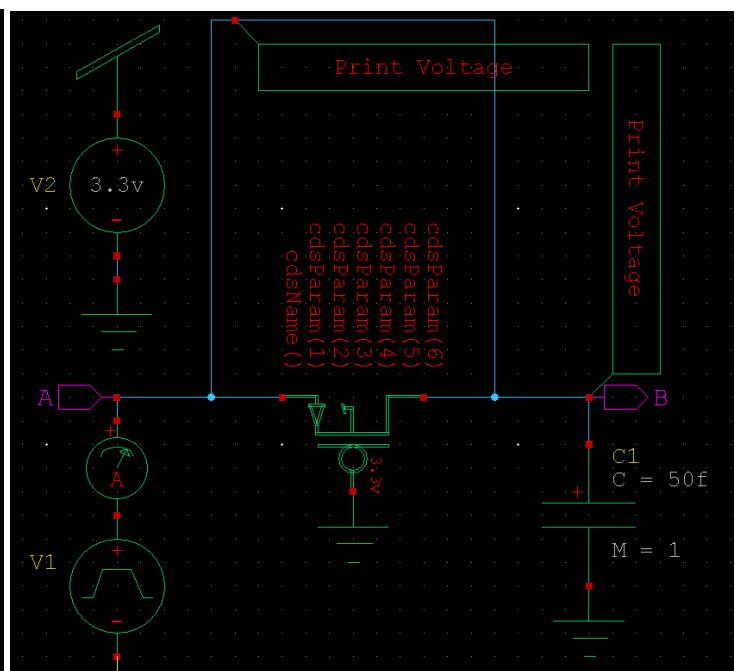
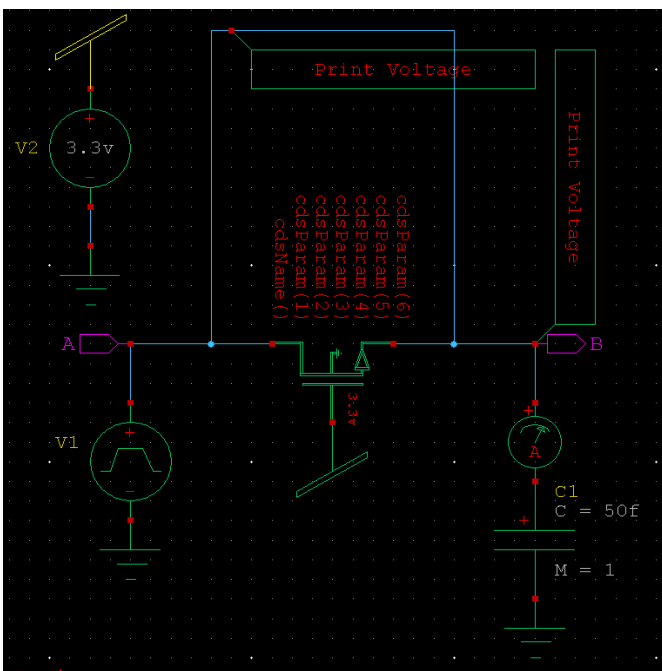
Novelty: Advanced integration of compact device models, offering accurate representation of semiconductor behaviour. Its enhanced capabilities provide engineers with a powerful tool for development of integrated circuits.

Circuits:

1. CMOS Inverter – (without and with capacitor)



2. Effective Resistance of CMOS Transmission Gate



The circuit diagram shows a common-emitter amplifier configuration. The input signal is applied to the base of the 2N2222 transistor through a 1kΩ resistor (R2). The base is biased by a 12V DC source (V1) through a 1kΩ resistor (R1). The collector is connected to the 12V source through a 1kΩ resistor (R2). The output is taken from the collector and connected to a load resistor (RL). The circuit is simulated using LTspice, showing the transient response of the output voltage (V2) and the collector current (I1). The output voltage (V2) is shown as a square wave, and the collector current (I1) is shown as a square wave. The output voltage (V2) is measured across the load resistor (RL) and the collector current (I1) is measured through the collector resistor (R2).

The diagram shows a two-port network. The input port on the left is connected to a 1M resistor and a voltage source V1. The output port on the right is connected to a 1V voltage source U2. The network consists of two dependent current sources, each labeled '1.2u'. Each current source is controlled by a voltage source 'OUT' through a 'Print Voltage' block. The current sources are connected to the input and output nodes of the network. The circuit is simulated using a SPICE engine, as indicated by the text 'SPICE' in the top right corner.

1. Arjit Avadhanam (S20210020257) – Simulation of the circuits – Effective Resistance of CMOS Transmission Gate, Gate Capacitance extension using ckt simulator.
2. Moses Jalli (S20210020282) – CMOS circuit with and without capacitor, Threshold voltage circuit.