ARJIT CHAUBEY

+91 6366333210 arjitchaubey2005@gmail.com LinkedIn GitHub

SUMMARY

Passionate ECE undergraduate with hands-on experience in RTL design, Verilog coding, and digital system simulation. Strong interest in ASIC design flows and physical design. Actively seeking internships as a front-end VLSI design engineer to apply and expand my skills in chip design.

EDUCATION

B.Tech Electronics and Communication Engineering - VLSI Design CGPA: 9.4/10
SRM University, Kattankulathur *Graduating year: 2027*

TECHNICAL SKILLS

Tools: Xilinx Vivado, ModelSim, Synopsys TCAD Suite: Sentaurus Workbench, Sentaurus Device, Sentaurus Process, LT Spice

Programming: C, Verilog, SystemVerilog, Python- libraries: numpy, pandas, matplotlib, beautifulsoup, tensorflow

EDA Scripting: Tcl (for automated workflow in Xilinx Vivado and Synopsys Sentaurus), python

Concepts: Digital Logic Design, Computer Organisation, RTL design, ASICS/FPGA synthesis flow, PCB design, device physics, CMOS design technology

Version Control: Git, Github

PROJECTS

Simulation and Implementation of a RISC V (5 staged) pipelined processor ***github***

- Designed and implemented a 32 bit 5 stage pipelined RISC V (RV32I) processor in Vivado using verilog.
- Synthesized the design at 100 MHz clock frequency. Achieved timing closure with a Worst Negative Slack (WNS) of 4.472 ns, indicating a theoretical max frequency of ~180 MHz.
- Analyzed post-implementation metrics, optimizing for 142 mW power and ~1.5k FF resource utilization.
- Modular design comprising of hazard detection, and forwarding units.

Hybrid RTL-ML CNN Hardware Accelerator ***github***

- Designed a SIMD-style convolution engine with 9 parallel MAC units for high-throughput 3x3 feature extraction.
- Built a Hybrid Verification environment using Python/TensorFlow to quantize weights (float32 to uint8) and generate golden reference vectors.
- Applied VLSI concepts such as pipelining and FSM design to enhance throughput and area efficiency.
- Implemented a software-based quantization model in Python to convert 32-bit floating-point weights to 8-bit integers (uint8), bridging the gap between software ML models and hardware implementation.

Audio-Visual Handwritten Digit Classifier ***github***

- Developed a Convolutional Neural Network (CNN) to classify MNIST digits, achieving 98%+ accuracy on the test dataset.
- Integrated the gTTS (Google Text-to-Speech) API to convert classification inference into real-time audio feedback.
- Built an end-to-end pipeline in Python including data normalization, model training, and an interactive front-end for real-time user input.

28nm HKMG NMOS Characterization & PDK Calibration ***github***

- Developed a physics-based model of a 28nm HKMG NMOS transistor, implementing Density Gradient Quantization and Trap-Assisted Tunneling models.
- Performed DC calibration against a reference PDK model, tuning Philips Unified Mobility (PhuMob) and saturation velocity parameters to achieve >95% agreement in subthreshold and saturation regions.
- Executed AC Small-Signal Analysis (1 MHz) to extract Gate Capacitance (Cgg) curves, successfully verifying Accumulation, Depletion, and Inversion regions.

EXTERNAL COURSES AND CERTIFICATIONS

- Samsung Fellowship (ISWDP TCAD Track) : *Comprehensive Level 1-3 training in semiconductor device modeling and physics simulation using Synopsys TCAD suite*
- Workshop: Accelerating AI Hardware (OpenPower) : *Explored hardware-software co-design for AI accelerators on the OpenPower ISA.*
- Remote Sensing and Digital Image Analysis : *ISRO IIRS Certification on image processing algorithms.*
- Hardware Modelling using Verilog (NPTEL) : *RTL coding, testbench generation, and FSM design for digital systems.*
- 8086 Microprocessor (Udemy) : *Studied x86 architecture, assembly language programming, and memory interfacing.*
- Digital Logic Design (Udemy) : *Comprehensive study of combinational / sequential circuits and boolean algebra optimization.*

RESEARCH EXPERIENCES

Research Intern: Indian Institute of Astrophysics, Bengaluru

- Conducted research supporting the Aditya L1 solar project under the guidance of of Dr. Wageesh Mishra.
- Analysed scientific literature on Coronal Emission Maps (CEMS) to identify existing research gaps, contributing to the team's efforts to address the existing scientifc questions.

Research Intern: Indian Institute of Technology, Roorkee

- Worked on the quantum aspects of Young's double slit experiments under Dr. Akhilesh Kumar Mishra.
- Developed analytical models to compute the wavelengths and frequencies of monochromatic and dichromatic waves
- Literature synthesis and review