ARJIT CHAUBEY

B.TECH Undergraduate student | Aspiring VLSI engineer

+91 6366333210 arjitchaubey2005@gmail.com LinkedIn GitHub

ABOUT ME

Passionate ECE undergraduate with hands-on experience in RTL design, Verilog coding, and digital system simulation. Strong interest in ASIC design flows and physical design. Actively seeking internships as a front-end VLSI design engineer to apply and expand my skills in chip design.

EDUCATION

SRM Institute of Science and Technology, Kattankulathur
CGPA: 9.4/10

SKILLS

Tools: Xilinx Vivado, ModelSim, Synopsis TCAD Suite: Sentaurus Workbench, Sentaurus Device, Sentaurus Process, LT Spice

Programming: C, Python- libraries: numpy, pandas, matplotlib, beautifulsoup, tensorflow, Verilog

Concepts: Digital Logic Design, Computer Organisation, RTL design, PCB design

Version Control: Git, Github

RESEARCH AND INTERNSHIP EXPERIENCES

Research Intern: Indian Institute of Astrophysics, Bengaluru

- Researched and studied the specifics of the Aditya L1 solar project under Dr. Wageesh Mishra.
- Analysed literature and understood the research gaps in CEMS, providing insights to tackle some of the existing scientific questions.

Research Intern: Indian Institute of Technology, Roorkee

- Worked on the quantum aspects of Young's double slit experiments under Dr. Akhilesh Kumar Mishra.
- Computed the wavelengths and frequencies of monochromatic and dichromatic waves.
- Literature synthesis and review

PROJECTS

Simulation and Implementation of a RISC V (5 staged) pipelined processor ***github***

- Designed and implemented a 5 stage pipelined RISC V processor in Vivado using verilog.
- Synthesized and deployed on Xilinx FPGA XC7K70TFBG484, achieving stable operation at 100 MHz.
- Modular design comprising of hazard detection, and forwarding units.

Handwritten digit classification with audio reproduction ***github***

- Developed a neural network in Python to classify MNIST digits with over 98 percent accuracy.
- Implemented text-to-speech output using the gTTS API to audible annouce the recognized digit in real-time.
- Demonstrated in Google Colab which included the image display and mp3 audio file generation.

Simulation and synthesis for a CNN hardware accelerator ***github***

- Designed and implemented a Verilog output buffer for a custom CNN accelerator, optimizing high-speed data flow.
- Developed and verified RTL code using industry-standard EDA tools for reliable buffer management.
- Applied VLSI concepts such as pipelining and FSM design to enhance throughput and area efficiency.
- Ensured seamless integration between accelerator logic and off-chip memory access.