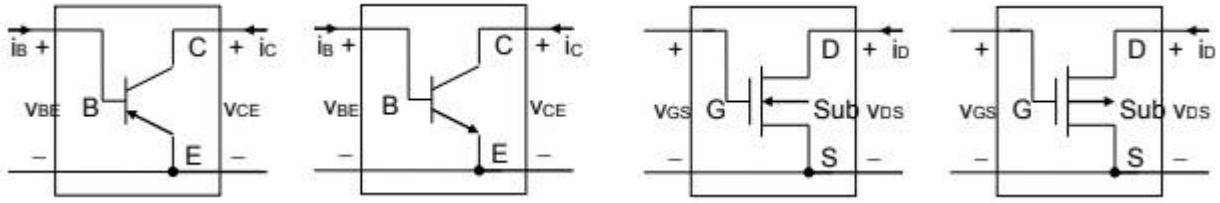
# Lab Experiment 1

## Characteristics of Basic Active Devices

In this experiment, we will examine the characteristics of the two basic active devices used in electronic circuits – the Bipolar Junction Transistor (BJT) and the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). Both these devices are active three-terminal devices, and have to be represented by controlled-source models, as shown in ***Fig. 2.1***, where the input voltage $v_1$, the input current $i_1$, the output voltage $v_2$ and the output current $i_2$ are denoted in terms of the currents and voltages at the respective device terminals – Base (B), Emitter (E) and Collector (C) for BJT; and Gate (G), Source (S) and Drain (D) for MOSFET.




**(a) pnp BJT** **(b) npn BJT** **(c) n-channel MOSFET (PMOS)** **(d) p-channel MOSFET (NMOS)**

**Fig. 2.1 Controlled Source Configurations of BJTs and MOSFETs**

As you will observe in this experiment, a BJT behaves as a current-controlled current source (CCCS), and a MOSFET, as a voltage-controlled current source (VCCS). Moreover, these devices can be active only for one polarity of all currents and voltages. All voltages and currents must be positive for npn BJT and NMOS, whereas they must all be negative for pnp BJT and PMOS.

In this experiment, the characteristics of BJT and MOSFET are verified using both hardware experiment and computer simulations.

1. In the first part, SPICE models of BJT and MOSFET are simulated using LT SPICE to obtain the input and output V-I characteristics of the devices.
2. In the second part, BJT and MOSFET are connected in proper biasing along with supply voltage to obtain the characteristics using hardware experiment.
3. The results from both SPICE simulations and hardware experiment are compared and verified if they are matching.

***Note for the TAs:***

*The lab shall start at 01.35 PM sharp. The whole agenda of the lab shall be briefly explained to the students by the TAs initially withing 5-6 minutes.*

### Part A. BJT Identification

**1.** You have to identify the type (npn or pnp) and the base terminal of each of two given BJTs – SL100 and BC557. The identification will be based on the property of a pn junction that it has a low (up to a few hundreds of ohms) forward resistance and a high (in the range of hundreds of thousands of kΩ) reverse resistance. The emitter and collector terminals cannot be identified by simple measurements, and they are indicated by markings on the device.

**2.** Measure the resistances between different pairs of leads of each BJT by the multimeter, taking two readings for each pair of terminals by reversing the multimeter polarity. A low resistance indicates that the red (+) terminal of the multimeter is connected to the p side of a pn junction. On the other hand, a high resistance indicates that the multimeter is either connected across a pn junction with the n side connected to the red (+) terminal of the multimeter, or connected between the collector and emitter terminals of the transistor.

***Note for the TAs for Part A:***

***Briefing by the TAs:*** *The TAs shall explain the methods to identify the BJTs terminals from its datasheet, and then they shall show a demo of how the device can be tested from a multimeter. Details of the 4007 IC (Pin Diagram, identifying nMOS and pMOS GATE, Substrate and Drain, etc.) shall also be explained. The explanation shall be done withing 5-10 minutes approximately. Henceforth, the students will be asked to perform the said task in point 1 and 2*

*within 10 minutes.*

***Grade:*** *This part does not contain any grading points, however it needs to be checked for assessing the understanding.*

***Expected Time for Completing of the task of Part A by the students:*** *10 minutes.*

**Part B. Arrangement for Displaying Output i-v Characteristics (5 points)**

**1.** The circuit you will use to display the output i-v characteristics of BJT and MOSFET is given in Fig. 2.2. The FG(Function/Wave Generator) is used to apply a suitable voltage across the output terminals of the DUT(Device Under Test) (C-E for BJT, D-S for MOSFET), and a potential divider consisting of two 10-kΩ resistors and one 10-kΩ potentiometer provides a variable control input to the input terminals of the DUT (B-E for BJT, G-S for MOSFET). Note that the return path of the current i2 is not to ground, but to the virtual ground created by the op-amp. This enables one to generate, using a 1.0 kΩ resistor in the feedback path of the op-amp, an output voltage vo equal in magnitude but opposite in sign to the DUT output current i2 in mA, assuming $|i1| << |i2|$. Thus you see an inverted display of the i-v characteristic of the output port for any chosen value of DUT control input (v1 or i1), which can be adjusted by the potentiometer.

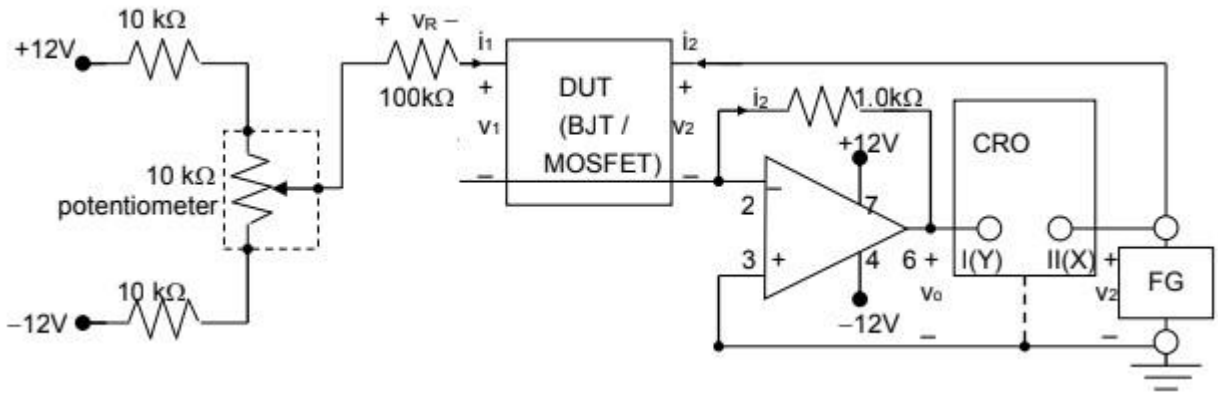



**Fig. 2.2 Circuit for displaying the output i-v characteristics of BJT/MOSFET**

**2.** Set up the circuit given in **Fig. 2.2** ***without a DUT***. Verify that $v_1$ varies from –4V to +4V (dc) as the potentiometer is turned from one extreme position to the other. Switch on the FG and the Power Supply, and set the FG controls to give a 100-Hz sine wave with a peak-to-peak value of 5V. The D-C Offset control of the FG will be used to add either +2.5V or –2.5V to this so as to ensure that $v_2$ and hence $i_2$ have the appropriate sign for each DUT as mentioned earlier. Remember that a characteristic with ***positive $i_2$ and $v_2$*** will be displayed in the ***4th quadrant***, while a characteristic with ***negative $i_2$ and $v_2$*** will be displayed in the ***2nd quadrant***.

***Note for the TAs for Part B:***

***Briefing by the TAs:*** *After the conclusion of the first part, this part shall be explained to the students within 15 minutes. The explanation shall include elaboration on the task as said in Part C and D.*

***Grade:*** *This part includes the circuit connection and hence if the desired i-v plot is not coming as expected in Part C and Part D, and if in the circuit connections made by the student on the breadboard, satisfies the following (I-IV) award* ***5 marks.***

*I. Op-amp is given correct supply voltage and that is reaching to its supply pins*
*II. Potentiometer is connected as expected.*
*III. The DUT is connected in a proper way as expected.*
*IV. FG and CRO channels are connected as expected.*

*Scope of* ***partial marks****:* ***2.5*** *if at least three of the above are correct. Zero elsewise.*

***Expected Time for Completing of the task of Part A from the students:*** *25 minutes.*

**Part C. BJT Output Characteristics (2.5 Ponits)**

1. Adjust the D-C Offset of the FG so that the FG output waveform is a sine wave having minimum and maximum values –5V and 0V respectively. Insert the ***pnp*** BJT as the DUT in the circuit of **Fig. 2.2** according to the configuration given in **Fig. 2.1(a)** [$v_1 = v_{BE}$, $i_1 = i_B$, $v_2 = v_{CE}$ and $i_2 = i_C$].
2. Observe the displayed $i_2$ vs $v_2$ characteristic. Note that the characteristic becomes practically flat, indicating a nearly constant current $|i_2|$ (say $I_{2S}$) beyond a small value of $|v_2|$. Observe the minimum and maximum values of $I_{2S}$ corresponding to the two extreme positions of the potentiometer. Obtain five different values of $I_{2S}$ over this range by suitably setting the potentiometer, and measure the values of $v_R$ and $v_1$ at each setting with the multimeter. Calculate $i_1$ from the measured value of $v_1$ and verify that $|i_1| << |i_2|$ ($\approx I_{2S}$). Sketch all the five curves on the same coordinates, labelling each curve by the corresponding value of $i_1$. Verify from the curves that the output current $i_2$ has very little dependence on the output voltage $v_2$, and thus the DUT indeed behaves like a controlled current source.
3. Plot $I_{2S}$ vs $|i_1|$ ($= |i_B|$) and verify that a BJT indeed behaves as a nearly linear CCCS with the input current $i_1$ ($= i_B$) controlling the output current $i_2$ ($= i_C$). Determine the value of the control parameter β of the BJT from the slope of this plot.
4. Remove the ***pnp*** BJT from the position of the DUT and ***change the D-C Offset*** of the FG so that $v_2$ is a sine wave having minimum and maximum values equal to 0V and +5V respectively. Now insert the ***npn*** BJT as the DUT and repeat step **C.2** and **C.3**.

***Note for the TAs for Part C:***

***Briefing by the TAs:*** *This part will is assumed to be explained by the TAs while explaining Part A. After the completion of Part B as per the expected time, announce to the whole class to proceed with this Part.*

***Grade:*** *Award **2.5 marks** if I - III is verified as mentioned.*

I. *Check the i2-v2 (Ic-Vc) response plotted in the DSO for npn and pnp [in case of pnp the FG setting should be changed in order to produced a sine wave of -5V - 0V]. The plot should be visible as expected.*
II. *Ask students to change the position of the wiper of the Potentiometer for npn case, the trace which depicts the ic plot should adjust accordingly in the DSO.*
III. *Ask students to point out minimum and maximum values of Ic=$I_{2S}$, as asked.in the active region of the device for any two different $i_B$.*

*Scope of **partial marks**: **1.5** if at least two of the above are correct. Zero elsewise.*

***Expected Time for Completing of the task of Part A from the students:*** *20 minutes.*

**Part D. NMOS Output Characteristic**

1. Remove the ***npn*** BJT from the DUT position and recheck the waveform of $v_2$. Note that the MOSFET to be tested is not an isolated device, but is one of several MOSFETS forming part of a 14-pin IC CD4007. The MOSFET you are going to use is an n-channel device (NMOS) having its Gate, Source and Drain terminals available at pins 3, 4 and 5 of the IC. All NMOS devices in the IC have a common substrate (pin 7). Connect the NMOS as the DUT, with pin 7 connected to Ground, following the configuration given in **Fig. 2.1(c)** [$v_1 = v_{GS}$, $i_1 = i_G \approx 0$, $v_2 = v_{DS}$ and $i_2 = i_D$].
2. Observe the displayed $i_2$ ($= i_D$) vs $v_2$ ($= v_{DS}$) characteristic of the NMOS, and repeat step **C.2**.
3. Plot $I_{2S}$ vs $v_1$ ($= v_{GS}$) and verify that a MOSFET indeed behaves as a nearly linear VCCS with the input voltage $v_1$ ($= v_{GS}$) controlling the output current $i_2$ ($= i_D$). Determine the value of the control parameter $g_m$ of the NMOS from the slope of this plot.

***Note for the TAs for Part D:***

***Briefing by the TAs:*** *The circuit part is assumed to be explained by the TAs while explaining Part A. Before proceeding with this part the students should be familiar with 4007 IC (Pin Diagram, identifying nMOS and pMOS GATE, Substrate and Drain, etc.). After the completion of Part B and C as per the expected time, announce to the whole class to proceed with this Part.*

***Grade:*** *Award **2.5 marks** if I - III is verified as mentioned.*

I. *Check the i2-v2 ($i_D$-$v_{DS}$) response plotted in the DSO for an nMOS, available in 4007 IC [FG setting should be changed in order to produced a sine wave of 0- 5V]. The plot should be visible as expected.*
II. *Ask students to change the position of the wiper of the Potentiometer keeping the nMOS connected, the trace which depicts the $i_D$ plot should adjust accordingly in the DSO.*
III. *Ask students to point out minimum and maximum values of $i_D$ as asked in the active region of the device for any two different $\mathbf{v}_{GS}$.*

*Scope of **partial marks**: **1.5** if at least two of the above are correct. Zero elsewise.*

***Expected Time for Completing of the task of Part A from the students:*** *20 minutes.*

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