Lab Experiment 4

Single Stage Common Emitter BJT Amplifier with Voltage Divider Bias

In this lab, a single stage Common Emitter (CE) BJT amplifier will be studied and characterized. We will determine the load line & operating point of the CE amplifier circuit and measure the voltage gain of the circuit. The CE BJT ampifier configuration with voltage divider bias is shown in the Figure 1.

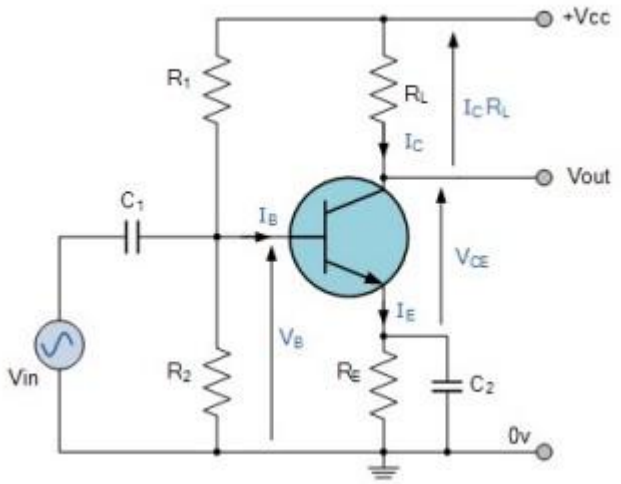

Figure 1: A Single Stage Common Emitter BJT Amplifier with Voltage Divider Bias

The DC operating point of the amplifier can be determined by drawing the load line onto the output characteristics of the BJT. From the DC analysis of the circuit shown in Figure 1,

$$
\begin{aligned}
V_B &= \frac{R_2}{R_1 + R_2} V_{CC} \\
V_E &= V_B - V_{BE} \\
V_C &= V_{CC} - I_C R_C \\
I_E &= \frac{V_E}{R_E} \\
I_C &= \frac{\beta}{\beta + 1} I_E \\
I_B &= \frac{I_E}{\beta + 1}
\end{aligned}
$$

Model parameters in terms of DC bias currents:

$$g_m = I_C/V_T$$

$$r_e = V_T/I_E$$

$$r_\pi = V_T/I_B = \beta/g_m$$

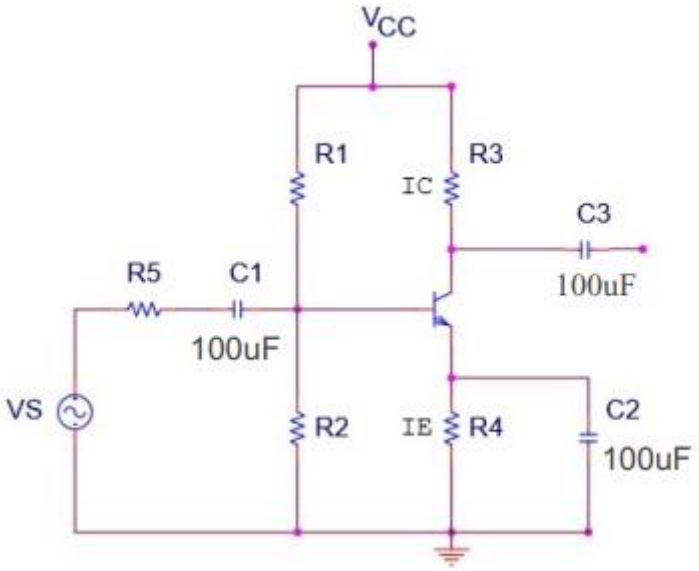

Figure 2

Part A: Setting Bias Point **(5 Points)**

1. Figure 2 shows the experimental setup for CE BJT amplifier configuration with voltage divider bias.
2. The transistor in circuit of Figure 2 has the parameters, V_{BE} = 0.7V and β = 150.
3. The capacitor values are as shown in the figure and are used to make operating point insensitive to input signal source impedance.
4. The resistors R_1 and R_2 are 5.1kΩ and 1kΩ respectively. The value of resistor R_5 is 25kΩ. Connect the voltage supply, V_{CC} to 12V.
5. Using DC signal analysis, find the values of R_3 and R_4 to obtain a collector current of 1.5mA and overall voltage gain of 5.

***Grade:* Award 5 points, if the followings are satisfied:**

1. *R3 and R4 is calculated as expected.*
2. *Bias point is achieved as expected, and able to demonstrate it in the lab.*

***Scope of partial marking:* 2 points, if:**

1. *R3 and R4 are correct, circuit is properly connected, but not able to demonstrate the bias points.*

Part B: Common Emitter Amplifier Operation **(5 Points)**

1. Connect the circuit as shown in Figure 2 using SL100 transistor and resistor values obtained from previous step.
2. Apply a Sine wave of 1Vpp and frequency 1kHz as input.
3. Measure the amplitude of output voltage and calculate the voltage gain, A_v of the amplifier.
4. Measure voltage drop across the resistor R_5 to calculate the input current. Note down the voltage at the input of the amplifier.
5. Using these values, calculate the input resistance of the amplifier circuit.
6. Vary the amplitude of the input to find the bounds on the input signal voltage for which the amplifier gives reliable output.

7. Vary the frequency of input signal by keeping the voltage constant at 1V and find the low frequency and high frequency cutoffs(-3db cutoff).

(At the cutoff points the ratio of the mid band gain to the actual gain will be equal to $\sqrt{2}$, hence if the mid band gain is 5, the gain of the amplifier at -3db cutoff will reduce to 3.5).

***Grade:* Award 5 points, if the followings are satisfied:**

1. *Steps 3, 4, 5, 6 and 7 are verified.*

***Scope of partial marking:* 2 points, if:**

2. *The circuit connection is correct, gain is seen in the DSO but the student is not able to correlate it with his/her ex[erimental data and relevant calculations.*

Notes:

1. Complete the write-up for the experiment before coming to lab. Presenting the lab report in each lab is mandatory.
2. All the observations made must be noted down in the lab report and get the report verified at the end of each experiment.
3. Plot figures from previous lab must be completed and get the same signed at the end of lab. Take a printout of any plots from SPICE simulations and staple them with corresponding experiment.

Common Point for Rubric:

If there are minor mistake in any connections, cross check the MOSFET IC and give hints to rectify the bug. Even after the hints, the students are not able to make the right connections as said, zero marks will be given.