

Lab Experiment 4

Single Stage Common Emitter BJT Amplifier with Voltage Divider Bias

In this lab, a single stage Common Emitter (CE) BJT amplifier will be studied and characterized. We will determine the load line & operating point of the CE amplifier circuit and measure the voltage gain of the circuit. The CE BJT amplifier configuration with voltage divider bias is shown in the Figure 1.

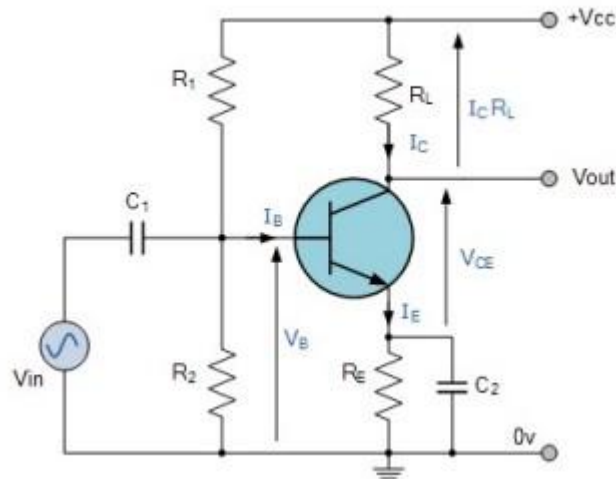


Figure 1: A Single Stage Common Emitter BJT Amplifier with Voltage Divider Bias

The DC operating point of the amplifier can be determined by drawing the load line onto the output characteristics of the BJT. From the DC analysis of the circuit shown in Figure 1,

$$\begin{aligned}
 V_B &= \frac{R_2}{R_1 + R_2} V_{CC} \\
 V_E &= V_B - V_{BE} \\
 V_C &= V_{CC} - I_C R_C \\
 I_E &= \frac{V_E}{R_E} \\
 I_C &= \frac{\beta}{\beta + 1} I_E \\
 I_B &= \frac{I_E}{\beta + 1}
 \end{aligned}$$

Model parameters in terms of DC bias currents:

$$\begin{aligned}
 g_m &= I_C / V_T \\
 r_e &= V_T / I_E \\
 r_\pi &= V_T / I_B = \beta / g_m
 \end{aligned}$$

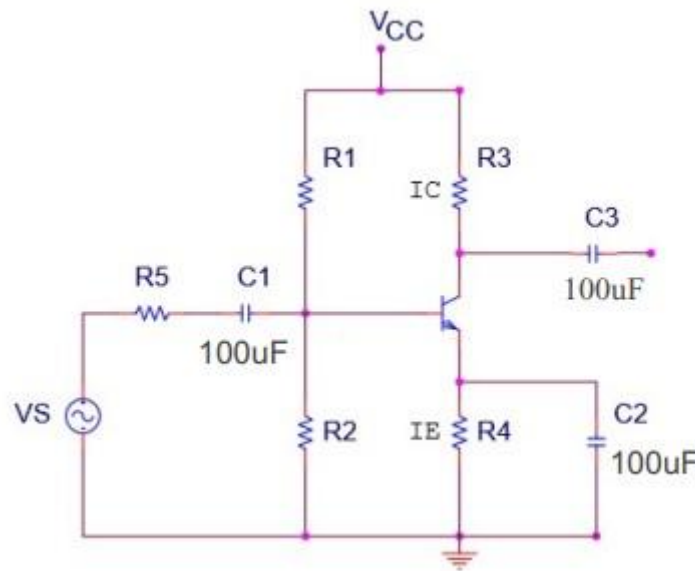


Figure 2

Part A: Setting Bias Point (5 Points)

- Figure 2 shows the experimental setup for CE BJT amplifier configuration with voltage divider bias.
- The transistor in circuit of Figure 2 has the parameters, $V_{BE} = 0.7V$ and $\beta = 150$.
- The capacitor values are as shown in the figure and are used to make operating point insensitive to input signal source impedance.
- The resistors R_1 and R_2 are $5.1k\Omega$ and $1k\Omega$ respectively. The value of resistor R_5 is $25k\Omega$. Connect the voltage supply, V_{CC} to 12V.
- Using DC signal analysis, find the values of R_3 and R_4 to obtain a collector current of 1.5mA and overall voltage gain of 5.

Grade: Award 5 points, if the followings are satisfied:

- R_3 and R_4 is calculated as expected.
- Bias point is achieved as expected, and able to demonstrate it in the lab.

Scope of partial marking: 2 points, if:

- R_3 and R_4 are correct, circuit is properly connected, but not able to demonstrate the bias points.

Part B: Common Emitter Amplifier Operation (5 Points)

- Connect the circuit as shown in Figure 2 using SL100 transistor and resistor values obtained from previous step.
- Apply a Sine wave of 1Vpp and frequency 1kHz as input.
- Measure the amplitude of output voltage and calculate the voltage gain, A_v of the amplifier.
- Measure voltage drop across the resistor R_5 to calculate the input current. Note down the voltage at the input of the amplifier.
- Using these values, calculate the input resistance of the amplifier circuit.
- Vary the amplitude of the input to find the bounds on the input signal voltage for which the amplifier gives reliable output.

7. Vary the frequency of input signal by keeping the voltage constant at 1V and find the low frequency and high frequency cutoffs(-3db cutoff).

(At the cutoff points the ratio of the mid band gain to the actual gain will be equal to $\sqrt{2}$, hence if the mid band gain is 5, the gain of the amplifier at -3db cutoff will reduce to 3.5).

Grade: Award 5 points, if the followings are satisfied:

1. Steps 3, 4, 5, 6 and 7 are verified.

Scope of partial marking: 2 points, if:

2. The circuit connection is correct, gain is seen in the DSO but the student is not able to correlate it with his/her experimental data and relevant calculations.

Notes:

1. Complete the write-up for the experiment before coming to lab. Presenting the lab report in each lab is mandatory.
2. All the observations made must be noted down in the lab report and get the report verified at the end of each experiment.
3. Plot figures from previous lab must be completed and get the same signed at the end of lab. Take a printout of any plots from SPICE simulations and staple them with corresponding experiment.

Common Point for Rubric:

If there are minor mistake in any connections, cross check the MOSFET IC and give hints to rectify the bug. Even after the hints, the students are not able to make the right connections as said, zero marks will be given.

Lab Experiment 5

MOSFET Current Mirror Circuits

A current mirror is a circuit block which functions to produce a copy of the current in one active device by replicating the current in second active device. An important feature of the current mirror is a relatively high output resistance which helps to keep the output current constant regardless of load conditions. Another feature of the current mirror is a relatively low input resistance which helps to keep the input current constant regardless of drive conditions. Conceptually, an ideal current mirror is simply an ideal current amplifier with a gain of -1. The current mirror is often used to provide bias currents and active loads in amplifier stages. Given a current source as the input, we convert the current (entering the current mirror) into a voltage and then use this voltage to control a current sink (the current exiting the mirror). A current mirror consists of a current-to-voltage converter consecutively connected to a voltage-to-current converter.

BJT and MOSFET current mirrors are widely used to produce supply voltage and temperature independent current sources in integrated circuits. These circuits replicate a golden current produced using sophisticated methods. A basic current mirror circuit using MOSFETs is shown in Fig. 1.

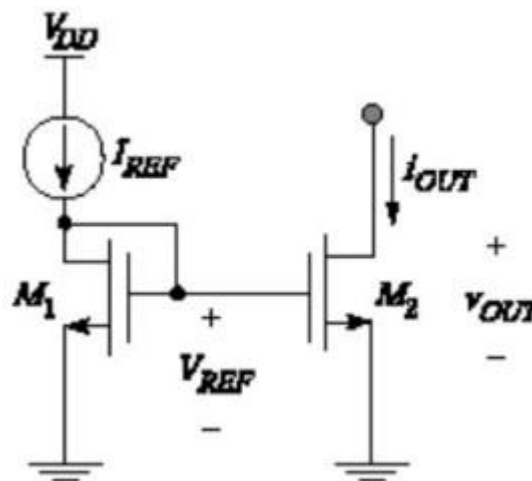


Figure 1: MOSFET Current Mirror Circuit with Constant Supply Current

In the above circuit, the constant supply current at drain of MOSFET M_1 results in a constant voltage across its gate terminal. This same voltage is applied as input voltage to the gate terminal of MOSFET M_2 and hence the current i_{OUT} at its drain remains constant and is given by

$$i_{OUT} = I_{REF} \frac{(W/L)_1}{(W/L)_2} \quad (1)$$

The above equation assumes that both MOSFETs are perfectly matched in all other parameters like threshold voltage and mobility.

MOSFET Parameters: $K = 0.5\text{mA/V}^2$, $V_T = 1\text{V}$.

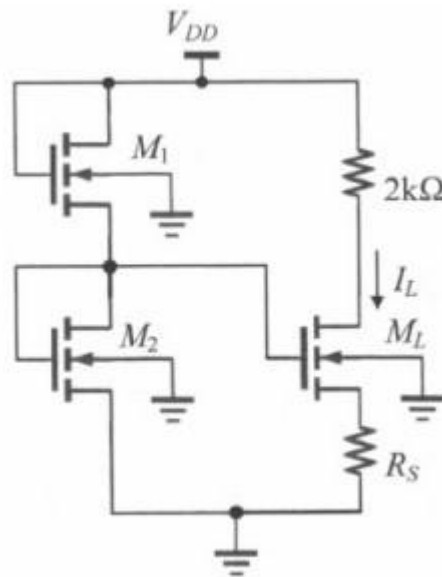


Figure 2: Widlar Current Mirror Circuit

Experimental Setup (10 Points)

1. The Widlar current mirror circuit using MOSFET is shown in Figure 2.
2. Short out R_S , and adjust V_{DD} such that $I_{D-M1} = I_{REF} = 1\text{mA}$. V_{DD} will be given from the DC power supply available in the lab.
3. Set R_S to $1\text{K}\Omega$, and $2\text{K}\Omega$ and measure the respective I_L ?
4. I_L can be calculated by measuring the voltage drop across the $2\text{k}\Omega$ resistor.
5. Short out R_S , and adjust V_{DD} such that $I_{D-M1} = I_{REF} = 5\text{mA}$.
6. Repeat Step 3.
7. Comment on your results, esp. with respect to the Widlar current mirror.

Grade: Award 10 points, if the followings are satisfied:

1. The current mirror circuit is connected as expected.
2. The student is able to demonstrate the reference current with $R_S=0$, as asked in point 2.
3. All the other steps are verified by changing R_S and I_{ref} as asked.

Scope of partial marking: 6 points, if:

1. The circuit connection is proper, and the supplies are reaching to the desired points.
2. The student is able to demonstrate at least for one case of R_S (1k or 2k).

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Common Point for Rubric:

If there are minor mistake in any connections, cross check the MOSFET IC and give hints to rectify the bug. Even after the hints, the students are not able to make the right connections as said, zero marks will be given.

Lab Experiment 6

Power Amplifiers

In this lab, we will analyse and experimentally test the working of Class A and Class B Push-Pull power amplifiers. We will determine the load line & operating point of the said amplifier circuits and measure their efficiency.

Power conversion efficiency of these amplifiers are given as,

$$\frac{\text{AC power in the Load}}{\text{Power delivered by the DC source or supplies}}$$

Now, let us say if the peak voltage seen across a resistive load is $\widehat{v_o}$ then the AC power in the load is given as,

$$P_{ac} = \frac{(\widehat{v_o}/\sqrt{2})^2}{RL} = \frac{\widehat{v_o}^2}{2RL} \quad (1)$$

$\widehat{v_o}$ can be measured from the DSO by looking at the output signal.

- a. For Class A amplifier as shown, the average DC power drawn from the supply will be

$$P_{DC} = V_{CC}I_{CQ} \quad (2)$$

$$\begin{aligned} \eta &= (P_{AC}/P_{DC}) \cdot 100 \\ \Rightarrow \eta &= \frac{(\widehat{v_o})^2}{2RL.V_{CC}.I_C} \end{aligned} \quad (3)$$

- Here we see that the efficiency will be maximum at $\widehat{v_o}$ will be equal to V_{CC} .

- b. For Class B amplifier, the current drawn from each supply will consist of half-sine waves of peak amplitude $\widehat{v_o}/RL$. Thus the average current drawn from each of the two power supplies will be $\frac{\widehat{v_o}}{\pi RL}$. It follows that the average power drawn from each of the two power supplies will be the same,

$$P_{S+} = P_{S-} = \left(\frac{\widehat{v_o}}{\pi RL} \right) \cdot V_{CC}$$

Hence, the total supply power will be,

$$P_S = P_{DC} = \left(\frac{2\widehat{v_o}}{\pi RL} \right) \cdot V_{CC} \quad (4)$$

$$\begin{aligned} \eta &= (P_{AC}/P_{DC}) \cdot 100 \\ \Rightarrow \eta &= \frac{\pi \widehat{v_o}^2}{4V_{CC}} \end{aligned} \quad (5)$$

- Here we see that the efficiency will be maximum when $\widehat{v_o}$ will be equal to V_{CC} .

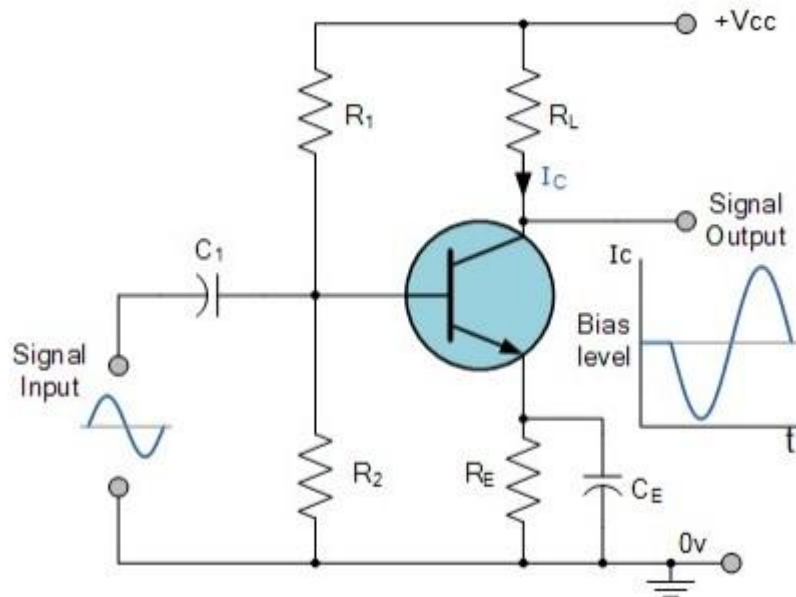


Figure 1: Class A Power Amplifier

Part A: Class A Power Amplifier (5 Points)

1. A single stage Class A power amplifier circuit is shown in Figure 1.
2. The load resistance $R_L = 1\text{K}\Omega$, emitter resistance $R_E = 100\Omega$ and supply voltage $V_{CC} = 12\text{V}$, $C_E = 100\mu\text{F}$ and $C_1 = 10\mu\text{F}$.
3. The transistor has the parameters $\beta = 150$ (SL100) and $V_{BE} = 0.7\text{V}$.
4. Determine the values of resistors R_1 and R_2 to obtain $V_{BB} = 3.5\text{V}$ and $V_{CEQ} = 6\text{V}$.
5. Connect the class A power amplifier circuit as shown in the figure.
6. Apply a sinusoidal signal of frequency 1kHz .
7. Calculate the output AC power (refer to equation 1) and power drawn from the supply voltage ($P_{DC} = V_{CC}I_{CQ}$) (refer to equation 4).
8. Calculate the efficiency of the amplifier, $\eta = (P_{ac}/P_{DC}) * 100$ (refer equation 5).
9. Repeat the experiment for different values of input voltage signal (take at least three sample, where within the samples a largest peak value of the input should be selected such that $\widehat{v_o} = V_{CC}$).

Grade: Award 5 points, if the followings are satisfied:

1. Bias points are verified as expected in point 4.
2. Point no. 7 and 8 are verified for atleast two input samples.

Scope of partial marking: 2 points, if:

1. R_1 and R_2 are correct, circuit is properly connected, and able to demonstrate the bias points.

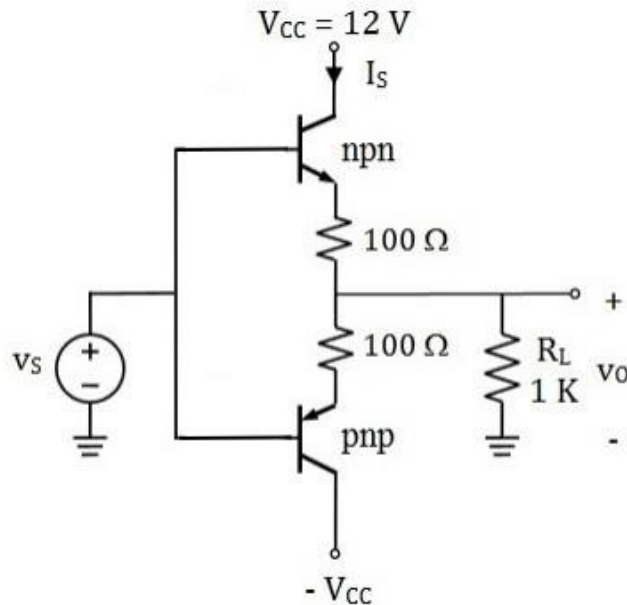


Figure 2: Class B Power Amplifier

Part B: Class B Push Pull Power Amplifier (5 Points)

1. A Class B power amplifier in push pull configuration is shown in Figure 2.
2. Connect the circuit as shown in the figure and apply a sinusoidal signal of frequency 1 kHz .
3. Observe output signal voltage and determine its maximum voltage.
4. Calculate the output ac power (refer equation 1) and power drawn from the supply voltage (refer equation 1). Calculate the efficiency of Class B power amplifier.
5. Repeat the experiment for different values of input voltage signal (take at least three sample, where within the samples a largest peak value of the input should be selected such that $\hat{v}_o = V_{cc}$).

Grade: Award 5 points, if the followings are satisfied:

3. The circuit is properly connected as expected and point no. 3 is verified.
4. Point no. 4 and 5 are verified for atleast two input samples.

Scope of partial marking: 2 points, if:

2. The circuit is properly connected as expected and point no. 3 is verified. However, not able to measure or get the results for point 4 and 5.

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