PROJECT WORK

"Verilog Implementation of Digital Circuit Designs on FPGA using Vivado"

Topic: Traffic Light Controller Design using Verilog

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ACKNOWLEDGEMENT

I take this opportunity to express my profound gratitude and deep regards to my guide Professor Poonam Kasturi and Ankur Sangal for their exemplary guidance, monitoring and constant encouragement throughout the course of this project.

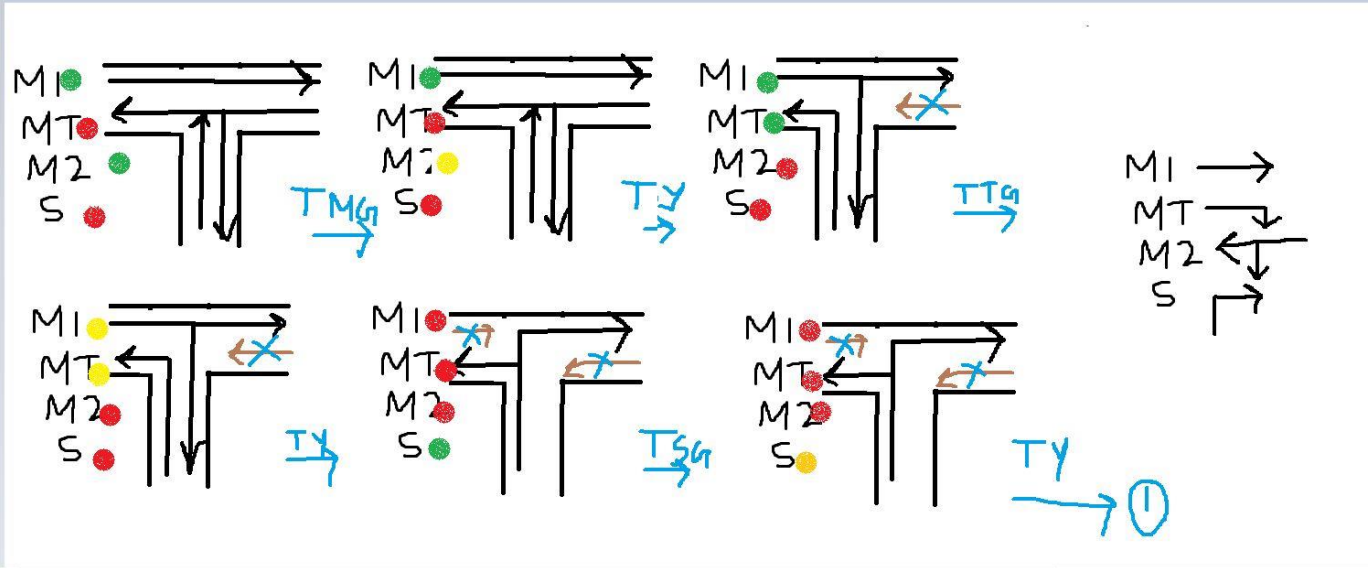
The blessing, help and guidance given by him time to time shall carry me a long way in the journey of life on which I am about to embark.

My thanks and appreciations also go to my colleague in developing the project and people who have willingly helped me out with their abilities

PROBLEM STATEMENT

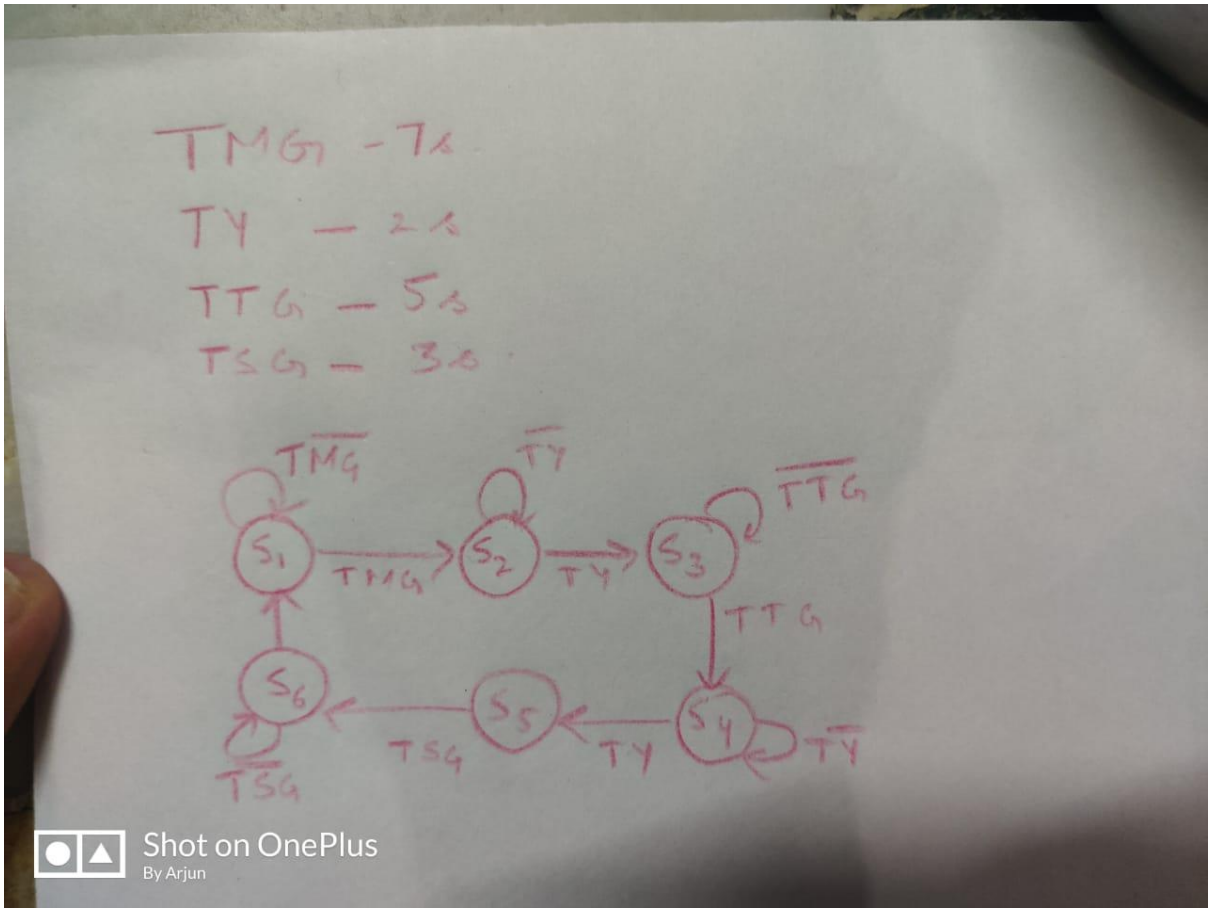
The aim of the project is to design a traffic controller for a T-intersection.

Let’s understand the problem statement through the image given below.

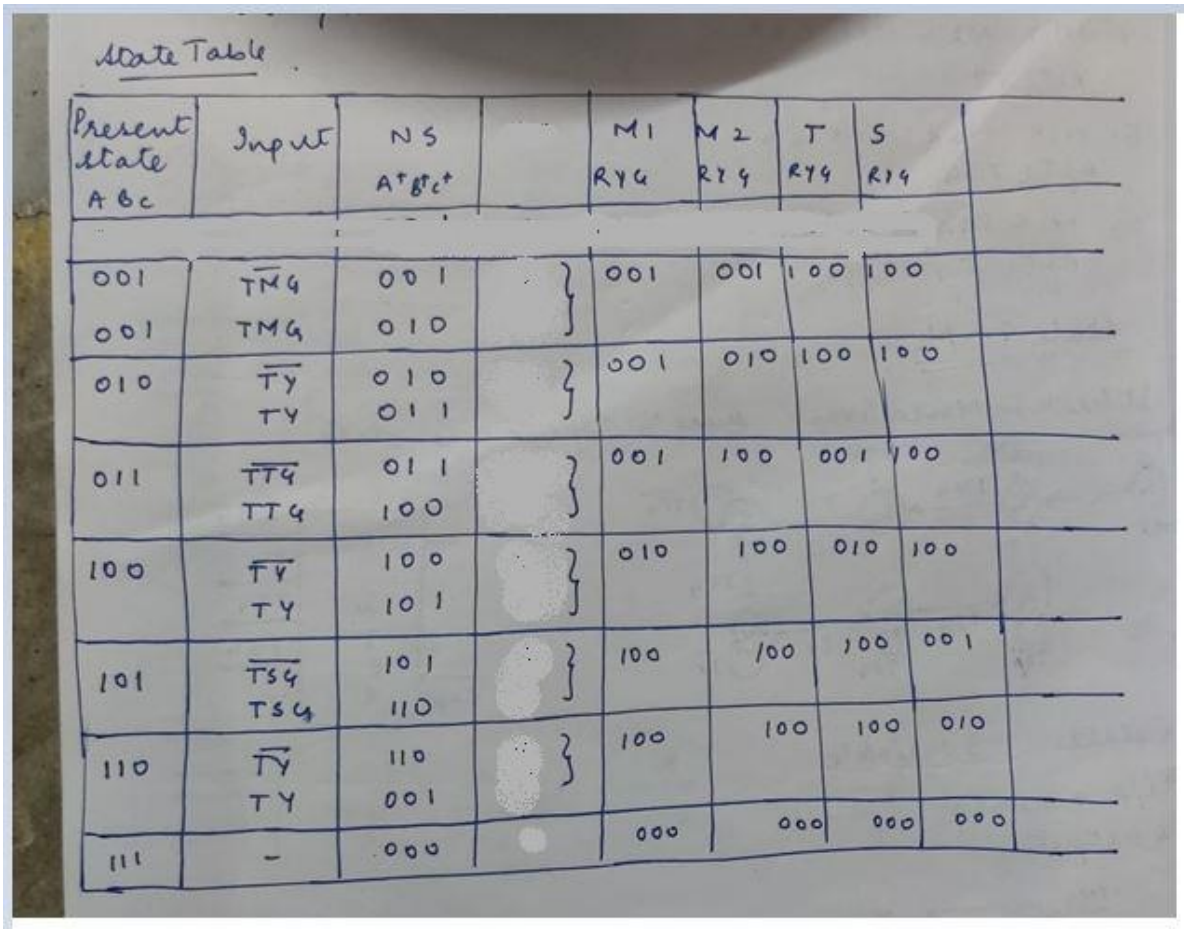


The six cases present here eventually turn to the six states .

This is the state diagram:



From the state diagram we for the state table:



State Table

Present state A B c	Input	NS $A^+B^+c^+$		M1 R Y G	M2 R Y G	T R Y G	S R Y G
001	$\overline{TMG}$	001	}	001	001	100	100
001	TMG	010					
010	$\overline{TY}$	010	}	001	010	100	100
	TY	011					
011	$\overline{TTG}$	011	}	001	100	001	100
	TTG	100					
100	$\overline{TY}$	100	}	010	100	010	100
	TY	101					
101	$\overline{TSG}$	101	}	100	100	100	001
	TSG	110					
110	$\overline{TY}$	110	}	100	100	100	010
	TY	001					
111	-	000		000	000	000	000

VERILOG CODE

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 16.07.2020 12:53:25
// Design Name:
// Module Name: Traffic_Light_Controller
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module Traffic_Light_Controller(


    input clk,rst,
    output reg [2:0]light_M1,
    output reg [2:0]light_S,
    output reg [2:0]light_MT,
```

```
output reg [2:0]light_M2
);

parameter  S1=0, S2=1, S3 =2, S4=3, S5=4,S6=5;
reg [3:0]count;
reg[2:0] ps;
parameter  sec7=7,sec5=5,sec2=2,sec3=3;



always@(posedge clk or posedge rst)
   begin
   if(rst==1)
   begin
   ps<=S1;
   count<=0;
   end
   else



      case(ps)
         S1: if(count<sec7)
               begin
               ps<=S1;
               count<=count+1;
               end
            else
               begin
```

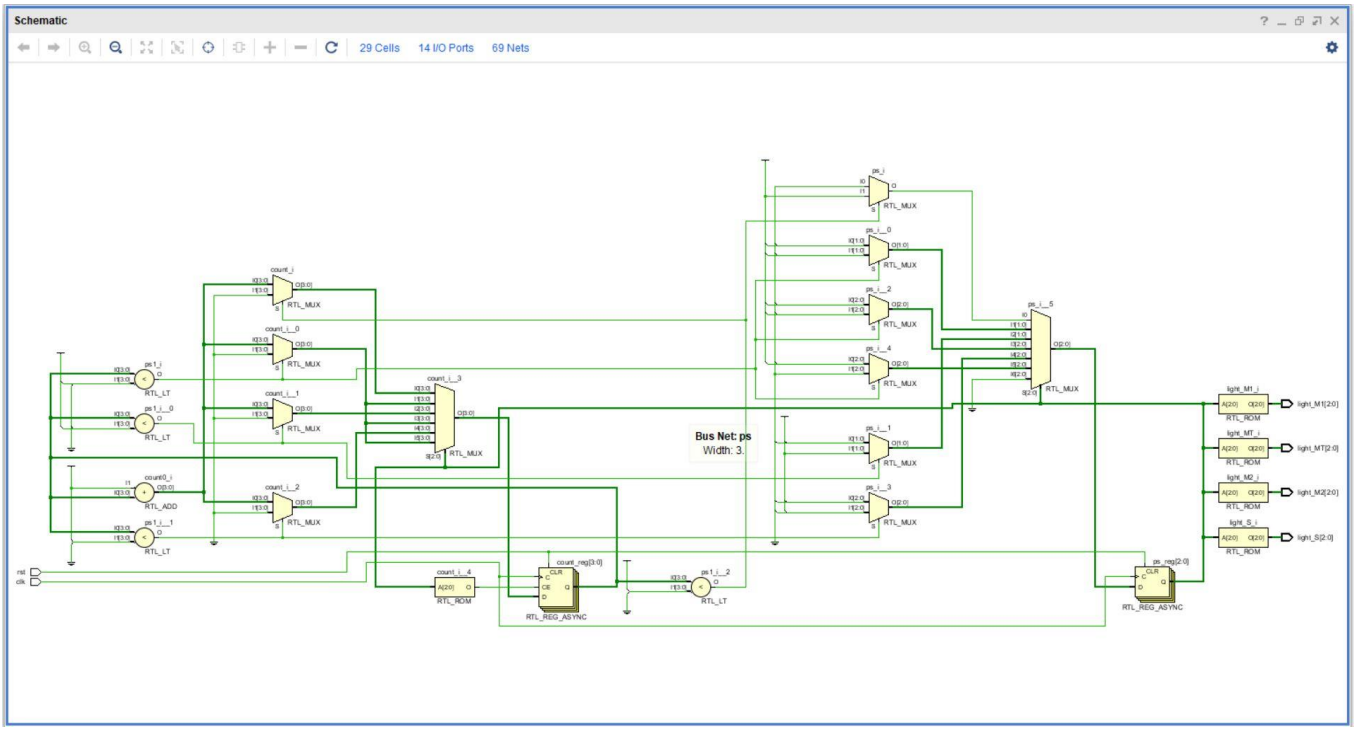
```
        ps<=S2;
        count<=0;
        end
S2: if(count<sec2)
        begin
        ps<=S2;
        count<=count+1;
        end

    else
        begin
        ps<=S3;
        count<=0;
        end
S3: if(count<sec5)
        begin
        ps<=S3;
        count<=count+1;
        end

    else
        begin
        ps<=S4;
        count<=0;
        end
S4:if(count<sec2)
        begin
        ps<=S4;
        count<=count+1;
        end
```

```
    else
        begin
        ps<=S5;
        count<=0;
        end
S5:if(count<sec3)
        begin
        ps<=S5;
        count<=count+1;
        end

    else
        begin
        ps<=S6;
        count<=0;
        end

S6:if(count<sec2)
        begin
        ps<=S6;
        count<=count+1;
        end

    else
        begin
        ps<=S1;
        count<=0;
        end
default: ps<=S1;
```

```
    endcase
end

always@(ps)
begin
    case(ps)

        S1:
        begin
          light_M1<=3'b001;
          light_M2<=3'b001;
          light_MT<=3'b100;
          light_S<=3'b100;
        end
        S2:
        begin
          light_M1<=3'b001;
          light_M2<=3'b010;
          light_MT<=3'b100;
          light_S<=3'b100;
        end
        S3:
        begin
          light_M1<=3'b001;
          light_M2<=3'b100;
          light_MT<=3'b001;
          light_S<=3'b100;
        end
        S4:
        begin
```

```
            light_M1<=3'b010;
            light_M2<=3'b100;
            light_MT<=3'b010;
            light_S<=3'b100;
        end
        S5:
        begin
            light_M1<=3'b100;
            light_M2<=3'b100;
            light_MT<=3'b100;
            light_S<=3'b001;
        end
        S6:
        begin
            light_M1<=3'b100;
            light_M2<=3'b100;
            light_MT<=3'b100;
            light_S<=3'b100;
        end
        default:
        begin
            light_M1<=3'b000;
            light_M2<=3'b000;
            light_MT<=3'b000;
            light_S<=3'b010;
        end
        endcase
    end

endmodule
```

RTL-SCHEMATIC

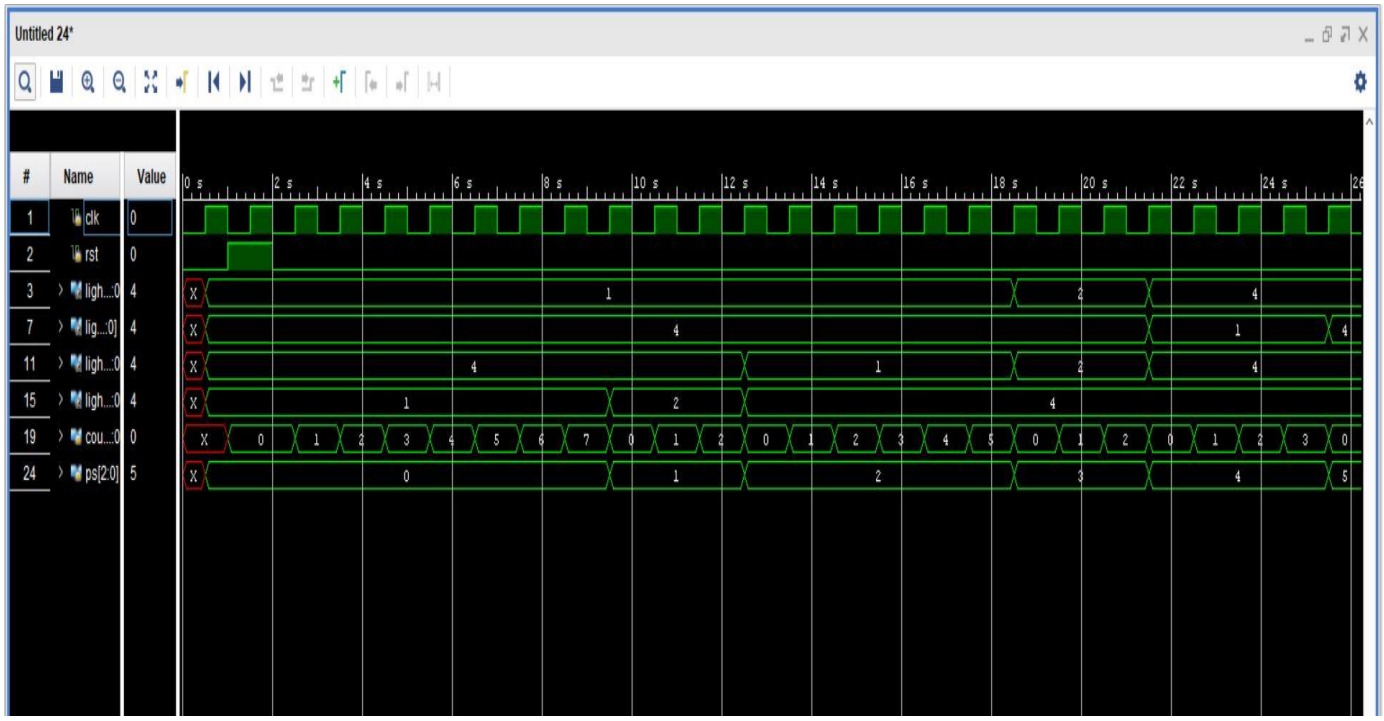


TESTBENCH

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 16.07.2020 23:44:40
// Design Name:
// Module Name: Traffic_Light_Controller_TB
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
```

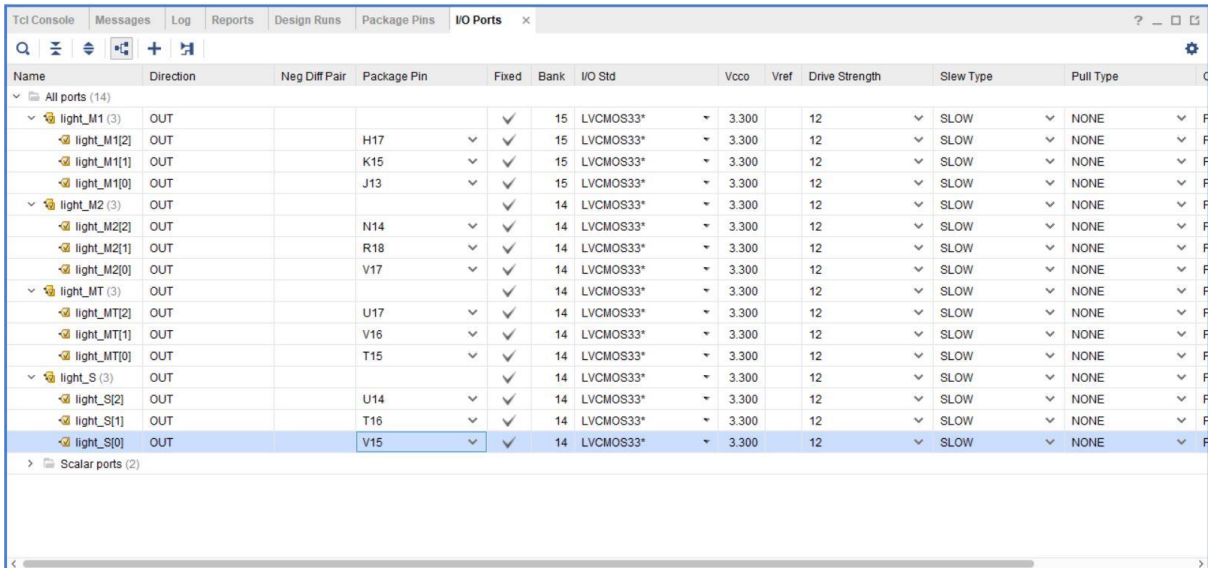
```
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module Traffic_Light_Controller_TB;
reg clk,rst;
wire [2:0]light_M1;
wire [2:0]light_S;
wire [2:0]light_MT;
wire [2:0]light_M2;
Traffic_Light_Controller dut(.clk(clk) , .rst(rst) , .light_M1(light_M1) , .light_S(light_S)
,.light_M2(light_M2),.light_MT(light_MT)    );
initial
begin
    clk=1'b0;
    forever #(1000000000/2) clk=~clk;
end
initial
begin
    rst=0;
    #1000000000;
    rst=1;
    #1000000000;
    rst=0;
    #(1000000000*200);
    $finish;
    end
endmodule
```

SIMULATED WAVEFORM



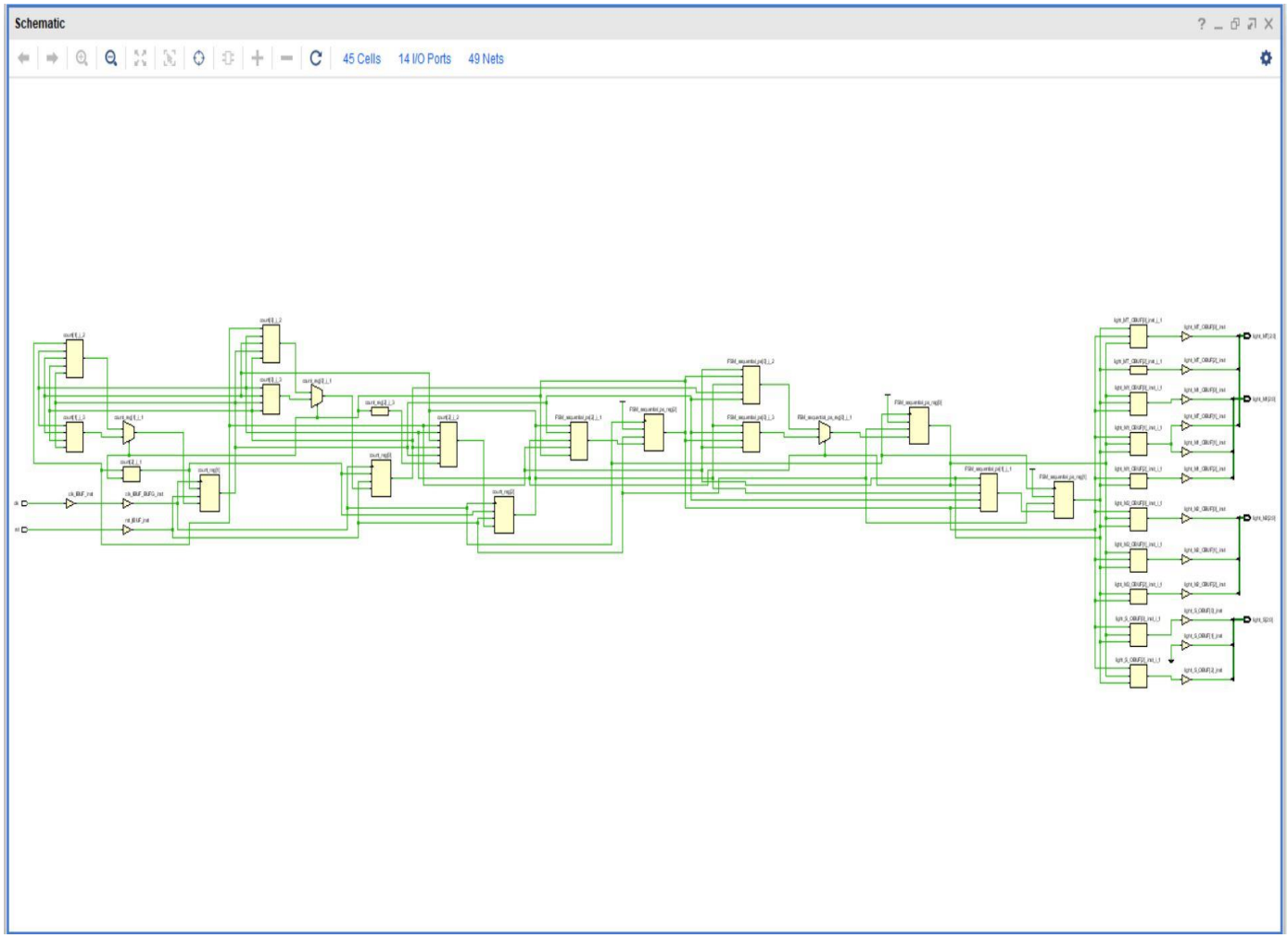
Upon analysing the waveform we can clearly see that the FSM works perfectly.

IO PORT ASSIGNMENT



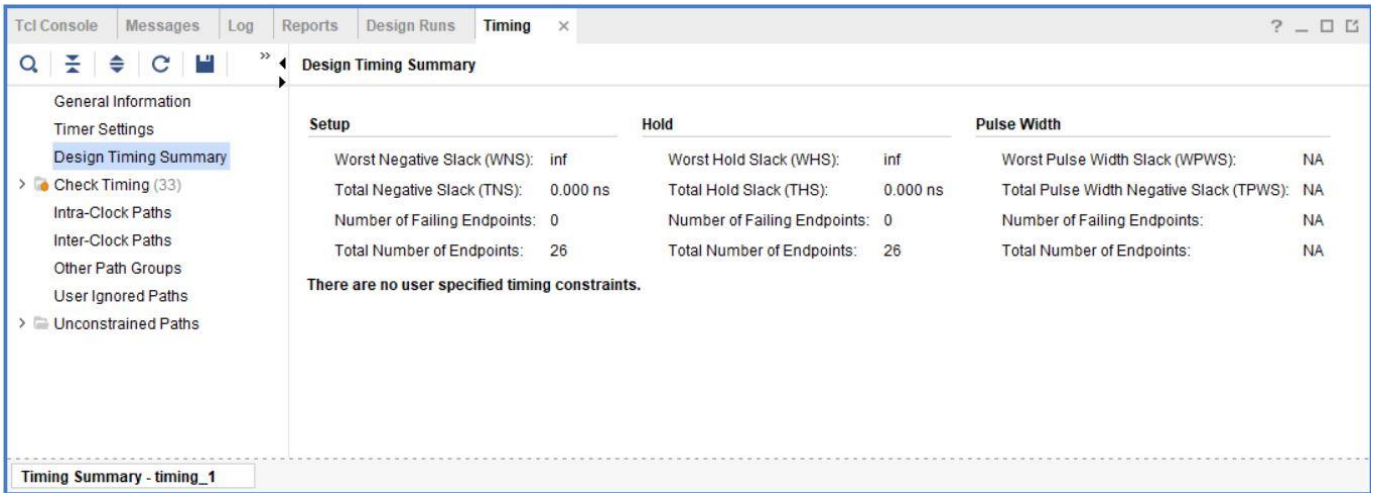
The ports are assigned from the ucf file .

SCHEMATIC AFTER SYNTHESIS

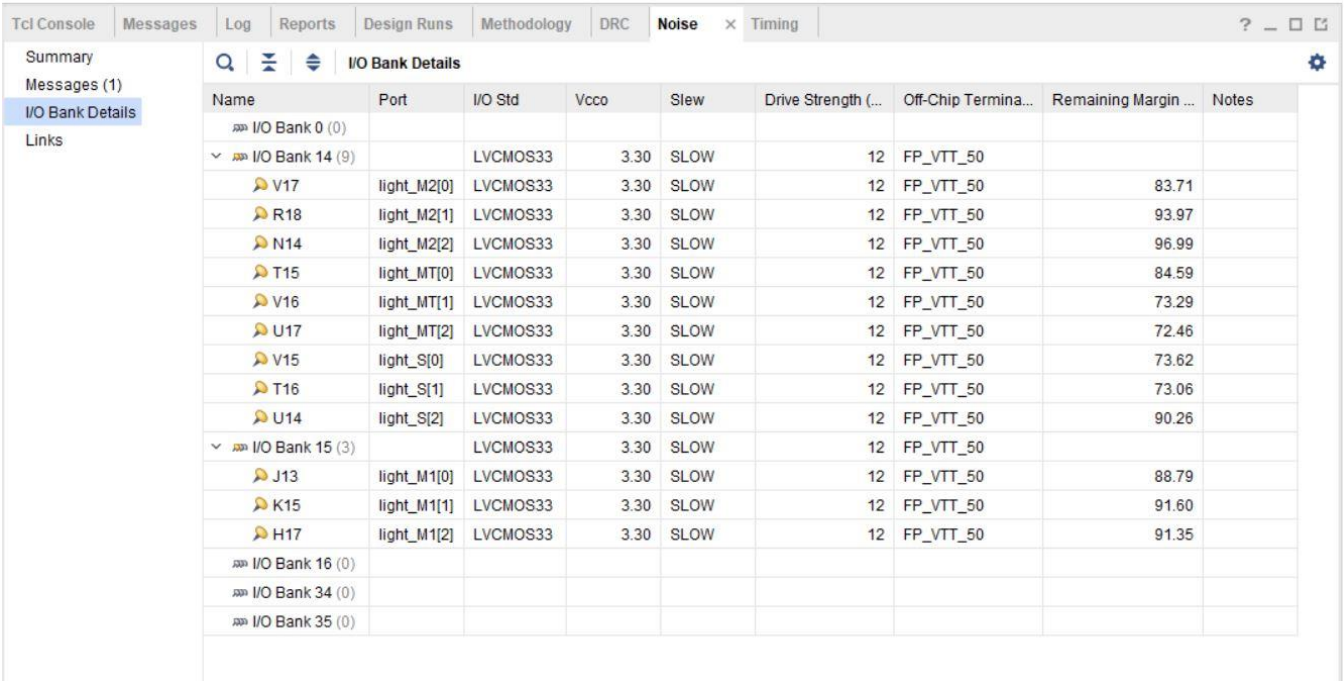


REPORTS AFTER SYNTHESIS

TIMING REPORT

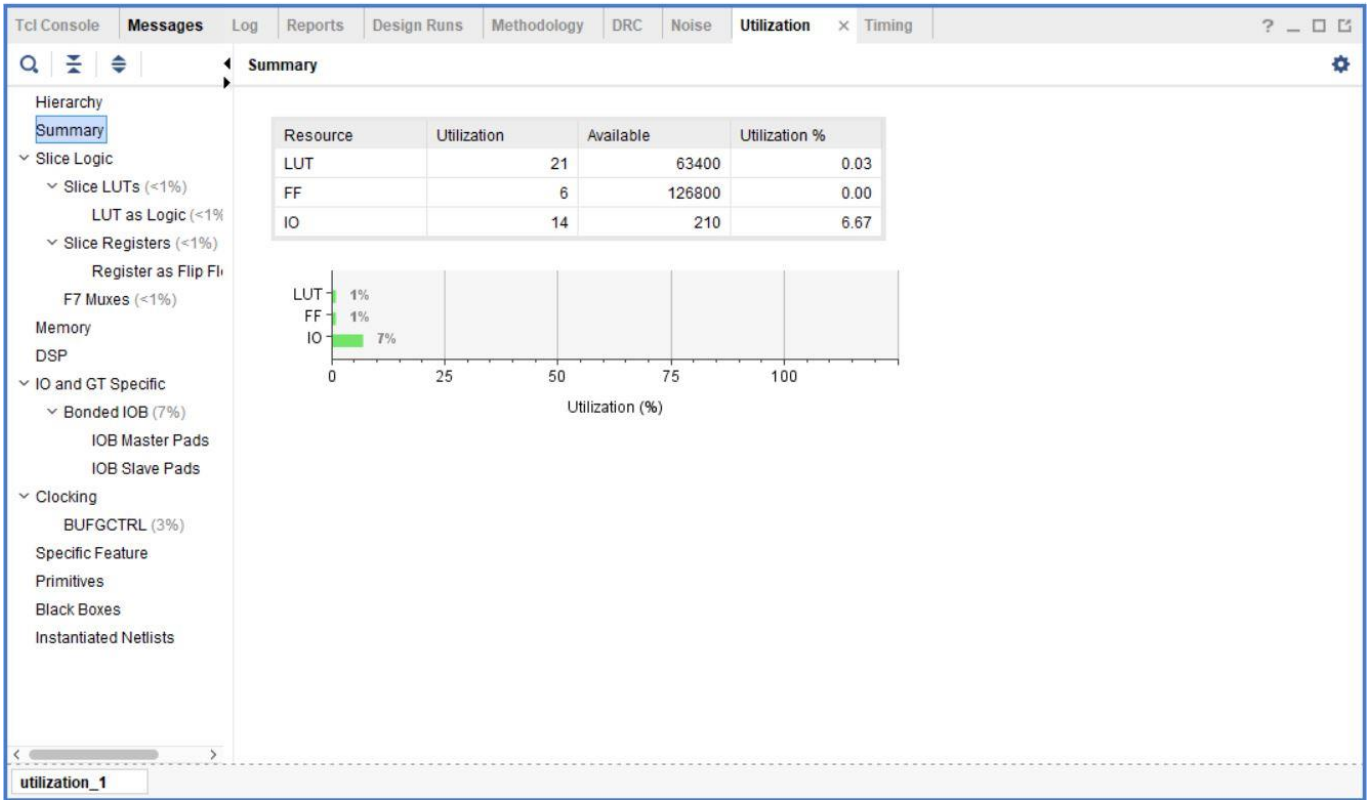


NOISE REPORT



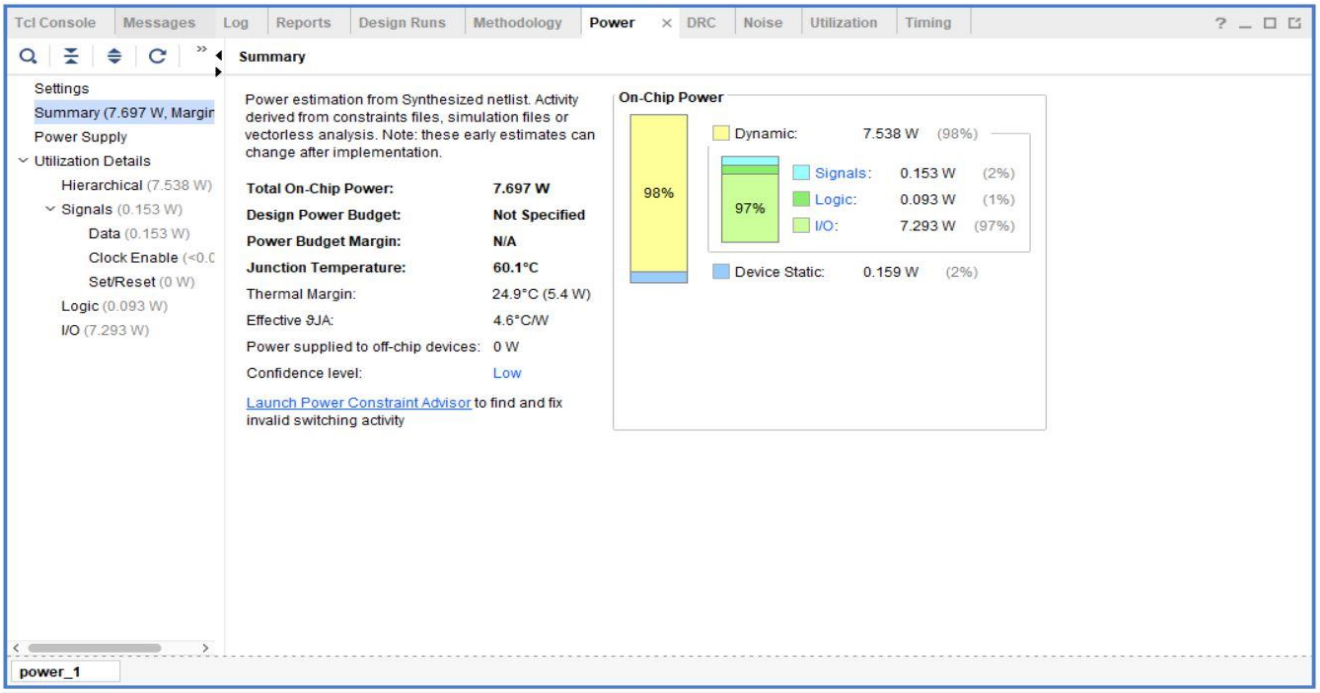
Name	Port	I/O Std	Vcco	Slew	Drive Strength (...	Off-Chip Termina...	Remaining Margin ...	Notes
I/O Bank 0 (0)								
I/O Bank 14 (9)		LVCMOS33	3.30	SLOW	12	FP_VTT_50		
V17	light_M2[0]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	83.71	
R18	light_M2[1]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	93.97	
N14	light_M2[2]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	96.99	
T15	light_MT[0]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	84.59	
V16	light_MT[1]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	73.29	
U17	light_MT[2]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	72.46	
V15	light_S[0]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	73.62	
T16	light_S[1]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	73.06	
U14	light_S[2]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	90.26	
I/O Bank 15 (3)		LVCMOS33	3.30	SLOW	12	FP_VTT_50		
J13	light_M1[0]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	88.79	
K15	light_M1[1]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	91.60	
H17	light_M1[2]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	91.35	
I/O Bank 16 (0)								
I/O Bank 34 (0)								
I/O Bank 35 (0)								

UTILIZATION REPORT

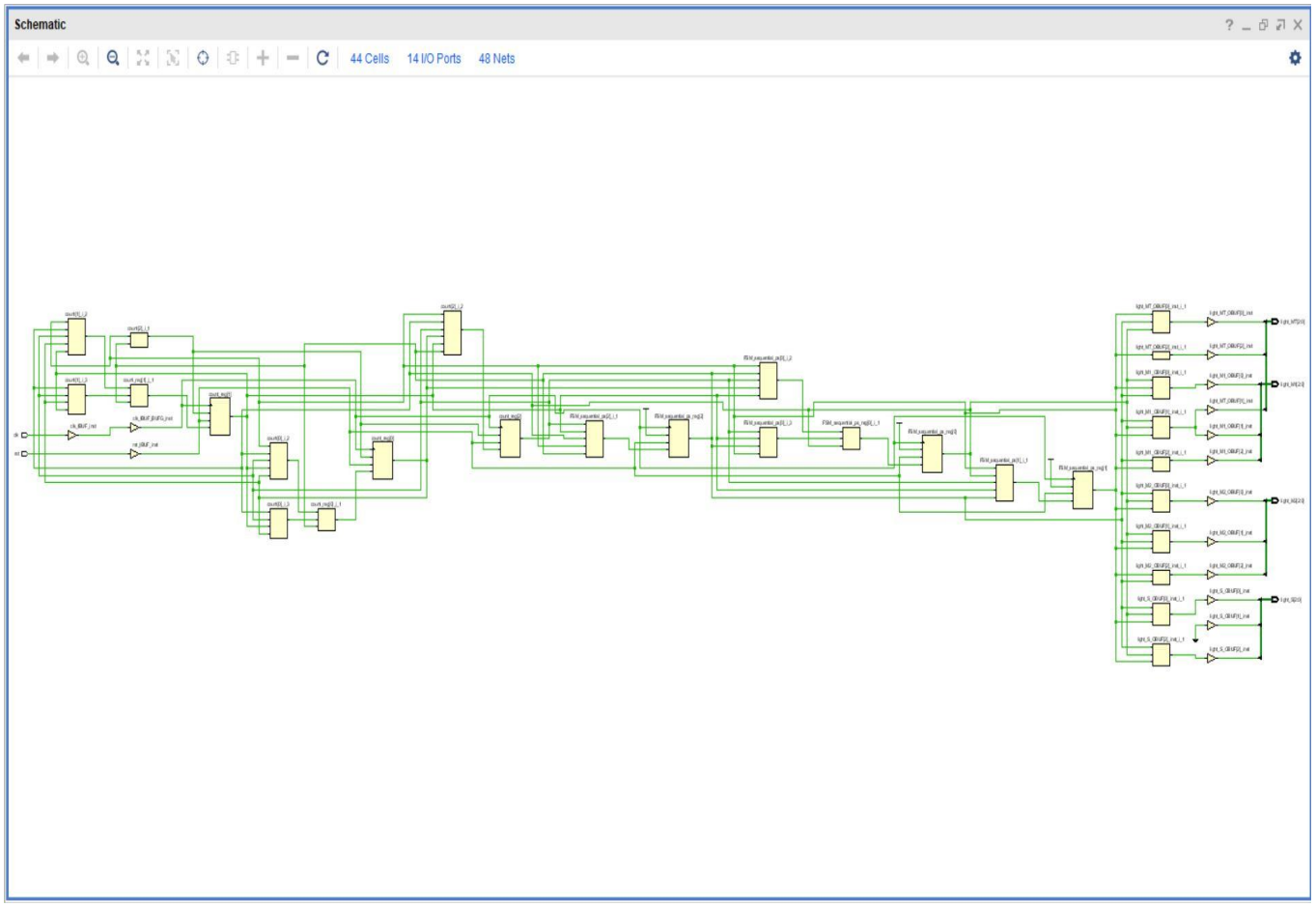


Resource	Utilization	Available	Utilization %
LUT	21	63400	0.03
FF	6	126800	0.00
IO	14	210	6.67

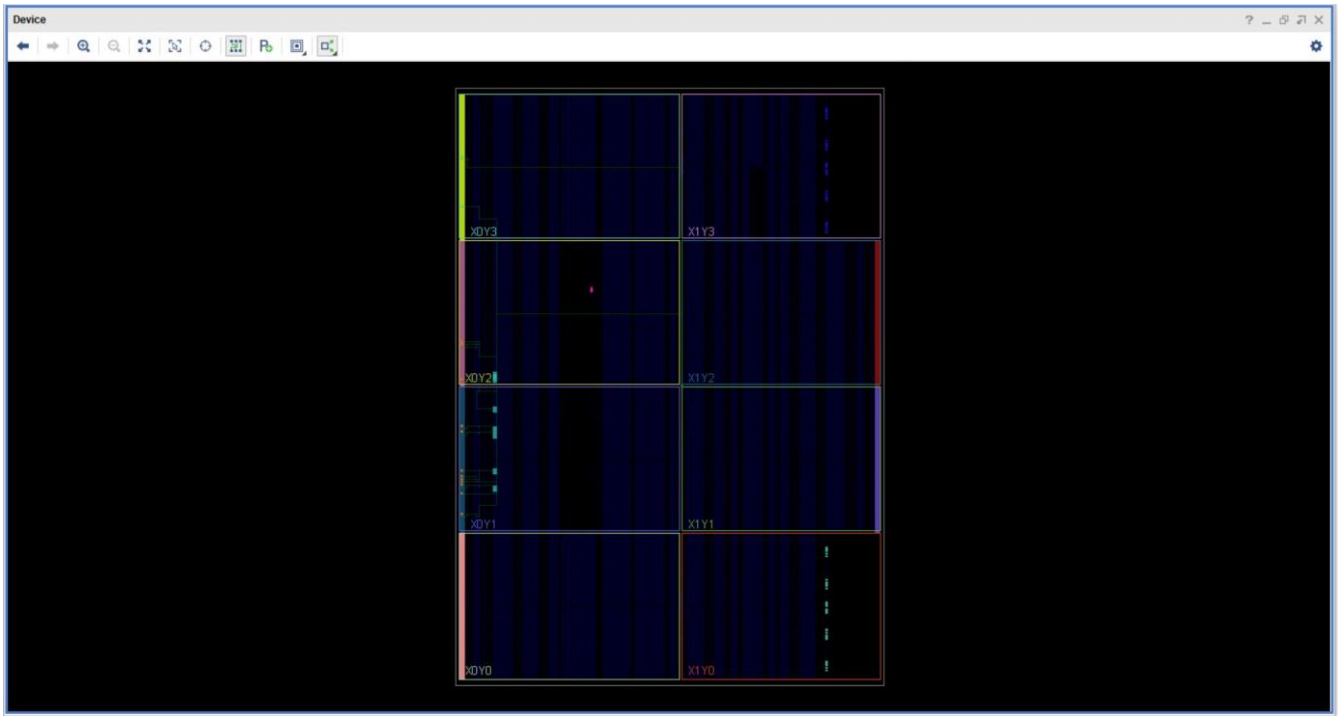
POWER REPORT



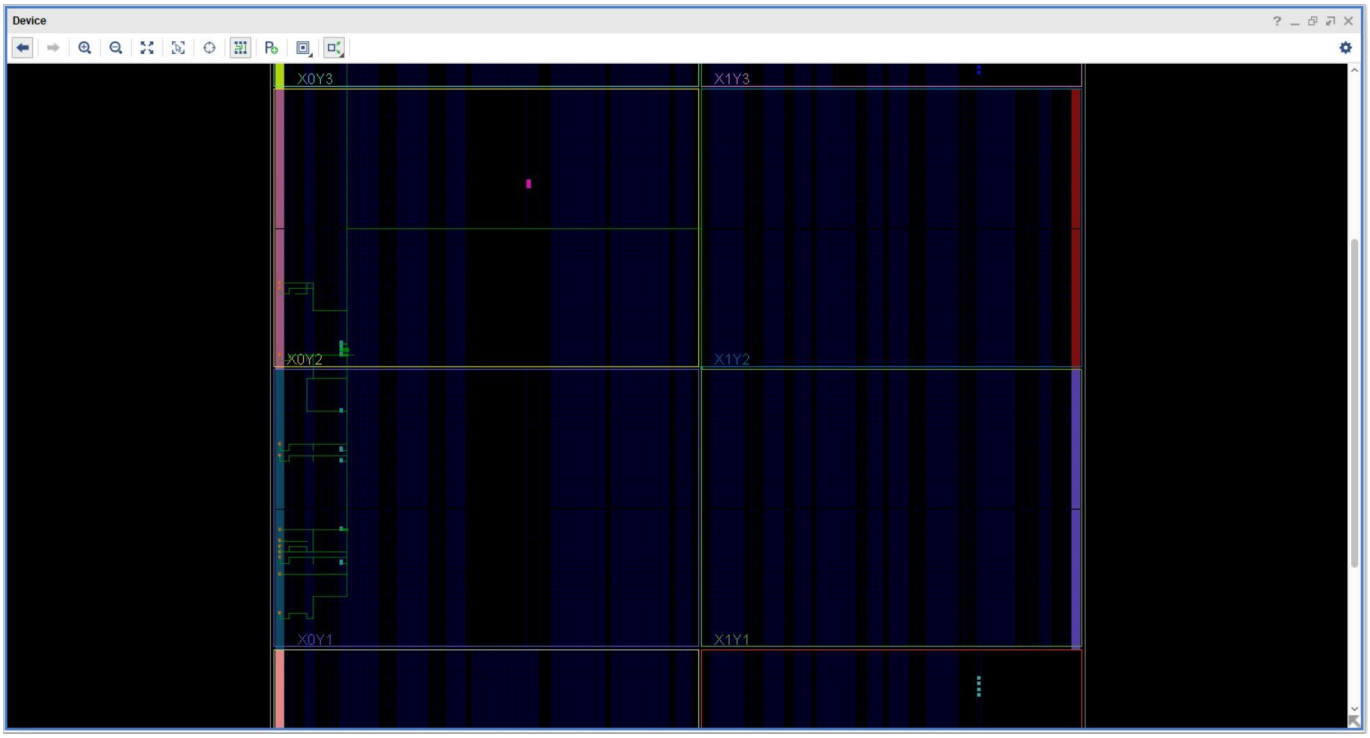
SCHEMATIC AFTER IMPLEMENTATION



DEVICE LAYOUT AFTER IMPLEMENTATION

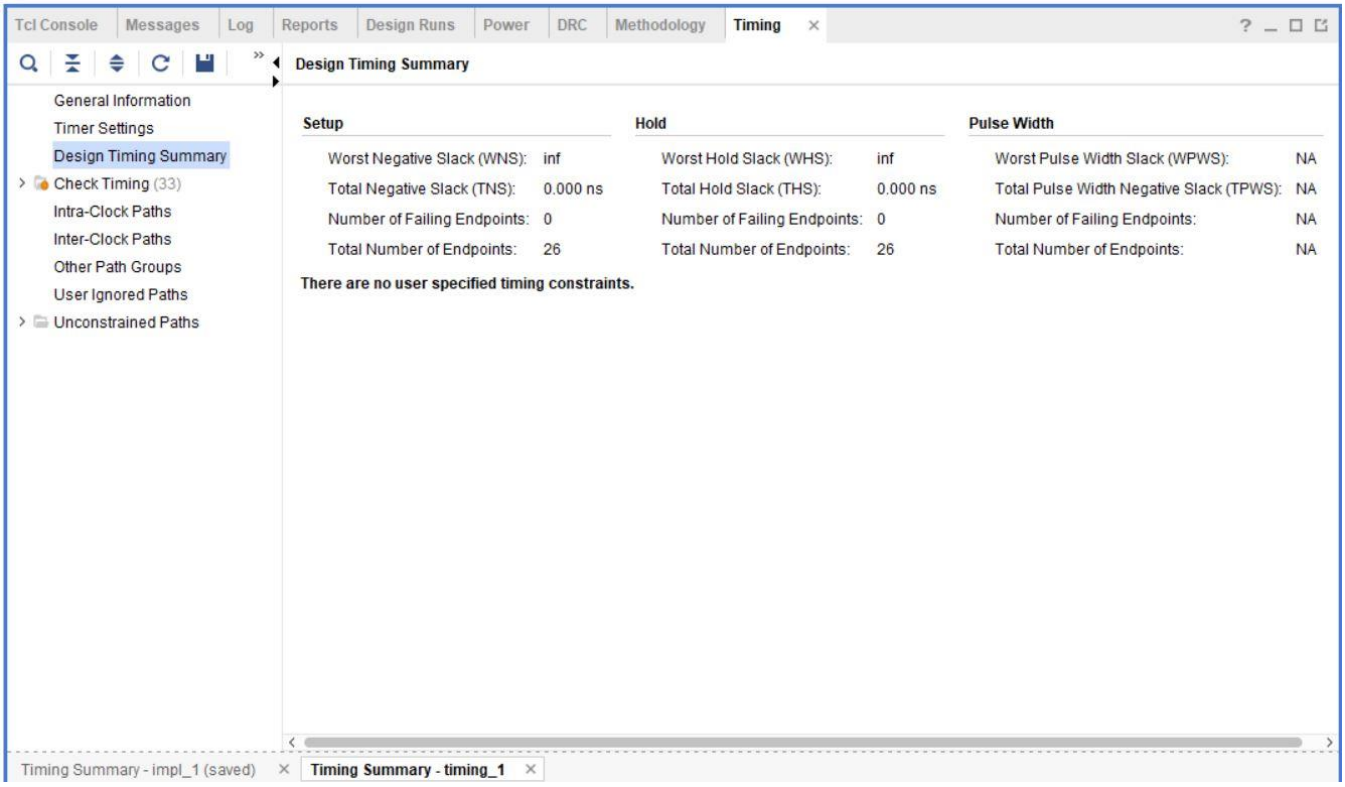


ZOOM IN VIEW

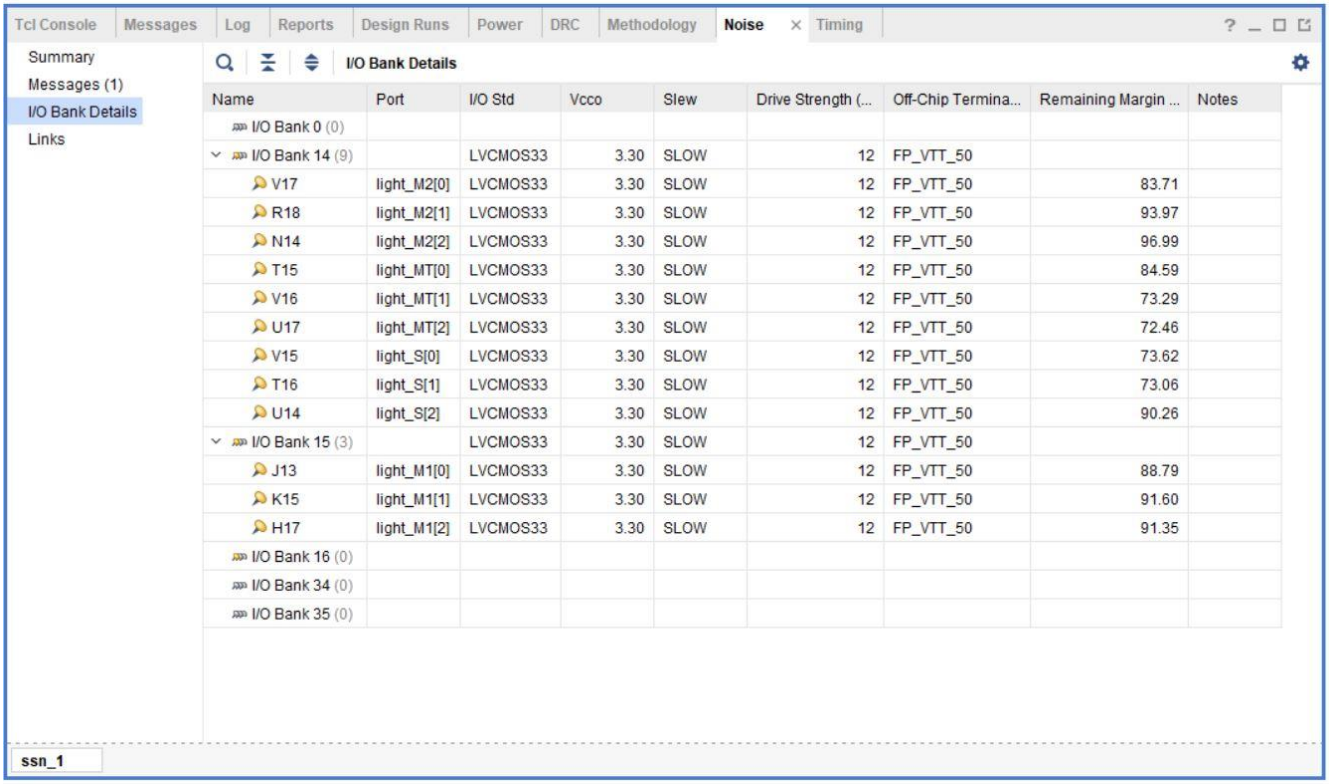


REPORTS AFTER IMPLEMENTATION

TIMING REPORT



NOISE REPORT



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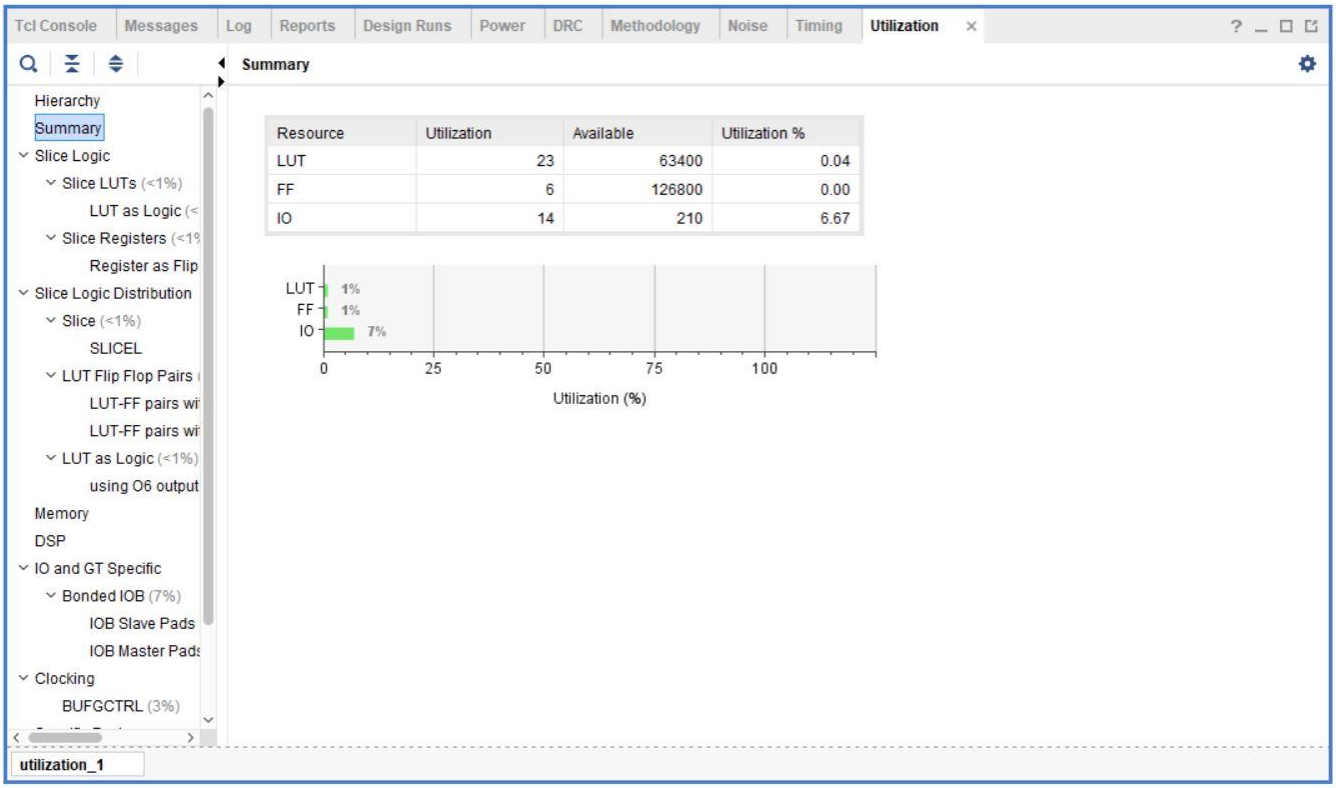
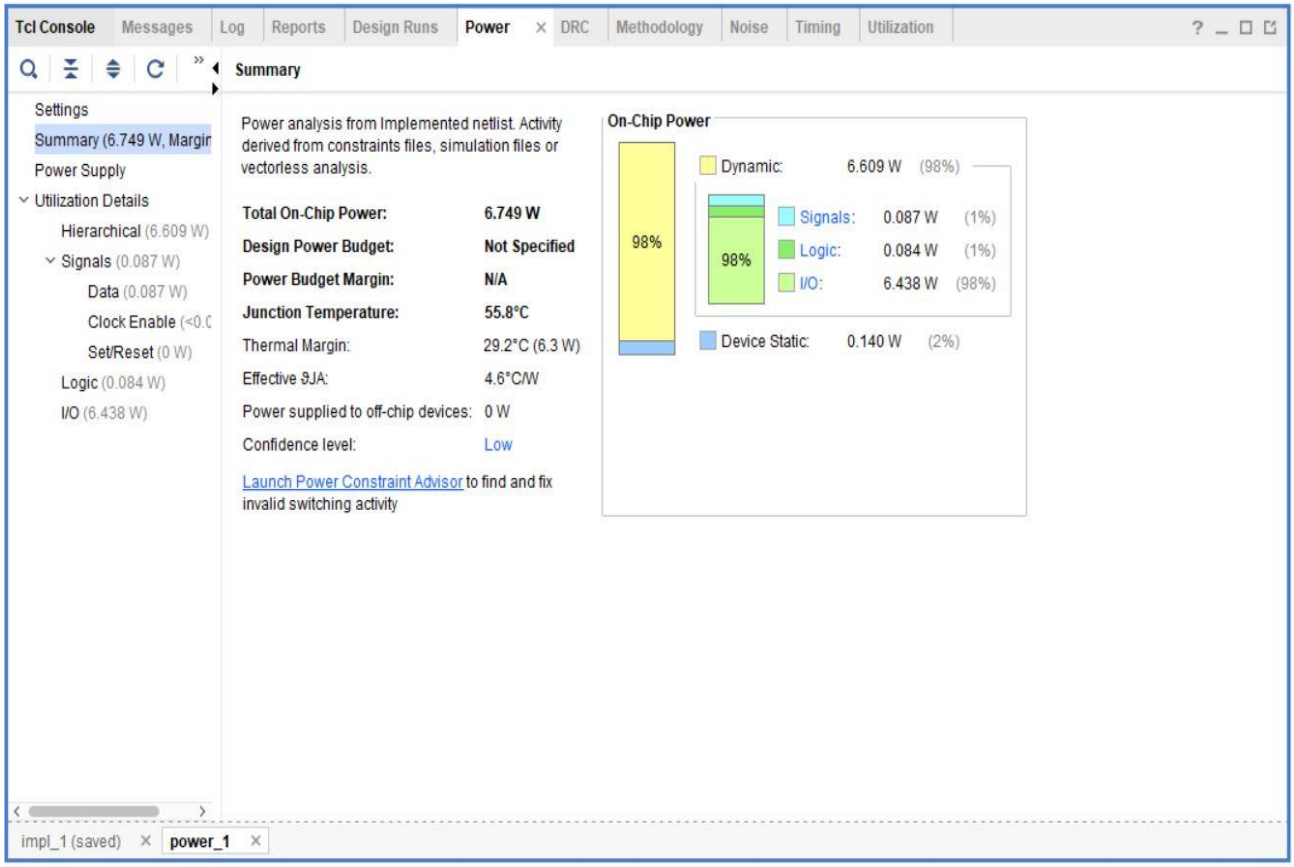
I/O Bank 34 (0)								
I/O Bank 35 (0)								

UTILIZATION REPORT



POWER REPORT



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REFERENCES:

1) Ucf file for io assignment.
2) Nptel lectures on Digital design by prof. Srinivasan
3) Pdf given by Prof. Poonam Kasturi
4) http://www.asic-world.com/tidbits/verilog_fsm.html