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An Interleaved Totem-pole Bridgeless Boost PFC Converter with Soft-Switching Capability Adopting Phase-Shifting Control

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***Abstract*— This paper proposes an interleaved totem-pole bridgeless boost power factor correction (PFC) converter with soft-switching capability. In the proposed converter, an inductor is added compared with the conventional interleaved totem-pole bridgeless boost PFC converter. The added inductor is located between two PFC converter units, and by utilizing the energy of the added inductor, all switches can achieve the zero-voltage-switching (ZVS). In addition, by applying the phase-shifting control between two PFC converter units, the proposed converter can control the magnitude of the current flowing on the added inductor as an optimal value. Therefore, the proposed converter can achieve the ZVS operation, while minimizing the additional conduction loss and core loss of the added inductor. As a result, the proposed converter can achieve the high efficiency. The feasibility of the proposed converter is confirmed with 180-264V_{RMS} input and 1.6 kW (400 V / 4 A) output prototype.**

***Index Terms*— AC/DC power conversion, high switching frequency, interleaved totem-pole boost bridgeless PFC converter, soft switching.**

I. Introduction

HIGH power factor (PF) reduces the current flowing in the commercial or residential building wiring and saves the energy. In addition, low total harmonic distortion causes less interference to other electronic devices. Therefore, power supplies are generally required to meet the power quality standard such as IEC 61000-3-2 [1] and 80 PLUS® certification [2]. To satisfy those requirements, power factor correction (PFC) converter is essential for power supplies to achieve the high power quality [3]-[5].

Fig. 1 illustrates the general structure of the power supply. In this figure, the bridge diode rectifies the full-wave AC input voltage to the half-wave AC voltage. After bridge diode, PFC converter makes high DC voltage. Finally, DC/DC converter provides tightly regulated DC output voltage to the electronic device. In order to relieve the environmental concerns, the high efficiency of the power supply is a great issue. In the general power supply, the considerable conduction loss occurs in the bridge diode, and this loss limits maximum achievable efficiency. To reduce the conduction loss of the bridge diode,

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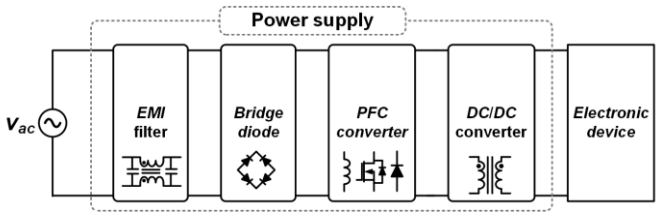

Fig. 1. General structure of the power supply.

there have been a lot of research for the various bridgeless PFC converters [6]–[9].

Among the several types of the bridgeless boost PFC converter, totem-pole bridgeless boost PFC converter is the remarkable topology due to the small number of circuit elements and low common mode noise problem [10]–[17]. In high power applications, the continuous conduction mode (CCM) operation is used generally to reduce the conduction loss and the burden of input filter. However, because of the poor reverse recovery characteristic of the body diode in the switch, totem-pole bridgeless boost PFC converter have been limited to be used with the CCM operation. Nowadays, through the development of the wide-band-gap devices such as Gallium Nitride (GaN) and Silicon Carbide (SiC) switches which have good reverse recovery characteristic of the body diode, more focuses are put on using the totem-pole bridgeless boost PFC converter in various power supply applications [18]-[21]. However, the totem-pole bridgeless boost PFC converter still has large switching loss due to the hard switching of the main switches even with the reduced switching loss by wide-band-gap devices. Meanwhile, in high power applications, the interleaved structure is widely used to relieve a burden on high power and the design of input filter. However, in the interleaved structure, the switching loss is severe due to the increased number of switches, which degrades the efficiency of the PFC converter. Thus, reducing the switching loss can be a considerable issue.

In order to reduce the switching loss, many soft switching techniques have been studied. The zero-voltage-transition techniques are proposed in [22]–[26] for the boost PFC converters. However, it is very complicated to apply above research to the totem-pole bridgeless boost PFC converter, because bidirectional current flow on the boost inductor should be considered in the totem-pole structure. As a result, twice as many components are required, which considerably increase the complexity. In [27], improved totem-pole bridgeless boost PFC converter is proposed. By using a coupled inductor and two additional diodes, the zero-current-switching at the turn-off state is achieved. However, it still shows not only hard switching at turn-on state, but also the large conduction loss in the added diode due to the large circulating current.

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Furthermore, since it is hard to apply former research to the interleaved structure due to the many required circuit elements, a simple approach to reduce the switching loss is required. The soft switching techniques for interleaved totem-pole bridgeless boost PFC converter were proposed in [28] and [29]. In these methods, two boost inductors are combined to form one coupled inductor to reduce the switching loss by using the leakage inductance of the coupled inductor. Although the reverse recovery loss is reduced with low *di*/*dt* rate over entire load condition, it is hard to achieve the ZVS operation under the light load condition.

In [30], the additional inductor is added to the interleaved boost converter. Due to the current on the additional inductor, ZVS can be achieved. The variable frequency method is adopted, and the frequency changes according to the input voltage and the load condition to make the proper magnitude of the current on the additional inductor. However, it is difficult to make the very small current on the additional inductor to prevent large conduction loss under the light load condition. In addition, magnetic component has large volume due to the wide switching frequency range.

To solve the aforementioned problems, the interleaved totem-pole bridgeless boost PFC converter with one additional inductor and phase-shifting control is proposed in this paper. In the proposed converter, only one inductor L_A is added compared to the conventional interleaved totem-pole bridgeless boost PFC converter as shown in Fig. 2. By utilizing the energy stored in L_A, the ZVS turn-on can be achieved over all input voltage range and entire load condition. In addition, by adopting the phase-shifting control, it can adjust the magnitude of the current on L_A. Therefore, the proposed converter can minimize the conduction loss and core loss of L_A, while achieving the ZVS turn-on, which results in high efficiency.

II. Proposed Converter

A. Circuit Configuration

As shown in Fig. 2, two PFC converter units are connected in parallel like the general interleaved structure. Boost inductor L_{B1}, switches Q_{1L}, Q_{1H} comprise the first PFC converter unit, while the components with subscript "2" form the second unit. The additional inductor L_A connects the middle point of each leg in PFC units. The voltage across the additional inductor v_{LA} can have three level V_O, $-V_O$ or zero according to the status of switches. Therefore, the current flowing on the additional inductor i_{LA} is controlled by the magnitude and duration time of v_{LA}. Due to i_{LA}, the proposed converter can achieve the ZVS turn-on of the main switches and reduce the reverse recovery loss.

B. Mode Analysis

Before illustrating the steady-state operation, several assumptions are made as follows:

1) The switches Q_{1L}-Q_{2H} are ideal switches except for their output capacitances and body diodes.
2) The output capacitance C_{oss} of the switches are identical.
3) The diodes D_1 and D_2 are ideal components.
4) The output voltage V_O is constant.
5) The AC input voltage V_{ac} is constant during one switching period.

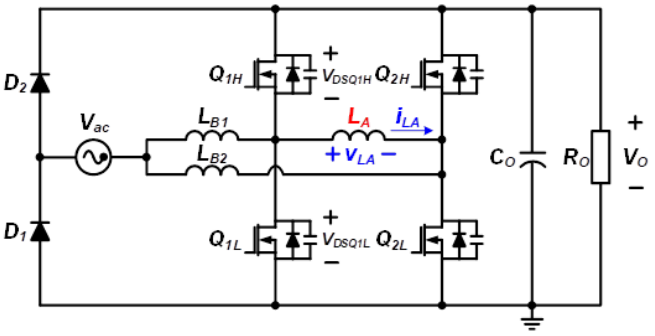

Fig. 2. Circuit diagram of the proposed converter.

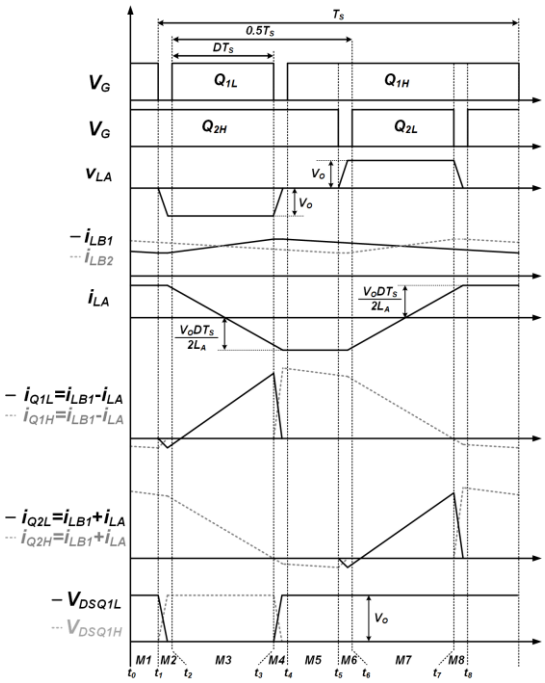

Fig. 3. Key waveforms.

Because of the symmetric structure and operation of the proposed converter, only the operation process of the positive half-line cycle is explained. There are eight modes in positive half-line cycle, and key waveforms are illustrated in Fig. 3. Mode 1-4 are for the ZVS process of Q_{1L} in first PFC unit and mode 5-8 are for that of Q_{2L} in second PFC unit. In this paper, due to the similarity, only mode 1-4 are explained, and their equivalent circuits are illustrated in Fig. 4.

Mode 1 [t_0-t_1] : Q_{1H} and Q_{2H} are ON state. Therefore, both PFC units transfer power to the output load. Currents on L_{B1} (i_{LB1}), L_{B2} (i_{LB2}), and L_A (i_{LA}) are as follows:

$$i_{LB1}(t) = i_{LB1}(t_0) + \frac{V_{ac} - V_O}{L_{B1}}(t - t_0), \tag{1}$$

$$i_{LB2}(t) = i_{LB2}(t_0) + \frac{V_{ac} - V_O}{L_{B2}}(t - t_0), \tag{2}$$

$$i_{LA}(t) = i_{LA}(t_0). \tag{3}$$

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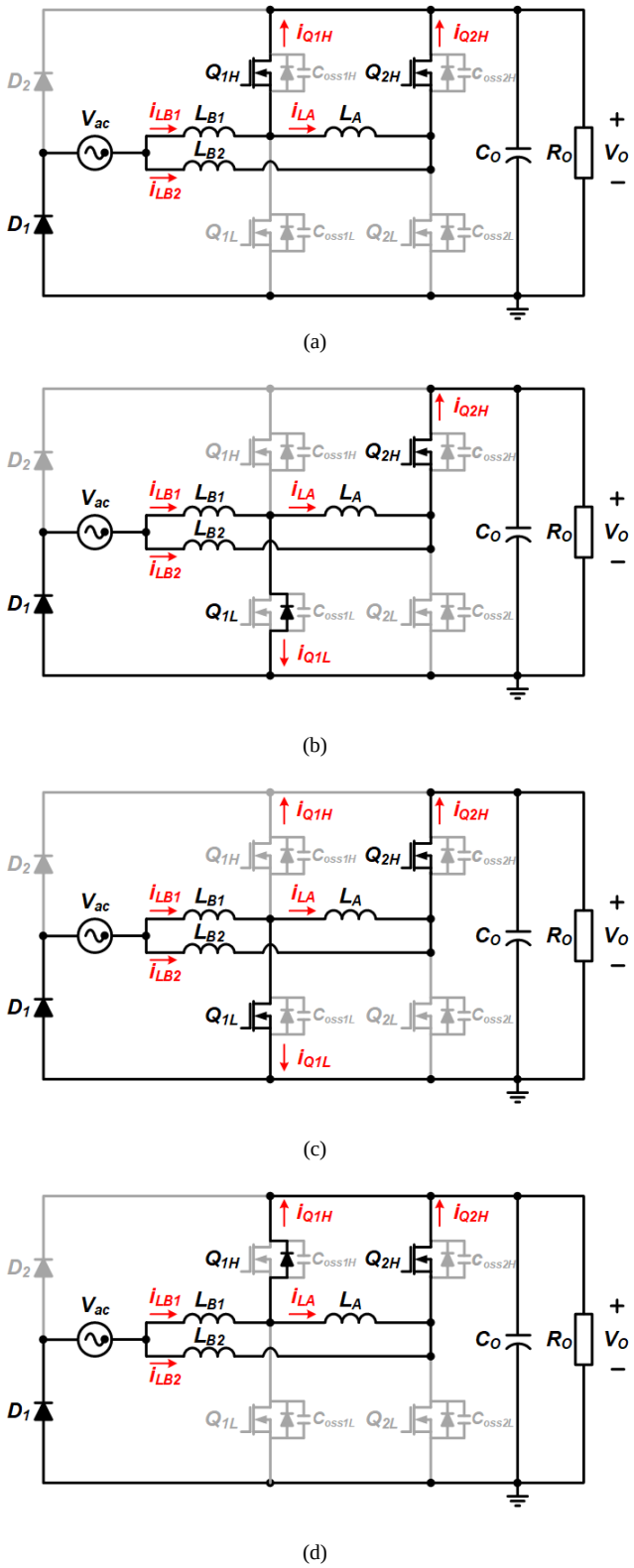

Fig. 4. Equivalent circuits. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

i_{LB1} and i_{LB2} decrease while i_{LA} is maintained because the both nodes of L_A is connected to V_O. As illustrated in Fig. 4(a), i_{Q1H} is i_{LB1}-i_{LA} and i_{Q2H} is i_{LB2}+i_{LA}. Therefore, i_{Q1H} at t_1 has smaller value compared to the case without L_A. This phenomenon reduces the reverse recovery problem of the body diode.

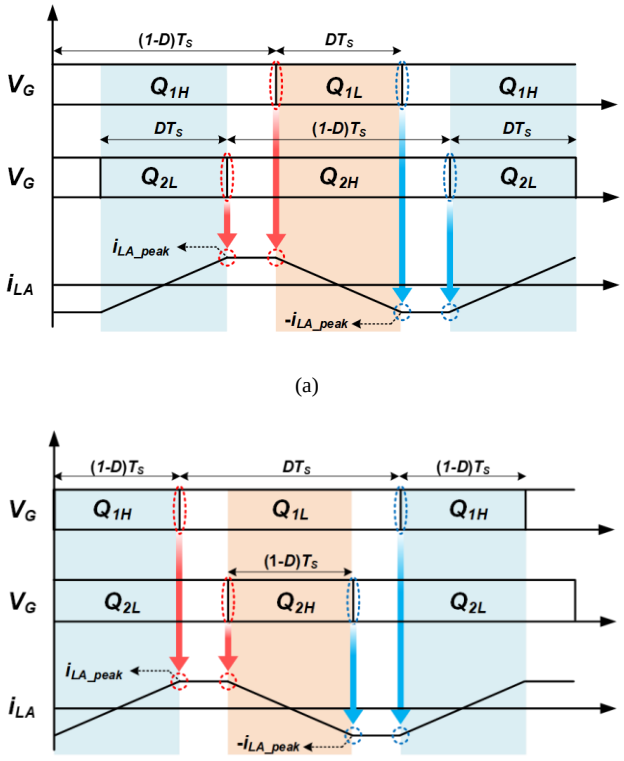

Fig. 5. Gate signals and i_{LA}. (a) Case of $D \leq 0.5$. (b) Case of $D > 0.5$

Mode 2 [t_1-t_2] : Because i_{LA} has larger value than i_{LB1}, negative current flows through Q_{1L}. The negative current discharges C_{oss1L}, and the voltage on Q_{1L} reaches zero. After C_{oss1L} is totally discharged, the body diode of Q_{1L} is conducted.

Mode 3 [t_2-t_3] : Q_{1L} is turned on with the ZVS because the voltage on C_{oss1L} already reaches to zero at t_2. i_{LB1} increases and i_{LB2} still decreases with following expressions :

$$i_{LB1}(t) = i_{LB1}(t_2) + \frac{V_{ac}}{L_{B1}}(t - t_2), \tag{4}$$

$$i_{LB2}(t) = i_{LB2}(t_2) + \frac{V_{ac} - V_O}{L_{B2}}(t - t_2), \tag{5}$$

$$i_{LA}(t) = i_{LA}(t_2) - \frac{V_O}{L_A}(t - t_2). \tag{6}$$

Since $-V_O$ is applied to L_A, Therefore, i_{LA} decreases steeply with large voltage and small inductance of L_A.

Mode 4 [t_3-t_4] : After C_{oss1H} is totally discharged, the body diode of Q_{1H} is conducted. Both PFC converter units transfer power to the output load. i_{LA} decreases until the conduction of Q_{1H} ends. The magnitude of i_{LA} at the turn-off state of Q_{1H} is approximately $-0.5V_ODT_S/L_A$. Since then, i_{LA} is maintained during rest time of mode 4. The expressions if i_{LB1} and i_{LB2} are as follows :

$$i_{LB1}(t) = i_{LB1}(t_3) + \frac{V_{ac} - V_O}{L_{B1}}(t - t_3), \tag{7}$$

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$$i_{LB2}(t) = i_{LB2}(t_3) + \frac{V_{ac} - V_O}{L_{B2}}(t - t_3). \quad (8)$$

Because of the varying duty cycle D according to the input voltage and load condition of the PFC converter, the intended operation must be ensured with all D. In the proposed converter, the ZVS turn-on is achieved with all D, and the case with D less than 0.5 is explained in the mode analysis.

The positive peak value of i_{LA} is helpful for the ZVS turn-on of Q_{1L} and Q_{2H}. In contrary, the negative peak value of i_{LA} is helpful for the ZVS turn-on of Q_{1H} and Q_{2L}. When D is larger than 0.5, i_{LA} increases or decreases during $(1\text{-}D)T_S$. As shown in Fig. 5, positive peak value of i_{LA} is shown before Q_{1L} or Q_{2H} are turned on with D larger than 0.5. Similarly, the negative peak value of i_{LA} is shown before Q_{1H} and Q_{2L} are turned on. Therefore, the proposed converter can make i_{LA} that helps the ZVS turn-on with all D.

III. Phase Shifting Control of Proposed Converter

A. Analysis of Current on L_A (i_{LA})

The operation mode (discontinuous conduction mode (DCM) or CCM) is determined according to the input voltage and the load condition. As the input current increases, the CCM region becomes more dominant in the half-line cycle. And i_{LA} takes a roll in achieving the ZVS in the CCM operation. Therefore, for the simple analysis about the effect of i_{LA} and the ZVS condition, all CCM operation is assumed as a heavy load condition. And then, the consideration for the DCM operation will be mentioned.

The CCM duty ratio D_{CCM} is illustrated in Fig. 6, and it is designed at 230 V_{RMS} input voltage and 400 V output voltage. The expression is as follows:

$$D_{CCM}(t) = 1 - \frac{v_{ac}(t)}{V_O} = 1 - \frac{\sqrt{2}V_{RMS}\sin(2\pi f_L t)}{V_O}. \quad (9)$$

As mentioned in part II, the peak value of i_{LA}, i_{LA_peak}, is proportional to D_{CCM} or 1-D_{CCM} according to the magnitude of D. It can be seen that i_{LA_peak} is proportional to -|D_{CCM}-0.5|+0.5. It is illustrated in Fig. 6 and is depicted without absolute value symbol as follows:

$$-\left|D_{CCM} - 0.5\right| + 0.5 = \begin{cases} D_{CCM} & \text{for} \quad D_{CCM} < 0.5 \\ 1 - D_{CCM} & \text{for} \quad D_{CCM} \geq 0.5 \end{cases}. \quad (10)$$

In order to achieve the ZVS turn-on of the switches, i_{LA_peak} should be larger than i_{LB1} and i_{LB2} right before the switches being turned on. The minimum magnitude of i_{LA_peak} that can achieve the ZVS turn-on is denominated as i_{req}. i_{req}-i_{LB1} should charge and discharge the output capacitor of switches during the dead time. Therefore, (11) and (12) should be satisfied.

$$\begin{aligned} i_{req} &= i_{LB1} + \frac{2C_{OSS}}{t_d} \\ &= \sqrt{2}I_{RMS}\sin(2\pi f_L t) - \frac{\sqrt{2}V_{RMS}\sin(2\pi f_L t)}{2L_{B1}}DT_S + \frac{2C_{OSS}}{t_d} \end{aligned} \quad (11)$$

$$i_{LA\_peak} > i_{req}, \quad (12)$$

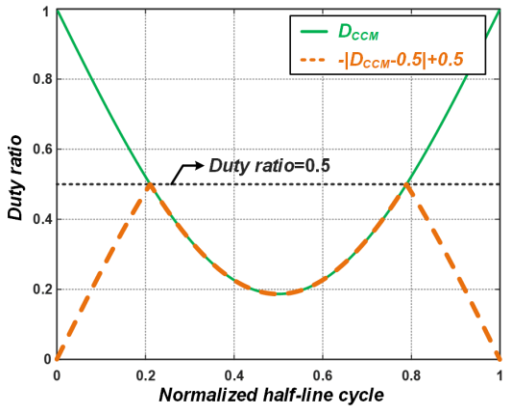
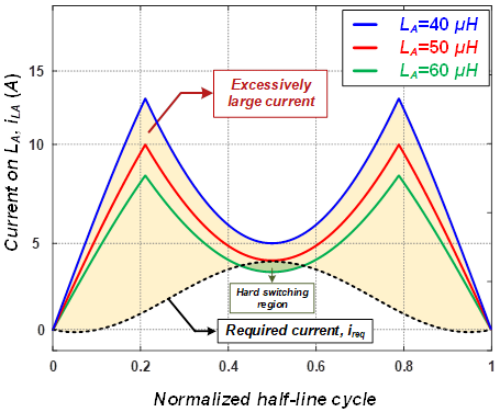


Fig. 6. D_{CCM} and -|D_{CCM}-0.5|+0.5 over half-line cycle at 230 V_{RMS} condition.



(b)

Fig. 7. i_{LA_peak} and i_{req} over half-line cycle at 230 V_{RMS} and full load condition.

where I_{RMS}, C_{OSS} and t_d are RMS input current, output capacitor of switch and dead time respectively.

With proper design of L_A, i_{LA_peak} can be larger than i_{req} at all switching cycles as illustrated in Fig. 7. If L_A is large, the ZVS turn-on cannot be achieved in certain region where i_{LA} is smaller than i_{req}. However, if L_A is too small, i_{LA} has very large magnitude that causes large additional conduction loss on switches.

When $v_{ac}(t)$ has the peak value, D_{CCM} has minimum value and i_{req} has maximum value as shown in Fig. 6. Therefore, to ensure the ZVS operation under the entire load range, L_A should be designed to cover maximum i_{req} with minimum D_{CCM}. The available range of L_A is as follows:

$$L_A < \frac{V_O D_{CCM\_min} T_S}{2 i_{req\_max}}. \quad (13)$$

where D_{CCM_min} is the minimum value of D_{CCM} and i_{req_max} is the maximum value of i_{req}. As shown in Fig. 7, if L_A is designed to achieve the ZVS turn-on over all half-line cycle, i_{LA_peak} is excessively larger than i_{LA_req} except for the middle point. This excessively large current causes additional conduction loss and core loss of L_A. Therefore, to achieve high efficiency this current should be minimized while achieving the ZVS turn-on.

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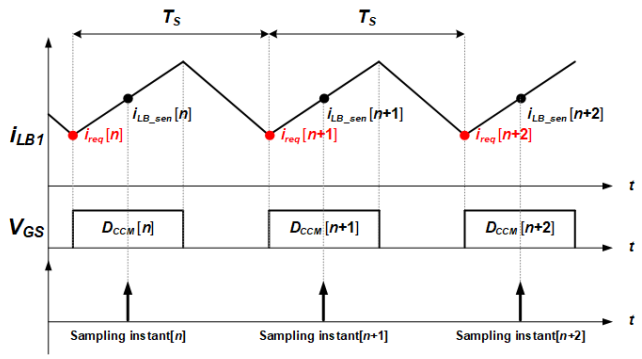


Fig. 8. Sensing process of the proposed converter.

B. Phase-shifting Control Scheme

Aforementioned before in the mode analysis, i_{LA} changes during the overlapping time of the low side switch and the high side switch. By decreasing overlapping time, i_{LA_peak} can be decreased. The maximum overlapping time is shown when the phase difference between two PFC converter units is 180 degrees. By applying phase-shifting control, phase difference and the overlapping time can be controlled.

With proper phase difference, not only the ZVS turn-on is achieved, but also the conduction loss of switches and L_A, and the core loss of L_A can be minimized. Ideally, i_{LA_peak} can be same with i_{req} by reducing i_{LA}. To calculate the required phase difference, the information of v_{ac}, V_O, i_{LB1} and i_{LB2} is required. However, since this required information is already sensed in the conventional PFC converter with the CCM operation, the phase-shifting control can be accomplished without any additional sensing or components.

Fig. 8 illustrates sensing process at n^{th} switching cycle in the CCM operation. i_{LB} is sensed at the center of the switch on-time by micro controller unit (MCU) to minimize the noise which emerges at switching state. Therefore, the sensed value of i_{LB} at n^{th} switching cycle $i_{LB\_sen}[n]$ is the median value of i_{LB}. Also, the duty ratio in the CCM operation at n^{th} switching cycle $D_{CCM}[n]$ is calculated by DSP. The required value of i_{LA} for the ZVS operation at n^{th} switching cycle $i_{req}[n]$ is as follows:

$$i_{req}[n] = i_{LB\_sen}[n] - \frac{v_{ac}[n] D_{CCM}[n] T_S}{2L_B}, \quad (14)$$

where $v_{ac}[n]$ is sensed input voltage at nth switching cycle.

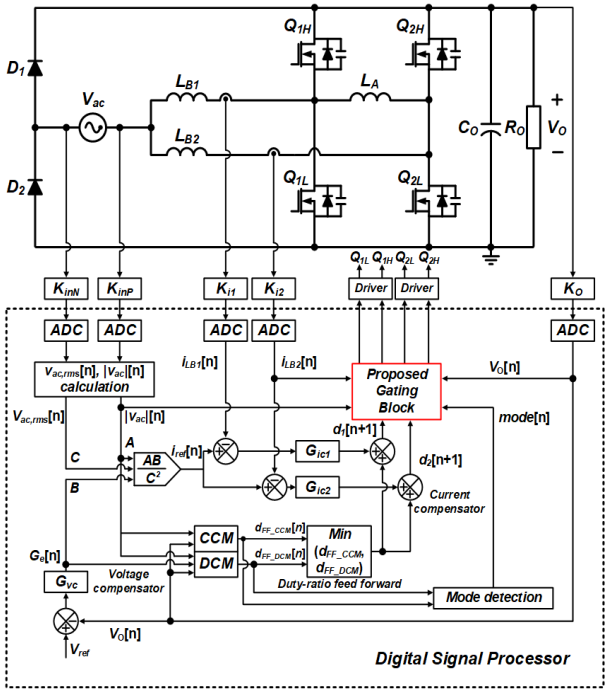
With phase difference at n^{th} switching cycle $\phi[n]$, i_{LA_peak} at n^{th} switching cycle $i_{LA\_peak}[n]$ is as follows:

$$i_{LA\_peak}[n] = \frac{V_O[n]\phi[n]T_S}{2L_A}. \quad (15)$$

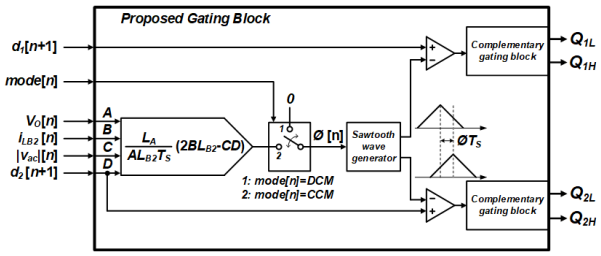
To satisfy the ZVS condition, $i_{LA\_peak}[n]$ should be larger than $i_{req}[n]$. From (7) and (8), $\phi[n]$ is expressed as follows:

$$\phi[n] > \frac{2L_A}{V_O[n]T_S}\left(i_{LB\_sen}[n] - \frac{v_{ac}[n] D_{CCM}[n] T_S}{2L_B}\right). \quad (16)$$

$\phi[n]$ has a value between 0 and 1. Therefore, $\phi[n]T_S$ is actual time difference between two PFC converter units. By applying calculated $\phi[n]$, the ZVS turn-on is achieved in all CCM operation regions with minimum additional losses. In DCM operation region, switching loss is small because i_{LB} starts at zero. Therefore, $\phi[n]$ is set to zero in the DCM region after distinguishing the operation mode.



(a)



(b)

Fig. 9. Control block diagrams of the proposed converter. (a) Entire PFC converter and control block diagram. (b) Detail block diagram of the proposed gating block.

Fig. 9(a) is control block diagram of the proposed converter. Overall process of control is same with conventional converter. Only the proposed gating block is added without using additional analog components. i_{L1} has constant phase and the phase of i_{L2} changes at every switching period. $d_1[n]$ and $d_2[n]$ are the outputs of each current compensator at n^{th} switching cycle.

Fig. 9 (b) illustrates the inner structure of the proposed gating block. First, after checking the operation mode, the parameter $mode[n]$ is set to 1 or 2. $\phi[n]$ is set to zero if the PFC converter is with the DCM operation. If the PFC converter is in the CCM operation, calculated $\phi[n]$ is applied to the saw-tooth wave generator. Two saw-tooth waves with different phase are generated and final gating signals are made with the output of current compensators $d_1[n+1]$ and $d_2[n+1]$.

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TABLE I
DESIGNED PARMETERS

Line voltage (Nominal voltage) / line frequency	180-264 V_{RMS} (Nominal : 230 V_{RMS}) / 50 Hz	
Output voltage and power	400 V, 1600 W	
Switching frequency	200 kHz	
Components	**Design results**	
	Conventional	**Proposed**
Switch(Q_{1L},Q_{1H}, Q_{2L},Q_{2H})	GS66508T (V_{DS_MAX} : 650 V, R_{DS_ON} : 60 mΩ, C_{OSS_ER} : 88 pF)	
Diode (D_1, D_2)	TS50P07G (V_{MAX} : 1000 V, I_{MAX} : 50 A, V_F : 1.1 V)	
Boost inductor (L_{B1}, L_{B2})	122 μH (PQ3230, Ae : 161 mm^2, Aw : 149.6 mm^2)	
Additional inductor (L_A)	-	50 μH (PQI35/30, Ae : 196 mm^2, Aw : 110.3 mm^2)
Output capacitor (C_O)	820 μF (Rubycon MXK series *1EA, V_{MAX} : 450 V)	
Digital signal processor	TMS320F28377S	

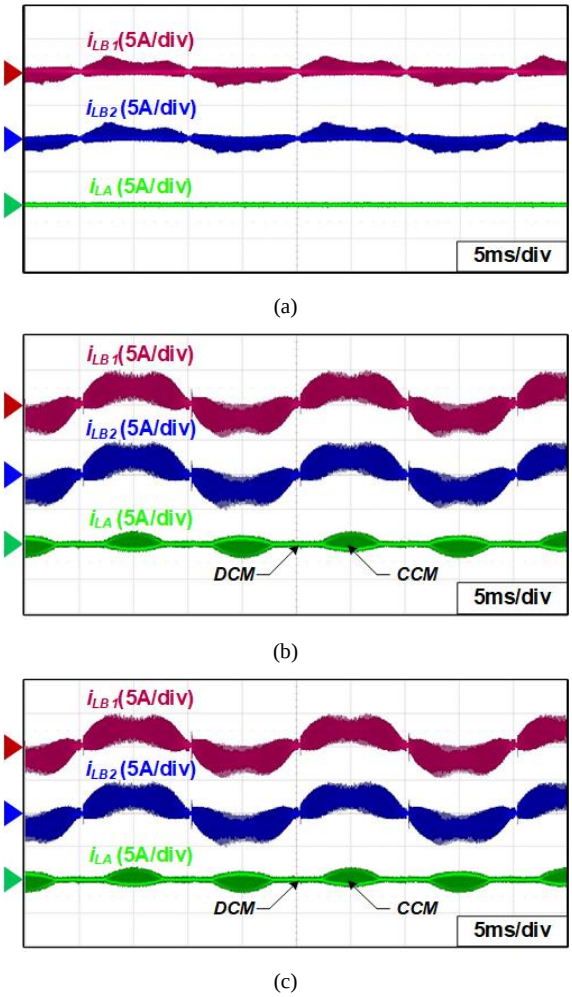

Fig. 10. Experimental waveforms of the proposed converter at 230 V_{RMS}. (a) 10% load condition. (b) 50% load condition. (c) 100% load condition.

IV. EXPERIMENTAL RESULTS

The proposed converter is verified with 230 V_{RMS} input voltage and 400 V/1.6 kW output specification. The proposed converter is designed with general design guideline of the interleaved totem-pole bridgeless boost PFC converter considering the boost inductor current ripple. To confirm only the effect of L_A, the other elements are designed identically. Therefore, only L_A is added to the conventional interleaved totem-pole bridgeless boost PFC converter design. The specification and circuit components are listed in Table I.

As illustrated in Fig. 10(a), i_{LA} is zero because two PFC converter units operates with same phase in the DCM operation. In Fig. 10(b), both DCM and CCM operation are shown, and i_{LA} flows only in the CCM region depending on the boost inductor current. In Fig. 10(c), i_{LA} flows over the entire line cycle due to the belonging the CCM region. The phase difference is controlled according to the boost inductor current and appropriate magnitude of i_{LA} for the ZVS is generated. Thus, the ZVS turn-on is achieved over entire input voltage condition and load condition. In addition, the DC offset current is not shown under the DCM region. When the operation mode enters to DCM from CCM, the voltage on the output capacitor of the switches are adjusted in the direction of eliminating i_{LA}. Since the tiem-delay values of the applied devices are very small, there is little effect on the duty ratio mismatch between two PFC converter unis. Therefore, DC offset current does not occur.

The measured efficiency is illustrated in Fig. 11. The proposed converter showed similar efficiency with the conventional converter under the light load condition where the DCM operation is dominant, because there is no current on L_A due to the zero phase difference between two PFC converter units. Therefore, the proposed converter operates similarly with the conventional converter. As the load condition increases, the proposed converter showed higher efficiency than conventional converter due to the reduced switching loss in the CCM region. Near the full load condition, large i_{LA} flows through the switches and L_A, resulting in large conduction losses and core loss of L_A. Therefore, the efficiency gap between the proposed and conventional converters is decreased. However, the proposed converter still shows higher efficiency than the conventional converter due to the reduced switching loss.

Fig. 12 illustrates the measured power factor (PF) and total harmonic distortion (THD). Due to the phase-shifting control, proposed converter has large input current ripple. Because the EMI filter and boost inductor are maintained for the proposed converter, PF and THD show a bit degradation by large ripple under the heavy load condition as illustrated in Fig. 13. However, the proposed converter shows high PF that is larger than 0.99 and harmonic components satisfies international standard IEC EN61000-3-2 [1] as illustrated in Fig. 14.

In addition, because the proposed converter has small switching loss by achieving the ZVS, larger boost inductance can be used. If the larger boost inductance is used, the input current ripple can be reduced and the performances of PF and THD can be improved.

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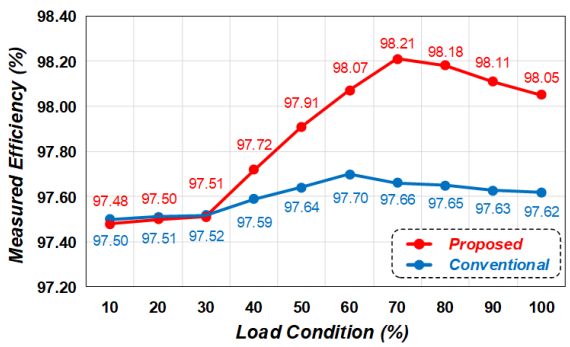
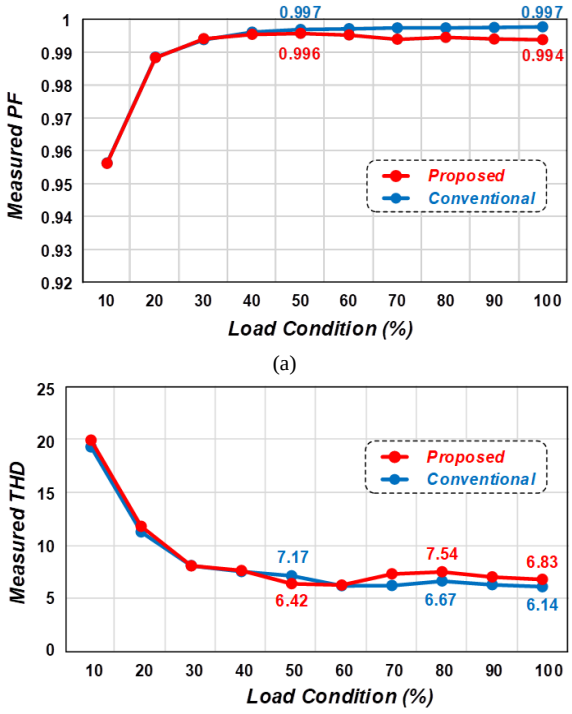


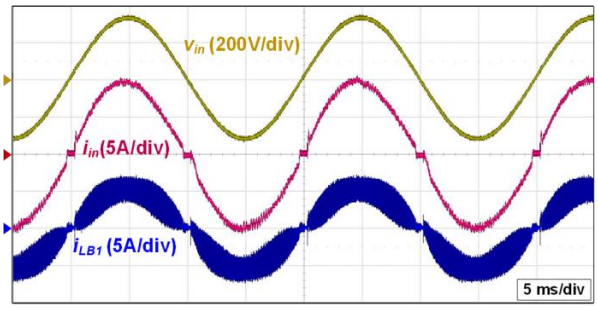
Fig. 11. Measured efficiency at 230 V_{RMS}.



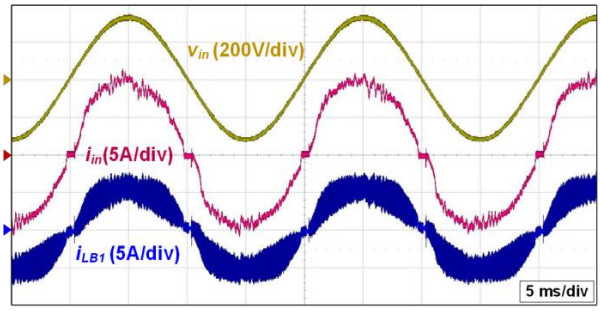
(a)

(b)

Fig. 12. Measured power quality at 230 V_{RMS}. (a) PF. (b) THD.



(a)



(b)

Fig. 13. Experimental waveforms of input current and boost inductor current at 230 V_{RMS} and 100% load condition. (a) Conventional converter. (b) Proposed converter.

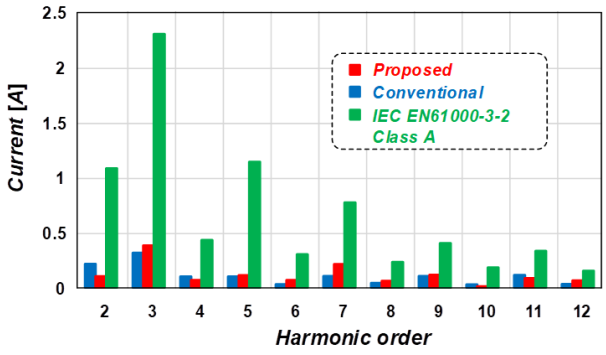


Fig. 14. Measured magnitude of the harmonic components at 230 V_{RMS} and 100% load condition.

V. Conclusion

In this paper, an interleaved totem-pole bridgeless boost PFC converter with soft-switching capability is proposed. All switches can achieve the ZVS turn-on with one additional inductor. Also, by applying the phase-shifting control, appropriate energy is generated in the added inductor that minimizes the additional loss without additional components. As a result, the proposed converter achieves higher efficiency than the conventional converter. Consequently, the proposed PFC converter is expected to be widely used for high power application such as on-board-charger and server power supply in high switching frequency.

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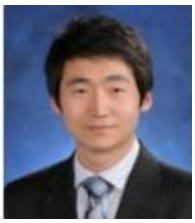

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