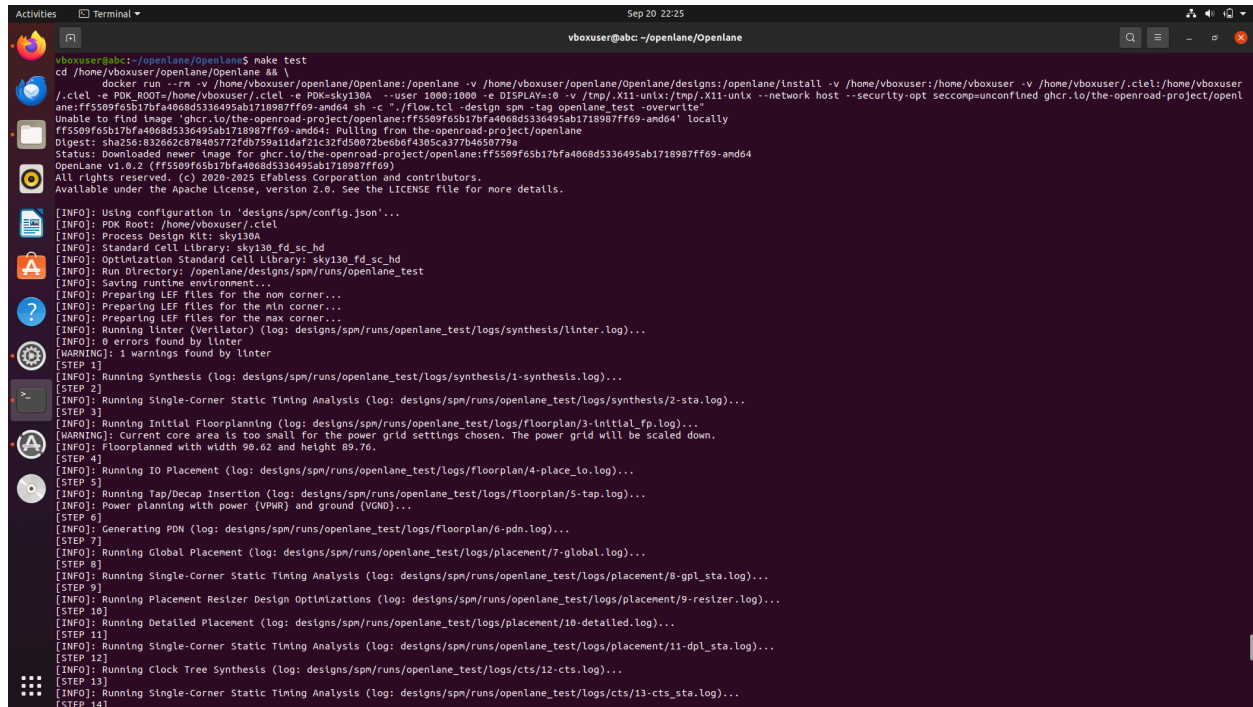


# Week 0 : Task 1

## Arjun Anand Mallya

The steps were followed and the tools have been installed. Below are the screenshots of the test in openlane and the versions of all the tools on the Virtual machine.



```
vboxuser@abc: ~/openlane/OpenLane
$ make test
cd /home/vboxuser/openlane/OpenLane && \
  docker run --rm -v /home/vboxuser/openlane/OpenLane:/openlane -v /home/vboxuser/openlane/designs:/openlane/install -v /home/vboxuser:/home/vboxuser -v /home/vboxuser/.cicel:/home/vboxuser/.cicel -e PDK_ROOT=/home/vboxuser/.cicel -e PDK=sky130a --user 1000:1000 -e DISPLAY=:0 -v /tmp/.X11-unix:/tmp/.X11-unix --network host --security-opt seccomp=unconfined ghcr.io/the-openroad-project/openlane:ff5509f65b17bfa4068d5336495ab1718987ff69-and64 sh -c ". /flow.tcl -design spn -tag openlane_test -overwrite"
Unable to find image 'ghcr.io/the-openroad-project/openlane:ff5509f65b17bfa4068d5336495ab1718987ff69-and64' locally
ff5509f65b17bfa4068d5336495ab1718987ff69-and64: Pulling from the-openroad-project/openlane
Digest: sha256:832602c878485772fdb759a11da721c32fd50072be0b0f4905ca377b4680779a
Status: Downloaded newer image for ghcr.io/the-openroad-project/openlane:ff5509f65b17bfa4068d5336495ab1718987ff69-and64
OpenLane v1.0.2 (ff5509f65b17bfa4068d5336495ab1718987ff69)
All rights reserved. (c) 2020-2025 Efabless Corporation and contributors.
Available under the Apache License, version 2.0. See the LICENSE file for more details.

[INFO]: Using configuration in 'designs/spn/config.json'...
[INFO]: PDK Root: /home/vboxuser/.cicel
[INFO]: Process Design Ktt: sky130a
[INFO]: Standard cell library: sky130_fd_sc_hd
[INFO]: Optimization Standard cell library: sky130_fd_sc_hd
[INFO]: Run Directory: /openlane/designs/spn/runs/openlane_test
[INFO]: Saving runtime environment...
[INFO]: Preparing LEF files for the nom corner...
[INFO]: Preparing LEF files for the min corner...
[INFO]: Preparing LEF files for the max corner...
[INFO]: Running linter (Verilator) (log: designs/spn/runs/openlane_test/logs/synthesis/linter.log)...
[INFO]: 0 errors found by linter
[WARNING]: 1 warnings found by linter
[STEP 1]
[INFO]: Running Synthesis (log: designs/spn/runs/openlane_test/logs/synthesis/1-synthesis.log)...
[STEP 2]
[INFO]: Running Single-Corner Static Timing Analysis (log: designs/spn/runs/openlane_test/logs/synthesis/2-sta.log)...
[STEP 3]
[INFO]: Running Initial Floorplanning (log: designs/spn/runs/openlane_test/logs/floorplan/3-initial_fp.log)...
[WARNING]: Current core area is too small for the power grid settings chosen. The power grid will be scaled down.
[INFO]: Floorplanned with width 90.62 and height 89.76.
[STEP 4]
[INFO]: Running IO Placement (log: designs/spn/runs/openlane_test/logs/floorplan/4-place_io.log)...
[STEP 5]
[INFO]: Running Tap/Decap Insertion (log: designs/spn/runs/openlane_test/logs/floorplan/5-tap.log)...
[INFO]: Power planning with power (VPWR) and ground (VGND)...
[STEP 6]
[INFO]: Generating PDN (log: designs/spn/runs/openlane_test/logs/floorplan/6-pdn.log)...
[STEP 7]
[INFO]: Running Global Placement (log: designs/spn/runs/openlane_test/logs/placement/7-global.log)...
[STEP 8]
[INFO]: Running Single-Corner Static Timing Analysis (log: designs/spn/runs/openlane_test/logs/placement/8-gpl_sta.log)...
[STEP 9]
[INFO]: Running Placement Resizer Design Optimizations (log: designs/spn/runs/openlane_test/logs/placement/9-resizer.log)...
[STEP 10]
[INFO]: Running Detailed Placement (log: designs/spn/runs/openlane_test/logs/placement/10-detailed.log)...
[STEP 11]
[INFO]: Running Single-Corner Static Timing Analysis (log: designs/spn/runs/openlane_test/logs/placement/11-dpl_sta.log)...
[STEP 12]
[INFO]: Running Clock Tree Synthesis (log: designs/spn/runs/openlane_test/logs/cts/12-cts.log)...
[STEP 13]
[INFO]: Running Single-Corner Static Timing Analysis (log: designs/spn/runs/openlane_test/logs/cts/13-cts_sta.log)...
[STEP 14]
```

```
Activities Terminal Sep 20 22:13
vboxuser@abc: ~/openlane/Openlane

final'...
[INFO]: Saving runtime environment...
[INFO]: Generating final set of reports...
[INFO]: Created manufacturability report at 'designs/spm/runs/openlane_test/reports/manufacturability.rpt'.
[INFO]: Created metrics report at 'designs/spm/runs/openlane_test/reports/metrics.csv'.
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/spm/runs/openlane_test/reports/signoff/31-rcx_sta.checks.rpt'.
[INFO]: There are no hold violations in the design at the typical corner.
[INFO]: There are no setup violations in the design at the typical corner.
[SUCCESS]: Flow complete.
[INFO]: Note that the following warnings have been generated:
[WARNING]: 1 warnings found by linter
[WARNING]: Current core area is too small for the power grid settings chosen. The power grid will be scaled down.
[WARNING]: Module sky130_fd_sc_hd__tapvprvrgnd_1 blackboxed during sta
[WARNING]: Module sky130_ef_sc_hd__decap_12 blackboxed during sta
[WARNING]: Module sky130_fd_sc_hd__fill_1 blackboxed during sta
[WARNING]: Module sky130_fd_sc_hd__fill_2 blackboxed during sta
[WARNING]: VSRC_LOC_FILES is not defined. The IR drop analysis will run, but the values may be inaccurate.
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/spm/runs/openlane_test/reports/signoff/31-rcx_sta.checks.rpt'.

Basic test passed
vboxuser@abc:~/openlane/Openlane$
```

```
Activities Terminal Sep 20 22:15
vboxuser@abc:~/openlane/Openlane

[INFO]: Running Single-Corner Static Timing Analysis at the nom process corner (log: designs/spm/runs/openlane_test/logs/signoff/31-rcx_sta.log)...
[WARNING]: Module sky130_fd_sc_hd__tapvprvrgnd_1 blackboxed during sta
[WARNING]: Module sky130_ef_sc_hd__decap_12 blackboxed during sta
[WARNING]: Module sky130_fd_sc_hd__fill_1 blackboxed during sta
[WARNING]: Module sky130_fd_sc_hd__fill_2 blackboxed during sta
[STEP 32]
[INFO]: Creating IR Drop Report (log: designs/spm/runs/openlane_test/logs/signoff/32-ir_drop.log)...
[WARNING]: VSRC_LOC_FILES is not defined. The IR drop analysis will run, but the values may be inaccurate.
[STEP 33]
[INFO]: Running Magic to generate various views...
[INFO]: Streaming out GDSII with Magic (log: designs/spm/runs/openlane_test/logs/signoff/33-gdsii.log)...
[INFO]: Generating MAGLER views...
[INFO]: Generating LEF with Magic (/openlane/designs/spm/runs/openlane_test/logs/signoff/33-lef.log)...
[STEP 34]
[INFO]: Streaming out GDSII with KLayout (log: designs/spm/runs/openlane_test/logs/signoff/34-gdsii-klayout.log)...
[STEP 35]
[INFO]: Running XOR on the layouts using KLayout (log: designs/spm/runs/openlane_test/logs/signoff/35-xor.log)...
[INFO]: No XOR differences between KLayout and Magic gds.
[STEP 36]
[INFO]: Running Magic Spice Export from LEF (log: designs/spm/runs/openlane_test/logs/signoff/36-spice.log)...
[STEP 37]
[INFO]: Writing Powered Verilog (log: designs/spm/runs/openlane_test/logs/signoff/37-write_powered_def.log, designs/spm/runs/openlane_test/logs/signoff/37-write_powered_verilog.log)...
[STEP 38]
[INFO]: Writing Verilog (log: designs/spm/runs/openlane_test/logs/signoff/37-write_powered_verilog.log)...
[STEP 39]
[INFO]: Running LVS (log: designs/spm/runs/openlane_test/logs/signoff/39-lvs.log)...
[STEP 40]
[INFO]: Running Magic DRC (log: designs/spm/runs/openlane_test/logs/signoff/40-drc.log)...
[INFO]: Converting Magic DRC database to various tool-readable formats...
[INFO]: No DRC violations after GDS streaming out.
[STEP 41]
[INFO]: Running OpenROAD Antenna Rule Checker (log: designs/spm/runs/openlane_test/logs/signoff/41-arc.log)...
[STEP 42]
[INFO]: Running Circuit Validity Checker ERC (log: designs/spm/runs/openlane_test/logs/signoff/42-erc_screen.log)...
[INFO]: Saving current set of views in 'designs/spm/runs/openlane_test/results/final'...
[INFO]: Saving runtime environment...
[INFO]: Generating final set of reports...
[INFO]: Created manufacturability report at 'designs/spm/runs/openlane_test/reports/manufacturability.rpt'.
[INFO]: Created metrics report at 'designs/spm/runs/openlane_test/reports/metrics.csv'.
[INFO]: There are no hold violations in the design at the typical corner.
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/spm/runs/openlane_test/reports/signoff/31-rcx_sta.checks.rpt'.
[INFO]: There are no setup violations in the design at the typical corner.
[SUCCESS]: Flow complete.
[INFO]: Note that the following warnings have been generated:
[WARNING]: 1 warnings found by linter
[WARNING]: Current core area is too small for the power grid settings chosen. The power grid will be scaled down.
[WARNING]: Module sky130_fd_sc_hd__tapvprvrgnd_1 blackboxed during sta
[WARNING]: Module sky130_ef_sc_hd__decap_12 blackboxed during sta
[WARNING]: Module sky130_fd_sc_hd__fill_1 blackboxed during sta
[WARNING]: Module sky130_fd_sc_hd__fill_2 blackboxed during sta
[WARNING]: VSRC_LOC_FILES is not defined. The IR drop analysis will run, but the values may be inaccurate.
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/spm/runs/openlane_test/reports/signoff/31-rcx_sta.checks.rpt'.

Basic test passed
vboxuser@abc:~/openlane/Openlane$
```

```
Activities Terminal vbxuser@abc:~/openlane/Openlane Sep 20 22:15
[INFO]: Running Magic to generate various views...
[INFO]: Streaming out GDSII with Magic (log: designs/spm/runs/openlane_test/logs/signoff/33-gdsii.log)...
[INFO]: Generating MAGLEF views...
[INFO]: Generating lef with Magic (/openlane/designs/spm/runs/openlane_test/logs/signoff/33-lef.log)...
[STEP 34]
[INFO]: Streaming out GDSII with KLayout (log: designs/spm/runs/openlane_test/logs/signoff/34-gdsii-klayout.log)...
[STEP 35]
[INFO]: Running XOR on the layouts using KLayout (log: designs/spm/runs/openlane_test/logs/signoff/35-xor.log)...
[INFO]: No XOR differences between KLayout and Magic gds.
[STEP 36]
[INFO]: Running Magic Spice Export from LEF (log: designs/spm/runs/openlane_test/logs/signoff/36-spice.log)...
[STEP 37]
[INFO]: Writing Powered Verilog (logs: designs/spm/runs/openlane_test/logs/signoff/37-write_powered_def.log, designs/spm/runs/openlane_test/logs/signoff/37-write_powered_verilog.log)...
[STEP 38]
[INFO]: Writing Verilog (log: designs/spm/runs/openlane_test/logs/signoff/37-write_powered_verilog.log)...
[STEP 39]
[INFO]: Running LVS (log: designs/spm/runs/openlane_test/logs/signoff/39-lvs.lef.log)...
[STEP 40]
[INFO]: Running Magic DRC (log: designs/spm/runs/openlane_test/logs/signoff/40-drc.log)...
[INFO]: Converting Magic DRC database to various tool-readable formats...
[INFO]: No DRC violations after GDS streaming out.
[STEP 41]
[INFO]: Running OpenROAD Antenna Rule Checker (log: designs/spm/runs/openlane_test/logs/signoff/41-arc.log)...
[STEP 42]
[INFO]: Running Circuit Validity Checker ERC (log: designs/spm/runs/openlane_test/logs/signoff/42-erc_screen.log)...
[INFO]: Saving current set of views in 'designs/spm/runs/openlane_test/results/final ...
[INFO]: Saving runtime environment...
[INFO]: Generating final set of reports...
[INFO]: Created manufacturability report at 'designs/spm/runs/openlane_test/reports/manufacturability.rpt'.
[INFO]: Created metrics report at 'designs/spm/runs/openlane_test/reports/metrics.csv'.
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/spm/runs/openlane_test/reports/signoff/31-rcx_sta.checks.rpt'.
[INFO]: There are no hold violations in the design at the typical corner.
[INFO]: There are no setup violations in the design at the typical corner.
[SUCCESS]: Flow complete.
[INFO]: Note that the following warnings have been generated:
[WARNING]: 1 warnings found by linter
[WARNING]: Current core area is too small for the power grid settings chosen. The power grid will be scaled down.
[WARNING]: Module sky130_fd_sc_hd_tapwrvrgnd_1 blackboxed during sta
[WARNING]: Module sky130_ef_sc_hd_decap_i2 blackboxed during sta
[WARNING]: Module sky130_fd_sc_hd_fll1_1 blackboxed during sta
[WARNING]: Module sky130_fd_sc_hd_fll1_2 blackboxed during sta
[WARNING]: VSRC_LOC_FILES is not defined. The IR drop analysis will run, but the values may be inaccurate.
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/spm/runs/openlane_test/reports/signoff/31-rcx_sta.checks.rpt'.

Basic test passed
vbxuser@abc:~/openlane/Openlane$ yosys -V
Yosys 0.9 (git sha1 1979e0b)
vbxuser@abc:~/openlane/Openlane$ iverilog -V
Icarus Verilog version 10.3 (stable) ()

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it under the terms of the GNU General Public License as published by
the Free Software Foundation; either version 2 of the License, or
(at your option) any later version.
```

```
Activities Terminal vbxuser@abc:~/openlane/Openlane Sep 20 22:16
Icarus Verilog Preprocessor version 10.3 (stable) ()

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Icarus Verilog Parser/Elaborator version 10.3 (stable) ()

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FLAGS DLL vvp.tgt
vvp.tgt: Icarus Verilog VVP Code Generator 10.3 (stable) ()

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51 Franklin Street, Fifth Floor, Boston, MA 02110-1301, USA.

vbxuser@abc:~/openlane/Openlane$
```

```
Activities Terminal v Sep 20 22:16 vboxuser@abc: ~/openlane/Openlane

(at your option) any later version.

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51 Franklin Street, Fifth Floor, Boston, MA 02110-1301, USA.

Icarus Verilog Parser/Elaborator version 10.3 (stable) ()

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with this program; if not, write to the Free Software Foundation, Inc.,
51 Franklin Street, Fifth Floor, Boston, MA 02110-1301, USA.

vboxuser@abc:~/openlane/Openlane$ gtkwave --version
Gtk-Message: 22:10:10.148: Failed to load module "canberra-gtk-module"
GTKWave Analyzer v3.3.103 (w)1999-2019 BSI

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warranty; not even for MERCHANTABILITY or FITNESS FOR A PARTICULAR PURPOSE.
vboxuser@abc:~/openlane/Openlane$
```

```
Activities Terminal v Sep 20 22:16 vboxuser@abc: ~/openlane/Openlane

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51 Franklin Street, Fifth Floor, Boston, MA 02110-1301, USA.

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vvp.tgt: Icarus Verilog VVP Code Generator 10.3 (stable) ()

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51 Franklin Street, Fifth Floor, Boston, MA 02110-1301, USA.

vboxuser@abc:~/openlane/Openlane$ gtkwave --version
Gtk-Message: 22:10:10.148: Failed to load module "canberra-gtk-module"
GTKWave Analyzer v3.3.103 (w)1999-2019 BSI

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warranty; not even for MERCHANTABILITY or FITNESS FOR A PARTICULAR PURPOSE.
vboxuser@abc:~/openlane/Openlane$ ngspice -v
ngspice compiled from ngspice revision 31
Written originally by Berkeley University
Currently maintained by the NGSpice Project

Copyright (C) 1985-1996, The Regents of the University of California
Copyright (C) 1999-2011, The NGSpice Project
vboxuser@abc:~/openlane/Openlane$
```

```
Activities Terminal v Sep 20 22:16 vboxuser@abc: ~/openlane/Openlane

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51 Franklin Street, Fifth Floor, Boston, MA 02110-1301, USA.

FLAGS DLL vvp.tgt
vvp.tgt: Icarus Verilog VVP Code Generator 10.3 (stable) ()

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with this program; if not, write to the Free Software Foundation, Inc.,
51 Franklin Street, Fifth Floor, Boston, MA 02110-1301, USA.

vboxuser@abc:~/openlane/Openlane$ gtkwave --version
Gtk-Message: 22:10:10.148: Failed to load module "canberra-gtk-module"
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vboxuser@abc:~/openlane/Openlane$ ngspice -v
ngspice compiled from ngspice revision 31
Written originally by Berkeley University
Currently maintained by the NGSpice Project

Copyright (C) 1985-1996, The Regents of the University of California
Copyright (C) 1999-2011, The NGSpice Project
vboxuser@abc:~/openlane/Openlane$ magic --version
Unknown option: '-version'
usage: magic [-g gport] [-d devType] [-n nonType] [-i tabletPort] [-D] [-F objfile saveFile]
[-t technology] [-r configFile] [-nrcfile] [-noconsole] [-nowindow] [-wrapper] [file]
vboxuser@abc:~/openlane/Openlane$ magic --version
8.2.157
vboxuser@abc:~/openlane/Openlane$
```

```
Activities Terminal Sep 20 22:33 vboxuser@abc-
vboxuser@abc:~$ git --version
git version 2.25.1
vboxuser@abc:~$ docker --version
Docker version 20.1.3, build 20.1.3-0ubuntu1-20.04.1
vboxuser@abc:~$ python3 --version
Python 3.8.10
vboxuser@abc:~$ make --version
GNU Make 4.2.1
Built for x86_64-pc-linux-gnu
Copyright (C) 1988-2016 Free Software Foundation, Inc.
License GPLv3+: GNU GPL version 3 or later <http://gnu.org/licenses/gpl.html>
This is free software: you are free to change and redistribute it.
There is NO WARRANTY, to the extent permitted by law.
vboxuser@abc:~$ python3 -m venv -h
usage: venv [-h] [--system-site-packages] [--symlinks | --copies] [--clear] [--upgrade] [--without-pip] [--prompt PROMPT] ENV_DIR [ENV_DIR ...]

Creates virtual Python environments in one or more target directories.

positional arguments:
  ENV_DIR                A directory to create the environment in.

optional arguments:
  -h, --help            show this help message and exit
  --system-site-packages
                        Give the virtual environment access to the system site-packages dir.
                        Try to use symlinks rather than copies, when symlinks are not the default for the platform.
  --symlinks            Try to use symlinks rather than copies, even when symlinks are the default for the platform.
  --copies              Delete the contents of the environment directory if it already exists, before environment creation.
  --clear              Upgrade the environment directory to use this version of Python, assuming Python has been upgraded in-place.
  --upgrade             Skips installing or upgrading pip in the virtual environment (pip is bootstrapped by default)
  --without-pip         Provides an alternative prompt prefix for this environment.
  --prompt PROMPT

Once an environment has been created, you may wish to activate it, e.g. by sourcing an activate script in its bin directory.
vboxuser@abc:~$
```

```
Activities Terminal Sep 20 22:33 vboxuser@abc-
GNU Make 4.2.1
Built for x86_64-pc-linux-gnu
Copyright (C) 1988-2016 Free Software Foundation, Inc.
License GPLv3+: GNU GPL version 3 or later <http://gnu.org/licenses/gpl.html>
This is free software: you are free to change and redistribute it.
There is NO WARRANTY, to the extent permitted by law.
vboxuser@abc:~$ python3 -m venv -h
usage: venv [-h] [--system-site-packages] [--symlinks | --copies] [--clear] [--upgrade] [--without-pip] [--prompt PROMPT] ENV_DIR [ENV_DIR ...]

Creates virtual Python environments in one or more target directories.

positional arguments:
  ENV_DIR                A directory to create the environment in.

optional arguments:
  -h, --help            show this help message and exit
  --system-site-packages
                        Give the virtual environment access to the system site-packages dir.
                        Try to use symlinks rather than copies, when symlinks are not the default for the platform.
  --symlinks            Try to use symlinks rather than copies, even when symlinks are the default for the platform.
  --copies              Delete the contents of the environment directory if it already exists, before environment creation.
  --clear              Upgrade the environment directory to use this version of Python, assuming Python has been upgraded in-place.
  --upgrade             Skips installing or upgrading pip in the virtual environment (pip is bootstrapped by default)
  --without-pip         Provides an alternative prompt prefix for this environment.
  --prompt PROMPT

Once an environment has been created, you may wish to activate it, e.g. by sourcing an activate script in its bin directory.
vboxuser@abc:~$ docker run hello-world
Unable to find image 'hello-world:latest' locally
17fec7b9c9d7: Pull complete
Digest: sha256:54e6dc1dd1fc1c3c58bd8017914dbed8701e2d8c74d9262e26bd9cc1642d31
Status: Downloaded newer image for hello-world:latest

Hello from Docker!
This message shows that your installation appears to be working correctly.

To generate this message, Docker took the following steps:
1. The Docker client contacted the Docker daemon.
2. The Docker daemon pulled the "hello-world" image from the Docker Hub.
   (and4)
3. The Docker daemon created a new container from that image which runs the
   executable that produces the output you are currently reading.
4. The Docker daemon streamed that output to the Docker client, which sent it
   to your terminal.

To try something more ambitious, you can run an Ubuntu container with:
$ docker run -it ubuntu bash

Share images, automate workflows, and more with a free Docker ID:
https://hub.docker.com/

For more examples and ideas, visit:
https://docs.docker.com/get-started/
vboxuser@abc:~$
```