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Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

- RTL ANALYSIS

▶ Run Linter

- Open Elaborated Design

SYNTHESIS










▶ Run Synthesis

- Open Synthesized Design

▼ IMPLEMENTATION

▶ Run Implementation

- Open Implemented Design

Name	Value
 wr_clk	0
 rd_clk	1
 rst	0
 wr_en	0
 rd_en	1
>  din[7:0]	0d
>  dout[7:0]	63
 full	0
 empty	0

