

Lab Report: Experiment 4

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Experiment:
Single-Stage Differential Amplifier



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1 Objective

Design and simulate a single-stage MOS differential amplifier with an active (current-mirror) load. Extract DC operating point, differential small-signal gain, input-referred offset, CMRR, input pair transconductance (gm), output resistance (ro), 3-dB bandwidth, and transient response (step). Compare measured results with hand calculations (small-signal approximations).

Circuit description:

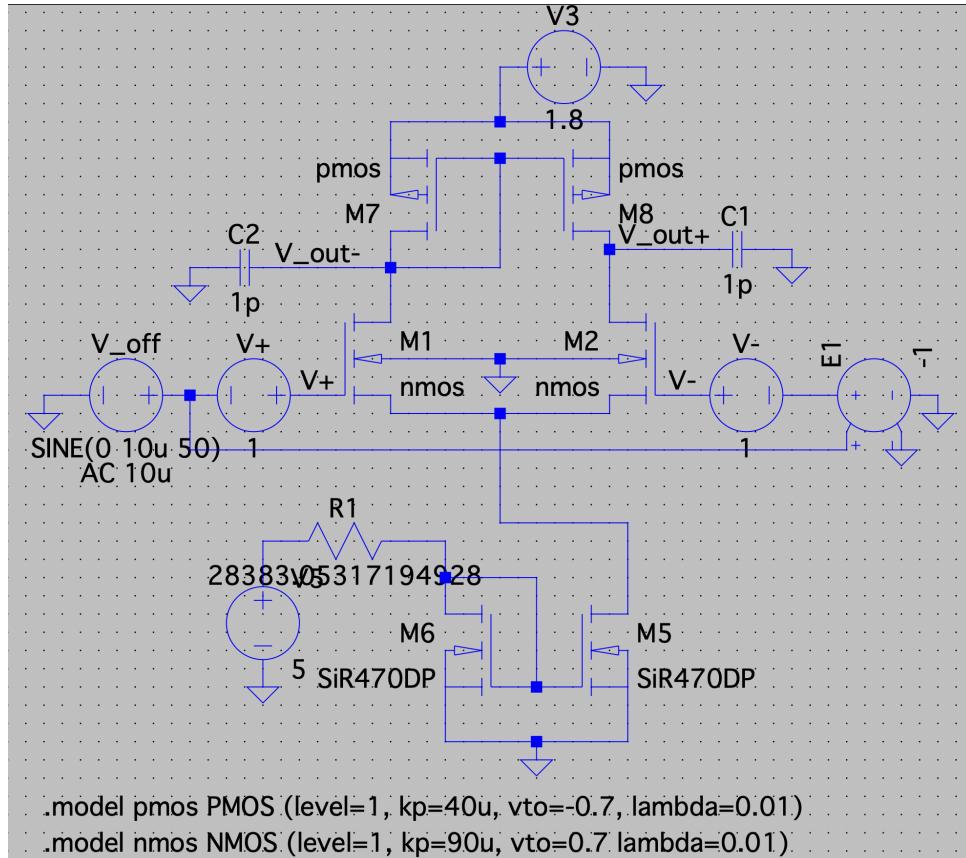
Input pair: NMOS differential pair (M1, M2) Tail current source: NMOS current source (Iss) or ideal current source Active load: PMOS current mirror load (M3, M4) forming a differential-to-single-ended conversion (use one side for single-ended output at drain of M2). Bias: $VDD = 1.8$ V (suggested), $VSS = 0$ Capacitive load: $CL = 1$ pF (for frequency/transient testing)

Recommended component values (please use as you desire):

- Supply: $VDD = 1.8$ V
- Tail current: $Iss = 100 \mu A$ (total differential tail current; $50 \mu A$ per transistor at balance)
- NMOS input devices (M1/M2): $W/L = 50 \mu m / 1 \mu m$
- PMOS load devices (M3/M4): $W/L = 100 \mu m / 1 \mu m$ (larger W for higher ro)
- Current-mirror transistor (M5) for biasing as needed: similar sizing to M3/M4
- Output load capacitance: $CL = 1$ pF
- Small input differential test source: $V_{test} = 1$ mV AC for small-signal gain measurement

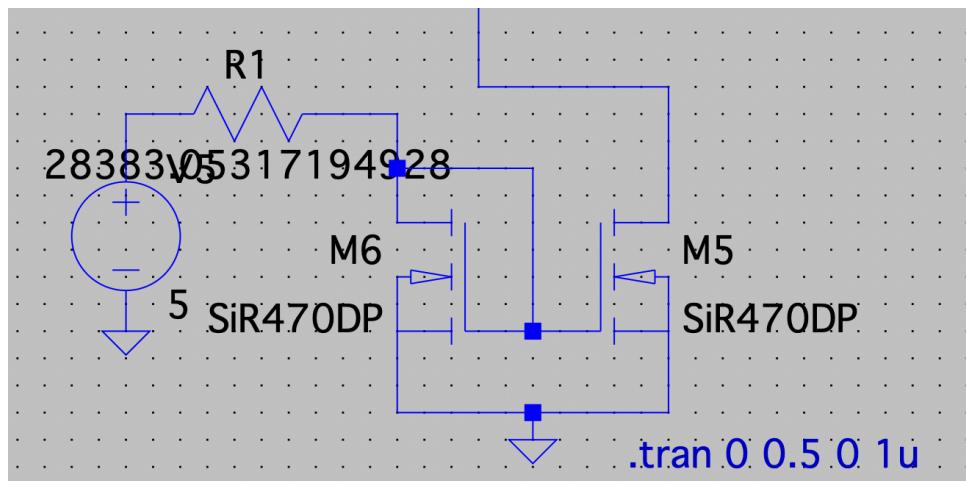
2 Circuit

Differential Amplifier built using NMOS input, current mirror, PMOS active load.

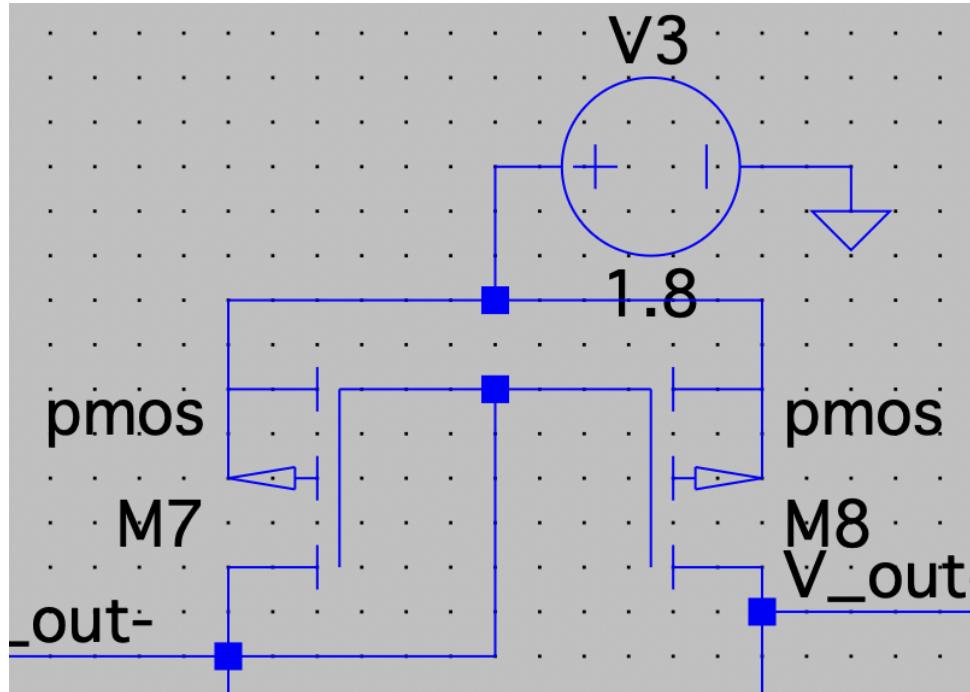


We can analyze each section separately,

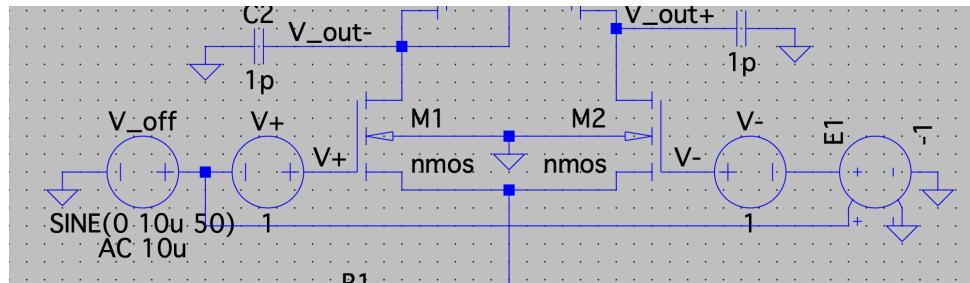
2.1 Current Mirror



2.2 PMOS Active load



2.3 Input NMOS



2.4 MOSFET Parameters

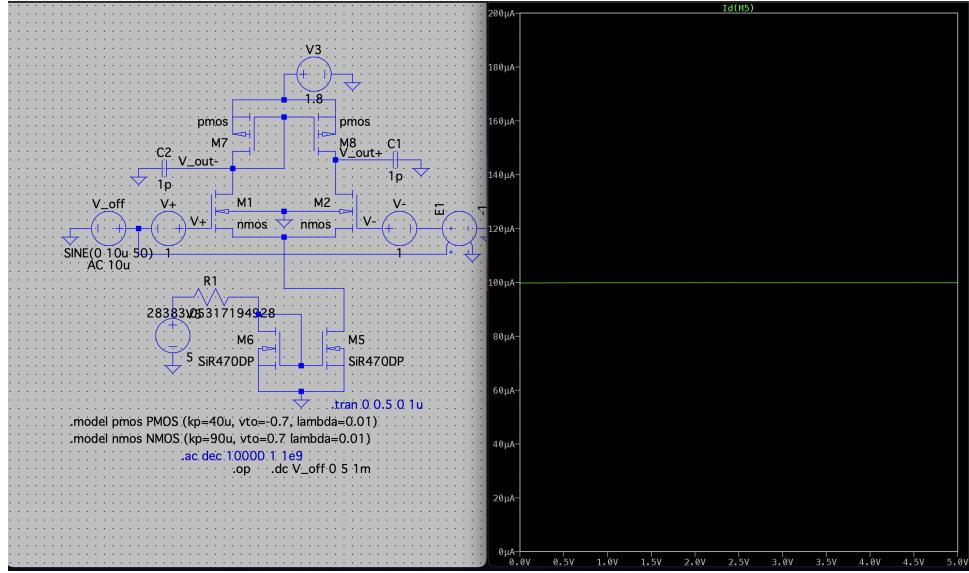
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.model pmos PMOS (kp=40u, vto=-0.7, lambda=0.01)
.model nmos NMOS (kp=90u, vto=0.7 lambda=0.01) .
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For PMOS, $W = 100\mu\text{m}$, $L = 1\mu\text{m}$ and NMOS $W = 50\mu\text{m}$, $L = 1\mu\text{m}$. For the MOSFETs used in current mirror, $k_p = 69.6391$, $V_{to} = 2.16\text{V}$.

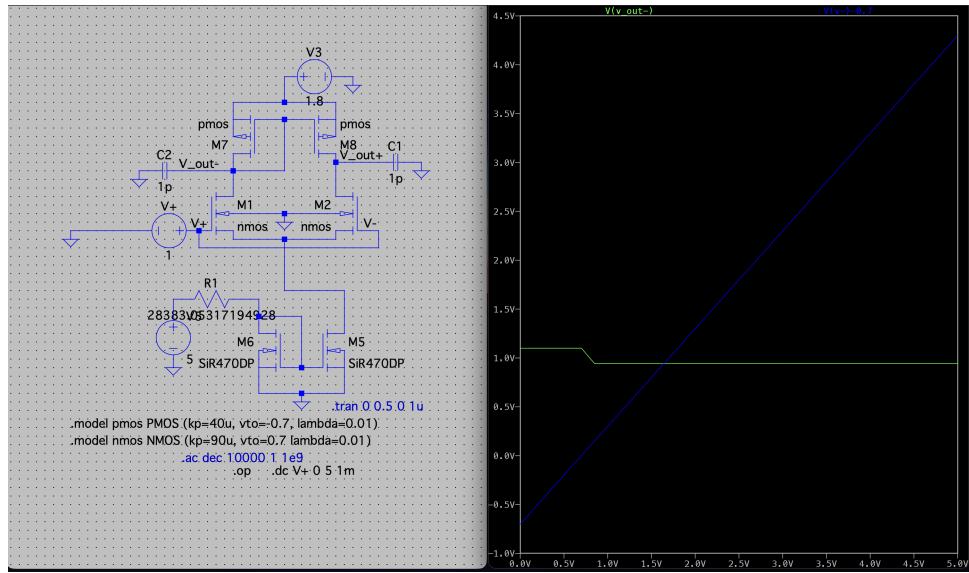
3 DC OP point

Current obtained through current mirror can be adjusted through adjusting the R value. It is done by solving the equations,

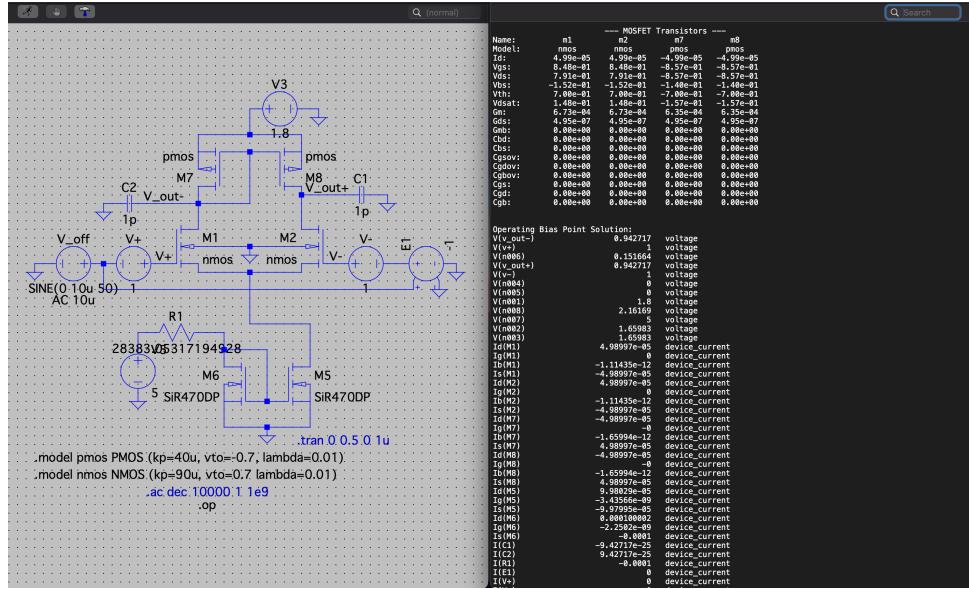
$$I = 100\mu A = \frac{V_S - V_D}{R} = \frac{k_p}{2} (V_{GS} - 2.16)^2$$



We have to choose V_+ , V_- values such that MOSFETs M1 and M2 are in saturation. We do so by plotting V_{DS} vs $V_{GS} - V_{TO}$ and choose V_+ appropriately,



We choose bias point to be 1V so that MOSFETs M1 and M2 are comfortably in saturation.



4 Differential Gain

Small signal parameters of MOSFETs are given by,

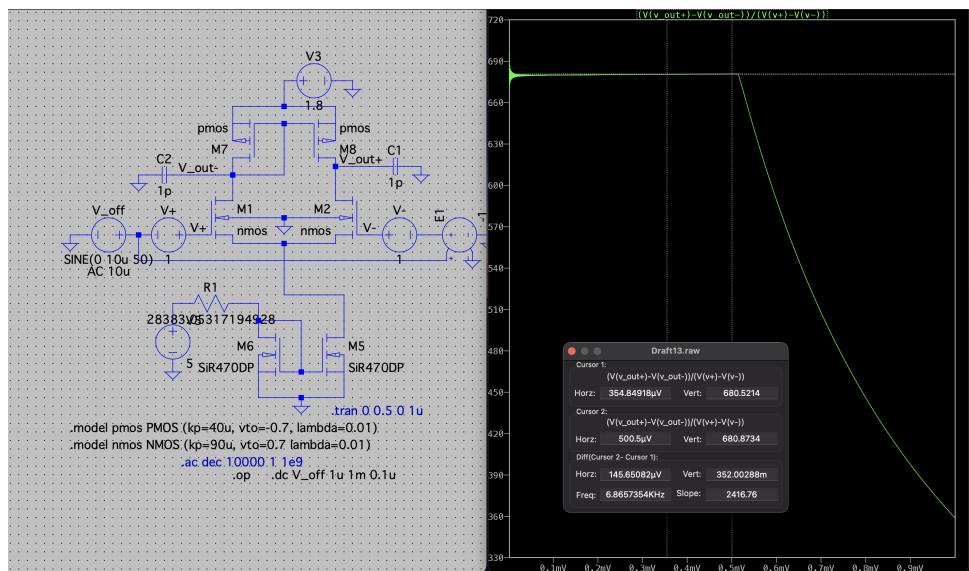
$$g_m = \frac{2I_D}{V_{GS} - V_{TO}} = \frac{\partial I_D}{\partial V_{GS}}$$

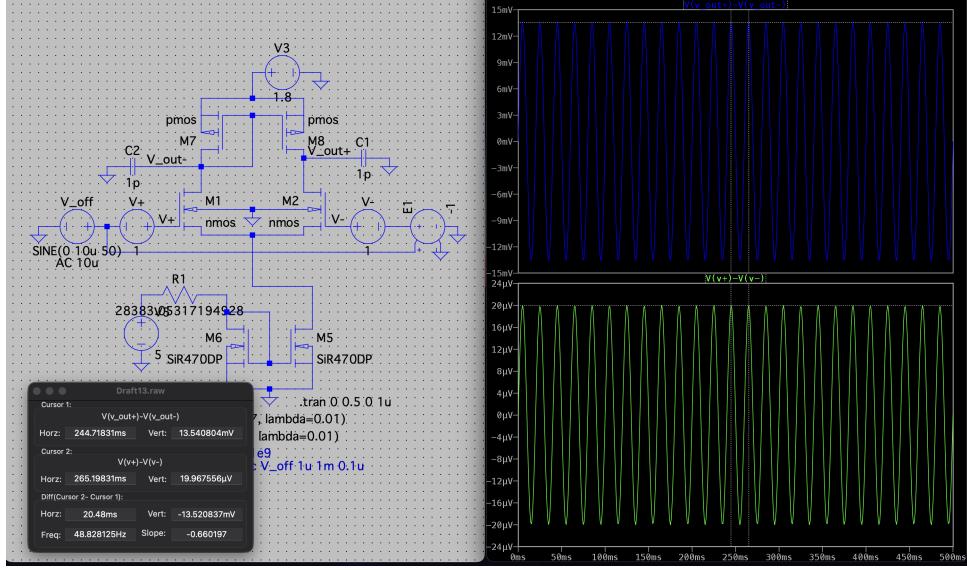
$$r_o = \frac{1}{\lambda I_D} = \frac{\partial V_{DS}}{\partial I_D}$$

Differential gain is given by

$$A_d = g_{m1}(r_{o1} \parallel r_{o7}) = \frac{V_{out}}{V_{id}}$$

Where $V_{id} = V_+ - V_-$, g_{m1} is transconductance of NMOS M1, r_{o1}, r_{o7} are output resistances of NMOS M1 and PMOS M7 respectively.





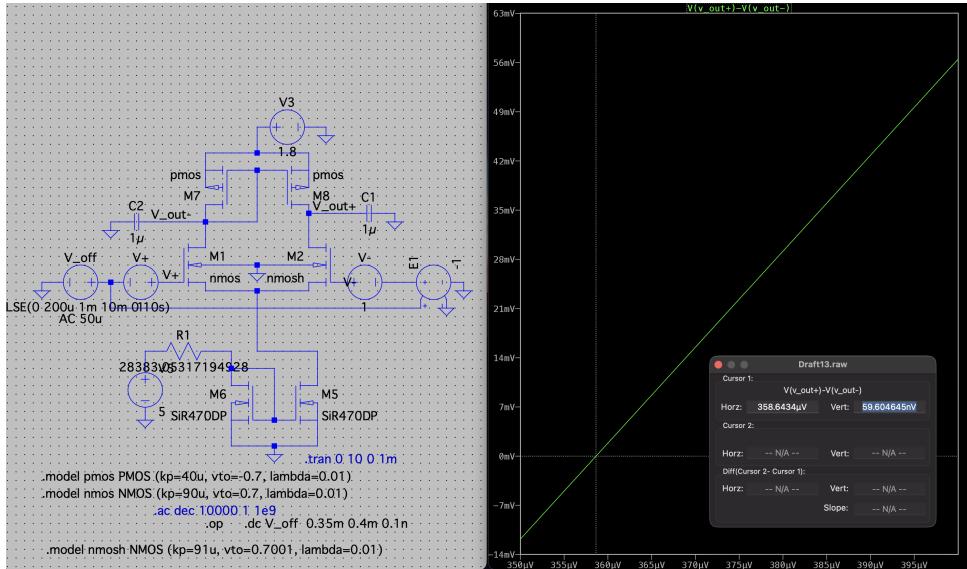
We get,

- Theoretical Gain: 674.145183906806
- Observed Gain: 680.5214

5 Input-Referred Offset

When we give inputs $V_+ = V_-$, we would expect V_{out} to be 0 (as it is a differential amplifier), but however it turns out not to be the case. This is due to factors such as non-ideality of current mirror, MOSFETs, and slight variation in MOSFET parameters despite being similar MOSFETs among others.

V_{OS} (Input-Referred Offset) is calculated by shorting V_+, V_- , sweeping across input voltage to find its value at the point where $V_{out} = 0$.



Here, we get $V_{OS} \approx 358.6434\mu V$. It comes out to be similar when calculated using the formula

$$V_{OS} = \frac{\Delta V_T}{2} + \frac{V_{OV}}{2} \frac{\Delta Kp}{Kp}$$

Where V_{OV} is overdrive voltage, $\Delta V_T, \Delta Kp$ account for slight variations in Kp, V_T values of seeming similar MOSFETs.

6 Common-Mode Rejection Ratio (CMRR)

$$\text{CMRR} = 20 \log \left(\frac{A_d}{A_{cm}} \right)$$

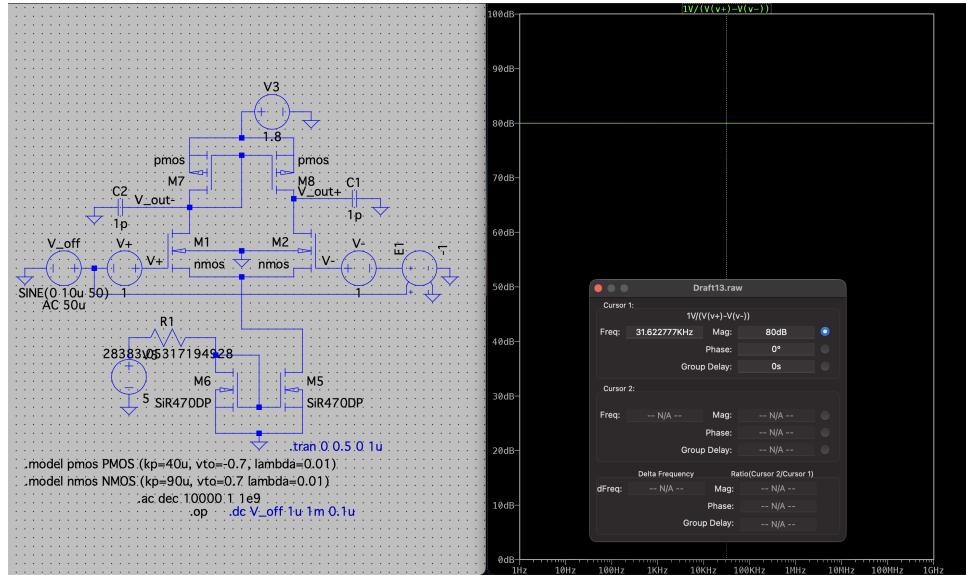
where A_{cm} is the common-mode gain,

$$A_d = \frac{V_{out}}{I_D} = g_{m1}(r_{o1} \parallel r_{o7})$$

$$A_{cm} = \frac{V_{out}}{V_{cm}} \approx \frac{g_{m1}(r_{o1} \parallel r_{o7})}{1 + 2g_{m1}r_{tail}}$$

$$r_{tail} = r_{o6} \parallel r_{o5}$$

$$\text{CMRR} \approx 20 \log (2g_{m1}r_{tail})$$

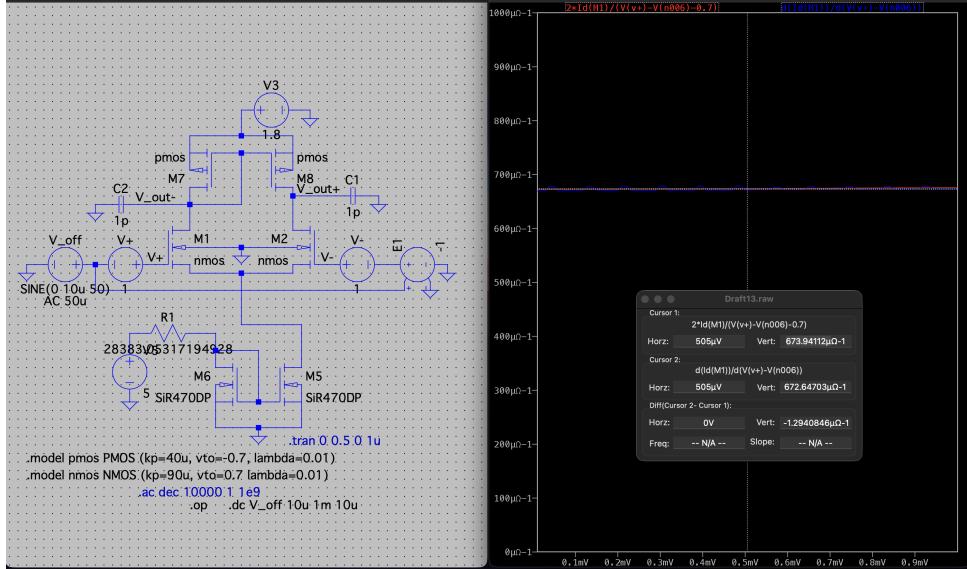


We get,

- Theoretical CMRR: $76.56610455194526dB$
- Observed CMRR: $80dB$

7 Transconductance (g_m)

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_D}{V_{GS} - V_{TO}}$$



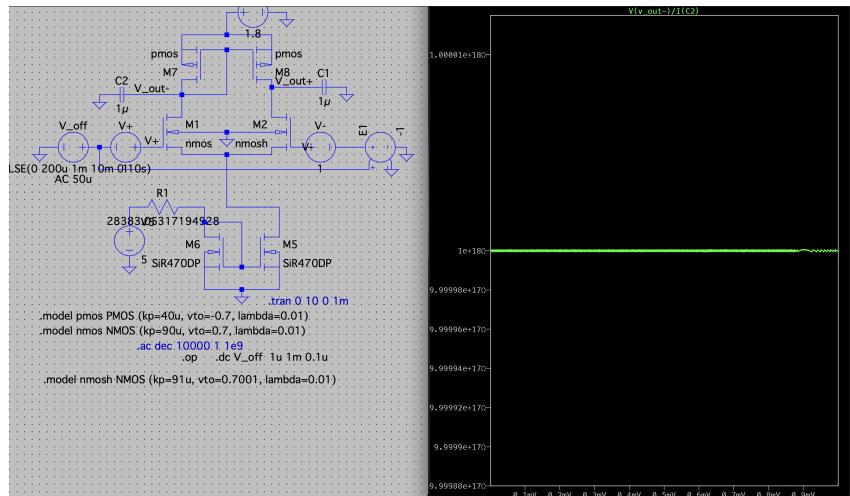
We get,

- Theoretical CMRR: $672.64703\mu\Omega^{-1}$
- Observed CMRR: $673.94112\mu\Omega^{-1}$

8 Output Resistance

Output Resistance is defined as the ratio of potential difference and current as seen from output terminal.

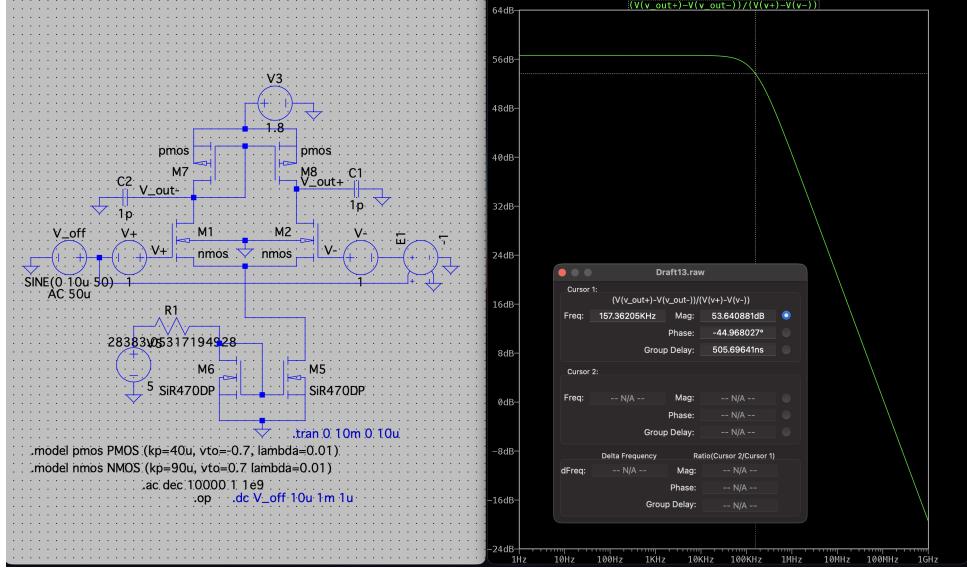
$$R_o = \frac{V_{out}}{I_{out}}$$



9 3dB Bandwidth (f_{3dB})

We need to calculate the frequency at which gain goes to Max. gain $-3dB$. That frequency is given by,

$$f_{3dB} = \frac{1}{2\pi R_{out} C_L}$$



We get,

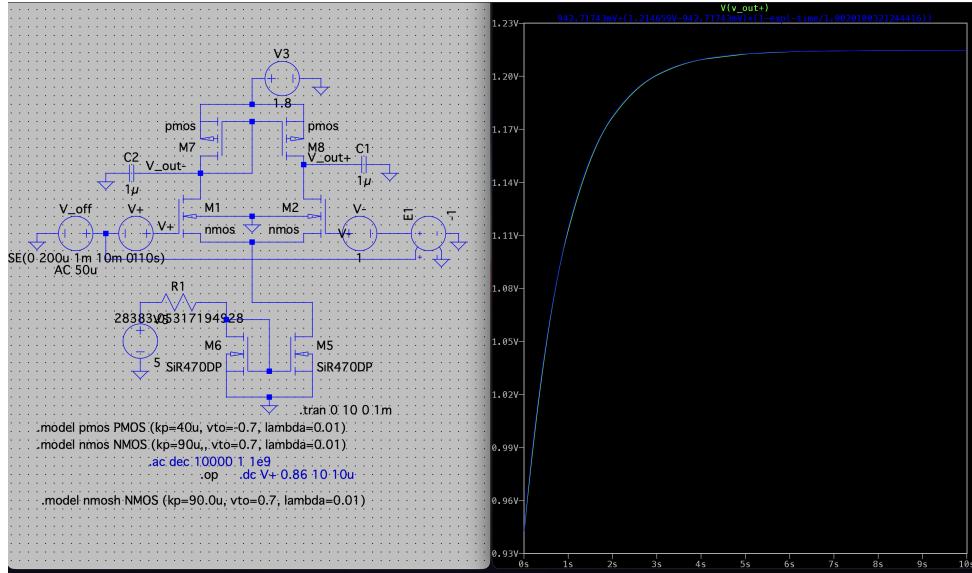
- Theoretical 3dB frequency: $158.835kHz$
- Observed 3dB frequency: $157.36205KHz$

10 Transient Response

We observe an exponential-charging (but shifted upward) like graph (similar to RC charging). This is given by the equation,

$$V_{out} = V_{initial} + (V_{steady} - V_{initial}) \left(1 - e^{-\frac{t}{\tau}} \right)$$

Where $\tau = R_{out}C_L = (r_{o1} \parallel r_{o7})C_L$. Load capacitors must be set to appropriate values (not too low, of order $\approx \mu F$) to properly observe exponential charging behaviour. While giving unit step input, rise time must be appropriately specified.



We observe that theoretical and observed transient response match.

11 Conclusion

In this experiment we have designed and simulated a differential amplifier using MOSFETs, current mirror and active PMOS load. And then calculated and verified differential gain, input-referred offset, CMRR (common mode rejection ratio), input pair transconductance, output resistance, 3-dB bandwidth, transient response to step input.

Some of the codes used may be found at https://github.com/ArjunPavanje/EE2301/tree/main/Simluations/Experiment_4/codes

Required circuit pictures (if needed) can also be found at, https://github.com/ArjunPavanje/EE2301/tree/main/Simluations/Experiment_4/figs