→ ARJUN vankani → 18021010706-0
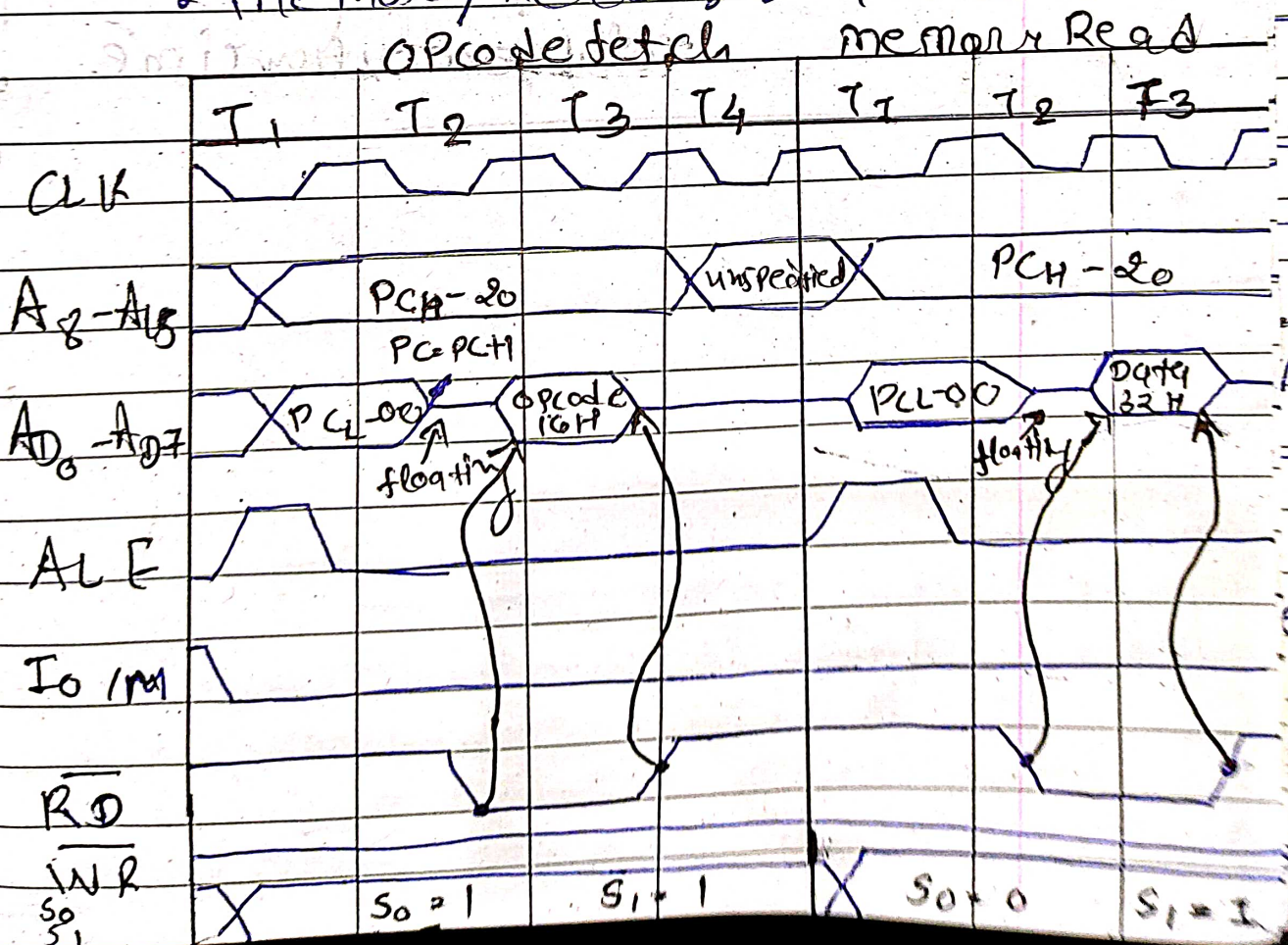
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# ( Assignment - 8)

## Timing Diagram

**Q-1** Draw the timing Diagram for the following given instruction

**I)** MVI A , 32H

→ Number of required machine cycles and T-states:

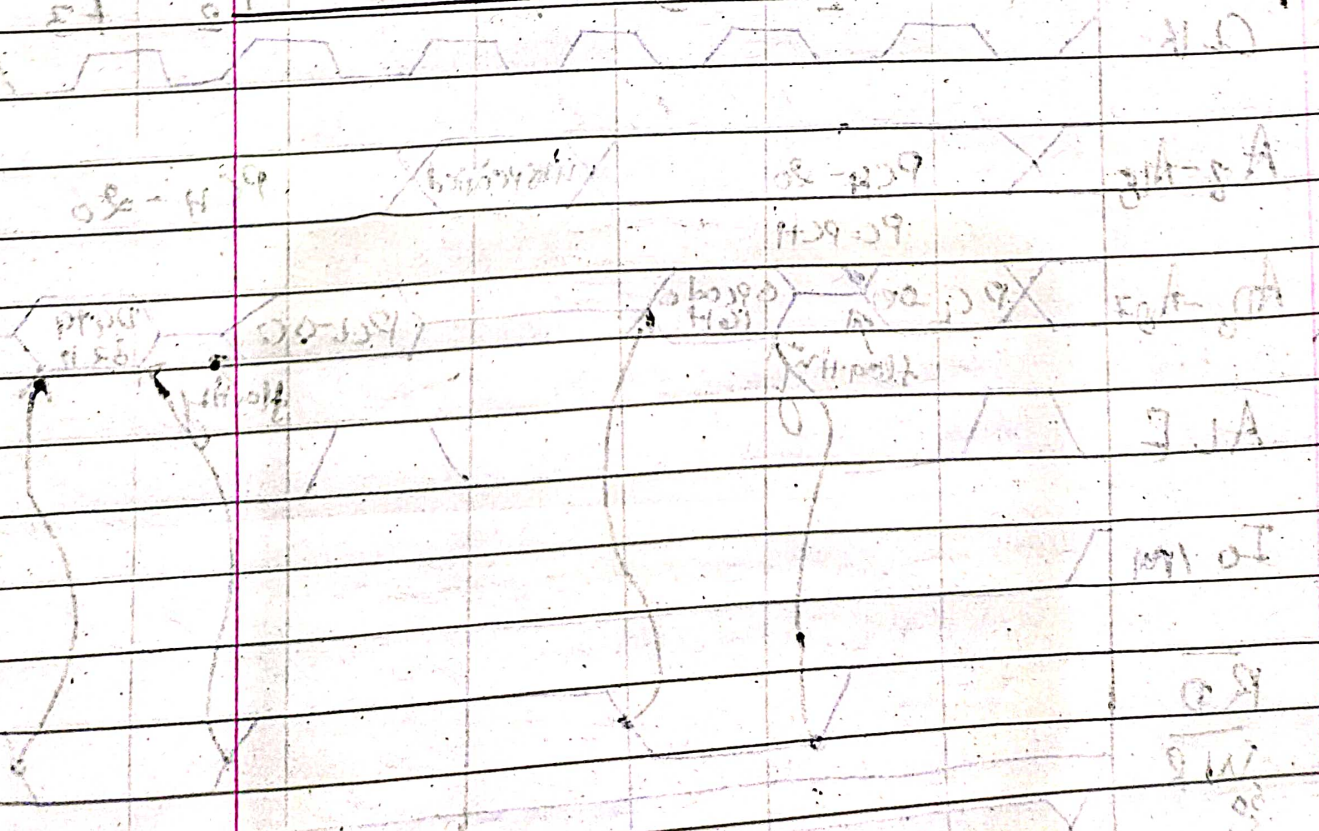- opcode fetch : 4 t-states
- memory Read : 3 t-states

| | opcode fetch | | | | memory Read | | |
|---|---|---|---|---|---|---|---|
| | $T_1$ | $T_2$ | $T_3$ | $T_4$ | $T_1$ | $T_2$ | $T_3$ |
| CLK | | | | | | | |
| $A_8-A_{15}$ | | PCH-20 PC=PCH | | unspecified | | PCH-20 | |
| $AD_0-AD_7$ | PCL-00 floating | opcode 16H | | | PCL-00 floating | | Data 32 H |
| ALE | | | | | | | |
| IO/M | | | | | | | |
| $\overline{RD}$ | | | | | | | |
| $\overline{WR}$ $S_0$ $S_1$ | | $S_0 = 1$ | $S_1 = 1$ | | $S_0 = 0$ | | $S_1 = 1$ |

→ clock frequency of 8085 $f = 3 MHz$

→ T-state clock period $= 1/f = 0.333 \mu s$

⇒ Total execution time ⇒

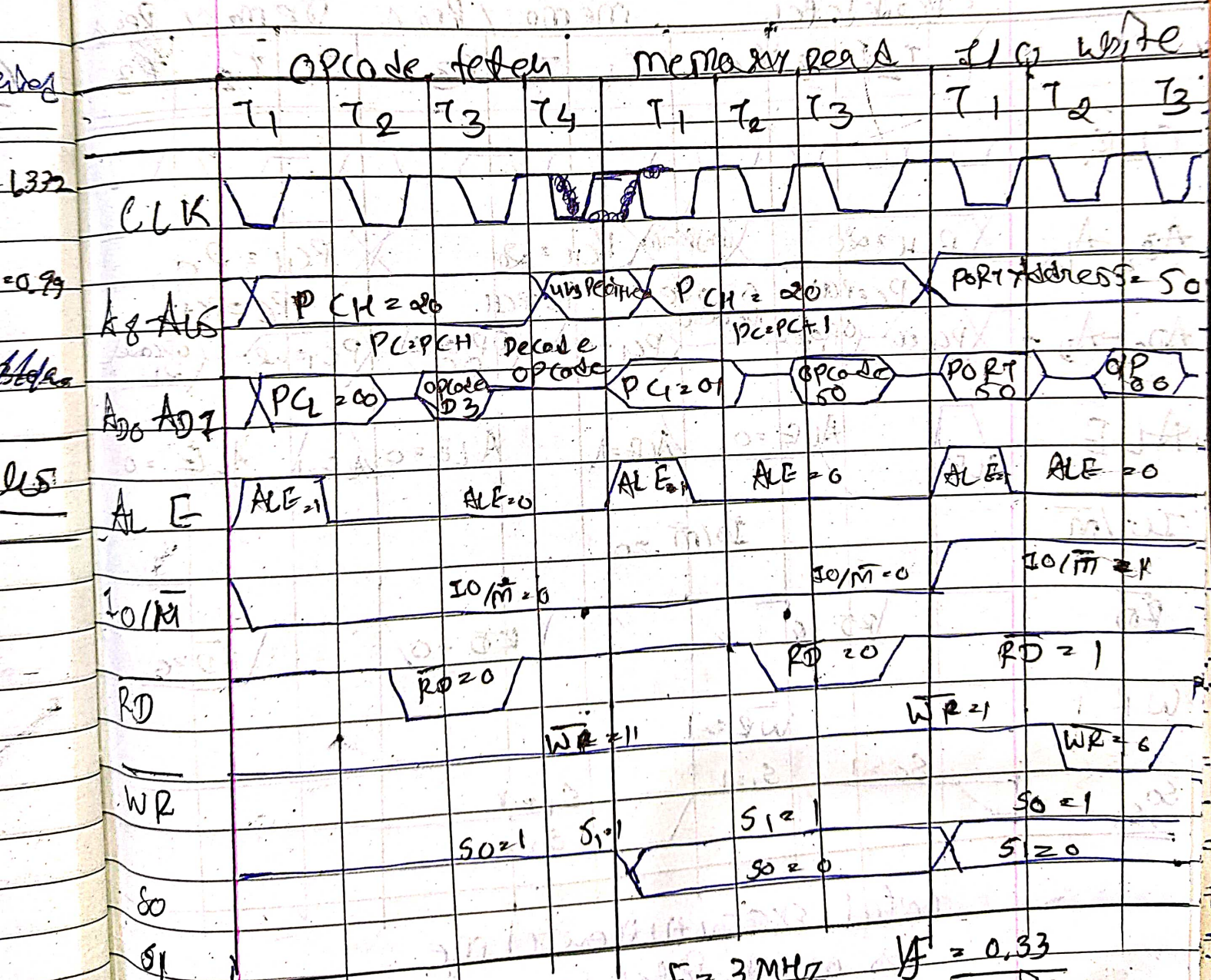| Machine cycle | No. of T-state | Clock period |
|---|---|---|
| Opcode fetch | 4T | $4 * 0.33 = 1.33$ |
| Memory Read | 3T | $3 * 0.33 = 0.9$ |
| Memory Read | 3T | $3 * 0.33 = 0.99$ |

Total execution time $3.33 \mu s$

(2)

## OUT 50H ⇒ Number of required Machine cycles and T-states.

- Opcode fetch : 4 T-states
- Memory Read : 3-states
- I/O Write : 3-states

| | Opcode fetch | | | | Memory Read | | | I/O Write | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $T_1$ | $T_2$ | $T_3$ | $T_4$ | $T_1$ | $T_2$ | $T_3$ | $T_1$ | $T_2$ | $T_3$ |
| CLK | | | | | | | | | | |
| A8-A15 | PCH = 20 | | | unspecified | PCH = 20 | | | PORT Address = 50 | | |
| | | PC=PCH | Decode | | PC=PC+1 | | | | | |
| A0-AD7 | PCL=20 | opcode D3 | opcode | PCL=01 | opcode 50 | | PORT 50 | OP 06 | | |
| ALE | ALE=1 | ALE=0 | | ALE=1 | ALE=0 | | ALE=1 | ALE=0 | | |
| IO/M̄ | | IO/M̄=0 | | | IO/M̄=0 | | | IO/M̄=1 | | |
| RD̄ | | RD=0 | | | RD=0 | | | RD=1 | | |
| WR̄ | | WR=1 | | | WR=1 | | | WR=6 | | |
| S0 | | S0=1 | S1=1 | | S1=1 | | | S0=1 | | |
| S1 | | | | | S0=0 | | | S1=0 | | |

Clock frequency $f = 3 MHz$     $\frac{1}{f} = 0.33$

= opcode + memory Read + I/O Write

Total execution = $4T + 3T + 3T$ ⇒ $4*0.33 + 3*0.33 + 3*0.33$
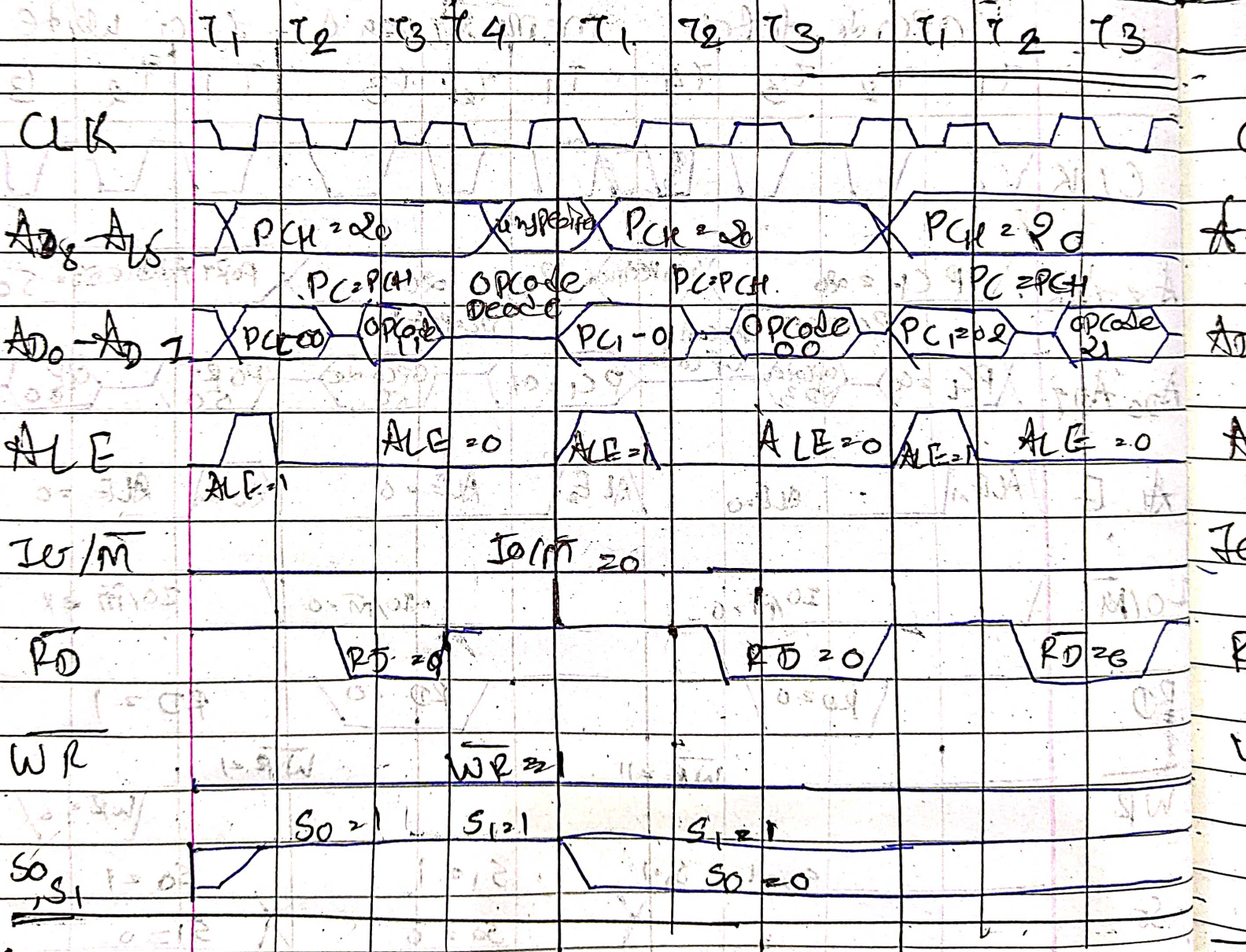
⇒ $\boxed{3.33 \mu s}$

③ LXI B, 2100H, ⇒ Number of required machine
cycles and T-states
- Opcode fetch: 4 T-states
memory Read : 3 T-states
memory Read : 3 T-states
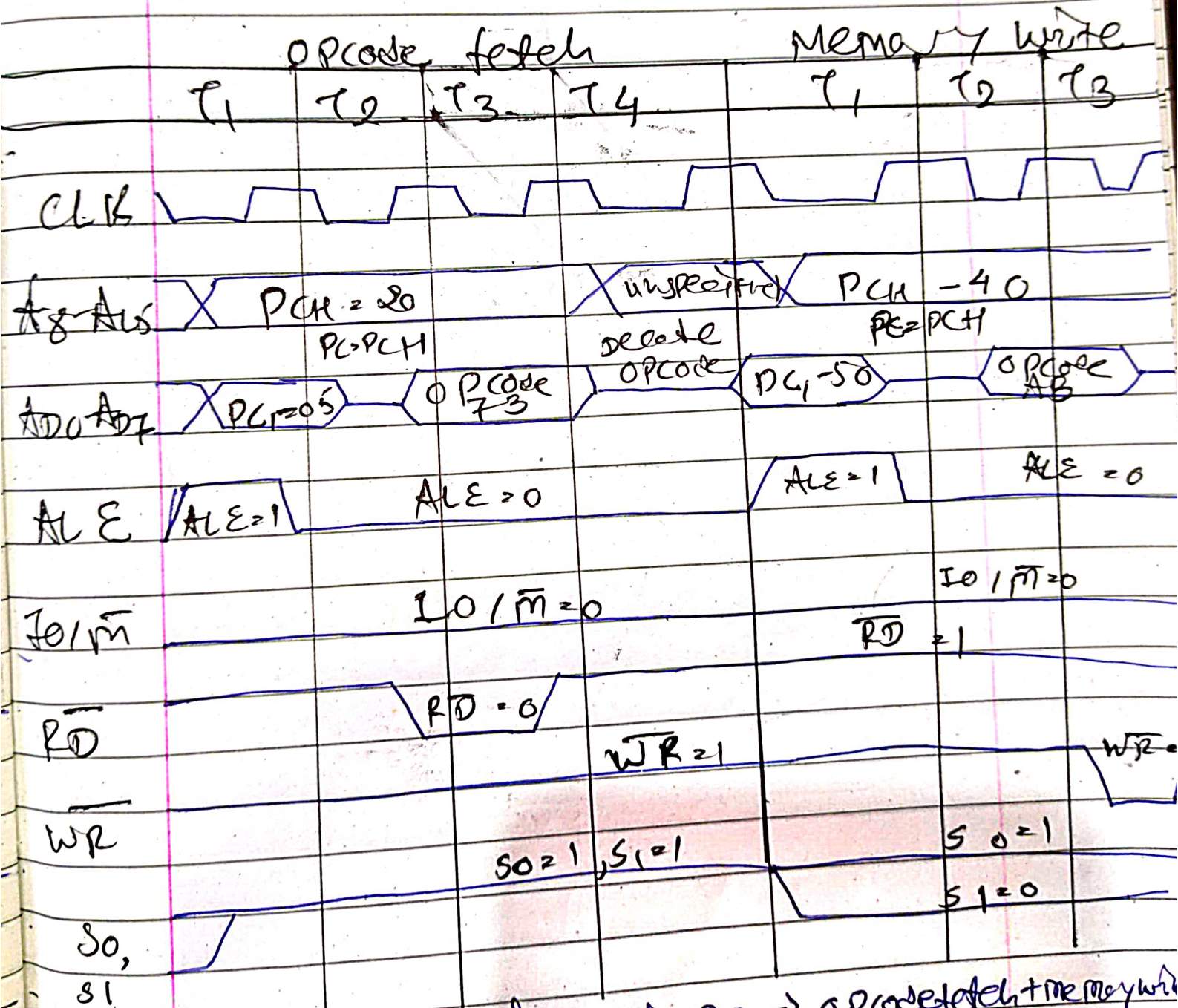
| | Opcode fetch | | | | Memory Read | | | Memory Read | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $T_1$ | $T_2$ | $T_3$ | $T_4$ | $T_1$ | $T_2$ | $T_3$ | $T_1$ | $T_2$ | $T_3$ |
| CLK | | | | | | | | | | |
| $A_8 - A_{15}$ | PCH=20 | | unspecified | PCH=20 | | | | PCH=20 | | |
| $AD_0 - AD_7$ | PC=00 PC=PCH | Opcode 01 | Opcode Decode | PC=PCH PC1=0 | | Opcode 00 | | PC=PCH PC1=02 | Opcode 21 | |
| ALE | ALE=1 | ALE=0 | | ALE=1 | ALE=0 | | ALE=1 | ALE=0 | | |
| $IO/\overline{M}$ | | | $IO/\overline{M}=0$ | | | | | | | |
| $\overline{RD}$ | | $\overline{RD}=0$ | | | $\overline{RD}=0$ | | | $\overline{RD}=0$ | | |
| $\overline{WR}$ | | | $\overline{WR}=1$ | | | | | | | |
| $S_0, S_1$ | $S_0=1$ | $S_1=1$ | | | $S_1=1$ $S_0=0$ | | | | | |

→ Total execution time
⇒ opcode fetch + memory Read + memory Read
⇒ 4T + 3T + 3T
⇒ 4*0.33 + 3*0.33 + 3*0.3 ⇒ 3.33 μs

**4/**

→

**MOV M, B** → Number of required machine cycles and T-states

→ • opcode fetch : 4 T-states
• memory write : 3 states



|  | Opcode fetch | | | | Memory write | | |
|---|---|---|---|---|---|---|---|
|  | T₁ | T₂ | T₃ | T₄ | T₁ | T₂ | T₃ |

CLK

A₈-A₁₅ : PCH = 20, PC→PCH / unspecified decode opcode / PCH - 40, PC=PCH

AD₀-AD₇ : PCL=05 / Opcode 73 / DC₁-50 / Opcode AB

ALE : ALE=1 / ALE=0 / ALE=1 / ALE=0

IO/M̄ : IO/M̄=0 / IO/M̄=0

RD̄ : RD=0 / RD=1

WR̄ : WR=1 / WR=

S0, S1 : S0=1, S1=1 / S0=1, S1=0

Total Execution Time → opcode fetch + memory write
→ 4T + 3T
⇒ 4*0.33 + 3*a 33
⇒ 2.331 μs