TPS65217 Test B'd (Rev.A)

[1] Index

Rev	Date	Designer	Description
A	25.07.09	Ganghyeok Lim	Create design project

Index

Title	TPS65217_Test_Bd.PrjPcb
Rev	A
Doc	Index.SchDoc
Sheet # 1 of 5	Engineer Ganghyeok Lim
Date	2025-01-26

TPS65217 Test B'd (Rev.A)

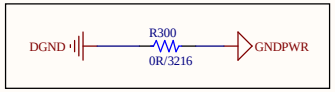
[2] Overview

Title	**TPS65217_Test_Bd.PrjPcb**	Rev *****
Doc	**Overview.SchDoc**	
Sheet # **2** of **5**	Engineer *****	
Date *****		

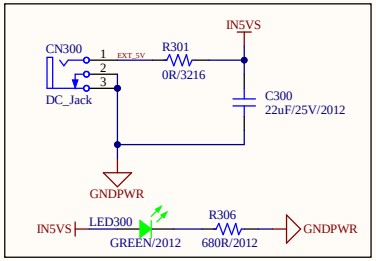
TPS65217 Test B'd (Rev.A)

[3] TPS65217DRSLR

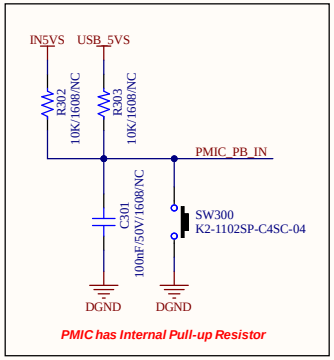
Digital GND



Power Connector (5V)

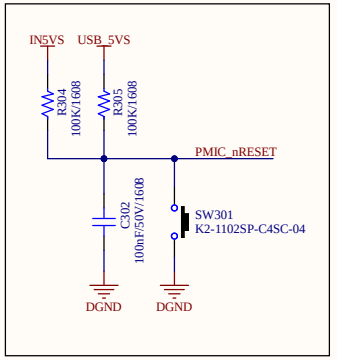


PMIC Power-On Button

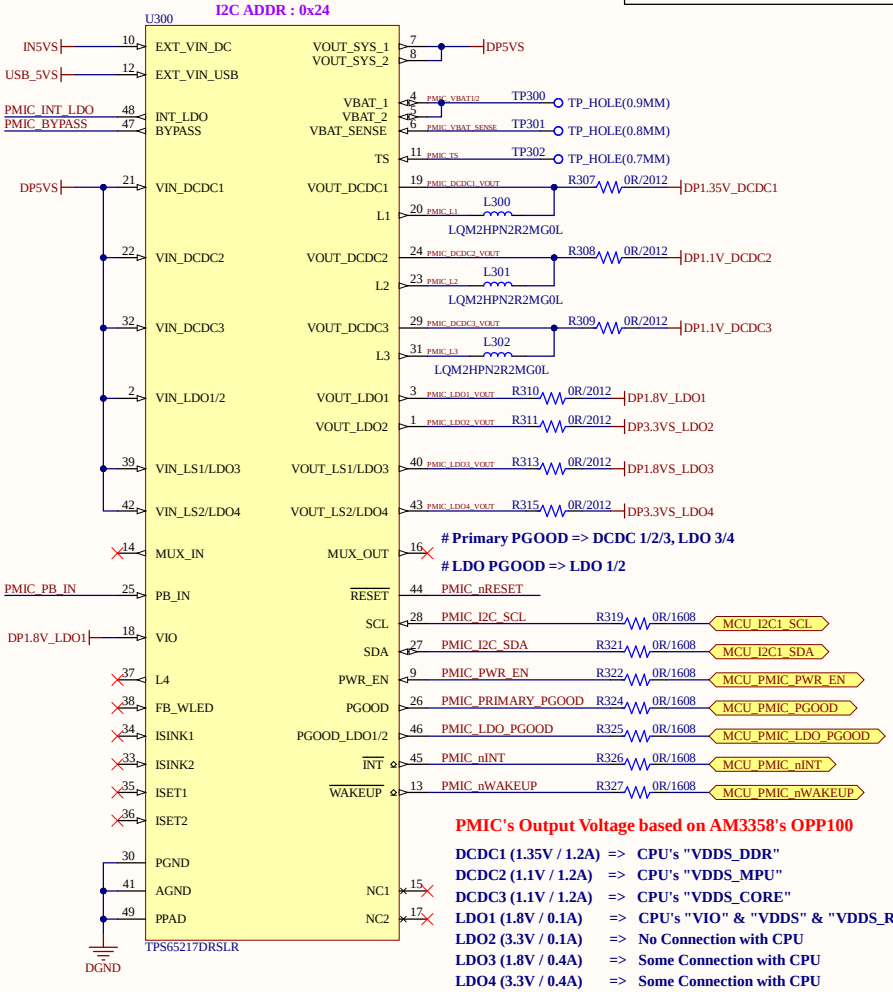


PMIC has Internal Pull-up Resistor

PMIC Reset Button



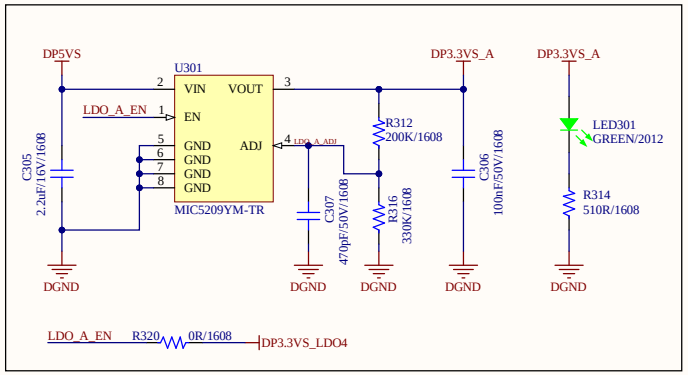
I2C ADDR : 0x24



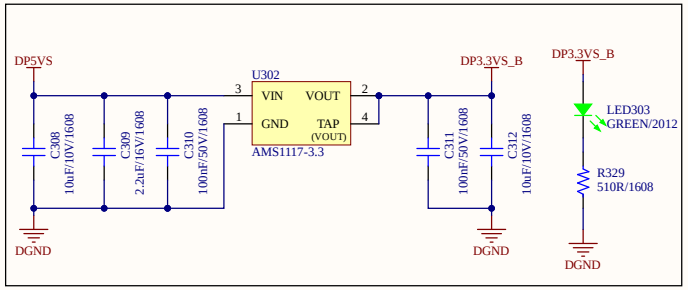
PMIC's Output Voltage based on AM3358's OPP100

DCDC1 (1.35V / 1.2A)	=>	CPU's "VDDS_DDR"
DCDC2 (1.1V / 1.2A)	=>	CPU's "VDDS_MPU"
DCDC3 (1.1V / 1.2A)	=>	CPU's "VDDS_CORE"
LDO1 (1.8V / 0.1A)	=>	CPU's "VIO" & "VDDS" & "VDDS_RTC"
LDO2 (3.3V / 0.1A)	=>	No Connection with CPU
LDO3 (1.8V / 0.4A)	=>	Some Connection with CPU
LDO4 (3.3V / 0.4A)	=>	Some Connection with CPU

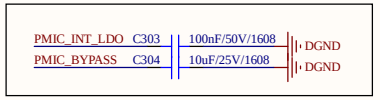
LDO (3.3V / 500mA)



LDO (3.3V / 1A)

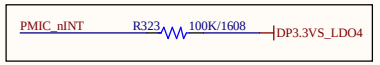


INT LDO / BYPASS Pin

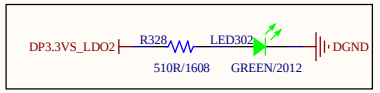


I2C Pull-up Resistor

nINT Pull-up



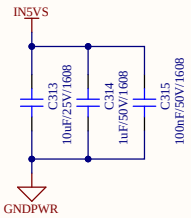
PMIC Power LED



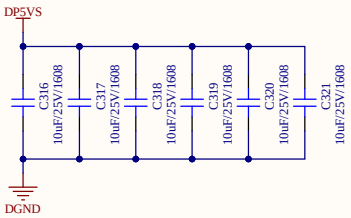
Rail	Output [V]	Sequence (Strobe)
DCDC1	1.35 [V] / 1.2 [A]	1
DCDC2	1.1 [V] / 1.2 [A]	5
DCDC3	1.1 [V] / 1.2 [A]	5
LDO1	1.8 [V] / 0.1 [A]	15
LDO2	3.3 [V] / 0.1 [A]	3
LS1 or LDO3	1.8 [V] / 0.4 [A]	2
LS2 or LDO4	3.3 [V] / 0.4 [A]	4

Decoupling Capacitors

Decap for IN5VS

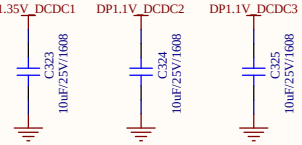


Decap for DP5VS

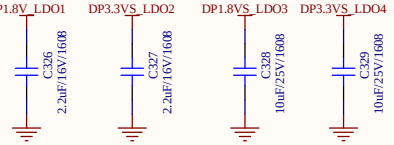


Decap for USB_5VS

Decap for DCDC 1/2/3



Decap for LDO 1~4

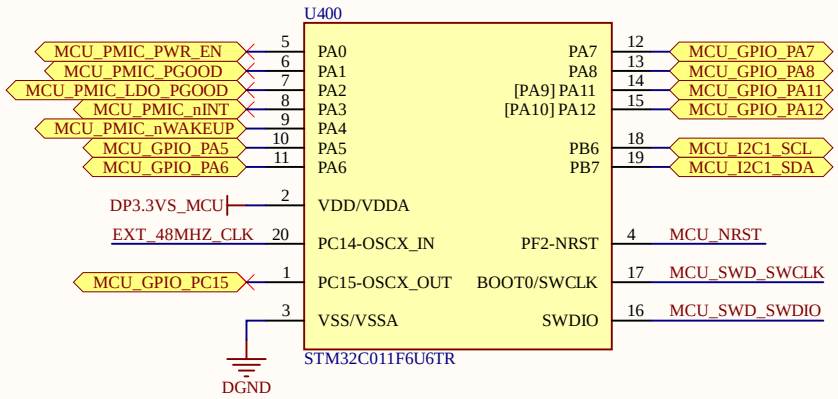


Place Decaps Closely to Each Pin of PMIC

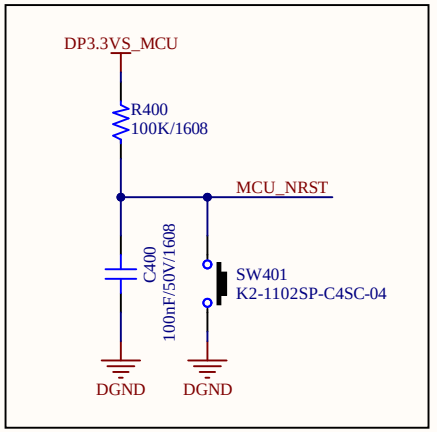
Title	TPS65217_Test_Bd.PrjPcb
Rev	*
Doc	TPS65217DRSLR.SchDoc
Sheet # 3 of 5	Engineer *
Date *	

TPS65217 Test B'd (Rev.A)

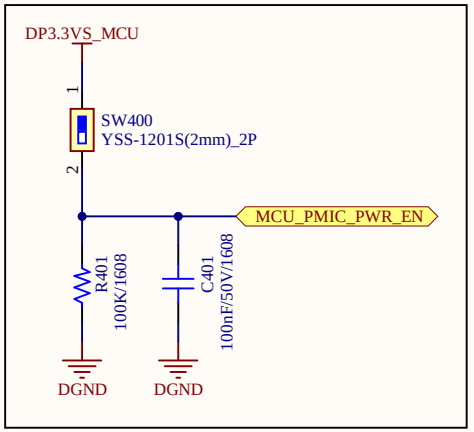
[4] MCU



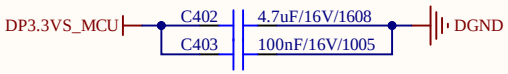
MCU RESET



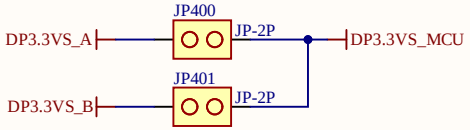
PMIC Power Enable



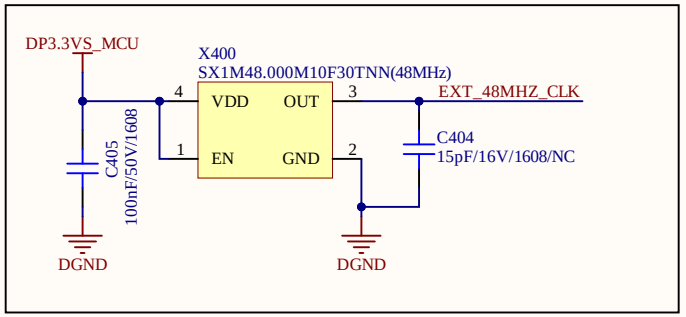
Decoupling Capacitors



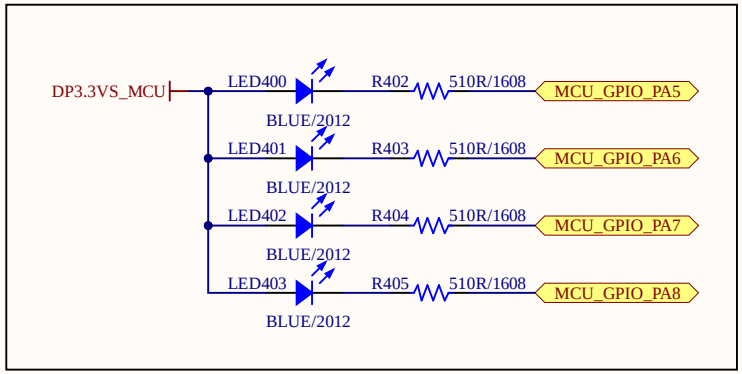
LDO Selection



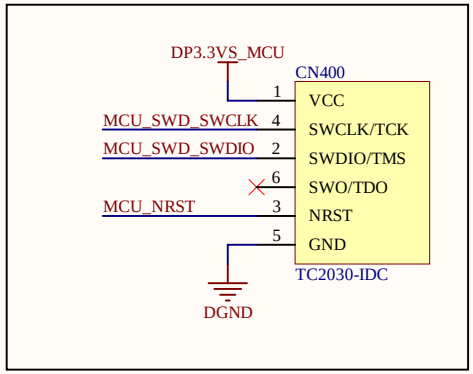
Oscillator (48MHz)



MCU STATUS LED



ST-LINK Connector

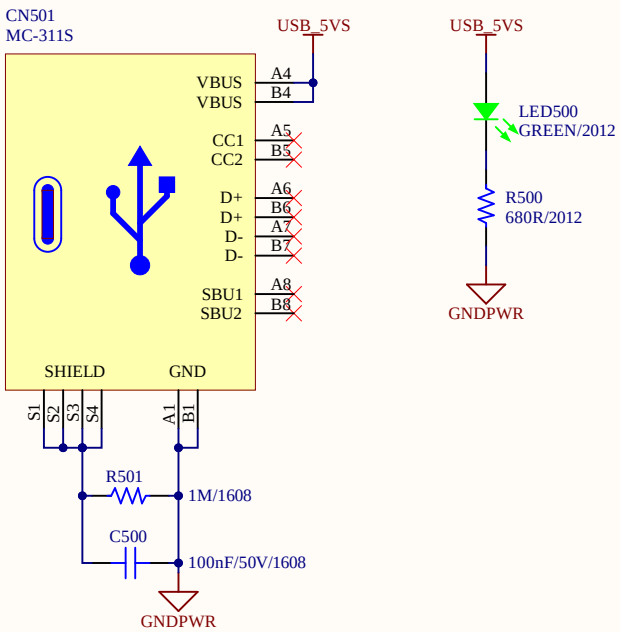


Title	**TPS65217_Test_Bd.PrjPcb**	Rev *
Doc	**MCU.SchDoc**	
Sheet # **4** of **5**	Engineer *	
Date *		

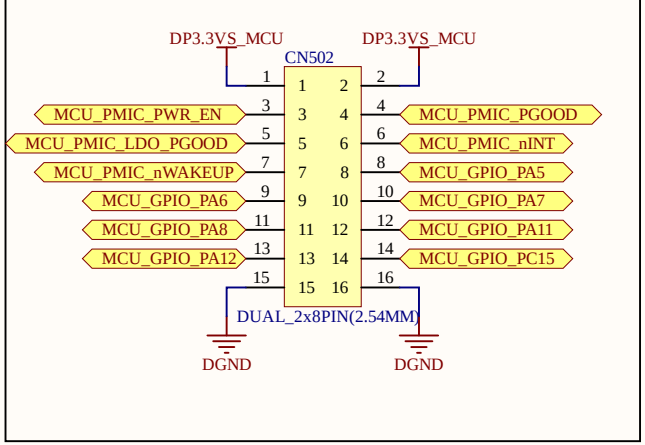
TPS65217 Test B'd (Rev.A)

[5] Connector

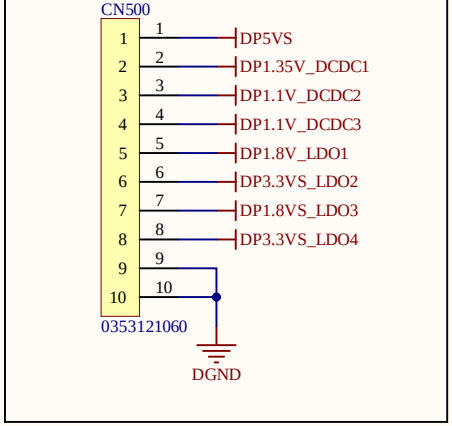
USB Connector (Type-C)



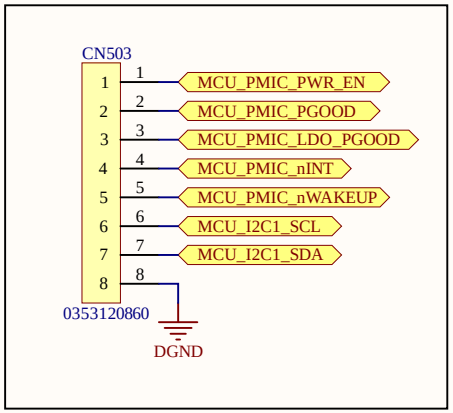
MCU GPIO Connector



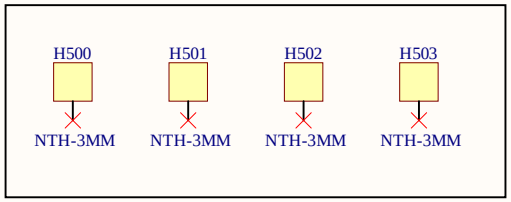
PMIC Output Rails



PMIC Status Signals



Mount Holes



Title	**TPS65217_Test_Bd.PrjPcb**	Rev *
Doc	**Connector.SchDoc**	
Sheet # **5** of **5**	Engineer *	
Date *		

# Layer Information	
L1	Top (Signal / GND)
L2	GND
L3	Power
L4	Signal / GND
L5	GND
L6	Bottom (Signal / GND)

# PCB Specification (JLCPCB)		
No	Category	Selection
1	Base Material	FR-4
2	Layer #	6 - Layer
3	Dimension	220(mm) * 160(mm)
4	Thickness	1.6T
5	Color	Black
6	Material Type	FR-4 TG155
7	Surface Finish	ENIG
8	Gold Thickness	2 U"
9	Outer Copper Weight	1 oz
10	Inner Copper Weight	0.5 oz
11	Impedance Control	No
12	Layer Stack-up	Default
13	Via Covering	Epoxy Filled & Capped
14	Min. Via Hole Size / Diameter	Hole : 0.2mm / Diameter : 0.35mm
15	Board Outline Tolerance	±0.2mm (Regular)
16	Confirm Production File	No
17	Remove Order Number	Yes
18	Flying Probe Test	Fully Test
19	Gold Fingers	No
20	30° Finger Chamfered	No
21	Castellated Holes	No
22	Edge Plating	No