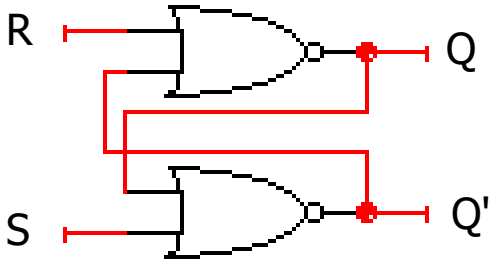
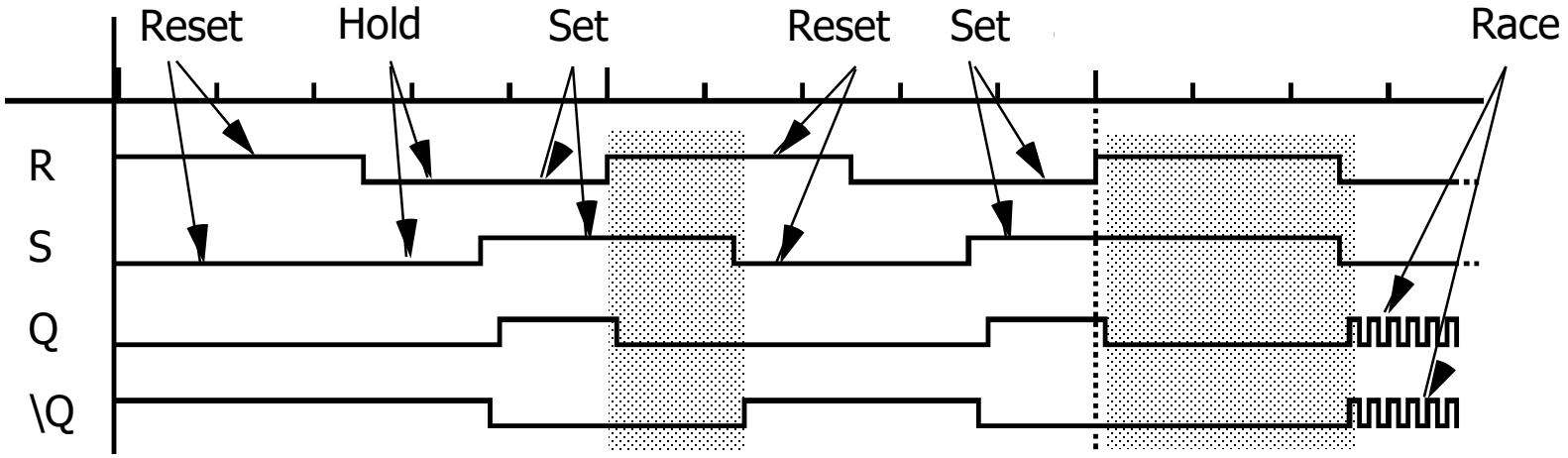
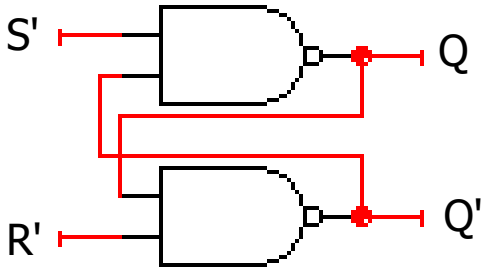
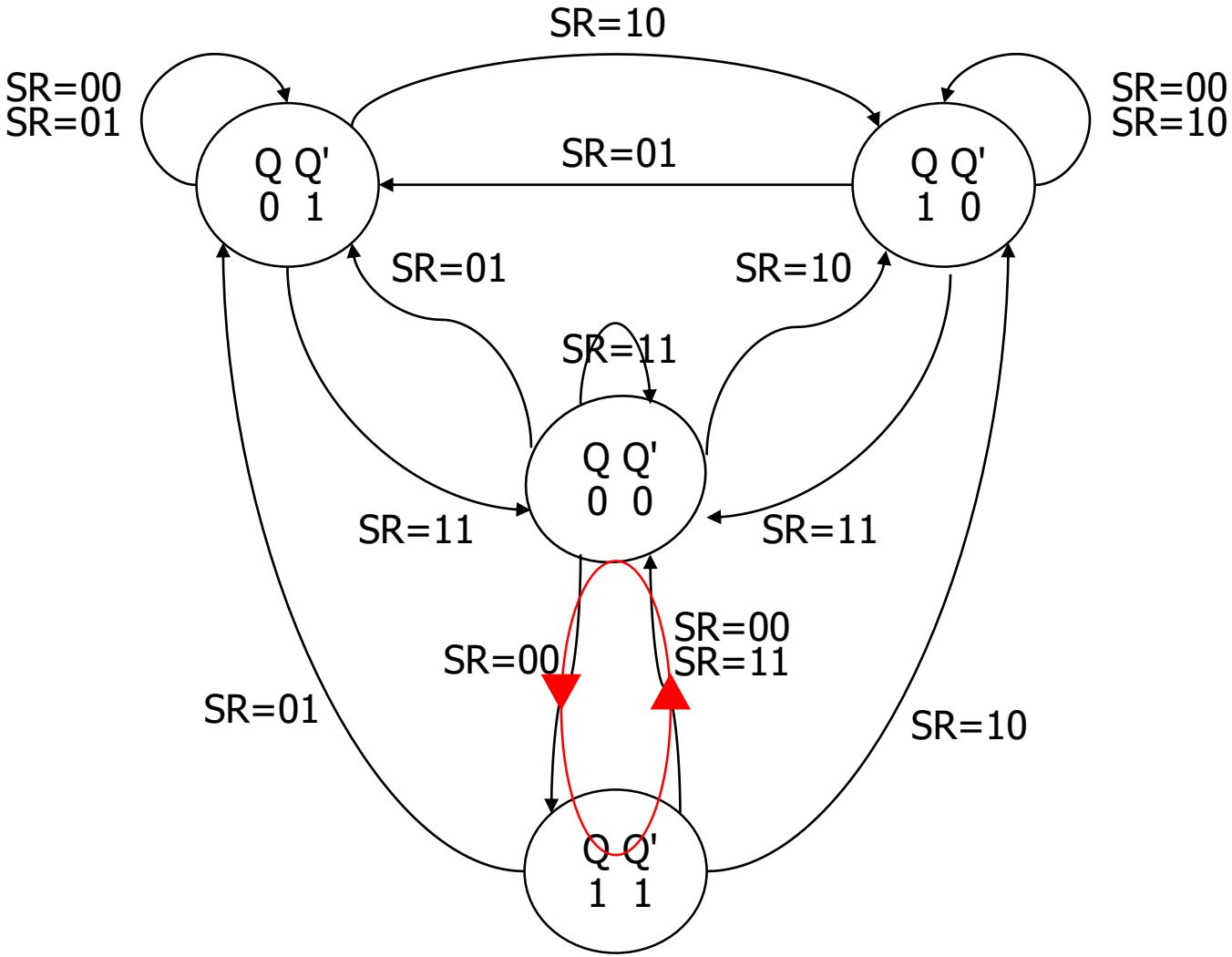
Sequential Circuits

SR Latch

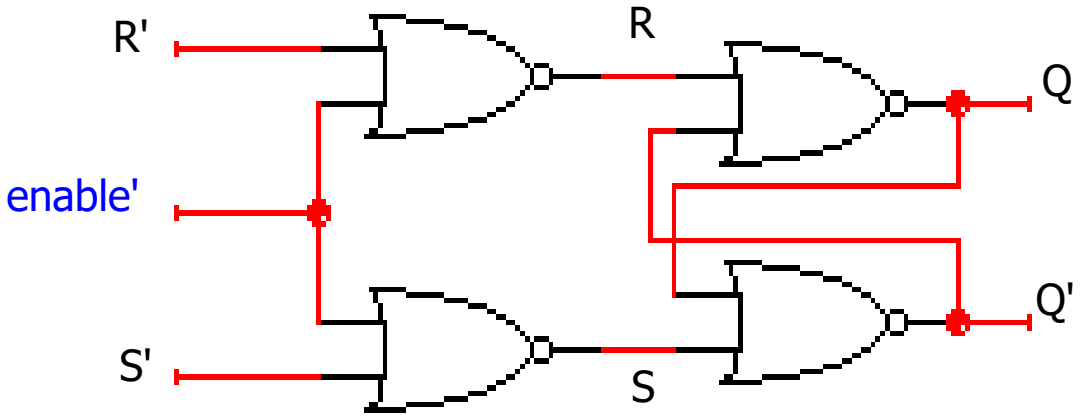


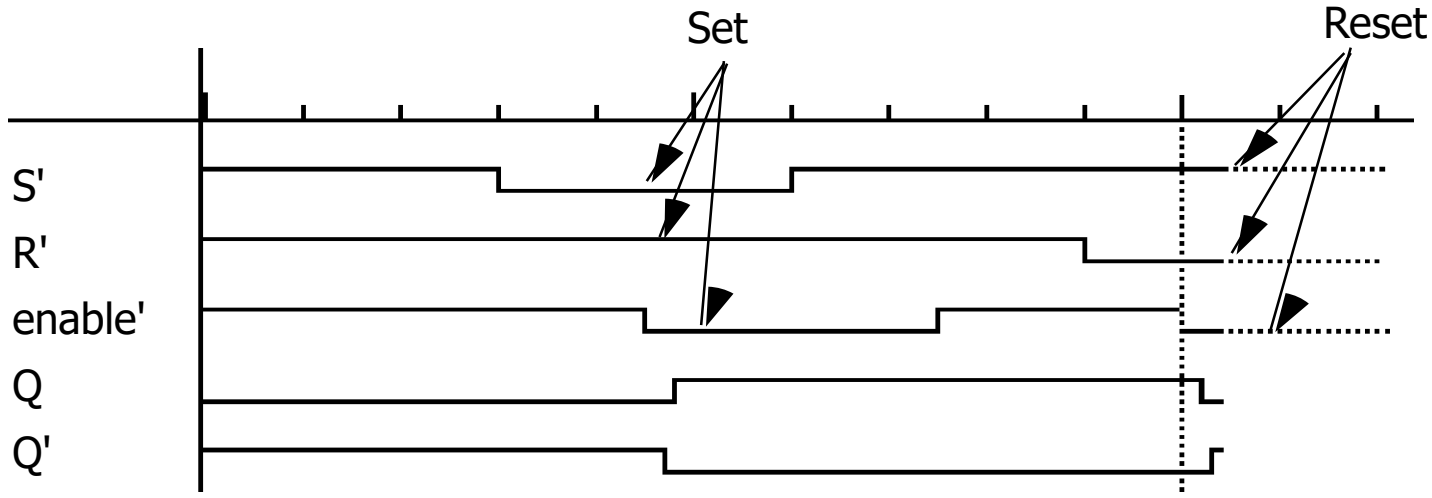




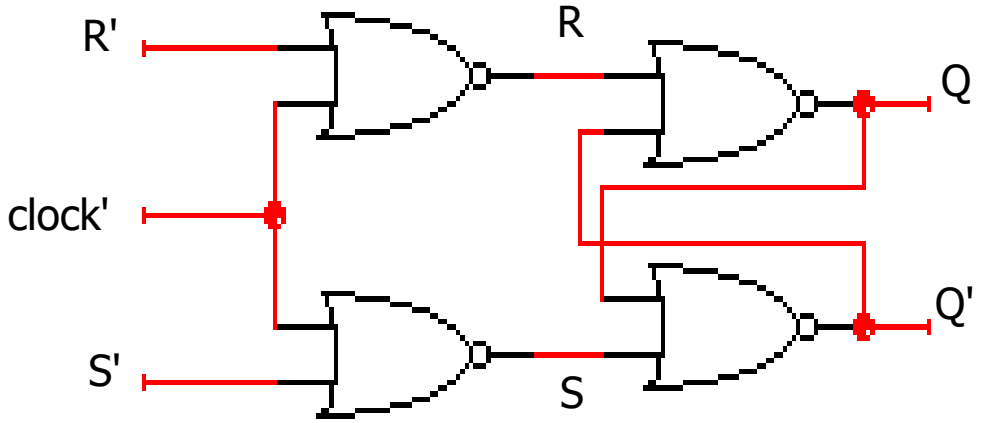

SR=10
SR=00
SR=01
Q Q'
0 1
SR=01
Q Q'
1 0
SR=00
SR=10
SR=01
SR=10
SR=11
Q Q'
0 0
SR=11
SR=11
SR=00
SR=11
SR=00
SR=01
SR=10
Q Q'
1 1

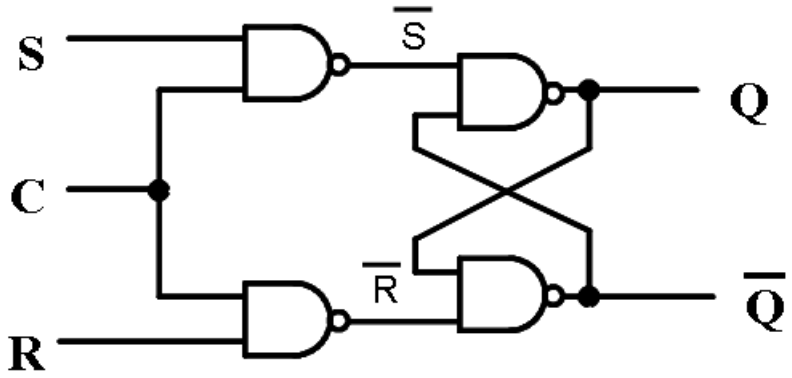
Gated SR Latch





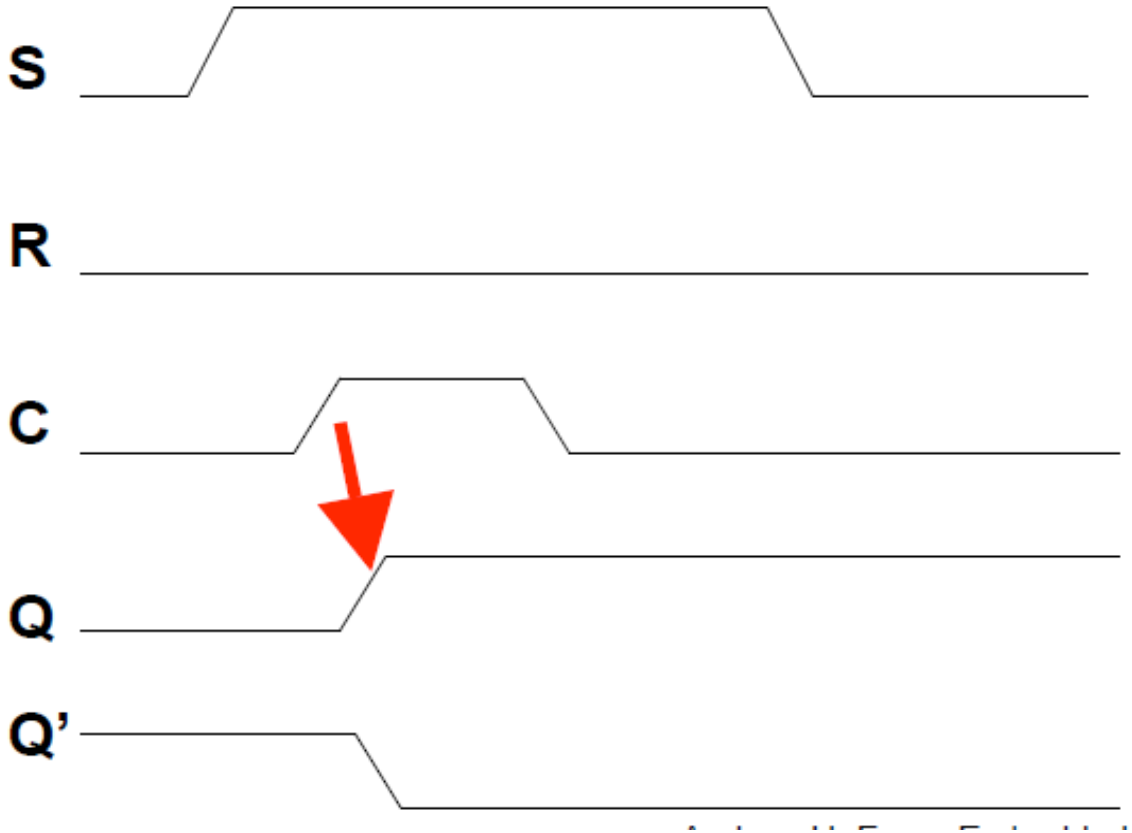
Using clock as gated signal





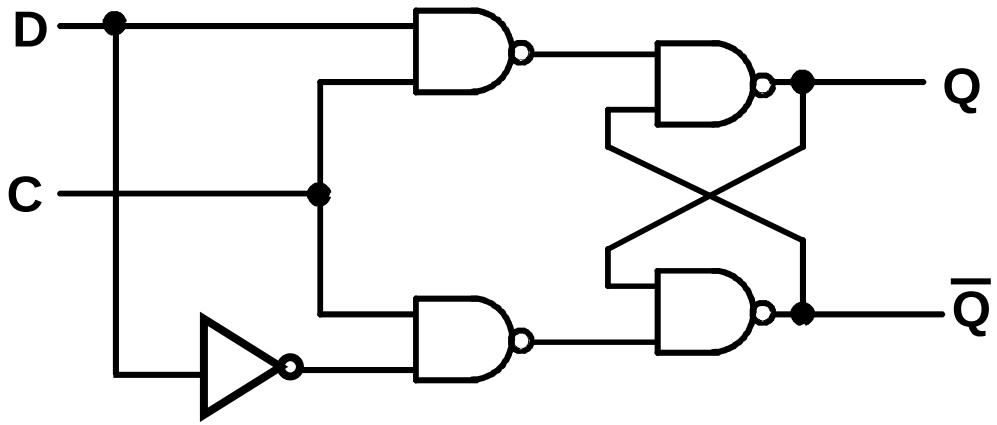
C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; Set state
1	1	1	Undefined

Clocked SR Latch

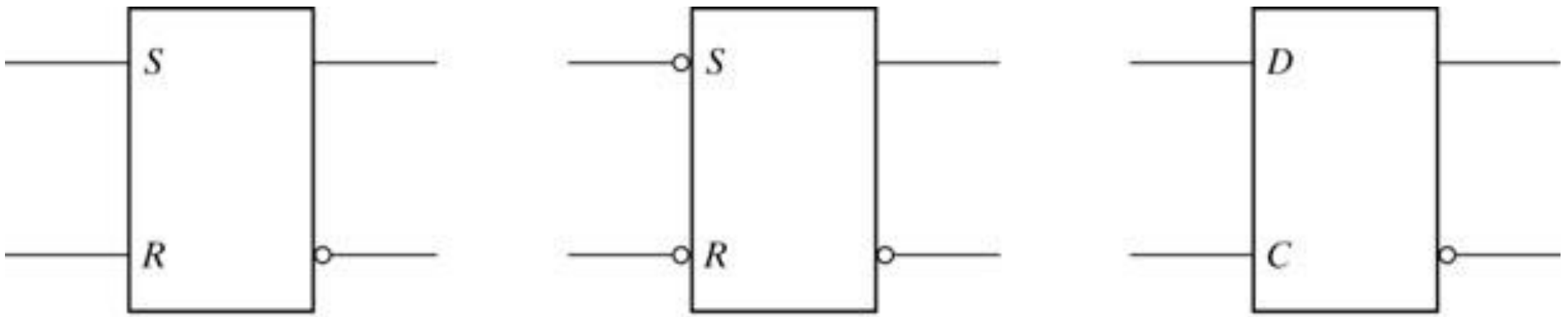


Q and Q' flip state when the clock is high

The D Latch

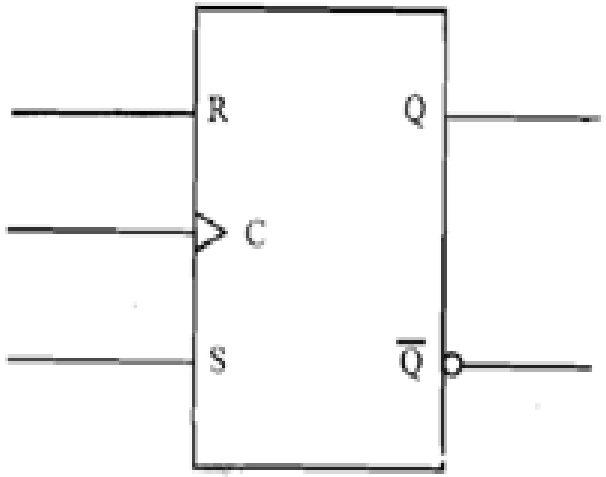


C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state



SR $\overline{S}\overline{R}$ D

Fig. 5-7 Graphic Symbols for Latches



(a) Graphic Symbol