NAME - ARPAN MANDAL

ROLL - 001910501061

3. My Roll no. is -61 so,

X = 6 Y = 1 i = Y + 8 = 1 + 8 = 1

```
LXI H, 4061 H
LDA 4461 H
MOV B, A
Loop: MOV A, M
      ANI 02 H
      JNZ SKIP
      MOV A, M
      ADD C
      JNC SKIP2
      INR D
SKIP2: MOV C, A
SKIP: INX H
      DCR B
      JNZ Loop
      MOV A, C
      STA 4561 H
      MOV A, D
      STA 4562 H
      HLT
```

2048 12 $2^{10} = 1000$

2. My ROLL = 61

So, Y = 1

Address range:

we have to interface 4K byte address:

So we need 12 address lines to $A_0 - A_{11}$ ($2^{12} = 4K$)

starting address :- 1000H.

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

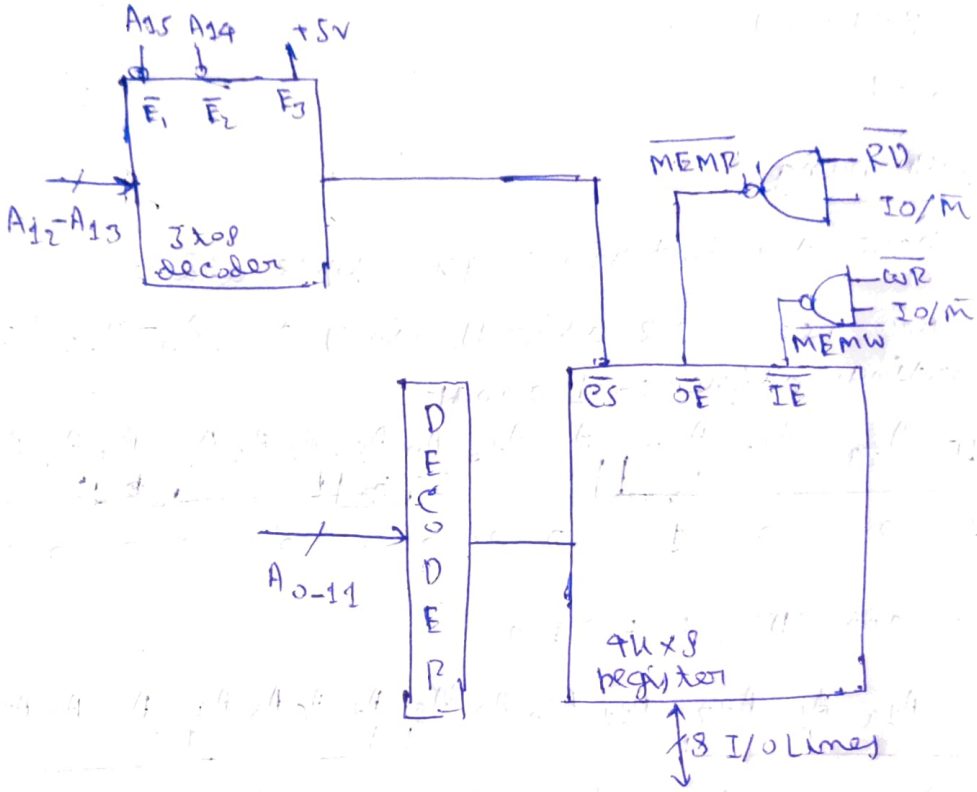
end address:- 1FFFH

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Address decoding technique

we have to use 12 address lines to address the memory. those address lines are $A_0 - A_{11}$, others $A_{12} - A_{15}$ will act as chip select signal. Now we have to pass those 12 lines ($A_0 - A_{11}$) to a decoder. The output will create 2^{12} lines, to address memory. The $\overline{MEMW}$ (memory write) and $\overline{MEMR}$ (memory read) will also add to $\overline{IE}$ and $\overline{OE}$.

For chip select lines we can either use a 4 input NAND gate or a decoder, the block diagram is-



1) (i) LHLD 2500H :-

full from of LHLD is load H-L pair direct, actually the address stores in H register.

So) LHLD 2500H means [2500H] stores in L register and [2501H] stores in H Register

eg

LHLD 2500H [L] ← 2500H
[H] ← 2501H

(ii) RLC - Rotate Accumulator Right, The content of the accumulator is rotated Left by one bit. The seventh bit of accumulator is moved to carry bit as well as the zero bit of the accumulator

only CS flag is affected.

So, $[A_{n+1}] \leftarrow [A_n]$, $[A_0] \leftarrow [A_7]$, $CS \leftarrow [A_7]$

e.g.:- Suppose accumulator content is 02 H

RLC → accumulator content becomes → 04 H

and carry becomes 0