B. E. Computer Science and Engineering Second Year First Semester Exam – 2022

DIGITAL LOGIC AND CIRCUITS

Time: 3 Hrs. **Full Marks: 70**

Answer all parts of a question in contiguous locations.

1. [CO3] Characteristic equation of J-K flip-flop is: **2**

a) $Q(t+1) = Q'(t) . J + Q(t) . K'$
b) $Q(t+1) = Q (t) . J' + Q'(t) . K'$
c) $Q(t+1) = Q (t) . J + Q'(t) . K'$
d) $Q(t+1) = Q (t) . J' + Q'(t) . K$

2. [CO3] Tick the correct statement(s): **2**

a) Serial adders are slow, requires less hardware and the carry propagation time is fixed.
b) Serial adders are slow, requires less hardware but the carry propagation time varies.
c) Parallel adders are fast, requires more hardware but the carry propagation time varies.
d) None of the above statements is true

3. [CO5] A 4-bit A / D converter implemented with parallel comparators require **2**

a) 4 nos. of comparators and 4 nos. of D flip-flops
b) 8 nos. of comparators and 8 nos. of D flip-flops
c) 12 nos. of comparators and 12 nos. of D flip-flops
d) 16 nos. of comparators and 16 nos. of D flip-flops

4. [CO5] Tick the correct statement(s): **2**

a) Weighted register type DAC is more accurate than R-2R Ladder DAC
b) R-2R Ladder DAC is more accurate than Weighted register type DAC
c) Both of them have the same accuracy.
d) R-2R Ladder DAC can be easily fabricated as an IC chip

5. [CO4] Tick the correct statement(s): **2**

a) Resistor Transistor Logic (RTL) suffers from current hogging.
b) For RTL fan-in and fan-out is limited
c) For RTL propagation delay is a function fan-in and fan-out.
d) Diode Transistor Logic (DTL) has lesser number of fan-in and fan-out.

6. [CO4] For 555 timer, tick the correct statement(s): **2**

a) Two comparator circuits control its function.
b) In astable mode, duty cycle of the waveform is controlled by one external capacitor and one external resistor.
c) monostable mode, timing is controlled by one external capacitor and one external resistor.
d) The output buffer contains a high value capacitor.

7. [CO3] The output of the right-most flip-flop of a 4-bit ring counter is used as the clock input to a 4-bit switch tail ring counter. If the frequency of the clock input is 160 Hz, what will be frequency of the output of the right-most flip-flop of the switch tail ring counter? **2**

a) 640 Hz
b) 40 Hz
c) 320 Hz
d) 5 Hz

8. [CO3] A 4-to-1 MUX realizes a 3-variable function f(x,y,z) = xy+xz', which of the following is correct? **2**

a) $I_0 = x, I_1 = 0, I_2 = y, I_3 = z$
b) $I_0 = x, I_1 = 0, I_2 = y, I_3 = z$
c) $I_0 = x, I_1 = 0, I_2 = y, I_3 = z$
d) $I_0 = x, I_1 = 0, I_2 = y, I_3 = z$

9. [CO1] Let a receiver receives a Hamming coded bit pattern 0011011. It is checked for any possible error during transmission. **2**

a) Received bit pattern is correct.
b) Error occurred at the 6^{th} bit position and correct one is 0011001
c) Error occurred at the 3^{rd} bit position and correct one is 0001011
d) Error occurred at the 4^{th} bit position and correct one is 0010011

10. [CO2] Let f(A,B,C,D) = A ⊕ B ⊕ C ⊕ D, then which one of the following is correct? **2**

a) f(A,B,C,D) = $\sum(1,2,6,8,10,12,13,14)$
b) f(A,B,C,D) = $\sum(1,2,4,7,8,11,13,14)$
c) f(A,B,C,D) = $\sum(2,4,5,6,12,13,14,15)$
d) f(A,B,C,D) = $\sum(2,4,5,6,12,13,14,15)$

11. [CO1] Let f(A,B,C,) = ((A(AB)')' (B(AB)')')', then which one of the following is correct? **2**

a) f(A,B,C,) = ((A' + AB) (B' + A'B'))'
b) f(A,B,C,) = ((A + B)' + (A' + B'))'
c) f(A,B,C,) = ((A' + A'B') (B' + AB))'
d) f(A,B,C,) = ((A + AB) (B' + A'B'))'

12. [CO3] A sequential circuit has two pulse inputs x_1 and x_2. The output of the circuit z becomes 1 when one or more x_1 pulses are followed by two x_2 pulses. The output then remains 1 for all subsequent x_2 pulses until an x_1 pulse occurs. **12**

a) Draw the state diagram and corresponding minimal state table.
b) Synthesize the circuit using R-S flip-flops.

13. [CO3] Given the following flow table of an asynchronous circuit. **12**

	Y_1Y_2			
	x_1x_2			
y_1y_2	00	01	11	10
00	00	11	00	11
01	11	01	11	11
11	11	11	00	11
10	00	10	11	11

a) Mark all the stable states.
b) Find all the races and indicate which of them are critical and which are not.
c) Is there any infinite race cycle?
d) Suggest a new set of state assignment so that the new flow table contains no critical races.

14. [CO2] Minimize the following Boolean function using Quine – McCluskey. **12**
F(A, B, C, D, E) = Σ (0,4,6,11,13,15,21,25,29) + d (2,9,17,27,31)
Show all steps clearly.

15. [CO3] Design a BCD to Excess – 3 encoder using multiplexers. Specify the type of multiplexers and number of such multiplexers to be used in the design. **12**
