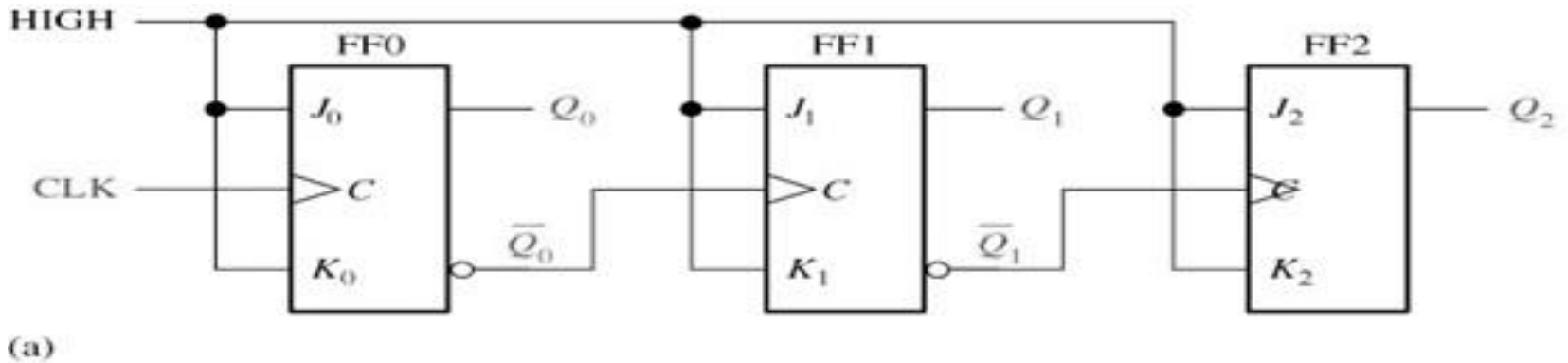
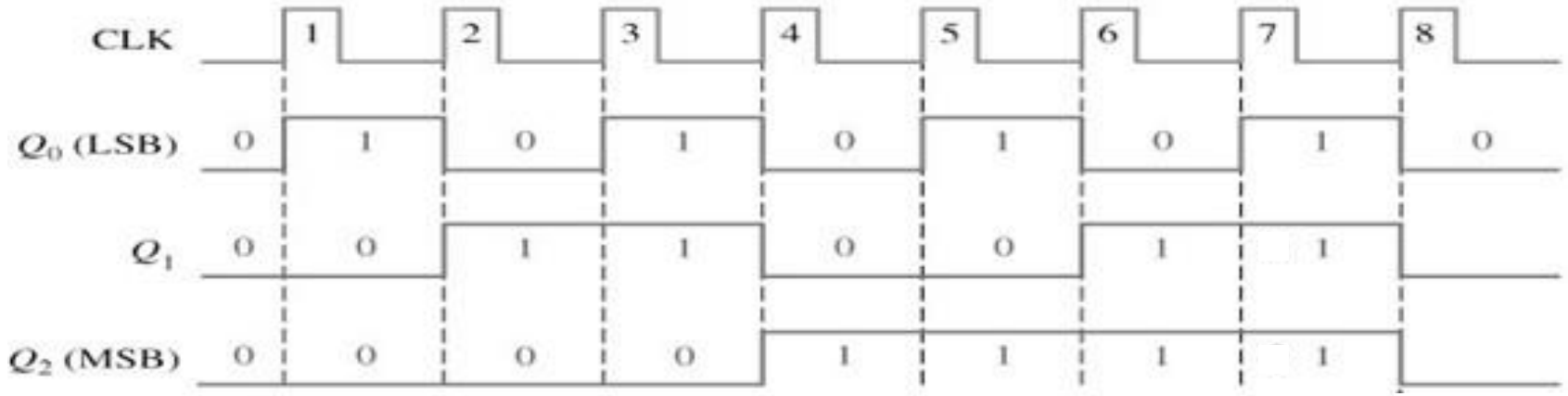
Sequential Circuit Design

3-bit asynchronous (ripple) binary counter

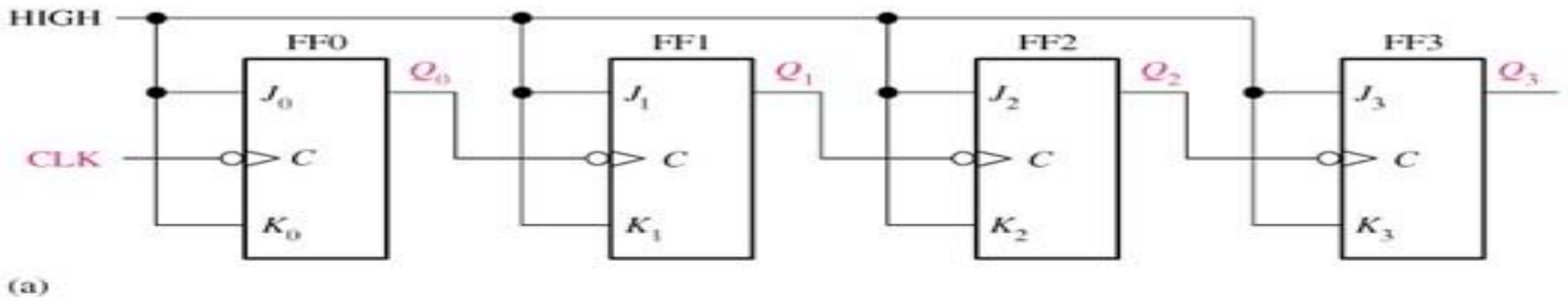


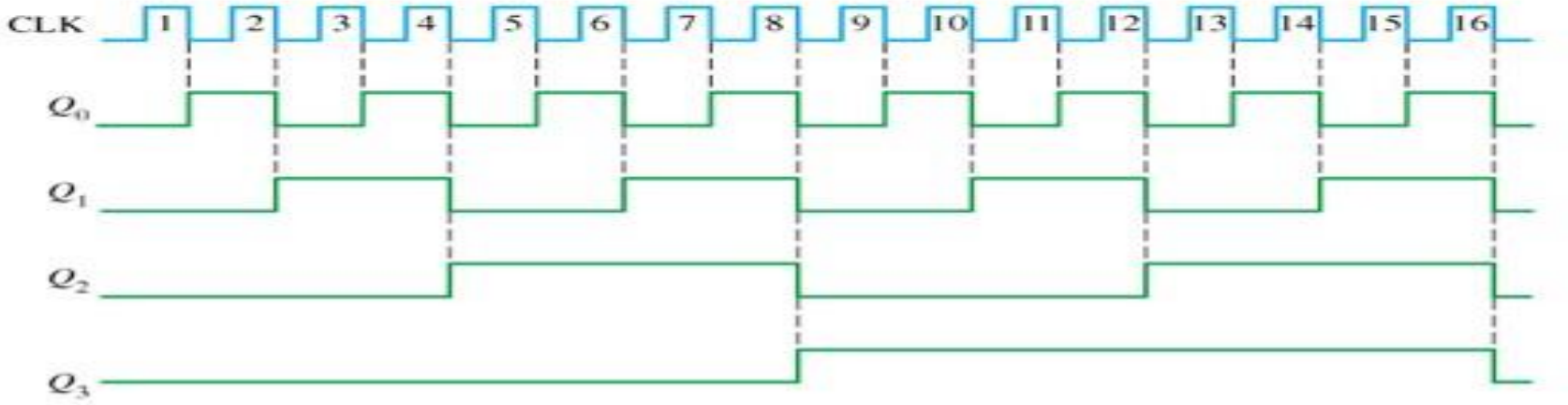
(a)



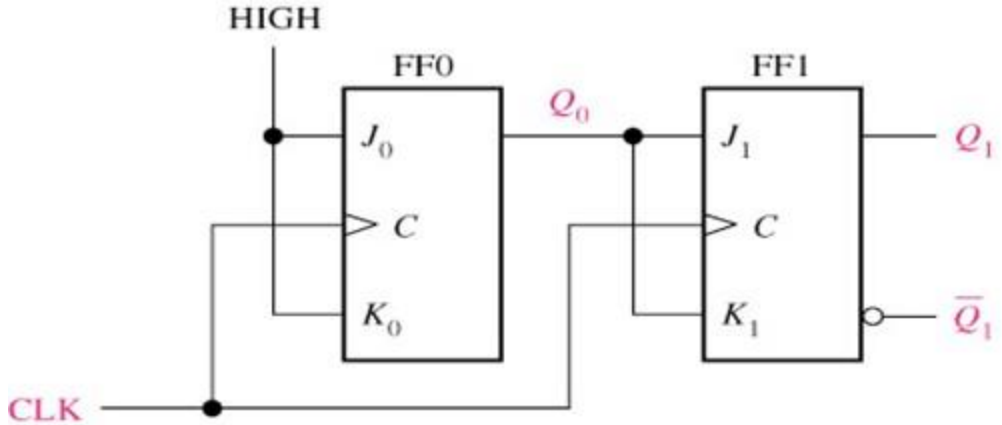
(b)

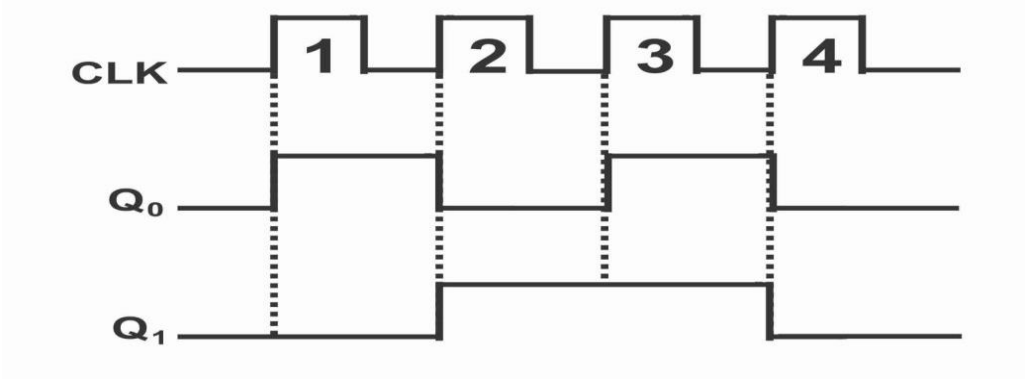
4-bit asynchronous (ripple) binary counter
(negative edge triggered)



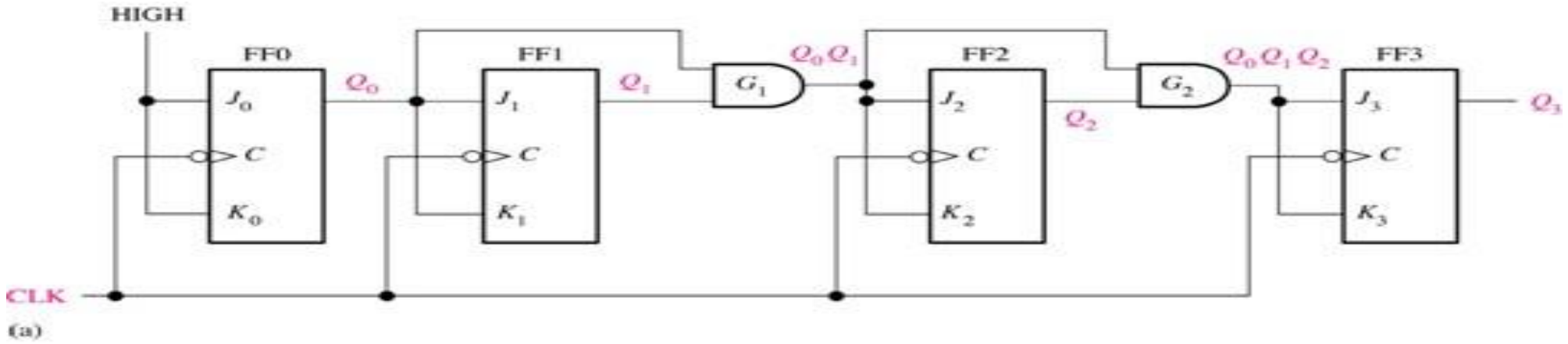


2-bit synchronous binary counter

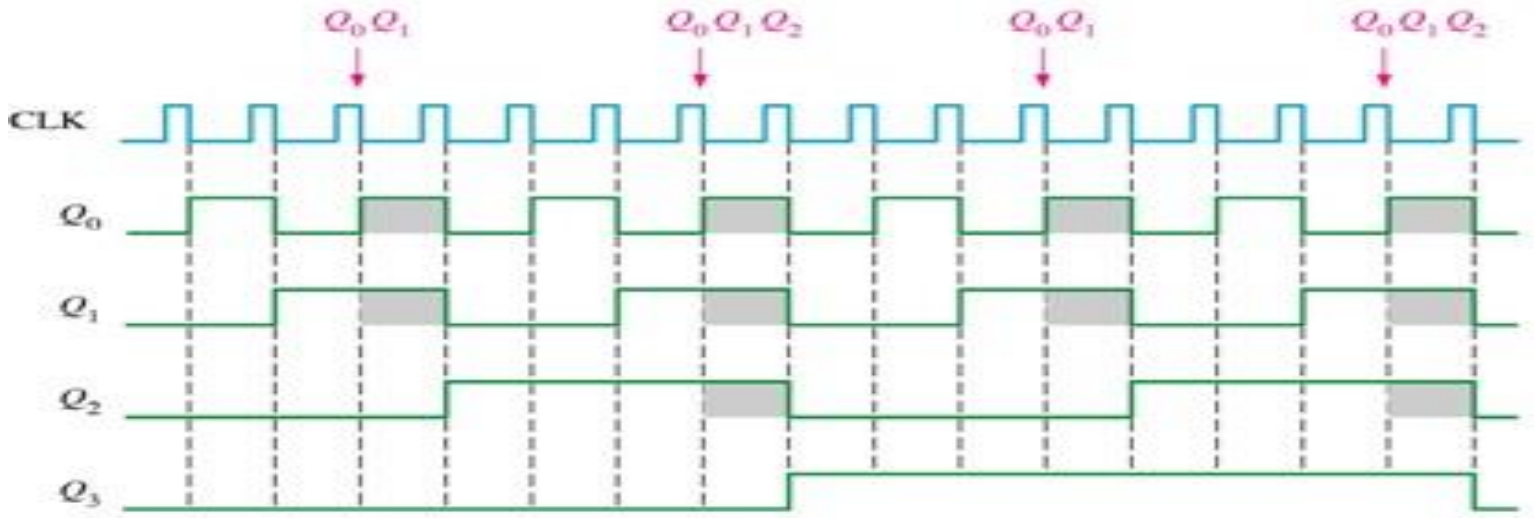




4-bit synchronous binary counter
(negative edge triggered)



(a)



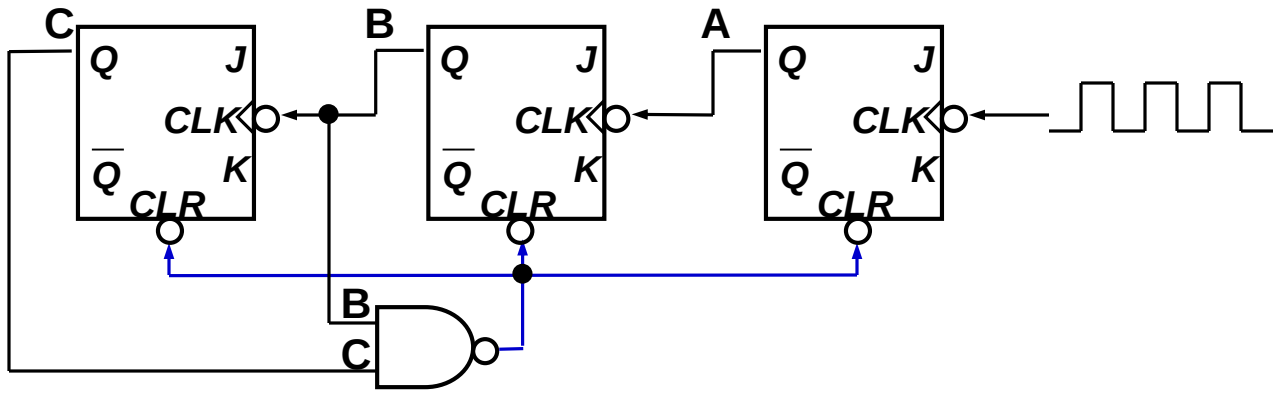
- The number of flip-flops determines the count limit or number of states.

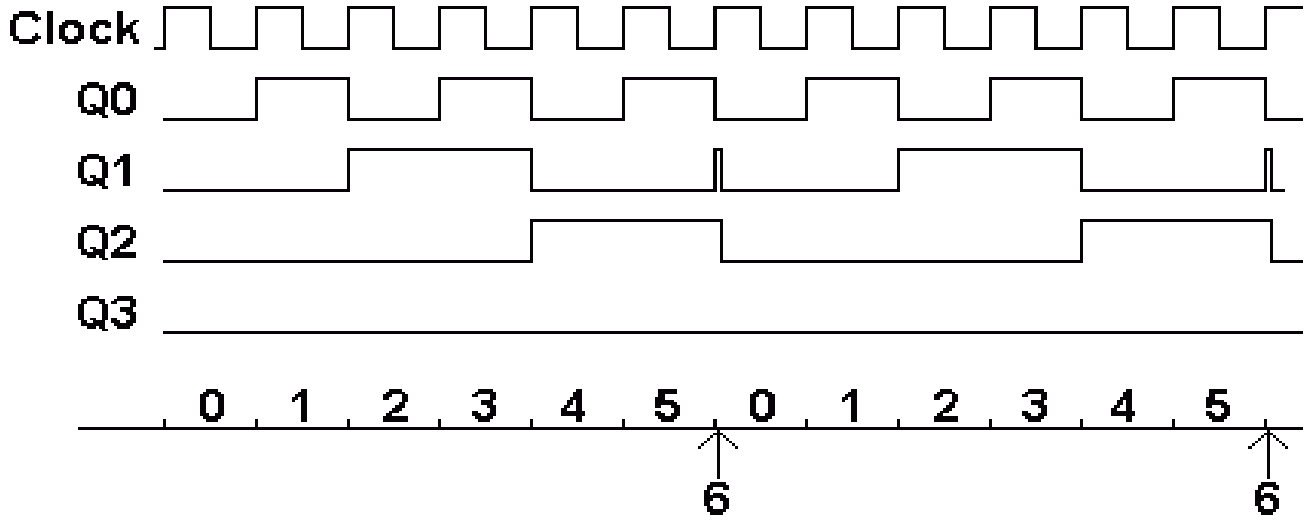
  (STATES = $2^{\text{\# of flip flops}}$)

- Number of states used is called the MODULUS
- A Modulus-12 counter would count from 0 (0000) to 11 (1011) and requires four flip-flops (16 states - 12 used).

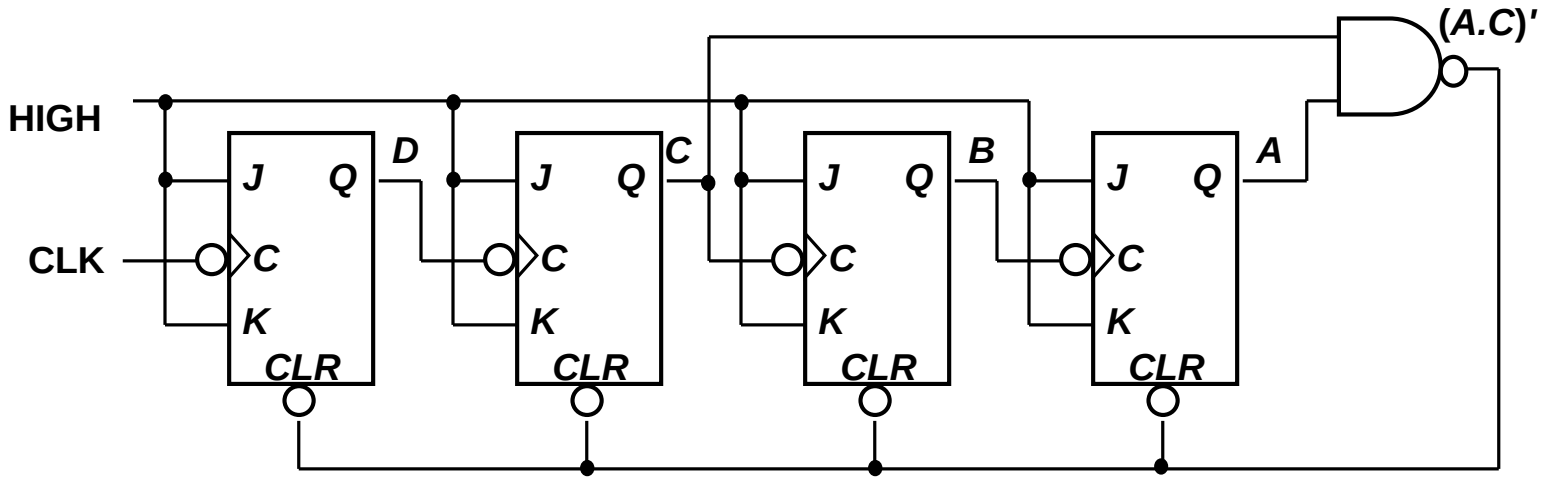
Modulo-6 counter (truncated counter)

All *J*, *K* inputs are 1 (HIGH).

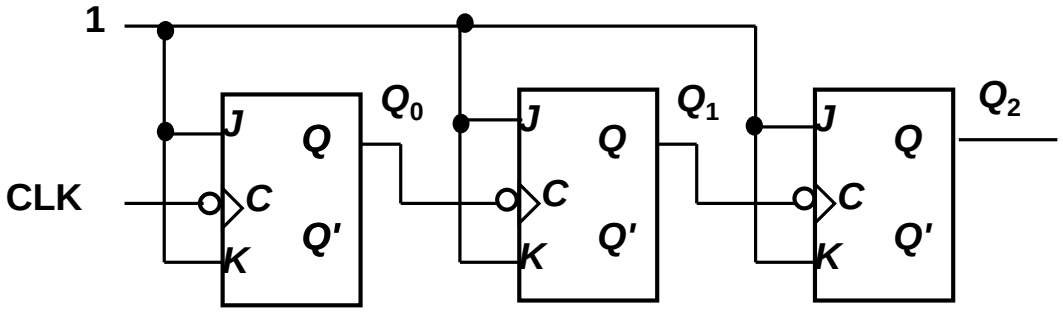




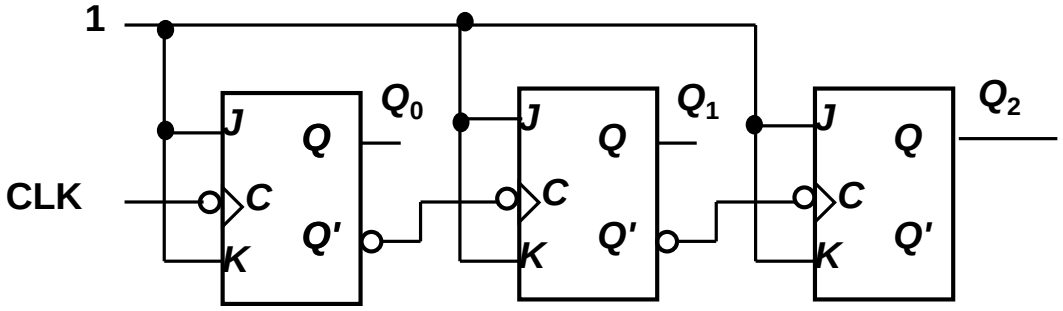
Decade counters (or BCD counters)



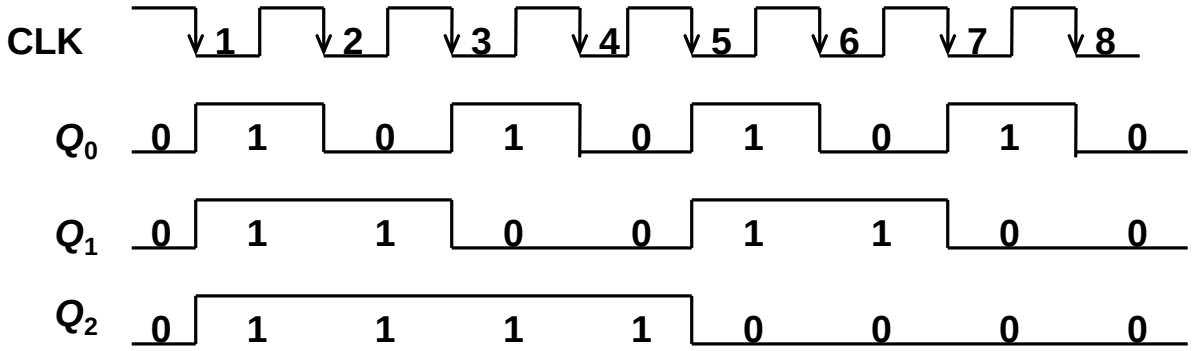
Up and down counter



3-bit binary up counter



3-bit binary down counter



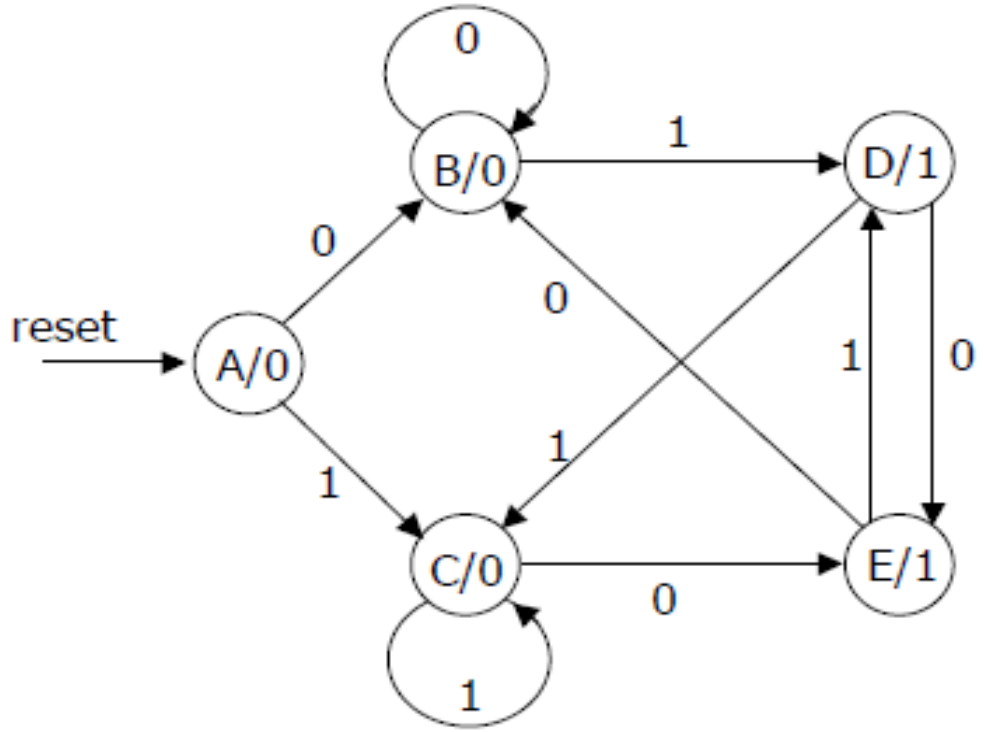
Sequential Circuit Design

- The most general model of a sequential circuit has inputs, outputs, and internal states.
- Mealy model and Moore model
  - They differ in the way the output is generated.
  - In the Mealy model, the output is a function of both the present state and input.
    - Outputs have immediate reaction to inputs
    - As inputs change, so does next state, doesn’t commit until clocking event
  - In the Moore model, the output is a function of the present state only.
    - Output does not react immediately to input change

Specifying Outputs for a Moore Machine

Output is only function of state

- Specify in state bubble in state diagram
- Example: sequence detector for 01 or 10

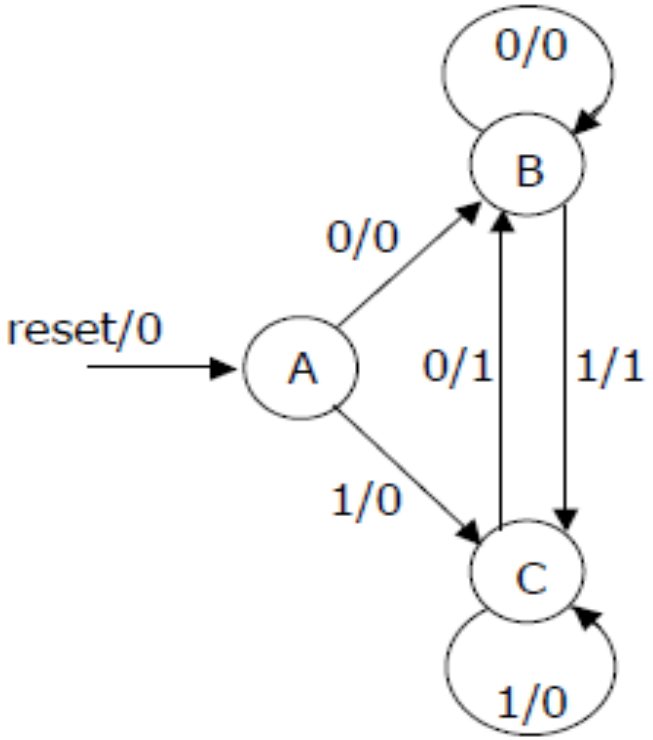


reset	input	current state	next state	output
1	–	–	A	
0	0	A	B	0
0	1	A	C	0
0	0	B	B	0
0	1	B	D	0
0	0	C	E	0
0	1	C	C	0
0	0	D	E	1
0	1	D	C	1
0	0	E	B	1
0	1	E	D	1

Specifying Outputs for a Mealy Machine

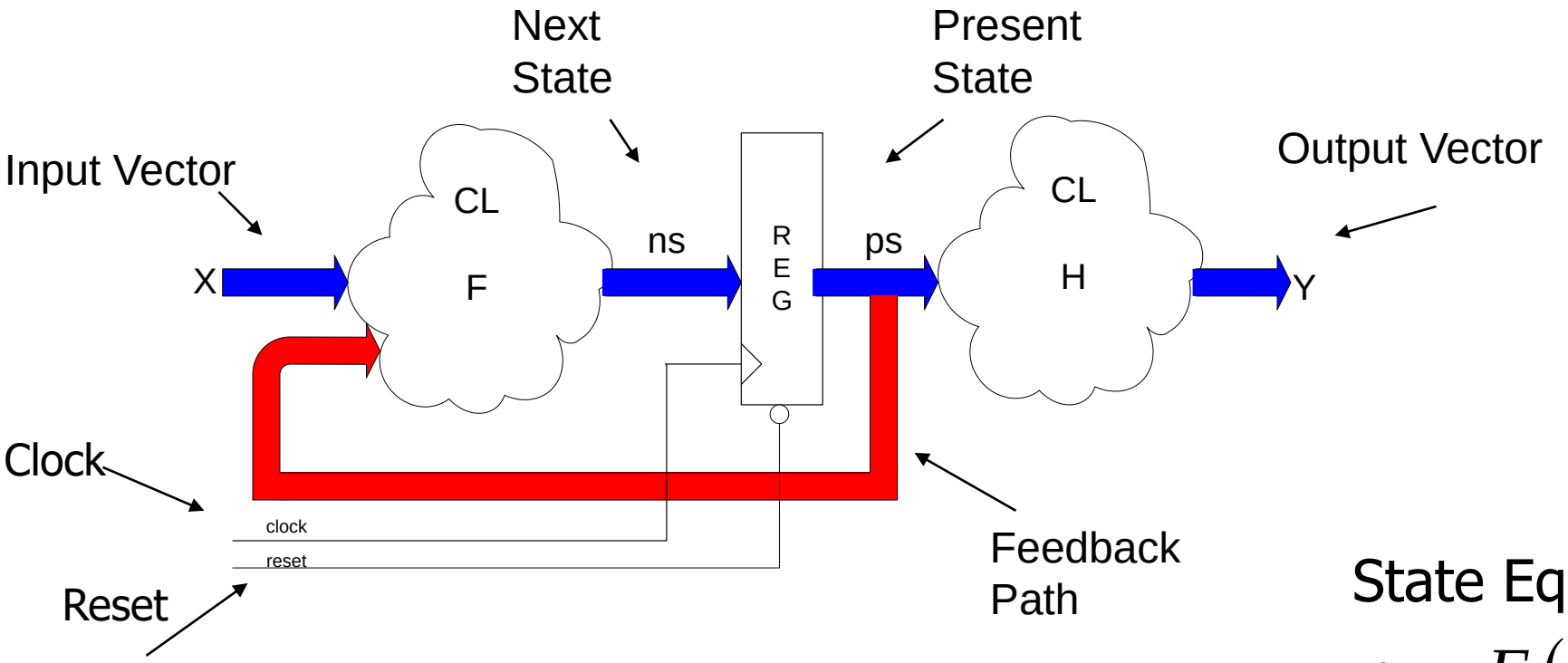
Output is function of state and inputs

- Specify output on transition arc between states
- Example: sequence detector for 01 or 10



reset	input	current state	next state	output
1	–	–	A	0
0	0	A	B	0
0	1	A	C	0
0	0	B	B	0
0	1	B	C	1
0	0	C	B	1
0	1	C	C	0

Moore FSM General Block Diagram



CL= Combinational Logic Cloud

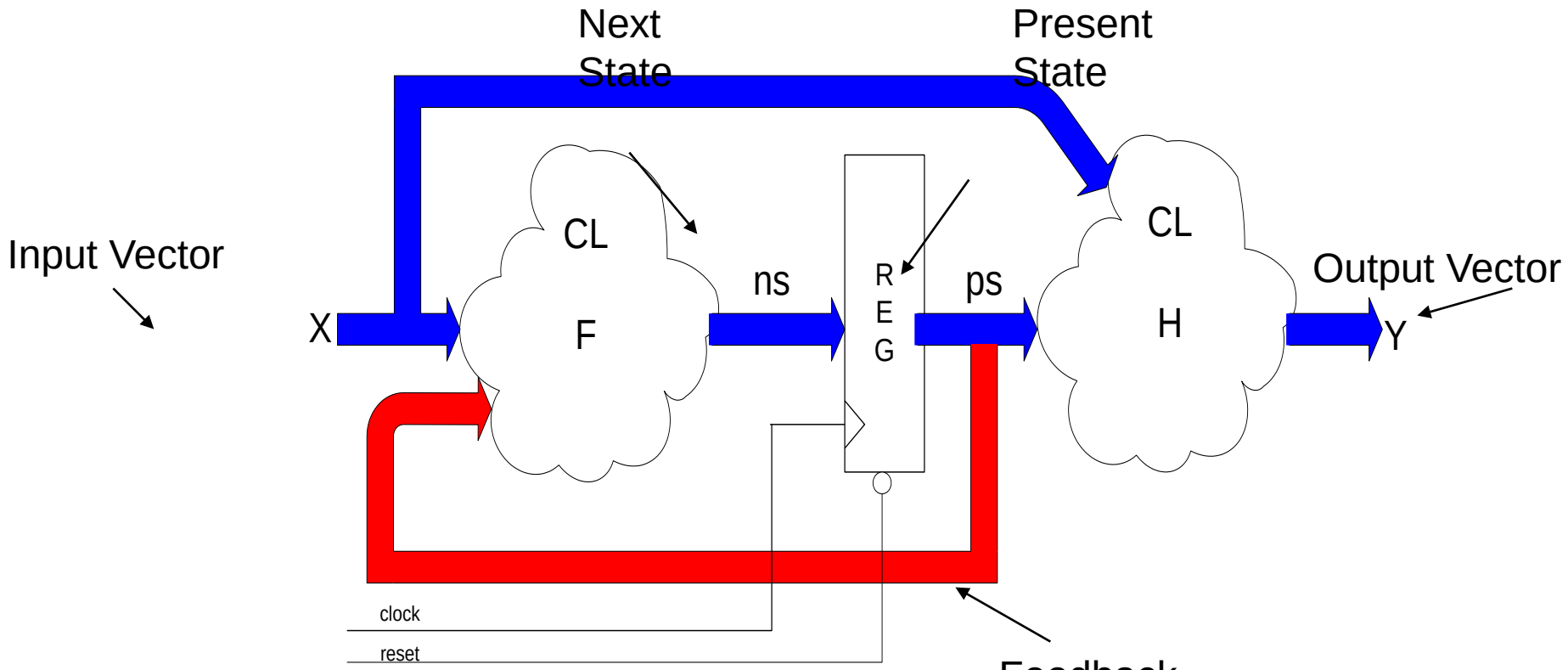
Reg= D Registers

State Equations

$$n_s = F\left(X, p_s\right)$$

$$Y = H\left(p_s\right)$$

Mealy FSM Block Diagram and State Equations



$$n_s = F\left(X, p_s\right)$$

$$Y = H\left(X, p_s\right)$$

Output Y is also a function of input X

Comparison of Mealy and Moore Machines

- Mealy Machines tend to have less states
  - Different outputs on arcs (n^2) rather than states (n)
- Moore Machines are safer to use
  - Outputs change at clock edge (always one cycle later)
  - In Mealy machines, input change can cause output change as soon as logic is done – a big problem when two machines are interconnected
- Mealy Machines react faster to inputs
  - React in same cycle – don't need to wait for clock
  - In Moore machines, more logic may be necessary to decode state into outputs – more gate delays after