BCSE-II (2019-20 2nd Sem)

Computer Architecture Class-Test #1 (Home-Assignment)

10 September 2020

Answer the following on plain paper, in your own handwriting. Scan your answer-sheet or take a legible snapshot. Send the resulting image-file within **SEVEN DAYS** to the following email-id:

hodcse@jadavpuruniversity.in

Q. Consider a 5-stage instruction–pipeline (IF, ID, EX, MEM, WB). There are four consecutive instructions B0, B1, B2, and B3 entering the pipeline. Instruction B0 is a branch, as detected in the ID-stage.

(a) Draw a timing-diagram to show how the branch hazard can be avoided by inserting a stall in the pipeline.

(b) Consider an alternative scheme in which every branch is **assumed** to be "NOT TAKEN". If the branch IS TAKEN (determined in ID-stage), corrective measures are taken.

Draw TWO timing diagrams, one for branch not taken and another for branch taken, in this alternative scheme.

Give a brief explanation (within 4 sentences) for each of your answers. 30
