BCSE-II (2019-2020 2nd Semester)

HOME ASSIGNMENT dt. 08.10.2020 **Full Marks: 50**

Write the answer in your own handwriting on plain paper. Scan your answer-script or take a snapshot of the pages. Email the resulting image file to the following ID: hodcse@jadavpuruniversity.in

within 24 hours, i.e. on 09 October 2020 before midnight.

GROUP-A

Answer all questions **20 × 2 =40**

Choose the correct answer.

1. If a processor writes into a block in its (local) cache, all other caches also obtain the new content immediately in the

(a) write-invalidate protocol

(b) write-update protocol

2. In the decentralized rotating arbiter scheme, arbiter-i is allowed to grant its coupled master if

(a) the priority (i-1) input line is passive

(b) the priority (i-1) input line is active

(c) the priority i output line (i.e. priority i+1 input line) is passive

(d) the priority i output line (i.e. priority i+1 input line) is active

3. In the daisy-chained bus-grant scheme, when a master does not require the bus and receives an active grant line, it

(a) signals an error condition

(b) accesses the bus although it doesn't need to

(c) activates its output grant line, enabling the next master to use the bus

(d) activates the common bus request line

4. In the centralized bus arbitration scheme,

(a) the bus request line is common

(b) the bus grant line is common

(c) the bus busy line is common

(d) none of the above

5. A crossbar is a

(a) switching network

(b) shared path network

6. A non-uniform memory access (NUMA) machine is a

(a) distributed memory system

(b) shared memory system

7. Highly scalable systems are usually

(a) shared memory systems

(b) distributed memory systems

8. Synchronization is relatively more complicated in

(a) shared memory systems

(b) distributed memory systems

For Q9-Q10.

Consider the following CRAY X-MP program:

Line		Instruction
1	A1	10
2	VL	A1
3	V4	V3 + FV2
4	V5	V4 * FV7

Instructions 3 and 4 are chained. Instruction-1 is issued in cycle-1.

9. The first result of line-3 emerges at the end of

(a) cycle-7

(b) cycle-12

(c) cycle-13

(d) cycle-21

10. Line-4 begins chained execution in

(a) cycle-12

(b) cycle-13

(c) cycle-14

(d) cycle-15

11.The first result of line-4 emerges at the end of

(a) cycle-15

(b) cycle-20

(c) cycle-21

(d) cycle-24

For Q12-Q13 Consider the MIPS Floating-Point Unit using Tomasulo's Algorithm.

12. All results from the functional units and from memory go to

(a) load buffers

(b) store buffers

(c) reservation stations

(d) common data bus

13. An instruction is issued to a Reservation Station. If its operands are not available in registers,

(a) the instruction is deleted from the Reservation Station

(b) a record of the functional unit that will generate the operand(s) is kept in the Reservation Station

(c) the instruction is sent back to the instruction queue

(d) the operands are obtained from the load buffers

---

14. Consider the loop:

```
Loop:  L.D      F0, 0(R1)
       DADDUI   R1, R1, # -8
       ADD.D    F4, F0, F2
       BNE      R1, R2, Loop
       S.D      F4, 8(R1)
```

If this loop is unrolled, the following instructions are NOT replicated.

(a) L.D and S.D

(b) DADDUI and ADD.D

(c) DADDUI and BNE

(d) BNE and S.D

15. After simple, mechanical unrolling, execution time can be improved (reduced) further by

(a) scheduling

(b) microprogramming

(c) hazard removal

(d) utilizing branch delay slots

For Q16-Q17: Consider a five-stage instruction pipeline (IM, Reg, EX, DM, Reg) executing the following sequence of instructions:

```
lw      $2, 20($1)
and     $4, $2, $5
or      $8, $2, $6
add     $9, $4, $2
-----------------------------
```

Suppose 'lw' passes through IM-stage in cycle-1.

16. 'and' passes through EX-stage in

(a) cycle-4

(b) cycle-5

(c) cycle-6

(d) none of the above

17. 'or' passes through EX-stage in

(a) cycle-5

(b) cycle-6

(c) cycle-7

(d) none of the above

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18. The present-day definition of 'Computer Architecture' refers to

(a) instruction set design

(b) organization

(c) hardware

(d) all of the above

19. If the processor of a computer system is replaced by a new processor that is ten (10) times faster, and the computation time and I/O time are 40% and 60% respectively, the overall speedup is

(a) 10

(b) 4

(c) 2.17

(d) 1.56

20. Consider the following instruction sequence:

```
mul     r1, r2, r3
add     r2, r4, r5
------------------------
```

The dependency between the two instructions is

(a) RAW

(b) WAR

(c) WAW

(d) RAR

GROUP-B

21. Draw a timing diagram for the following CRAY X-MP program:

Line	Instruction	
1	S1	S2 + S3
2	S1	S2 + S3
3	S2	S1 + S7
4	S1	S4 + S5

Explain your answer in at most five sentences. **10**