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STD: BCSE-2nd

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ROLL NO.: 28

YOUVA

SUBJECT: Digital Systems Lab

## INDEX

SR. NO.	EXPERIMENT	PAGE	DATE OF EXPERIMENT	DATE OF SUBMISSION	REMARKS
1	To determine the output from each logical gate by providing varying inputs		08/08/2019	8/8/2019	
2	Implement a decimal to binary encoder and a binary to decimal decoder using logic Gates		22/08/2019 29/08/2019	22/8/2019 29/8/2019	
3	Implement a 4 to 1 Multiplexer and a 1 to 4 Demultiplexer		05/09/2019		
4	Implement a comparator circuit for 2 3-bit numbers		12/9/2019		
5	Implement an odd/even parity generator		10/9/2019		
6	Implement a 3-bit adder/substrator circuit		26/9/2019		
7	Implement a modulo-n asynchronous counter		19/10/2019		

S.R. NO.	EXPERIMENT	PAGE	DATE OF EXPERIMENT	DATE OF SUBMISSION	REMARKS
7					
8	Verification of ROM / Design a 4bit ROM using diodes and resistors		14/11/2019		
9	Implement & verify the weighted resistor digital to analog converter.		14/11/2019		

Aim :- To determine the output from each logical gate by providing varying input.

Apparatus :-

- 1) Bread Board
- 2) Connecting wires
- 3) IC - 7400 (NAND Gate)
- 4) IC - 7404 (NOT Gate)
- 5) IC - 7408 (AND Gate)
- 6) IC - 7432 (OR Gate)

Theory :- The ICs used in the experiment have 14 pins where 14th pin is +Vcc and pin 4 is grounded.

Details of the ICs are as follows:-

- A) IC - 7400 → consists of NAND Gates
- B) IC - 7404 → consists of NOT Gates
- C) IC - 7408 → consists of AND Gates
- D) IC - 7432 → consists of OR Gates

Truth Table

<u>Input</u>		<u>Output</u>			<u>Input</u>	<u>Output</u>
input <sub>1</sub>	input <sub>2</sub>	OR	AND	NAND	input	NOT
0	0	0	0	1	0	1
0	1	1	0	1	1	0
1	0	1	0	1		
1	1	1	1	0		

Teacher's Signature:

EXPT.  
NO.

NAME:

Page No.:

Date:

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Observation Table :-

(i) IC - 7432 (OR Gate) →

input <sub>1</sub> (in volt)	input <sub>2</sub> (in volt)	V <sub>out</sub> (in volt)
0	0.04	0
5	0.08	4.97
0.07	4.97	4.97
5	5	5

(2) IC - 7408 (AND Gate) →

input <sub>1</sub> (in volt)	input <sub>2</sub> (in volt)	V <sub>out</sub> (in volt)
0.08	0.08	0.1
4.96	0.07	0
0.07	4.98	0
4.97	4.97	4.22

## AND (7408).

### Truth Table (Voltage).

#### Input

A	B	F.
0.08	0.08	0.1
4.96	0.07	0.
0.07	4.98	0.
4.97	4.97	4.22

(3) IC - 7400 (NAND Gate) →

input <sub>1</sub> (in volt)	input <sub>2</sub> (in volt)	V <sub>out</sub> (in volt)
0	0	4.95
0	5	4.95
5	0	4.95
4.98	5	0

(4) IC - 7404 (NOT Gate) →

input (in volt)	V <sub>out</sub> (in volt)
0.06	4.92
4.99	0

Inference :- The output '1' in the truth table corresponds to high voltage, while the output '0' corresponds to low voltage.

The pattern of high and low voltage in each gate is at par with the table, hence the experiment is successful.

Aim :- Implement a decimal to binary encoder and a binary to decimal decoder using logic Gates

Apparatus :- 1) Bread Board

2) Connecting Wires

3) IC 7432 (OR-GATE)

4) IC 7404 (NOT-GATE)

Theory :- For Decimal to Binary Encoder :-

Input

Output

	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Outputs are higher for  
 $D = 8 + 9$ ,  $C = 4 + 5 + 6 + 7$   
 $B = 2 + 3 + 6 + 7$ ,  $A = 1 + 3 + 5 + 4 + 9$

Theory (contd.)

An Encoder is a combinational circuit. It has maximum of  $2^n$  input lines and 'n' output lines, hence it encodes the information from  $2^n$  inputs into an n-bit code. The decimal to BCD encoder consists of 10 input lines & 4 output lines. This encoder accepts the decoded decimal data as an input and encodes it to the BCD output which is available on the output lines.

A Decoder is a combinational circuit. It has 'n' input lines and a maximum of  $2^n$  output lines. The BCD to decimal decoder consists of 4 input lines and 10 output lines. This decoder accepts the encoded BCD data as an input and decodes it to the decimal output which is available on the output lines.

From the truth table :-

Encoder

$$\begin{cases} A = 1 + 3 + 5 + 7 + 9 \\ B = 2 + 3 + 6 + 7 \end{cases} \quad \begin{cases} C = 4 + 5 + 6 + 7 \\ D = 8 + 9 \end{cases}$$

Decoder

$$\begin{cases} D_0 = \bar{A}\bar{B}\bar{C}\bar{D} \\ D_1 = \bar{A}\bar{B}\bar{C}D \\ D_2 = \bar{A}\bar{B}C\bar{D} \\ D_3 = \bar{A}\bar{B}CD \\ D_4 = \bar{A}B\bar{C}\bar{D} \\ D_5 = \bar{A}B\bar{C}D \end{cases} \quad \begin{cases} D_6 = \bar{A}BC\bar{D} \\ D_7 = \bar{A}BCD \\ D_8 = A\bar{B}\bar{C}\bar{D} \\ D_9 = A\bar{B}\bar{C}D \end{cases}$$

Teacher's Signature:

For Binary to Decimal Decoder (Truth Table) :-

Input

Output

A	B	C	D	$D_0$	$D_1$	$D_2$	$D_3$	$D_4$	$D_5$	$D_6$	$D_7$	$D_8$	$D_9$
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	1	0	0	0
0	1	1	0	0	0	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	0	0	1	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1

Observations :-

Encoder

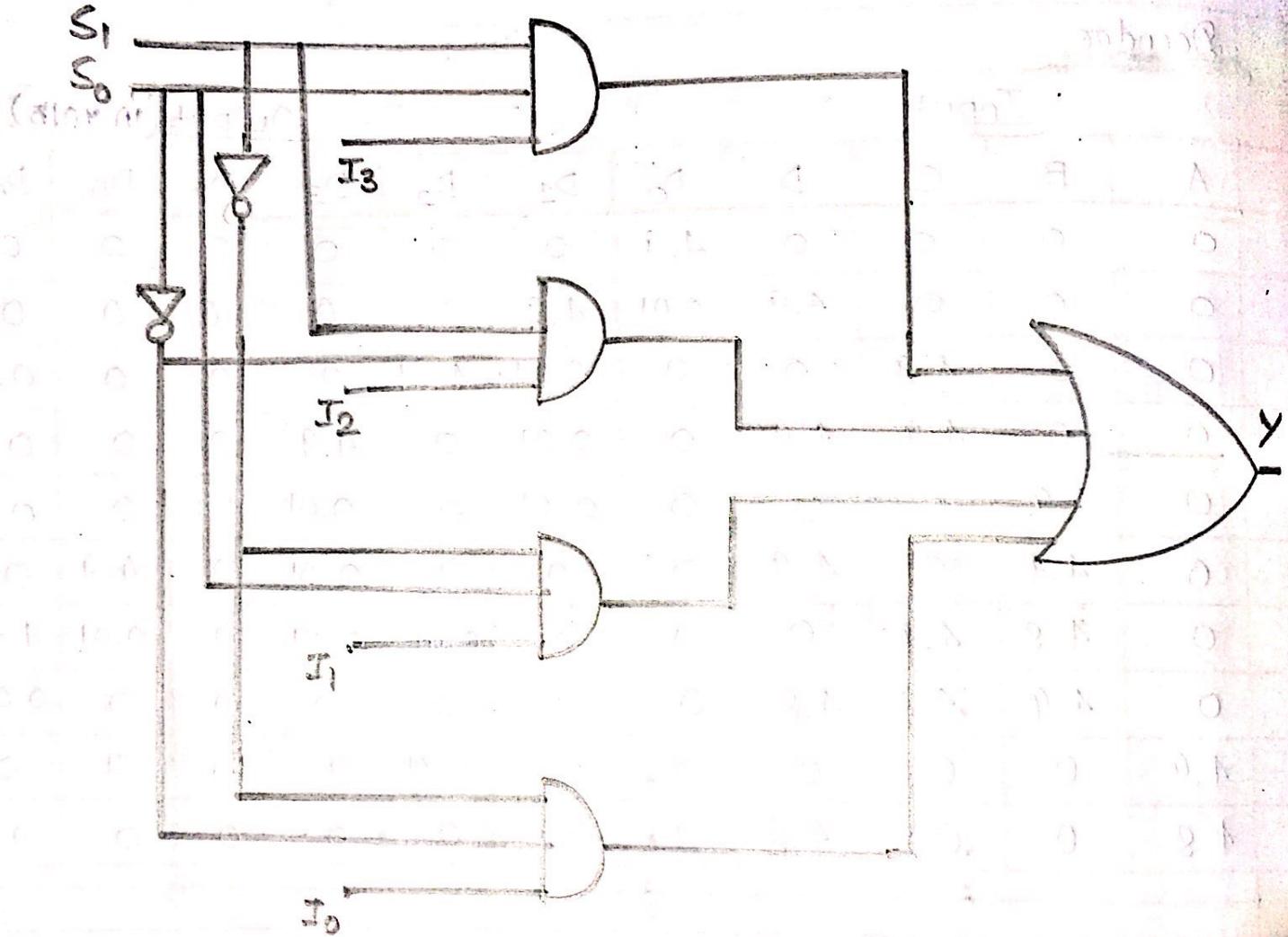
Output (Volts)

<u>Input</u>	<u>D</u>	<u>C</u>	<u>B</u>	<u>A</u>
0	0.01	0	0	0.01
1	0	0.01	0	4.9
2	0.01	0	4.89	0.01
3	0	0.01	4.9	4.9
4	0.01	4.89	0.1	0.0
5	0.01	4.9	0	4.89
6	0	4.9	4.9	0.01
7	0	4.8	4.89	4.89

8	4.9	0.01	0.01	0
9	4.9	0	0	4.9

## Decoders

Inference :- The observed outputs are the expected output as evident from the truth table. Hence experiments were successful.



4-1 multiplexer

Aim :- Implement a 4 to 1 Multiplexer and a 1 to 4 DeMultiplexer

Apparatus :-

- 1) Bread Board
- 2) Connecting wires
- 3) IC - 7404 (NOT Gate)
- 4) IC - 7408 (AND Gate)
- 5) IC - 7432 (OR Gate)

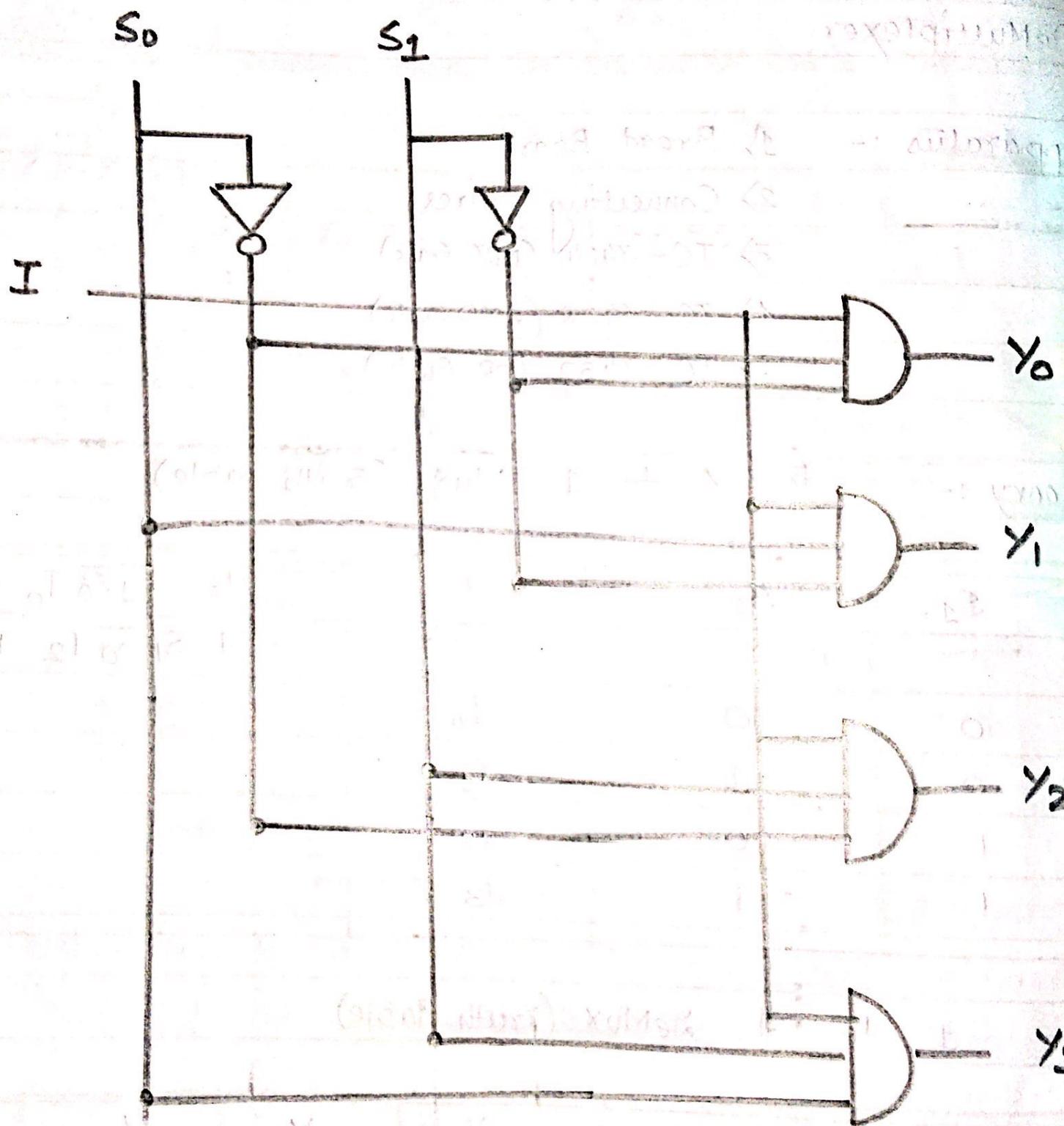
Theory :- For 4 to 1 Mux (Truth Table)

<u><math>S_1</math></u>	<u><math>S_0</math></u>	<u><math>y</math></u>	$y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$
0	0	$I_0$	
0	1	$I_1$	
1	0	$I_2$	
1	1	$I_3$	

For 1 to 4 DeMux (Truth Table)

<u><math>S_1</math></u>	<u><math>S_0</math></u>	<u><math>y_0</math></u>	<u><math>y_1</math></u>	<u><math>y_2</math></u>	<u><math>y_3</math></u>
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

$$y_0 = \bar{S}_1 \bar{S}_0 I, \quad y_1 = \bar{S}_1 S_0 I, \quad y_2 = S_1 \bar{S}_0 I, \quad y_3 = S_1 S_0 I$$



1 - 4 demultiplexer.

### Theory (Contd)

A Multiplexer or Mux is a device that has many inputs and a single output. The selected line decides which input is connected to the output, and also increases the amount of data that can be sent over within a certain amount of time. A multiplexer is also called as a data selector.

The  $4 \times 1$  multiplexer consists of 4 input bits, 1-output bit & 2 control bits. The 4 input bits are namely  $D_0, D_1, D_2, D_3$ ,  $I_0, I_1, I_2, I_3$  respectively, and only one of the input bit is transmitted to the output. The output  $Y$  depends on the value of  $S_0, S_1$ . For example, when  $S_0S_1 = 00$  then the higher AND is allowed while the remaining AND gates are restricted. If the state  $S_0S_1 = 11$ , then all gates are disabled except the bottom AND gate.

A De-Multiplexer is a device that has one input - & multiple output lines which are used to send a signal to one of the various devices.

~~1 x 4 demultiplexer~~ comprises 1-input bit, 4 output bits and control bits. The i/p bit is considered as  $I$ . The data bit is transmitted to the data bit of the o/p lines which depend on  $S_0S_1$  and control the input.

Teacher's Signature:

## Observations

1) For 1 to 4 Demultiplexer

$S_1$	$S_0$	In (in volts)	Output (in mV)			
			$y_0$	$y_1$	$y_2$	$y_3$
0	0	$I_0 = 0$	0	0.01	0	0.01
		4.9	4.9	0.01	0	0.01
0	1	$I_1 = 0$	0	0	0	0
		4.9	0	4.9	0	0
1	0	$I_2 = 0$	0	0	0.01	0
		4.9	0	0	4.9	0
1	1	$I_3 = 0.01$	0	0.01	0	0
		4.9	0	0	0	4.9

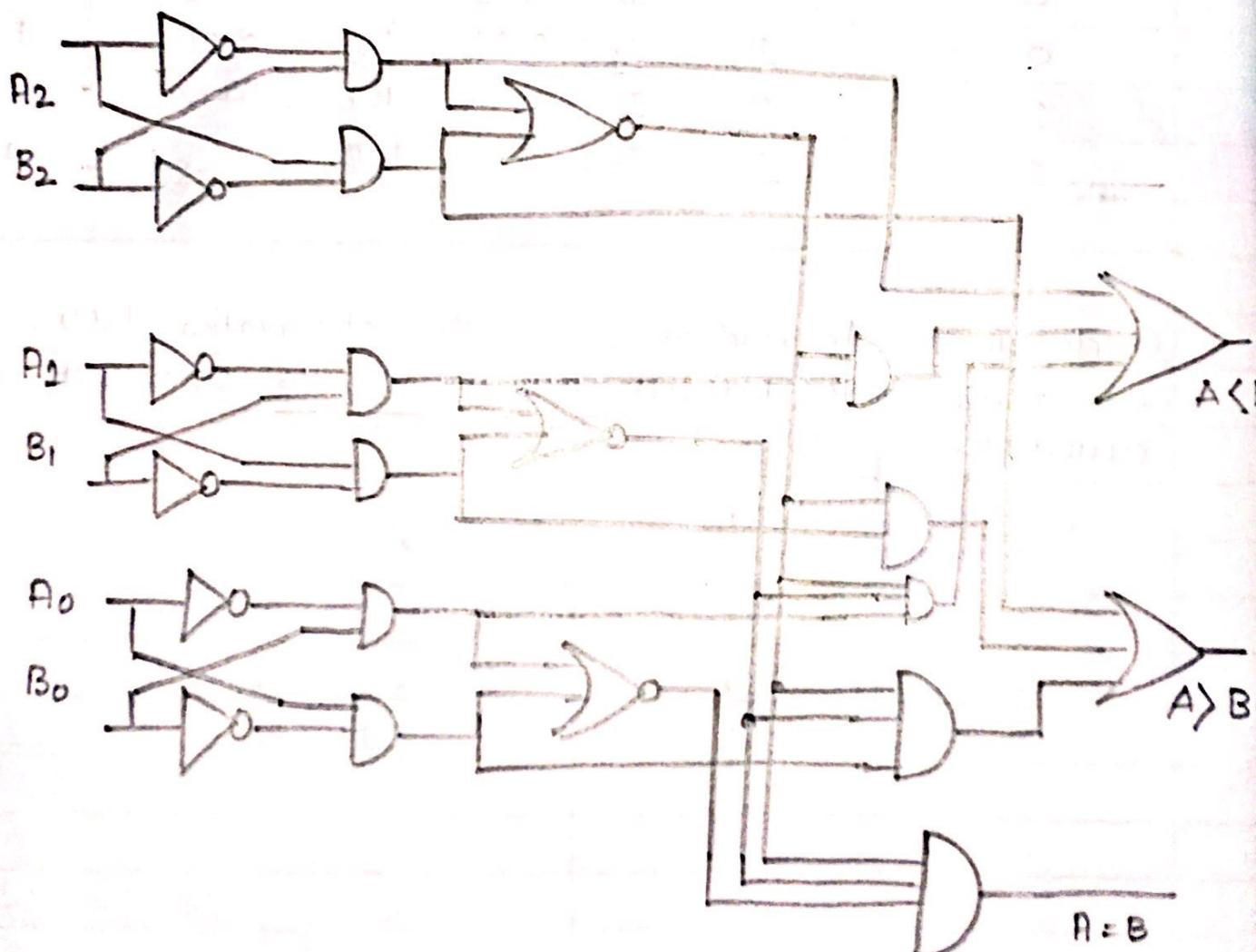
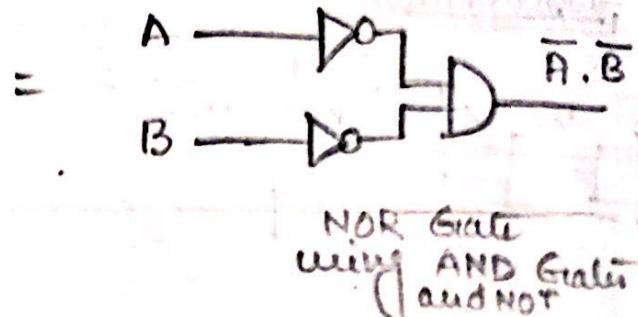
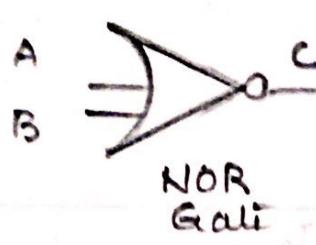
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Observations

2) For 4 to 1 MUX

<u><math>S_1</math></u>	<u><math>S_0</math></u>	<u><math>I_n</math></u> (in volts)	<u><math>y</math></u> (in volts).
0	0	$I_0 = 0.01$	4.9
0	1	$I_1 = 0.01$	4.89
1	0	$I_2 = 0$	4.9
1	1	$I_3 = 0$	4.9

Conclusion :- As evident from the observation table, the truth table matches with it. So, the experiment is successful.



3-bit comparator

Aim :- To implement a comparator circuit for two 3-bit numbers

- Apparatus :-
- 1) Bread Board
  - 2) Connecting Wires
  - 3) IC - 7404 (NOT Gate)
  - 4) IC - 7432 (OR Gate)
  - 5) IC - 7408 (AND Gate)

Theory :-

3-bit Comparator circuit (Truth Table)

$A_2$	$A_1$	$A_0$	$B_2$	$B_1$	$B_0$	$A > B$	$A < B$	$A = B$
0	0	0	0	0	0	0	0	1
0	0	0	0	0	1	0	1	0
0	0	0	0	1	0	0	1	0
0	0	0	0	1	1	0	1	0
0	0	0	1	0	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	0	1	1	1	0	0
1	1	1	1	0	0	1	0	0
1	1	1	1	0	1	1	0	0
1	1	1	1	1	0	1	0	1

Teacher's Signature:

## Theory (Contd)

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A magnitude digital comparator is a combinational circuit that compares 2 digital / binary numbers in order to find out whether one binary number is equal, less than/greater than the other binary number.

### 3-bit comparator

A comparator used to compare two binary numbers each of 3-bit is called a 3-bit magnitude comparator. It consists of six inputs each of two three-bit numbers and three outputs to generate less than, equal to and greater than between two binary numbers.

- (a)  $A > B \rightarrow$  case when (i)  $A_2 = 1$  and  $B_2 = 0$ , (ii)  $A_2 = B_2$ ,  $A_1 = 1$  and  $B_1 = 0$  (iii)  $A_2 = B_2$ ,  $A_1 = B_1$ ,  $A_0 = 1$  and  $B_0 = 0$
- (b)  $A < B \rightarrow$  case when (i)  $A_2 = 0$  &  $B_2 = 1$ , (ii)  $A_2 = B_2$ ,  $A_1 = 0$  &  $B_1 = 1$  (iii)  $A_2 = B_2$ ,  $A_1 = B_1$  &  $A_0 = 0$  and  $B_0 = 1$
- (c)  $A = B \rightarrow$  case when  $A_2 = B_2$ ,  $A_1 = B_1$  &  $A_0 = B_0$

EXPT. NO.	NAME:	Page No.:
		Date: <u>youva</u>

### Observations (in volts)

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	A > B	A < B	A = B
0.01	0	0.01	0	0	0.01	0	0	4.89
0.01	0.01	0	0.01	0	4.89	0	4.89	0.01
0.0	0	0	0.01	4.9	0	0	4.9	0.01
0.01	0	0	0	4.9	4.9	0	4.89	0
0.01	0	0	4.9	0	0	0	4.89	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
4.89	4.89	4.91	0.01	4.89	4.89	4.9	0	0
4.92	4.9	4.89	4.89	0	0	4.89	0	0
4.89	4.89	4.9	4.89	0	4.91	4.89	0	0
4.89	4.89	4.9	4.9	4.9	0	4.89	0	0
4.91	4.91	4.9	4.89	4.89	4.9	0	0	4.89

Inference: As evident from the observation table, the truth table matches with it. So, the experiment is successful.



XOR Gate



$$S = (A+B)(\bar{A}+\bar{B})$$

XOR Gate

using AND, OR and  
NOT Gates

### Even Parity Generator (3-bit)



EXPT.  
NO.

NAME:

Page No.:

Date:

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Aim:- To implement an odd/even parity generator

- Apparatus :-
- 1> Bread Board
  - 2> Connecting Wires
  - 3> IC-7404 (NOT Gate)
  - 4> IC-7432 (OR Gate)
  - 5> IC-7408 (AND Gate)

Theory :-

Even Parity Generator (Truth Table)

3-bit Input

Even-parity bit  
generator

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Theory (contd.)

A parity generator is a combinational logic circuit that generates the parity bit. (A parity bit is added to the word containing data in order to make number of 1s either even or odd. Thus, it is used to detect errors).

In even-parity scheme, the parity bit is '0' if there are even number of 1s in the data stream and parity bit is '1' if there are odd no. of 1s in the data stream. In odd parity bit scheme, the parity bit is '1' if there are even number of 1s in the data stream while the parity bit is '0' if there are odd no. of 1s in the datastream.

If we construct a simple K-Map from the Truth Table:-

		BC	00	01	11	10	(Even Parity Generator)
		A	00	01	11	10	
			0	1	0	1	
		00	0	1	0	1	
		01	1	0	1	0	

$$\begin{aligned}
 P &= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \\
 &= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC) \\
 &= \bar{A}(B \oplus C) + A(\bar{B} \oplus C)
 \end{aligned}$$

$$\Rightarrow P = A \oplus B \oplus C$$

NO.

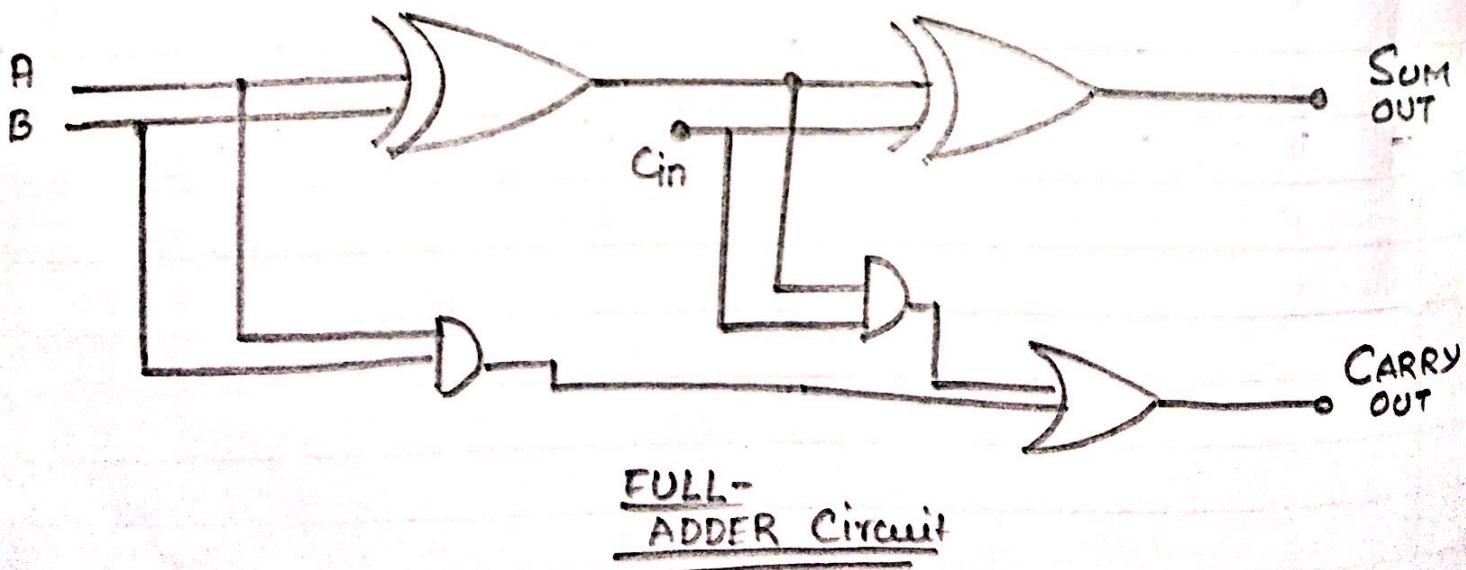
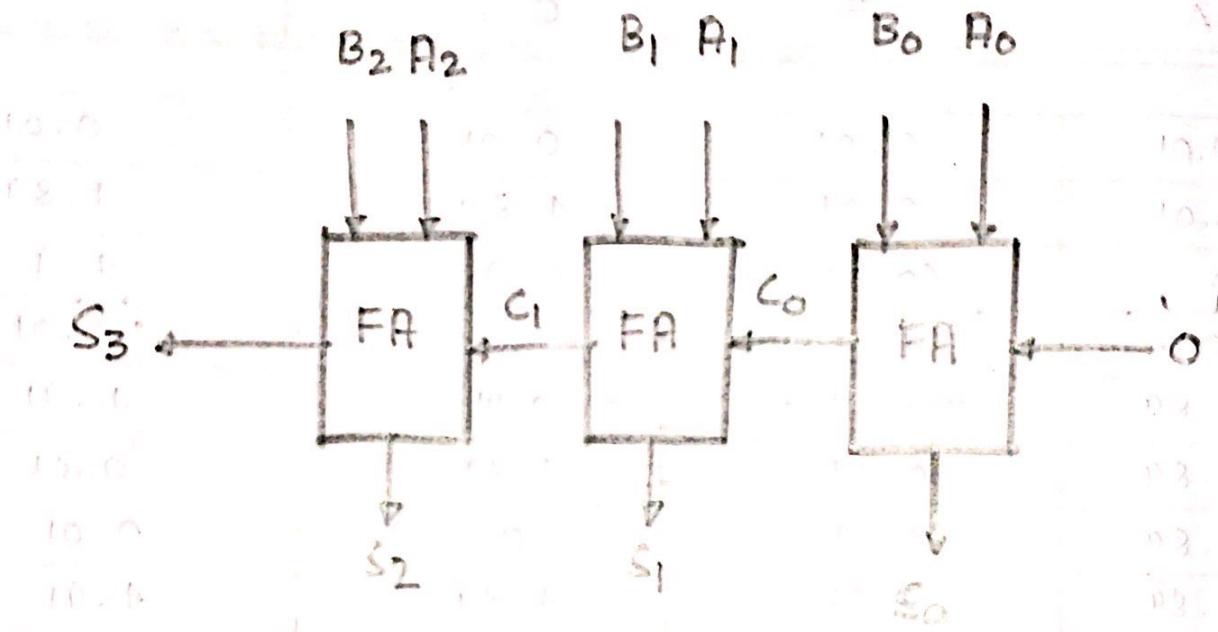
Observations

3-bit Input,  
(in volt)

Even-parity bit  
generator (in volt)

A	B	C	y
0.01	0.01	0.01	0.01
0.01	0.01	4.89	4.89
0	4.89	0.01	4.9
0	4.89	4.89	0.01
4.89	0.01	0.01	4.91
4.89	0.01	4.89	0.01
4.89	4.89	0	0.01
4.89	4.89	4.89	4.91

Inference:- As evident from the observation table,  
 the truth table matches with it. So, the experiment  
 is successful.



EXPT. NO.	NAME:	Page No.:
		Date: <u>youva</u>

Aim :- To implement a 3-bit adder/subtractor circuit

- Apparatus :-
- 1) Bread Board
  - 2) Connecting Wires
  - 3) IC-7404 (NOT Gate)
  - 4) IC-7432 (OR Gate)
  - 5) IC-7408 (AND Gate)

Theory :- Adder circuit (Truth Table).

$A_2$	$A_1$	$A_0$	$B_2$	$B_1$	$B_0$	$S_3$	$S_2$	$S_1$	$S_0$
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	0	1
0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	1	0	0	1	1
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	1	1	1	0	1	1	1	0	0
1	1	1	1	1	0	1	1	0	1
1	1	1	1	1	1	1	1	1	0

EXPT. NO.	NAME:	Page No.:
		Date: <b>youva</b>

### Theory (contd)

Full adder is the adder circuit which adds three inputs and produces 2 outputs. The first two ~~out~~ inputs are A & B and the third input is an input carry in  $C_{in}$ . The output carry is designated as  $C_{out}$  and the normal output is designated as S which is sum.

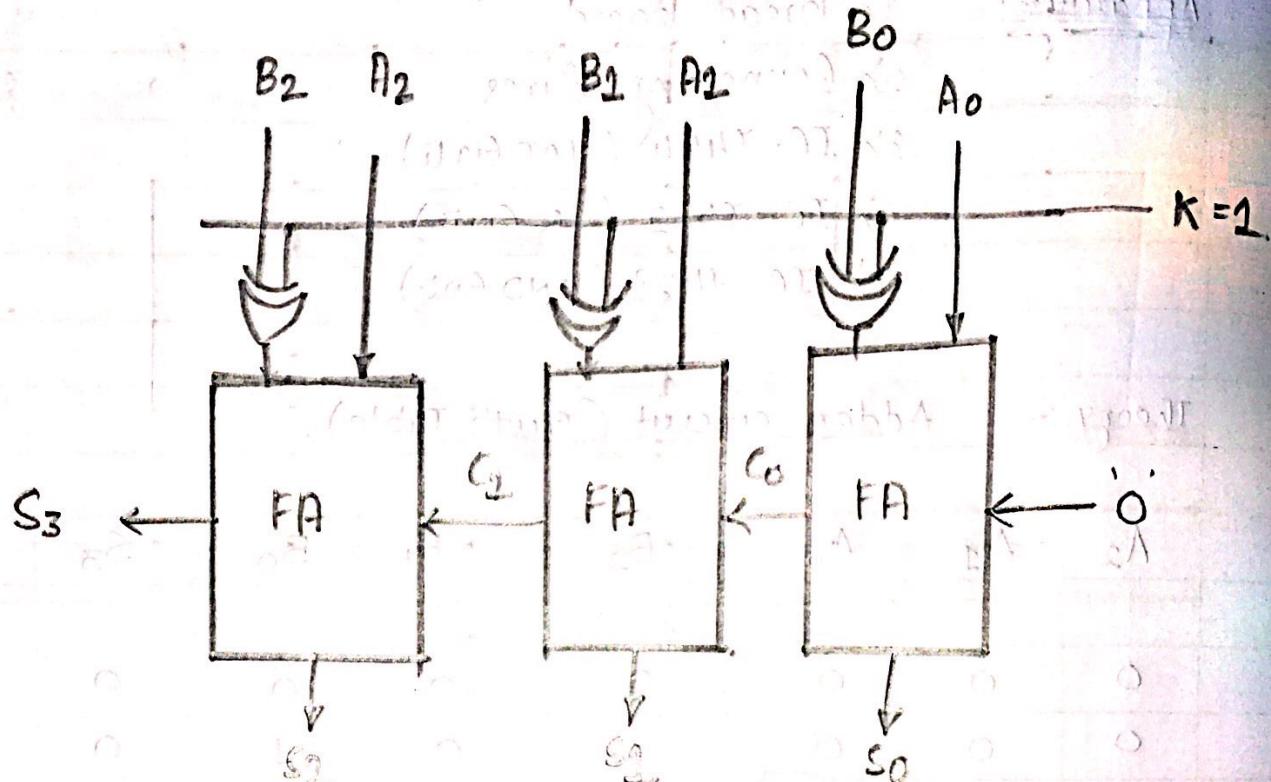
Cascading full adder circuits can be used to add two 3-bit numbers.

$C_{out} = AB + C_{in}$
$S = C_{in} \oplus A \oplus B$

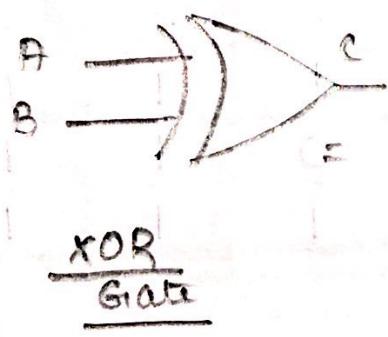
Adder-Subtractor Circuit is a circuit which is capable of adding as well as subtracting binary numbers in one circuit itself. The operations being performed depend upon the binary value the control signal holds.

There is a control line K that holds a binary value of either 0 or 1 which decides/determines the operation to be carried out. i.e. ... addition or subtraction respectively.

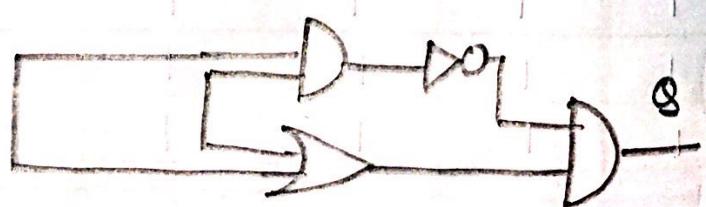
Two's complement addition (k=3) using full adder



Two 3-bit number adder-subtractor circuit



XOR Gate



$$Q = (A + B)(\bar{A} + \bar{B})$$

XOR Gate using AND, OR & NOT Gate

NAME: Theory (contd.) →

Page No.:

Date:

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### Subtractor circuit (Truth Table)

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	1	0	0	1
0	0	0	0	1	0	1	0	1	0
0	0	0	0	1	1	1	0	1	1
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	1	1	1	0	1	0	0	1	0
1	1	1	1	1	0	0	0	0	1
1	1	1	1	1	1	0	0	0	0

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## Subtractor circuit (Observation Table) (in volts)

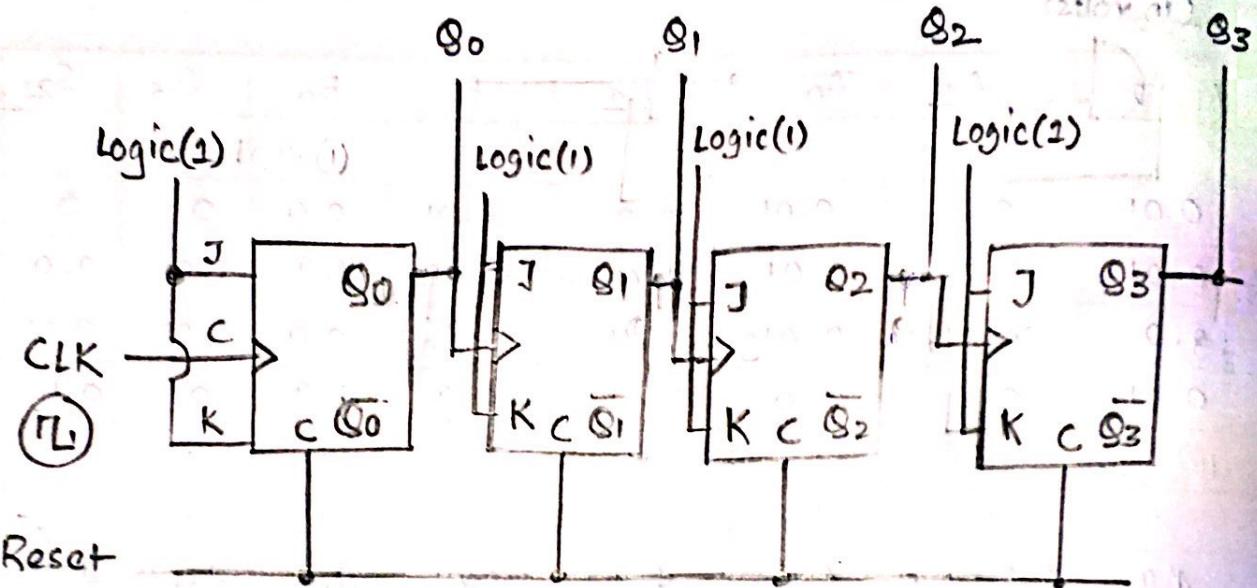
A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>
0.01	0.0	0.01	0.0	0.01	0.0	0.01	0.01	0.0	0.0
0.01	0	0.01	0.01	0.01	4.9	4.9	0	0	4.9
0	0.01	0.01	0.01	4.91	0.0	4.9	0	4.9	0
0.01	0	0.01	0.01	4.9	4.9	4.9	0	4.9	4.9
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
4.9	4.89	4.89	4.9	0.01	4.9	0.01	0.01	4.9	0
4.9	4.89	4.9	4.9	4.9	0.01	0	0.01	0	4.9
4.9	4.9	4.89	4.9	4.89	4.9	0	0	0.01	0.0

EXPT. NO.	NAME:	Page No.:
		Date: <u>youva</u>

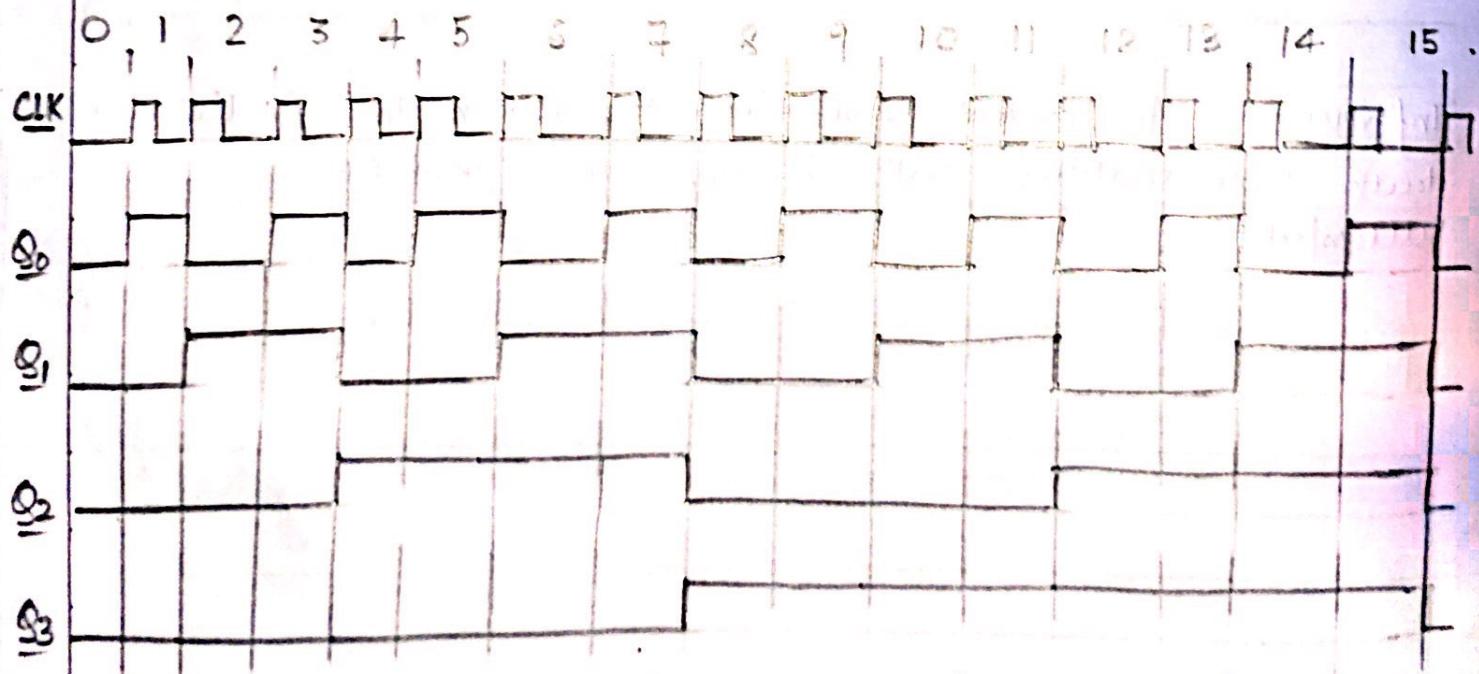
Observations:-  
(In volts)

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>
0.01	0.0	0.01	0.0	0.01	0.0	0	0	0.01	0.01
0.01	0.0	0.01	0.01	0.01	4.9	0.01	0.0	0.01	4.9
0.0	0.01	0.01	0.01	4.9	0.0	0.01	0.01	4.9	0
0.01	0.0	0.0	0.01	4.9	4.9	0	0.0	4.9	4.9
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
4.9	4.89	4.89	4.9	0.01	4.9	4.89	4.89	0	0
4.9	4.89	4.9	4.9	4.9	0.01	4.9	4.9	0	4.9
4.9	4.9	4.89	4.9	4.89	4.9	4.9	4.9	4.9	0

Inference:- As evident from the observation table, the truth table matches with it. So, the experiment is successful.



4 bit asynchronous up counter



Timing Diagram for the  
4-bit asynchronous up counter

Aim :- To implement a modulo-n asynchronous counter

Apparatus :- 1> Bread Board

2> Connecting Wires

3> Clock Pulse [Timer Circuit]

4> JK Flip-flops .

Theory :- 4-bit ripple counter (Truth table), [up-counter]

Clock Pulse State				$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	1	0	0	0	1
3	0	0	1	1	0	0	1
4	0	1	0	0	0	1	0
5	0	1	0	1	0	1	0
6	0	1	1	0	0	1	1
7	0	1	1	1	0	1	1
8	1	0	0	0	1	0	0
9	1	0	0	1	1	0	1
10	1	0	1	0	1	0	1
11	1	0	1	1	1	0	1
12	1	1	0	0	1	1	0
13	1	1	0	1	1	1	0
14	1	1	1	0	1	1	1
15	1	1	1	1	1	1	1
16	0	0	0	0	0	0	0

Teacher's Signature:

## Theory (contd)

A counter is a device which can count any particular event on the basis of how many times the particular event(s) has/have occurred. Most common types of counter is sequential digital logic circuit with a single clock input and multiple outputs. The outputs represent binary or binary coded decimal nos. Each clock pulse can either increase/decrease the number.

There are two types of counter:-

- (i) Synchronous counter
- (ii) Asynchronous counter

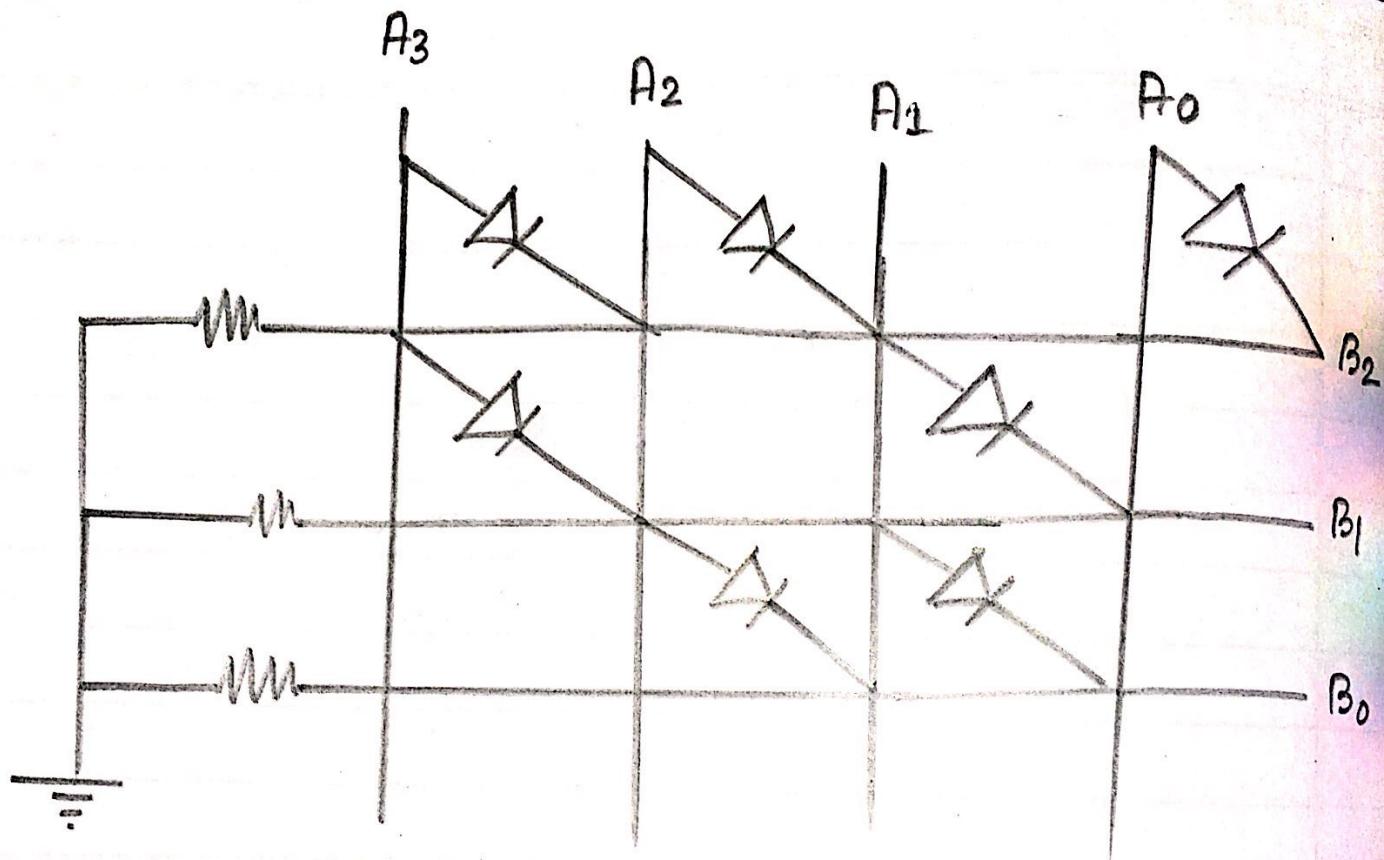
In asynchronous counter, the first flip flop is clocked by external pulse and then each successive stage flip-flop is clocked by  $Q$  or  $\bar{Q}$  output of previous stage. Because of inherent propagation delay time all flip-flops are not activated at the same time which results in asynchronous operation.

EXPT. NO.	NAME:	Page No.:	youva
		Date:	

### Observations (in volts)

	Clock	Pulse State		$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0.1	0	0.1	0	0.1	0	0.1 0.1
1	0	0	0.1	4.89	0.1	0	0 4.91
2	0	0	4.9	0.1	0.1	0	4.89 0.01
3	0	0	4.89	4.91	0.01	0	4.91 4.92
4	0.1	4.9	0.1	0	0.1	4.91	0.1 0
5	0.11	4.89	0	4.91	0.11	4.89	0 4.88
6	0.1	4.92	4.88	0.1	0.1	4.89	4.91 0.1
7	0	4.91	4.9	4.9	0	4.9	4.9 4.9
8	4.9	0.09	0.1	0.1	4.9	0.1	0.1 0.1
9	4.89	0.1	0.1	4.89	4.9	0.1	0.1 4.9
10	4.91	0.01	4.92	0.01	4.91	0.01	4.92 0
11	4.91	0	4.92	4.93	4.89	0	4.91 4.93
12	4.89	4.91	0.01	0.1	4.9	4.9	0 0
13	4.91	4.89	0.02	4.89	4.9	4.9	0 4.9
14	4.91	4.9	4.88	0.1	4.9	4.9	4.9 0.1
15	4.9	4.88	4.91	4.92	4.9	4.91	4.91 4.91
16	0.1	0.09	0.1	0.1	0.01	0.1	0.1 0.1

Inference :- As evident from the observation table, the truth table matches with it. So, the experiment is successful.



Circuit Diagram for ROM

Aim:- Verification of ROM / Design a 4 bit ROM using diodes & resistor

Apparatus Required :-

1> Breadboard

2> 7-diodes

3> Voltage Source

4> Connecting wires

5> Resistors ( $2.2\text{ k}\Omega$ )

Theory :- A read only memory is an LSI/VLSI circuit which consists of coupling devices (most often diodes). Binary data is stored in the ROM by coupling an address min-term line (word line) to an output line (bit line). It can be read out whenever desired, but the data which is stored cannot be changed under minimal operating conditions. A ROM which has  $n$  input lines and  $m$  output lines contains an array of  $2^n$  words & each word is  $m$ -bits long. The input line serves as an address to select one of the  $2^n$  words. When an input is applied to the ROM, the pattern of 1's & 0's which is stored in the corresponding word in the memory appears at the output line. The basic structure of the ROM consists of a decoder & a memory array. The  $n$ -inputs are directed to the  $n$ -inputs of the decoder and a pattern of  $n$  0's & 1's is applied to these. Exactly one of the 2 decoder outputs is 1. The decoder output pattern is stored in the word which is transferred to the memory output lines. Unlike RAM, ROM is a non-volatile memory device.

Truth Table

Input				Output	
A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	B <sub>2</sub>	B <sub>1</sub>
1	0	0	0	1	1
0	1	0	0	1	0
				0	1
				1	0

I/P				O/P.		
A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>
0	0	0	5	4.50	0	0
0	0	5	0	0	4.53	4.53
0	5	0	0	4.48	0	4.52
5	0	0	0	5.14	4.52	0

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14.11.2019

Roll - 26, 27, 28.

Observation taken during experiment

Teacher's Signature

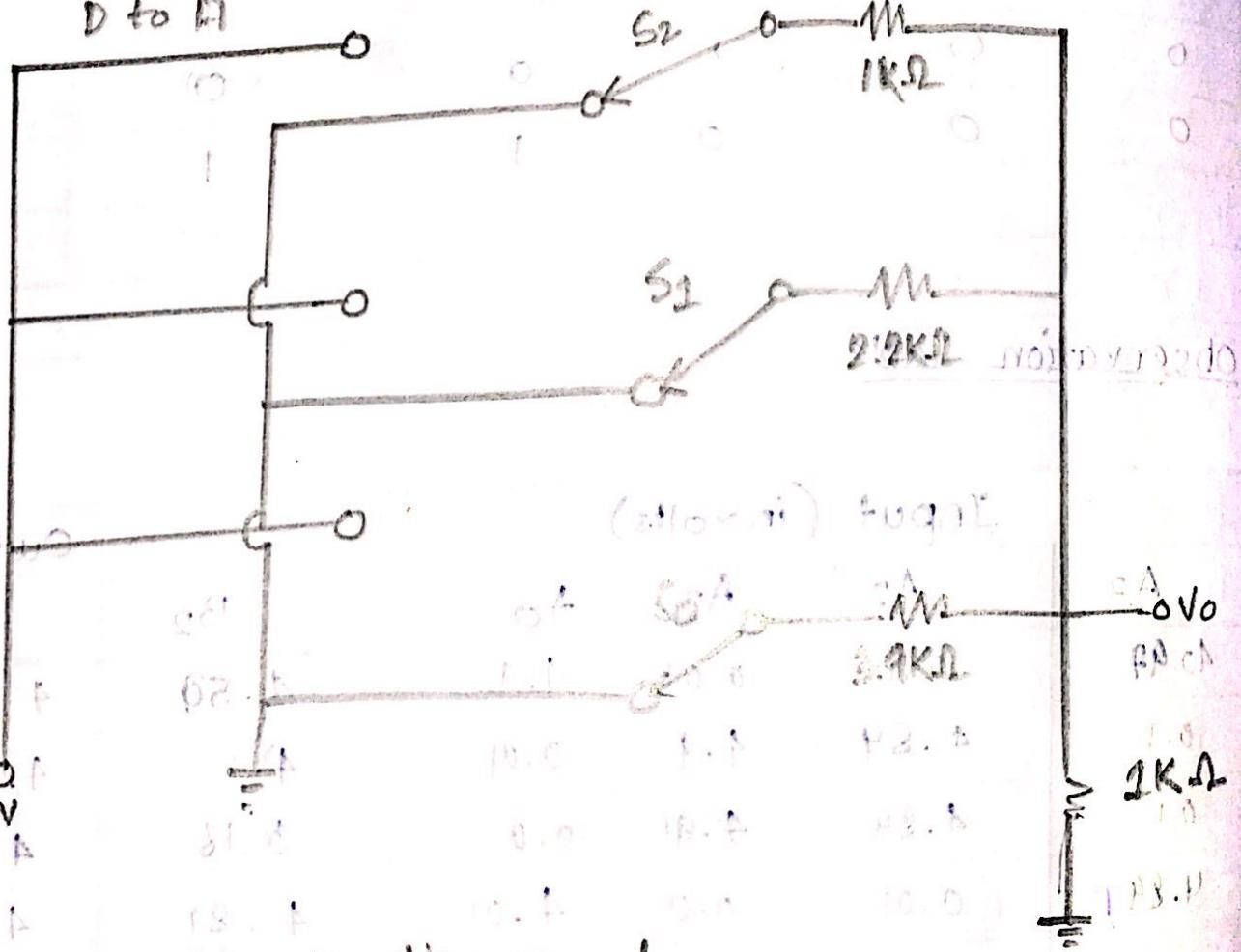
Truth Table

<u>Input</u>				<u>Output</u>		
A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>
1	0	0	0	1	1	0
0	1	0	0	1	0	1
0	0	1	0	0	1	1
0	0	0	1	1	0	0

Observation Table

<u>Input (in volts)</u>				<u>Output (in volts)</u>		
A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>
0.01	0.01	0.01	4.9	4.89	0.1	0.1
0.1	0.01	4.9	0.01	0.1	4.53	4.53
0.1	4.89	0.01	0.0	4.48	0.1	4.52
4.89	0.01	0.0	0.01	4.89	4.52	0.01

Inference :- As evident from the observation table, the truth table matches with it. So, the experiment is successful.



Circuit diagram for a  
Digital to

Analog converter

using resistive divider circuit;

Aim :- To implement and verify the weighted resistor digital to analog conversion

- Apparatus required :-
- 1) Bread board
  - 2) Connecting wires
  - 3) Multi-meter
  - 4) Resistors
  - 5) DC-Power supply

Theory :- A digital to analog converter is used when the binary output from a digital system is to be converted into the equivalent analog voltage / current. The binary output will be sequence of 1s & 0s. Thus, they may be difficult to follow. But a digital to analog converter help the user to interpret easily. It can be classified into 2 types :-

- (i) Digital to Analog converter using binary weighted resistors.
- (ii) Digital to Analog converter with R and 2R resistors.

The input is said to be an N-digit binary signal.  $V = V_{n-1}V_{n-2}\dots V_1V_0$  in which  $V_k$  is a voltage which represent either logic 0 or logic 1. It is assumed that  $V_k$  are made simultaneously available in parallel N lines, if the  $V_k$  appear suitable, the bits must be counted into a shift register so that all the bits can be made available simultaneously. The voltage  $V_k$  normally available to

I/P	$S_2$	$S_1$	$S_0$	%/P	V <sub>O</sub>
	5	5	5		3.32
5	5	5	0		3.08
5	0	5	5		2.86
5	0	5	0		2.50
0	5	5	0		2.30
0	5	0	5		1.82
0	0	5	5		1.2
0	0	0	5		0.

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 Debjani Chowdhury  
 14.11.2019

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drive the converter need not be precisely fixed value but identifiable as to represent the one logic level or the other. When V<sub>O</sub> corresponds to logic 1 or logic 0 the switch S<sub>0</sub> is connected to 1 or 0 position connecting a resistor R<sub>K</sub> to the precisely controlled voltage source V(1) or V(0) as shown. The LSB S<sub>0</sub> operates which switch S<sub>0</sub> which is connected to the output through the resistor of highest resistance. The MSB operates S<sub>n-1</sub> assuming that the resistors R<sub>0</sub>, R<sub>1</sub>, R<sub>2</sub>, R<sub>3</sub>, ..., R<sub>n-1</sub> are weighted so that their numerical significance of the corresponding binary digit. The operation of the inverter depend on the resistance value of successive resistors being related by a factor of 2 and does not depend on the absolute value of the resistor.

#### Observation Table :-

$S_2$	Input (in volt)		Output (in volt)
	$S_1$	$S_0$	
4.9	4.9	4.89	3.32
4.89	4.9	0	3.08
4.89	0	4.9	2.86
4.9	0	0	2.50
0.01	4.9	4.9	2.30
0.01	4.89	0	1.82
0.01	0.01	4.9	1.2
0.01	0.01	0.01	0.01

Teacher's Signature:-

drive the converter need not be precisely fixed value but identifiable as to represent the one logic level or the other. When  $V_1$  corresponds to logic 1 or logic 0, the switch  $S_1$  is connected to 1 or 0. position connecting a resistor  $R_K$  to the precisely controlled voltage source  $V(1)$  or  $V(0)$  as shown. The LSB  $S_0$  operates which switch  $S_0$  which is connected to the output through the resistor of highest resistance. The MSB operates  $S_{n-1}$  assuming that the resistors  $R_0, R_1, R_2, R_3, \dots, R_{n-1}$  are weighted so that their numerical significances of the corresponding binary digit. The operation of the inverter depends on the resistance value of successive resistors being related by a factor of 2 and does not depend on the absolute value of the resistor.

### Observation Table :-

<u>Input (in volt)</u>			<u>Output (in volt)</u>
$S_2$	$S_1$	$S_0$	$V_0$
4.9	4.9	4.89	3.32
4.89	4.9	0	3.08
4.89	0	4.9	2.86
4.9	0	0	2.50
0.01	4.9	4.9	2.30
0.01	4.89	0	1.82
0.01	0.01	4.9	1.2
0.01	0.01	4.89	0.01

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Date:

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Inference :- We can observe that for various combination of logic levels ( $S_0, S_1$  &  $S_2$ ) , we get different  $D_o$  , thus it acts as a digital to analog converter.