Name - ARPAN MANDAL
Exam roll - CSE214021
Class roll - 001910501061
YEAR - 2nd SEMESTER - 2nd

SUB - MICROPROCESSOR AND ASSEMBLY LANGUAGE PROGRAMING

1.

a)

Addressing Mode :- The term addressing mode refers to the way in which the operand of an instruction is specified. The addressing mode specifies a rule for interpreting or modifying the address field of the instruction before the operand is actually executed.

Here 2050H contains 25H

(i) In direct addressing mode, the data to be operated is available inside a memory location and that memory location is directly specified as an operand

So, Here, by using direct addressing mode we can read the content of a memory 2050H by accumulator as

LDA 2050H, (load the content of memory location into accumulator)

(ii) In register indirect addressing mode, the data to be operated is available inside a memory location and that memory location is indirectly specified by a register pair.

So, In this case at first we load 2050H in H-L register pair by LXI instruction,

then we load the accumulator

So, Here instruction is

LXI H, 2050H.

MOV A, M

---

b)

MVI A, 15H → [Stored from m/m 2500H]

Here the instruction stored in memory location like

Address	Mnemonics	M-cycle	T-states
2500	MVI A		
2501			

Here opcode for instruction MVI A is 3EH, so instruction stored in memory like -

Address	Mnemonics	Hexcode	M-cycles	T-states
2500	MVI A, 15H	3E	2	7
2501		15		

So, Here steps are -

(i) at first P.C. go to 2500H, here it find the opcode for MVI A, so at first it fatches the opcode by 1 machine cycle, The time taken by the processor to execute opcode fatch cycle is 4T / 4 T-states

(ii) then P.C. incremented and it performs memory read machine cycle ; to execute

this there need 3 T-States

So, Here to perform 2 byte instruction we need 2 machine cycle = 1 for opcode fatch + 1 for m/m read and 7 T-States = 4 for opcode fatch + 3 for m/m read.

c)

(i) MOV A, M

It moves the 8 bit Content of memory address stored at H-L register pair, to accumulator

[A] ← [[H-L]]

Let, H-L register pair have 2050 H

∴ [H] = 20H [L] = 50H

let, 15H Stored at 2050H memory address.

So, by Instruction MOV A, M, 15H stored at accumulator

(ii) LXI H, 2050H;

by this instruction 2050 H Stored at H-L register pair i.e. -[H] ← 20H [L] ← 50H

So, [H-L] = 2050H

(iii) LHLD 3000H

This instruction load H-L register pair with the Content of 3000H and 3001H, ie. →

[L] ← [3000H] and [H] ← [3001H]

(iv)

RAR ;

This instruction Rotate accumulator right through carry i.e →

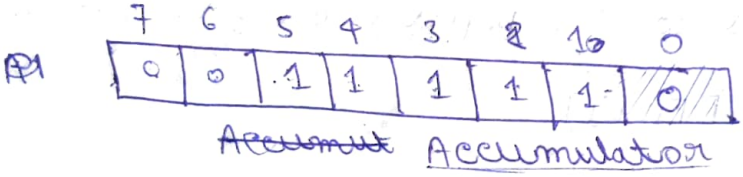
$[A^n] \leftarrow [A^{n+1}]$ { for $n = 6-0$ }

$[A^7] \leftarrow [CS]$ and $[A^7] \leftarrow [CS]$

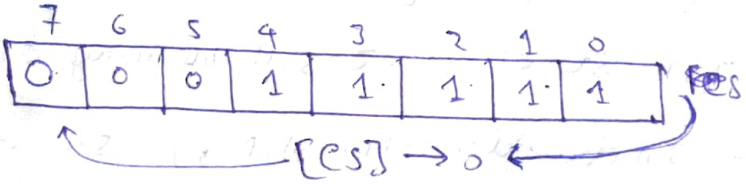
e.g

Let content of the accumulator is 3EH

[A] ← 3E



If we perform RAR then



3. a)

Last digit of my exam roll no. is

Y = 1

we have 2, 2K [$2K \approx 2^{11}$] chips

Starting address of first chip is 1000H

we need 800H memory location to interface 2K memory [$\because 2^{11} = 800H$]

So,

For ~~2K~~ chip M_1 of 2K memory address range ⇒

~~A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0~~

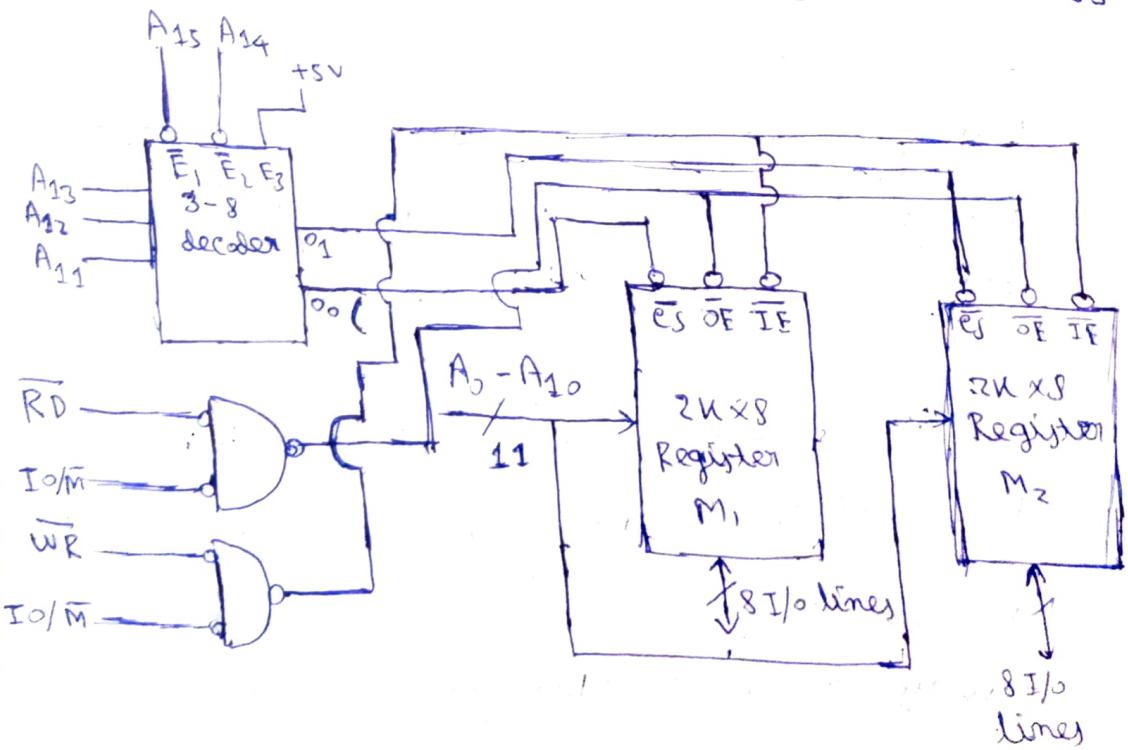
	A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0
Starting [1000H]	0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
ending [17FFH]	0 0 0 1 0 1 1 1 1 1 1 1 1 1 1 1

For, chip M_2 of 2K address range ⇒

	A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0
Starting [1800H]	0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0
ending [1FFFH]	0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1

Address decoding technique :-

Here we use a 3 to 8 decoder to decode address [we can also use NAND gate for this]



Here If $A_{13}=0$ $A_{12}=1$ $A_{11}=0$ then the decoder output O_0 activated and it activates M_1 and If $A_{13}=0$, $A_{12}=1$, $A_{11}=1$, then the O_1 line activated and it activates M_2 by activating $\overline{CS}$.

Thats how address decoding occures

b)

Partial decoding :- partial decoding occurs when we cannot use all the address lines of address bus in microprocessor.

In case of 4K byte memory interfacing we need only 12 lines because $2^{12} \approx 4K$ but there present 16 address lines in address bus. So, Here 4 buses have fixed input in this case and we can't utilise 16 address lines because we have not 2^{16} byte memory present in the RAM.

Here in case of above question for 4K byte memory interfacing we have address banges from 1000H to 1FFFH So Here $A_{15}, A_{14}, A_{13}, A_{12}$ are always respec-tively 0,0,0,1 So this lines cannot be

utilised.

For each combination of dont care address lines we have separate address ranges but size of the range is same in each case. Keeping one combination as primary address range, remaining address ranges are called foldback or mirror memory

In our case wrt above question we use the combination $A_{15}\ A_{14}\ A_{13}\ A_{12}$ as 0 0 0 1 for primary address range. So, 1 1 1 , 1 0 0 1 etc are mirror addresses

So, we have $2^4 - 1 = 15$ such combinations of foldback memory in this case

---

Q. a) Solution :-

JNZ Loop2

HLT

b) My exam roll no. is

5. a)

Last digit of my exam Roll = 1 So, i = 1 % 8 = 1

	MVI	D, 00H	D stores the carry
	MVI	B, 00H	B = Stores the value N
	MVI	C, 00H	C stores the sum
	LDA	2200H	[A] ← [2200H] : A = M
	CPI	00H	
	JZ	FINISH	If N = 0 then finish
	MOV	B, A	B = A = N [B] ← [A]
	LXI	H, 2500H	[H-L] ← 2500 H [First address]
Loop:	MOV	A, M	[A] ← [2500H]
	ANI	02H	And A with 02 H
	JNZ	SKIP	
	MOV	A, M	[A] ← [2500H]
	ADD	C	A = C + A
	JNC	SKIP2	
	INR	D	If carry generated then D is incremented by 1 each time
SKIP2:	MOV	C, A	
SKIP:	INX	H	[H-L] ← [H-L] + 1
	DCR	B	[B] ← [B] - 1 for Loop purpose
	JNZ	Loop	
FINISH:	MOV	A, C	[A] ← [C]
	STA	2300H	Sum is stored at 2300 and If carry
	MOV	A, D	generated then
	STA	2301H	Stored at 2301 H
	HLT		

(8)

i) Let the delay subroutine be called DLY

```
DLY:  PUSH  D   ; we will use DE
      MVI   E   , XXH ; we will fill it
Loop: DCR   E   ;          XXH later
      JNZ   Loop; execute silent
      POP   BD  ; restore BC
      RET       ; subroutine finished
```

Total time taken for the & execute the subroutine = (Time taken for 1 T-state) *
× [(T-States for CALL DLY)
+ (T-States for PUSH B)
+ (T- States for MVI E)
+ (T States for loop XXH)
- 3T-state {exciting condition in JNZ Loop takes 3 T-states less}
+ (T-States for POP B)
+ (T-States for RET)]

= TS × [18 + 12 + 7 + (4+10)×X - 3 + 10 + 10]

[∵ TS = time needed for 1 T-State]

= Here frequency = 2 MHz So time needed for 1 T-state = $\frac{1}{2\times10^6}$ S = 5×10^{-4} ms = TS

So, from the given data in question we can say

* 5×10^{-4} [18 + 12 + 7 + 14 × (X X) - 3 + 10 + 10] = 1

$\Rightarrow 5 \times 10^{-4}[54 + 14 \times XX] = 1$

$\Rightarrow 54 + 14\,XX = \frac{1}{5 \times 10^{-4}}$

$\Rightarrow 54 + 14\,XX = \frac{10 \times 10 \times 10 \times 10}{5}$

$\Rightarrow 54 + 14\,XX = 2000$

$\Rightarrow XX = \frac{2000 - 54}{14} = \frac{1946}{14} = 139$

So, $(XX)_{10} = 139 \Rightarrow$ 8B H. in

So, XX is 8BH in Hexadecimal

Hence final subroutine is $\Rightarrow$

```
DLY:  PUSH D
      MVI  E, 8BH
Loop: DCR  E
      JNZ  Loop
      POP  D
      RET
```

146
14 / 2000
   - 54
  2046
  2000
  - 54
  1946

8 54
- 42
  126