BCSE II

Digital Logic and Circuits – Class Test – II [SET – 2425]

GROUP – A

CO3 – [marks 5+10]

1. Show the logic diagram of a JK flip-flop. Give the flip-flop characteristic table. What is a RACE AROUND condition?
2. Design a synchronous counter for a sequence 0 → 2 → 4 → 6 → 7 → 0. Use JK Flip-flop for the circuit.

GROUP – B

CO3 and CO4

3. Write the full form of SSI. Why is it called SSI? [1+1]
4. Draw and explain the NAND gate using CMOS [4+4].
5. What is the function of diode in the path of totem-pole output stage in a standard TTL gate? [2]
6. Why ECL is faster than TTL? [2]
7. Write the definition of Fan-in. [1]

Alternative question for GROUP B

8. *What is a synchronous counter? Draw the timing diagram of a 4-bit –ve edge triggered synchronous counter. [5]*

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Digital Logic and Circuits – Class Test – II [SET – 1324]

GROUP – A

CO3 – [marks 5+10]

1. Show the logic diagram of an SR latch. Show the changes in the output signals for the following changes in inputs:
   Initially, R=1 and S=0; then R=0 and S=0; R=0 and S=1; R=1 and S=1; and finally R-0 and S=0.
2. Design a synchronous counter for a sequence 0 → 1 → 3 → 5 → 7 → 0. Use JK Flip-flop for the circuit.

GROUP – B

CO3 and CO4

3. Draw and explain the inverter gate using CMOS. [5]
4. Write the full form of VLSI. Why is it called VLSI? [1+1]
5. What are the advantages of ECL over other IC technologies? [2]
6. What is the function of diode in the path of totem-pole output stage in a standard TTL gate? [2]
7. Draw and explain RTL Using NOR gate. [4]

Alternative question for GROUP B

8. *What is a ripple counter? Draw the timing diagram of a 4-bit +ve edge triggered ripple counter. [5]*

BCSE II

Digital Logic and Circuits – Class Test – II [SET – 4822]

CO3 – [marks 4+5+6]

1. Show the state diagram of an RS latch. What is RACE condition in RS latch?
2. With a timing diagram explain the functioning of a 4-bit Serial-in to Parallel-out Shift Register.
3. What is the difference between a synchronous and an asynchronous counter? Draw a 2-bit asynchronous and a 2-bit synchronous counter.

GROUP – B

CO3 and CO4

4. Write the full form of LSI. Why is it called LSI? [1+1]
5. Draw and explain the NAND gate using TTL. [4+4]
6. Why ECL is faster than TTL? [2]
7. What is the function of diode in the path of totem-pole output stage in a standard TTL gate? [2]
8. Write the mode of operation of MOSFET. [1]

Alternative question for GROUP B

8. Show the logic diagram for a 3-bit down counter. Draw its timing diagram. [5]

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Digital Logic and Circuits – Class Test – I [SET – 2753]

CO1 – [marks 4+4]

1. Convert the following decimal numbers to their binary forms and find the results of the subtraction using 2's complement. Express the results in their decimal equivalent.
   (i) 99 – 55 (ii) 78 – 109
2. Determine the odd parity bits generated for the messages consisting of BCD equivalents of 49 to 52.

CO2 – [marks 8]

3. Minimize the following expressions using Karnaugh map and obtain the minimal SOP expressions –
   i) $\sum m(1,2,3,13,15)$
   ii) $\sum m(1,3,4,6,9,11) + \sum d(2,5,7)$

CO3 – [marks 8+6]

4. Draw an even-parity checker circuit for 4-bit codewords.
5. Show the implementation of a 1x4 demultiplexer using NAND gates.

↓

2×4 decoder

BCSE II

Digital Logic and Circuits – Class Test – II [SET – 3624]

CO3 – [marks 8+7]

1. Show the logic diagram of a master-slave JK flip-flop. Explain how it works.
2. Design a Modulo-5 counter.

GROUP – B

CO3 and CO4

3. Draw and explain the NOR gate using CMOS. [4+4]
4. Write the full form of MSI. Why is it called MSI? [1+1]
5. Where and why are the HTL gates used? [2]
6. What is meant by multi-emitter transistor? [2]
7. Write the definition of Fan-out. [1]

Alternative question for GROUP B

8. *What are the different types of Shift Registers? Using D Flip-flops, provide the design of a Serial In/Serial Out Shift Registers. [5]*

BCSE II

Digital Logic and Circuits – Class Test – I [SET – 2931]

CO1 – [marks 4+4]

1. Convert the following decimal numbers to their binary forms and find the results of the subtraction using 2's complement. Express the results in their decimal equivalent.
   (i) 126 – 53 (ii) 37 – 74 (4) +
2. Determine the odd parity bits generated for the messages consisting of BCD equivalents of 61 to 64.

CO2 – [marks 8]

3. Minimize the following expressions using Karnaugh map and obtain the minimal POS expressions –
   i) $\sum m\,(0,2,8,12,13)$ (8) +
   ii) $\sum m\,(1,3,7,11,15) + \sum d\,(0,2,5)$

CO3 – [marks 10+4]

4. A combinational circuit has four inputs and one output. The output is equal to 1 when (a) all the inputs are equal to 1 or (b) none of the inputs are equal to 1 or (c) an odd number of inputs are equal to 1.
   i) Obtain the truth table;
   ii) Find the simplified output function in product of sums;
   iii) Implement a combinational circuit using NAND gates.
5. Draw a full adder circuit using AND, OR and NOT gates.

(6) + 3 + 3 (4) +

$(\bar{c}+D)(\bar{c}+D)$

D

126
53
73

2 | 73
2 | 36 – 1
2 | 18 – 0
2 | 9 – 0
2 | 4 – 1
2 | 2 – 0

BCSE II

Digital Logic and Circuits – Class Test – I [SET – 2842]

CO1 – [marks 3+4]

1. Convert $(155.5)_{10}$ to binary and hexadecimal.
   Next perform binary addition of this number with binary equivalent of $(403.77)_{10}$
   (Use up to 4 decimal places of the binary numbers).
2. Find the hamming distances between each pair of the following codes. What is the minimum hamming distance? Is it an error correcting code? Justify.
   010010, 111001, 100001, 101010

CO2 – [marks 3+4]

3. Simplify Y= A + A'B +A'B'C +A'B'C'D
4. Convert the following to the other canonical form:
   i) $F(x,y,z) = \sum(1, 3, 7)$
   ii) $F(A,B,C,D) = \Pi (0, 1, 2, 3, 4, 6, 12)$

CO3 – [marks 8+9]

5. Design a circuit that compares two 3-bit numbers, A and B and produces a 1 output if the two numbers are equal, else it produces a 0 output.
6. Using a decoder and external gates, design the combinational circuit defined by the following Boolean functions:
   (a) $F1 = (y' + x)z$ (b) $F2 = xy'z' + x'y$ (c) $F3 = (x' + y)z$

BCSE II

Digital Logic and Circuits – Class Test – I [SET – 2664]

CO1 – [marks 3+4]

1. Convert $(225.25)_{10}$ to binary and hexadecimal.
   Next perform binary addition of this number with binary equivalent of $(403.77)_8$
   (Use up to 4 decimal places of the binary numbers).
2. Find the hamming distances between each pair of the following codes. What is the minimum hamming distance? Is it an error correcting code? Justify.
   110100, 111111, 000111, 001100

CO2 – [marks 3+4]

3. Simplify the given expression Y= A'B + ABD + AB'CD' + BC
4. a) Given the function, $F(A,B,C,D) = D(A' + B) + B'D$, express it as sum of minterms.
   b) Given the function, $F(A,B,C) = (A' + B)(B' + C)$, express it as product of maxterms.

CO3 – [marks 10+6]

5. Design a combinational circuit whose input is a three-bit number and output is the 2's complement of the input number.
6. Using a decoder and external gates, design the combinational circuit defined by the following Boolean functions:
   (a) F 1 = x'y'z' + xz (b) F 2 = xy'z' + x'y