EX/CSE/T/223A/81/2016

B. CSE 2ND YEAR 2ND SEMESTER EXAMINATION 2016

MICROPROCESSOR AND ASSEMBLY LANGUAGE PROGRAMMING

Time: Three Hours

Full Marks: 100

Answer any ***four*** questions

1. a) What is addressing mode? Describe different addressing modes of 8085 μP with examples.

   b) Let the instruction MVI A, AB_H is stored from m/m location 2500_H. Write the sequence of steps of fetch cycle and execution cycle to execute the instruction. 5

   c) Write the functions of the (i) MOV A, M (ii) LXI H, 2050_H (iii) LHLD 3000_H and (iv) RAR instructions with proper examples. 2+2+2+2

   2+10

2. (a) Interface 3K memory as two memory chips (modules) of 2K (M1) and 1K (M2) beginning at address 4000_H using suitable decoders. Explain its address decoding technique and find its RAM address range. Assume/generate appropriate signals and pins. 10+5

   b) What is partial decoding? Explain foldback memory using the data given in 2. (a). 5+5

3. a) Describe the sequence of steps required for data transfer between microprocessor and an I/O device with appropriate schematic diagram. 10

   b) Write the sequence of steps for DMA operation. 5

   c) Describe a scheme with a schematic diagram to resolve multiple interrupts from two or more peripherals simultaneously through INTR line. 10

4. a) A set of N data bytes is stored in m/m locations starting from 2501_H. The value of N is stored in 2500_H. Write a program (with comments) to store these data bytes from m/m location 2600_H if D_0 and D_7 are 1; otherwise reject the data byte. 13

   b) Write a program (with comments) to find the sum of even bytes out of N bytes stored in consecutive locations starting from 2500_H. The value of N is stored in 2200_H. Store the result in locations 2300_H and 2301_H. 12

5. a) There are N bytes stored from m/m location 2500_H. The value of N is stored in 2400_H. Write an 8085 program (with comments) to interchange the bits D_6 D_1 of these bytes and store them into the m/m locations starting from 5050_H. 13

   b) Write a program (with comments) to compute $2X^2$. The value of X is stored in 2050_H. Store the results in 2052_H and 2053_H. 12

6. a) Describe the functions of BIU and EU of the 8086 μP using their schematic diagrams. 10

   b) Describe how program execution speeds up in 8086 μP? 5

   c) If the CS register contains 2050_H and IP register contains $3BA2_H$, what is the physical address of the instruction to be fetched? 5

   d) What are the advantages of segmentation based approach to m/m accessing in 8086 μP. 5