Ring Amplifier for Scalable Amplification

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***Abstract*—In this report, the fundamental idea of ring amplifier is discussed. Ring amplifiers can perform efficiently in nanoscale CMOS technology as it has technology scaling benefits. The basics of the ring amplifier stabilization mechanism are explored. Ring amplifier operation phases are discussed in detail along with time-domain analysis. Some key advantages of ring amplifiers are presented. Few design considerations of the same are discussed. Correlated level shifting (CLS), a method to enhance the performance of ring amplifiers is discussed. This technique will reduce the effects of finite operational amplifier(opamp) gain and improve output voltage swing limitations in amplifiers.**

***Index Terms*-Ring amplifier, technology scaling, correlated level shifting (CLS), switched-capacitor amplifier.**

I. Introduction

As we are moving towards lower technology nodes, designing amplifiers has become more challenging. With scaling down the technology nodes, supply voltage is also reducing. As a result performance of conventional opamp is declining. There are not many amplifier topologies that can perform efficiently in nanoscale CMOS. The effect of this can be observed in the performance of ADCs, where amplifier-less ADC topologies (SAR) are performing better than the ADC topologies that heavily depend on underlying amplifiers [1]. The amplifier has become the bottleneck of ADC's performance in a scaled environment.

Ring amplifier is a scalable alternative of conventional amplifier in switch capacitor circuits. Ring amplifier has a simple design and it consists of cascade of inverters. It can charge efficiently using slew based charging, also have a near rail to rail output swing[2]. Though the ring amplifier has a simple architecture whose main building block is an 'inverter', the design of the ring amplifier is not straightforward. To achieve desired gain, speed, power requirement, and noise optimum sizing of the ring amplifier stages have to be reached.

In this paper, the ring amplifier working and its use are discussed. Section II describes the basic working of the ring amplifier. The details of ring amplifier operation and stabilization theory is discussed in section III. Some advantages of ring amplifiers are discussed in section IV. A study of ring amplifier design considerations is presented in section V. A method to enhance ring amplifier performance by resolving finite amplifier gain limitations is discussed in section VI.

II. Ring Amplifier Basics

Multiple topologies are available for ring amplifier realization. They have their advantages and disadvantages in terms of accuracy, efficiency, and speed. One such implementation is shown in Fig. 1. Some of the basic operations is addressed within the context of Fig. 1.

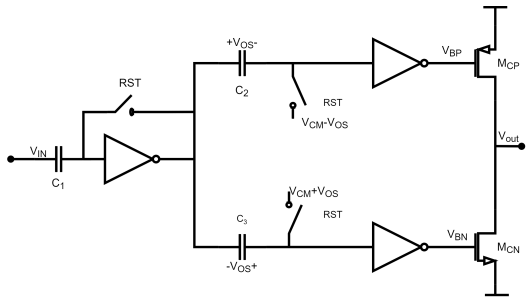

Fig. 1. Ring Amplifier Structure

A ring amplifier is a multi-stage amplifier consisting of inverter stages as shown in Fig. 1. A ring amplifier basically is a stable ring oscillator with signal path separated into two or more different paths. Ring amplifier can be stabilized by making a dominant pole. In this case, either internal pole p1 or external pole p3 can be pushed at low frequency. Miller's compensation technique can be used to make p1 a dominant pole. But this will increase capacitive loading at the internal node significantly. This can slow down the operation. So as an alternative, the external pole p3 can be made dominant using progressive reduction of overdrive voltage[2]. The output resistance of the third stage increases. As a result, this forms a dominant output pole with the load capacitance and stabilizes the ring amplifier. For optimum output pole location first, p1 and p2 can be placed at the highest possible frequency, then adjust p3 location until we have sufficiently low, stabilizing frequency. To get proper phase margin we need a few orders of magnitude separation between dominant and subdominant poles.

To ensure dynamic stabilization, the signal path is divided into two different paths. Into each signal path, a different offset is embedded to create a range of input values for which neither output transistor M_{CN} nor M_{CP} of Fig. 1 will fully conduct. This deadzone needs to be sufficiently large to stabilize the ring amplifier[1]. The resulting waveforms of Fig. 3 are produced by the ring amplifier charging and stabilizing operation upon placing in the switched capacitor feedback structure of Fig. 2. Before analyzing this behavior, it is useful to discuss some basic understanding of the structure itself. To

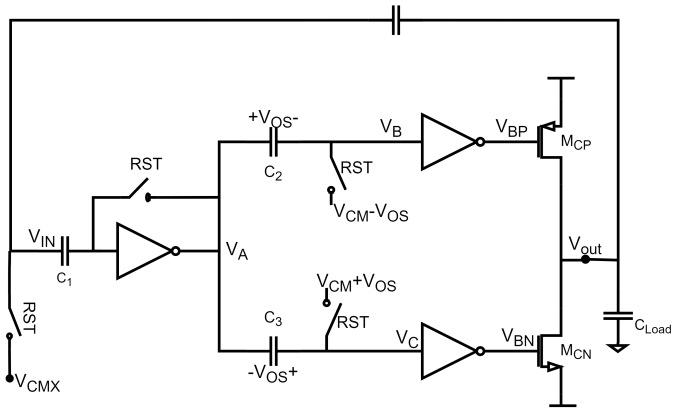

Fig. 2. Ring Amplifier in Switch Capacitor Feedback

begin with, consider the capacitor C_1 of Fig. 2. This makes V_{CMX}, the ideal settled value for V_{IN} independent of the actual inverter threshold. The offset voltage in the dual signal path is applied with the help of capacitors C_2 and C_3 placed before the second stage. There are many other ways for how and where to apply deadzone offset voltage into ring amplifier. According to design specifications, they have their advantages and disadvantages. By embedding offset voltages before the second stage we can set the dead zone voltage accurately and linearly with a high impedance.

III. Ring Amplifier Operation[1]

Complete understanding of the ring amplifier operation theory is quite complex, although ring amplifier's underlying structure is simple. The analysis of ring amplifier is a little different than the preferred approach in opamp design.

We can divide the operation theory into many simple subconcepts. Mainly ring amplifier operation in time can be subdivided into three phases: slewing, stabilization, and steady-state. These phases can be seen in Fig. 3. This is obtained from ring amplifier of Fig. 2. For analysis of different phases, this has been designed at the edge of stability and with low bandwidth. Obviously, real designs are not made in this way. This is done for the analyzing purpose only. Generally V_{OUT} is not shown for the sake of simplicity. As V_{OUT} is basically a scaled, shifted, signal-dependent replica of V_{IN}.

A. Initial Ramping

A ring amplifier is a dynamic system. At the start of operation poles will be placed much tighter such that probably in fact it will be an unstable oscillator type of system with negative phase margin but very high bandwidth, so very fast operation. Initially, ring amplifier operation starts with slew-charging. In this slew phase, the maximum possible overdrive voltage is applied to one of the output transistors for a given supply voltage. The selected output transistor (M_{CN} or M_{CP}) then performs as a maximally-biased current source and charges the output load with a ramp. There is an overshoot because of the delay of the system, which is given by

$$\Delta V_{overshoot} = \frac{t_d \times I_{RAMP}}{C_{OUT}} \tag{1}$$

where t_d is the finite time delay of the design, I_{RAMP} is the third inverter stage current while slewing and C_{OUT} is the output load capacitance.

B. Stabilization

After the initial slew phase, the ring amplifier will start oscillating near the target settled value. When no dead-zone is applied ring amplifier behaves like a three-inverter stage ring oscillator and will keep on oscillating indefinitely. The ring amplifier path is subdivided into two signal paths with an offset applied to each path. Due to this at each successive step of oscillation, the gate voltage applied to the third stage output transistors keep on reducing progressively. This is the most fundamental ring amplifier stabilization mechanism and leads to the successive reduction in the signal amplitude of the voltages V_{BP} and V_{BN}. As the average overdrive voltage applied to the output stage decreases, the output current also decreases. As a result the overshoot(which is proportional to output current) also decreases. This ripple effect leads to stabilizing the ring amplifier.

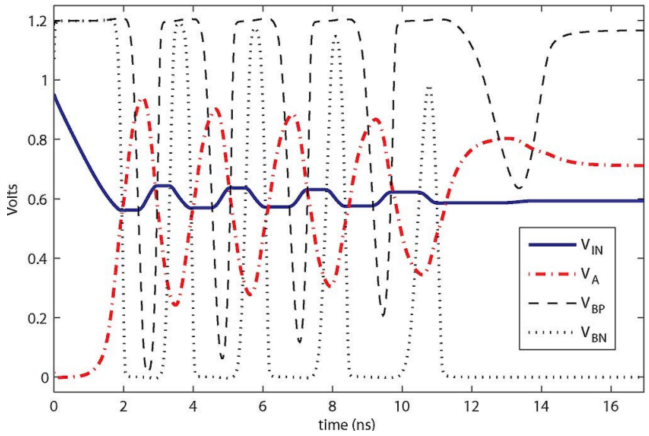

Fig. 3. Input Output Charging Waveform of Ringamp Placed in Switched Capacitor Circuit[1]

C. Steady State

At steady-state conditions, the output transistors of the ring amplifier operate in the subthreshold or complete cutoff. The input signal lies within the range of the dead-zone. The external pole pushed to the stabilized low frequency. The overdrive voltage of the output transistors is low, so is the output current. As a result, we can achieve a high output swing.

IV. Ring Amplifier Advantages

Ring amplifier function and construction are quite different from a conventional amplifier. Due to its inverter-based structure ring amplifier finds some benefits in the recent low voltage, nanoscale CMOS process.

A. Slew Based Charging[4]

In the initial slew state, output transistors drive with the highest possible overdrive voltage for a given supply voltage. One of the output transistor work as a maximally biased current source. So we can drive large capacitive loads even with small transistor sizes. We can get a high slew rate from small transistors. With the small size of output transistors, the second stage is negligibly loaded. This effectively removes the dependence of internal power requirement from the output load size. The output load capacitance does not affect the internal power requirements. This unique property of the power-loading relationship stands in stark contrast to that of a conventional opamp, where settling speed is typically proportional to $\frac{g_m}{C_{LOAD}}$.

B. Performance with Scaling[4]

For a ring amplifier to be truly scalable it must operate efficiently in a scaled environment. The ring amplifier performance improves with scaling down technology nodes. The ring amplifier is structurally similar to a ring oscillator. This is the main reason for the ring amplifier's performance with technology scaling. Even foundries use ring oscillators as a performance benchmark for a given technology node. The power consumption of conventional opamps depends on output load size. Whereas in ring amplifier internal power consumption mainly depends on power delay product of inverter and parasitics at internal nodes. There is a linear relationship between inverter power-delay product and feature size. As feature size decreases, inverter power-delay also decreases. The chain propagation delay, t_d, of ring amplifier scale down with decreasing feature size. This reduction results in improving the design specifications of the ring amplifier. This leads to enhancement of ring amplifier speed, power, and accuracy. Also, the static current reduces as we scale down, which helps in minimizing power consumption.

C. High Output Swing

In a steady-state, the output transistors (M_{CN} or M_{CP}) operate at subthreshold or cut-off region. The applied overdrive voltage at output transistors is less, so is the output current. As a result, we can have almost rail to rail output swing.

V. Ring Amplifier Design Considerations

Despite having an inverter-based simple architecture, designing a ring amplifier need some effort, as we have to find optimum sizing of each stage for given gain, noise, speed, and power requirements.

A. Gain

The ring amplifier's small signal gain is multiplication of gain of its all stages. The small-signal gain of a single inverter is given by:

$$A_v = (g_{mP} + g_{mN})(r_{oP}||r_{oN}) \tag{2}$$

where r_{oP},r_{oN} denote output resistance and g_{mP},g_{mN} denote transcoductance of PMOS and NMOS respectedly. This gain has a strong dependence on the channel length((L) of the transistor. The gain will increase with increasing L, but the parasitic capacitance also increases with L. As a result of this bandwidth(BW) got reduced. This results in increasing ring amplifier settling time. So there is a trade-off between gain and bandwidth. Thus, the BW can be maximized by choosing the smallest L which will satisfy the gain requirement. The inverter trip point is affected by each inverter stage PMOS and NMOS transistors size ratio. As a result, this also affects the output voltage swing.

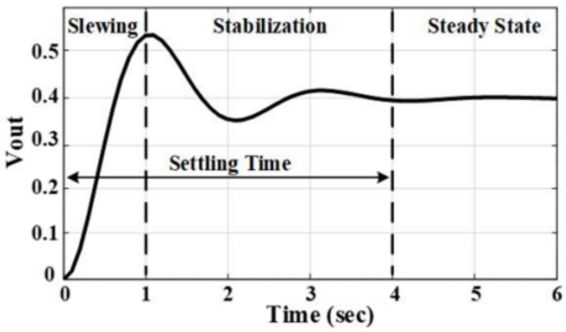

Fig. 4. Transient Output of Ring Amplifier Placed in Switched Capacitor Circuit[3]

B. Speed

The settling time consists of stabilization time and slewing time. This can be seen in Fig. 4. The ring amplifier speed is defined by the settling time. This time will depend on the ring amplifier's bandwidth. The ring amplifier begins its working with slew-charging or initial ramping. The slew rate is given by:

$$SR = \frac{I_{RAMP}}{C_L} = \frac{\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS,3} - V_{TH})^2}{C_L} \tag{3}$$

where I_{ramp} is the third inverter stage current during slew phase, and V_{TH} is the threshold voltage of MOSFET. It can be seen that the slew rate has a proportional relationship with the third stage inverter width(W/L). The overshoot voltage after the slew phase is given by (1). For proper operation of ring amplifier along with having positive phase margin, this overshoot voltage needs to be reduced. To have a positive phase margin is important but not sufficient to ensure appropriate operation.

Third stage inverter size of ring amplifier can control slew rate and delay can be controlled by the first two stage inverters. For proper operation of ring amplifier a balance between these two need to be achieved. Thus to obtain a good design it is needed to set the third inverter stage (W/L) to have a satisfactory slew rate with reference to the required settling time. The second stage sizing is adjusted in order to minimize the first two stages delay. Thus, to have the appropriate settling time, a balancing point needs to be reached between the sizing of the second stage and the third stage of the inverter. So there is a compromise between the T_{delay} and slew rate.

C. Noise

The noise performance is dominated by thermal noise. The first inverter stage is the major contributor of noise[8]. The thermal noise of an inverter is given by:

$$\overline{V_{n,in}^2} = \frac{4KT\gamma}{g_{mN1} + g_{mP1}} \tag{4}$$

where $\overline{V_{n,in}^2}$ is the input-referred thermal noise, K is Boltzmann constant, T is the temperature in Kelvin, γ is a process dependent parameter.

So for lower input-referred noise, we need higher transconductance. As transconductance increases power requirement of that stage also increases. So comparatively first stage of the ring amplifier requires more power to limit the noise.

D. Design Approach[4]

First, we have to select L, length of the MOSFETs of all the stages for suitable gain. The first stage inverter width(W1) is selected according to desired noise performance. The second stage inverter width(W2) is selected following the required delay, which is needed to minimize $V_{overshoot}$. Then choose the (W/L) ratio between NMOS and PMOS to adjust the inverter's trip-point to V_{CM}. This ratio is set to increase the voltage swing at the output. The settling time requirement derives from the slew rate requirement. The third stage inverter width is chosen to achieve the required slew rate.

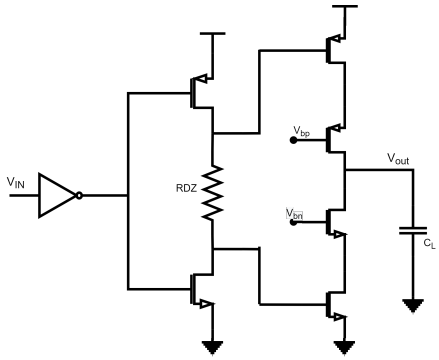

Fig. 5. Cascode Ring Amplifier Structure

E. Cascode Ring Amplifier[5]

We can increase the number of stages in the ring amplifier to increase gain but it will create complications. The power consumption will increase, propagation delay will also increase disrupting the stability. Increasing the output impedance of the first two stages have issues as well. The pole frequency associated with that stage reduces. To preserve the stability of ring amplifier via dominant pole, further reduction of output pole frequency must be made.

Increasing the output stage impedance by increasing L of output stage transistors is a good option. But increasing the device length of the output stage results in the reduction of slew rate. To recover the loss of slew current, if device width is increased, then it makes right-hand zeros coming close to entering into amplifiers bandwidth. In order to increase the output impedance of the output stage, cascode devices can be added to the output stage while mitigating the effects of RHP zero. Additional poles will be there at cascode node but the physical size of the output stage can be kept small and these poles will be at high frequency. A fixed bias cascoded output stage is shown in Fig 5.

VI. Ring Amplifier Performance Enhancement

Due to finite amplifier gain, the output is unable to reach the desired level. Finite amplifier gain also limits the output swing. For low voltage, nanoscale operation these limitations are even more critical. For switched-capacitor circuits, the correlated level shifting (CLS) technique effectively improves the system accuracy. Correlated level shifting (CLS) is a new technique that can allow the rail to rail operation and reduce the error due to finite amplifier gain.

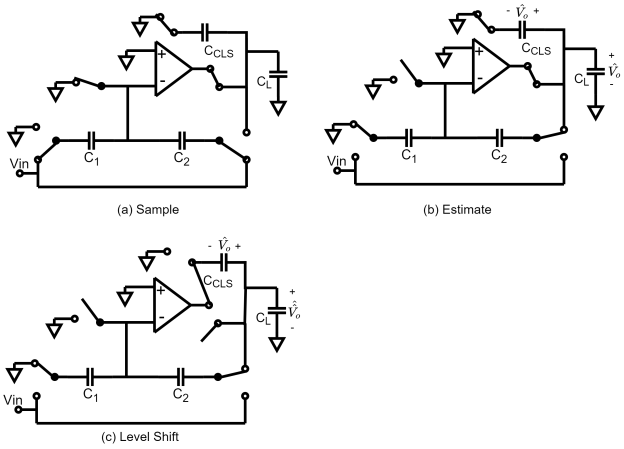

Fig. 6. CLS Phases

A. CLS operation

In CLS[6], there are three operation phases: 1) sample input, 2) estimate output signal and store it on C_{CLS}, 3) level shift to eliminate signal from an opamp. The C_{CLS} capacitor can be reset during the sample phase to eliminate memory effects.

The circuit in Fig. 6 can be analyzed to show that the output voltage at the end of the estimation phase is

$$\hat{V_o} = V_{in}(1 + \frac{C_1}{C_2})(\frac{1}{1 + \frac{1}{T}}) \tag{5}$$

where $T = \frac{A_{EST}C_2}{C_1+C_2+C_{in}}$ is the opamp loop gain during the estimation phase. This first estimate $\hat{V_o}$ is smaller in comparison to the error-less output (i.e. $V_o = V_{in}(1 + \frac{C_1}{C_2})$) because an imperfect virtual ground is produced due to finite amplifier gain, so the complete charge is not transferred to C_2 from C_1. Due to imperfect virtual ground the residual voltage on C_1 is

$$V_{C1(EST)} = \frac{-\hat{V_o}}{A_{EST}} \tag{6}$$

Usually, the amplifier DC gain is set as large as possible to reduce this error. Another technique to reduce this error is to make the output of the amplifier small. This is done by the CLS technique. It stores the initial estimate of the output signal on C_{CLS} and detaches it from the amplifier in the level shift phase. Output is charged through C_{CLS} in the level shift phase. Thus C_1 has a much smaller residue voltage after the level-shift phase ends. The voltage at C_1 after the level shift phase ends is:

$$V_{C1(LS)} \approx \frac{-(\hat{\hat{V}}_o - \hat{V}_o)}{A_{LS}} \tag{7}$$

where $\hat{\hat{V}}_o$ is estimated voltage after level shift phase. This is much smaller than (7). This means that almost complete charge from C_1 is transferred to C_2.

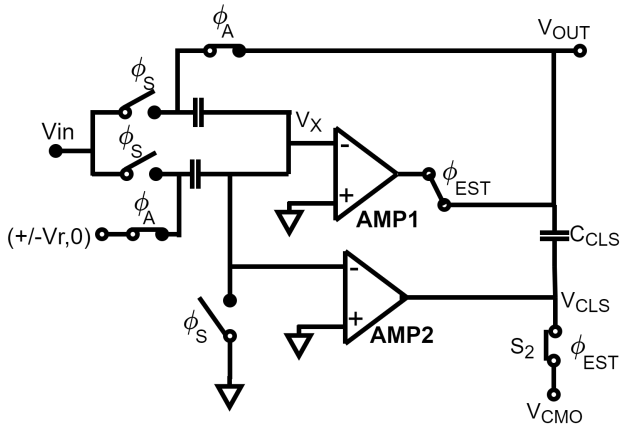

Fig. 7. Basic Split-CLS Structure

B. Split-CLS[7]

It is not necessary to use the same amplifier during the estimation phase and CLS phase. The job of a single amplifier can be subdivided into two different amplifiers and then each amplifier can be designed with its particular features to altogether boost the performance of CLS in terms of speed, power, accuracy. A generalized single-ended Split-CLS is shown in Fig. 7.

During ϕ_{EST}, the full signal is processed by AMP1. Therefore it should have large output swing and high slewing capabilities. Where AMP2 processes the small error term remaining after ϕ_{EST} and charges the output indirectly through C_{CLS}. The slew and swing requirement for AMP2 is much smaller than AMP1. The ring amplifier has a large output swing and high slew-based charging. It is an ideal candidate for AMP1. For the implementation of AMP2 double-cascode telescopic opamp can be used. It has a high gain but has the disadvantage of a small output swing due to the cascoding transistors and a low slew rate due to the lack of a high current output stage. However, neither a high slew rate nor rail to rail swing is required for AMP2. So ring amplifier for AMP1 and cadcode opamp as AMP2 can be used and the overall performance can be improved.

VII. Conclusion

A literature review of ring amplifier fundamentals is presented. The basics of ring amplifier stabilization, operation phases are discussed. Key advantages of the ring amplifier are presented. Ring amplifier has promising performance in a scaled environment. Ring amplifier is compatible with techniques like CLS, which counter finite amplifier gain problems. Due to the unique properties of ring amplifiers, their use can be explored in many other amplifier-dependent analog blocks.

References

[1] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita and U. Moon, "Ring Amplifiers for Switched Capacitor Circuits," in IEEE Journal of Solid-State Circuits, vol. 47, no. 12, pp. 2928-2942, Dec. 2012, doi: 10.1109/JSSC.2012.2217865.

[2] B. Hershberg, Un-Ku Moon, "The Ring Amplifier: Scalable Amplification With Ring Oscillators," in book: High-Performance AD and DA Converters, July. 2015, doi: 10.1007/978-3-319-07938-7-18.

[3] Z. Pei, Y. Wang and L. Han, "CMOS Ring Amplifier for Bio-Signal LNA," 2020 IEEE 4th Information Technology, Networking, Electronic and Automation Control Conference (ITNEC), 2020, pp. 319-323, doi: 10.1109/ITNEC48623.2020.9085045.

[4] K. M. Megawer, F. A. Hussien, M. M. Aboudina and A. N. Mohieldin, "A Systematic Design Methodology for Class-AB-Style Ring Amplifiers," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 9, pp. 1169-1173, Sept. 2018, doi:10.1109/TCSII.2018.2815705.

[5] C. Y. Lee, P. K. Venkatachala, A. ElShater, B. Xiao, H. Hu and Un K. Moon, "Cascoded Ring Ampli- fiers for High Speed and High Accuracy Settling," 2019 IEEE International Symposium on Circuits and Systems (ISCAS), 2019, pp. 1-5, doi: 10.1109/IS- CAS.2019.8702710.

[6] Gregoire, B. Robert. "Correlated level shifting as a power-saving method to reduce the effects of finite DC gain and signal swing in opamps." (2008).

[7] B. Hershberg, S. Weaver and U. Moon, "Design of a Split-CLS Pipelined ADC With Full Signal Swing Using an Accurate But Fractional Signal Swing Opamp," in IEEE Journal of Solid-State Circuits, vol. 45, no. 12, pp. 2623-2633, Dec. 2010, doi: 10.1109/JSSC.2010.2073190.

[8] Y. Lim and M. P. Flynn, "A 100 MS/s, 10.5 Bit, 2.46 mW Comparator-Less Pipeline ADC Using Self- Biased Ring Amplifiers," in IEEE Journal of Solid-State Circuits, vol. 50, no. 10, pp. 2331-2341, Oct. 2015, doi: 10.1109/JSSC.2015.2453332.