From Chisel to Chips in Fully Open-Source

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Open-Source SW is a BIG Success

- UC Berkeley's TCP/IP stack powers the Internet
- Gcc is used to compile Linux
- Linux runs the servers for the Internet
  - Mobile phones run with Linux
  - Linux is used in embedded devices
- Apache serves the web pages
- Java and the JVM run the cloud apps
- We can browse the Internet with OS Firefox
- Most languages have an open-source compiler

OS Hardware and Tools

- Some processor implementations are available
  - Eg., Rocket, Patmos, and some more
- Tools (simulators, synthesis) are mostly closed source
- With a few exceptions
  - Chisel as HW construction language
  - Verilator for simulation
  - Yosys and ABC for synthesis

Producing a Chip

- Is usually very expensive
- Needs expensive tools
- Needs a production development kit (PDK)
  - Closed source, NDA
- We can share a wafer with several projects
  - Multi-project wafer

Google Enters the HW Scene

- Tim Ansell was asking: what is missing to make HW design as “easy” as SW development?
  - We are missing digital designers
- How to provide incentives for students to learn hardware design?
  - The open-source infrastructure and
  - A free Chip!
    - Including test PCBs with the mounted Chip

Google and SkyWater

- SkyWater is a fab producing 130 nm chips
  - Former fab of Cypress
- SkyWater together with Google put the PDK into open source
- PDK is integrated with open-source tools
- If the hardware design is open source, Google pays the production

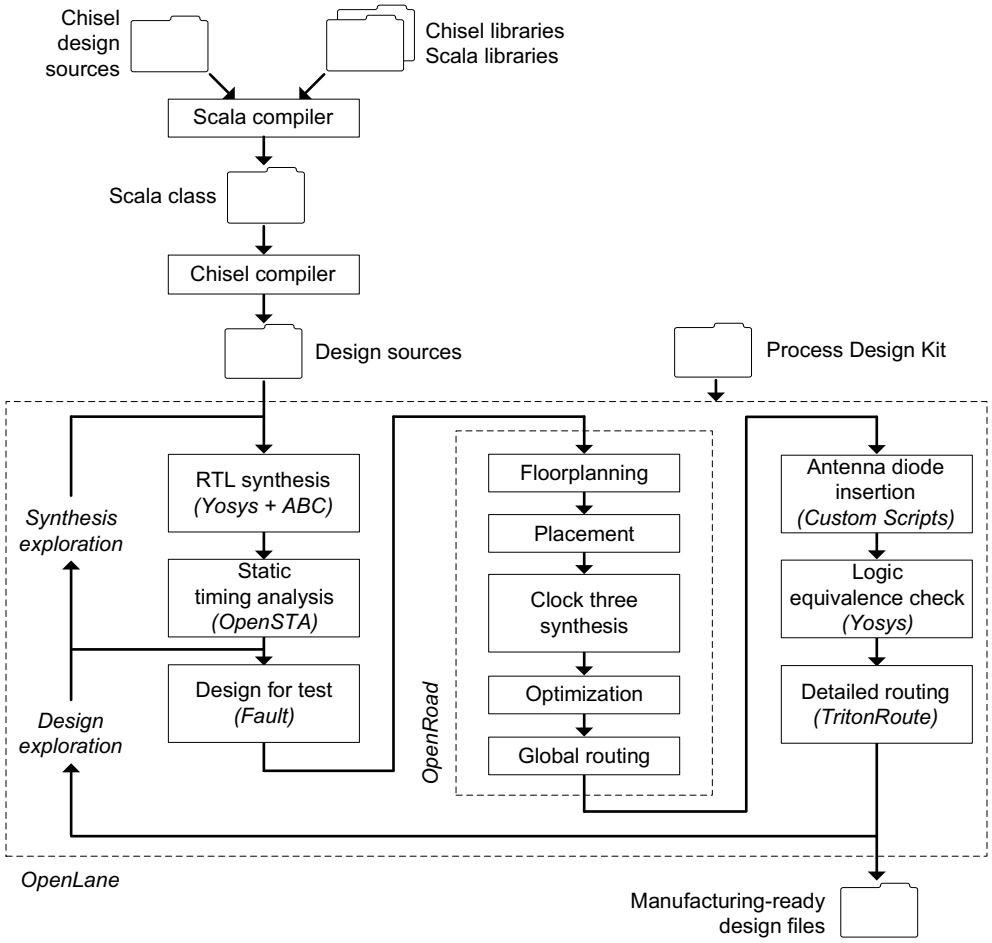
Open-Source Tools

- Chisel as a modern design language
  - I am using only Chisel since 2012
  - Teaching digital design with Chisel
  - Patmos is a processor written in Chisel
- Simulation
  - For Chisel we use Treadle for unit tests
  - For a full (Patmos) system: Verilator
  - For the chip tests Icarus Verilog

Synthesis

- YoSys as synthesis tool
  - Was a BSc project at TU Vienna (2013)
  - Now used for most OS tools flows
- ABC is integrated in YoSys
  - Translates design to primitives
  - Does the mapping
- OpenLane/Road for the rest
  - Floor planning, placement, clock tree, routing,…

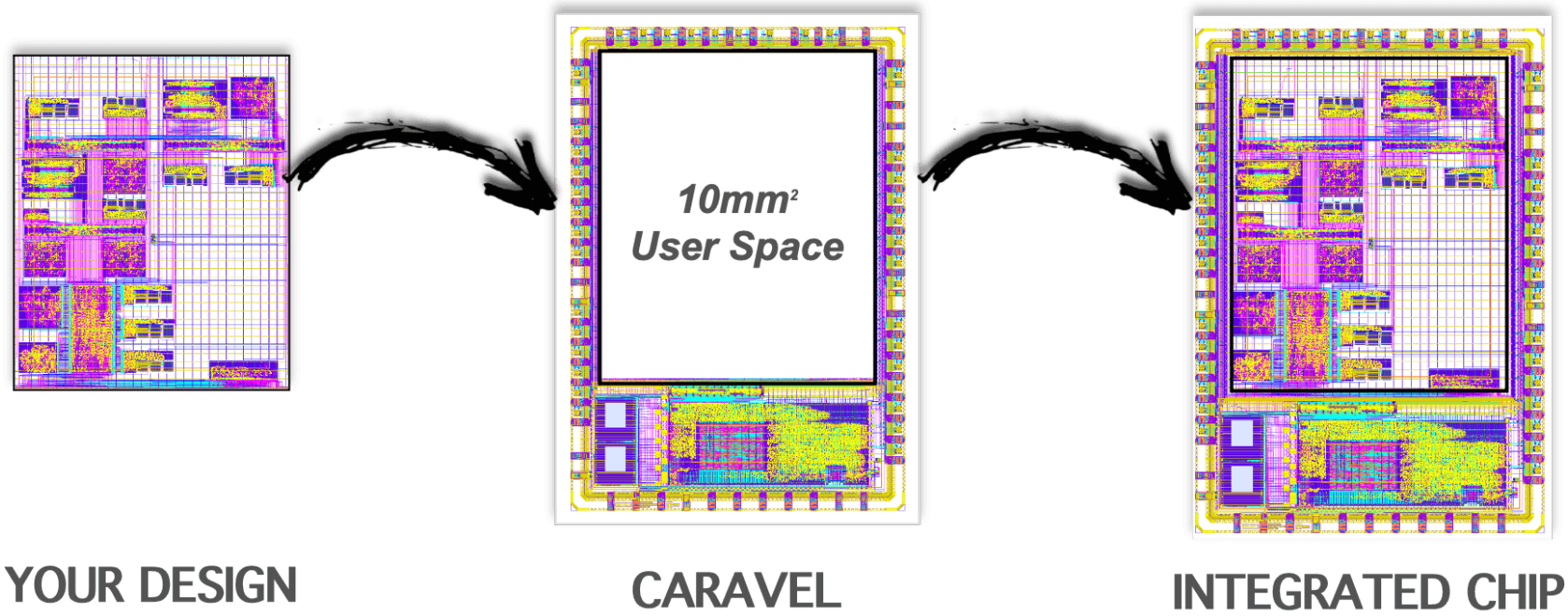
OpenLane Tool Flow



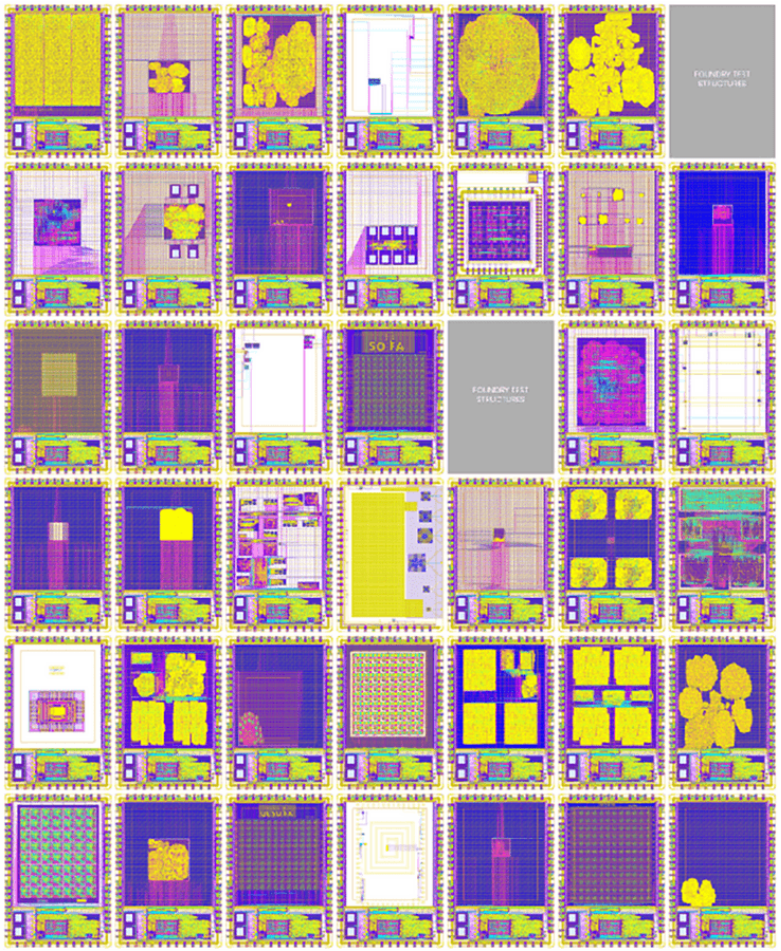
Caravel

- The harness for the design
  - With a 10 mm2 user area
- The harness contains a RISC-V processor
  - As management core
  - To communication via a UART
- Integrates all the mentioned tools
- Tests for precheck before tapeout

Caravel



A Multi-Project Waver



A Class Idea

- We (at our section) do not know the OS tools
  - Luca and me have no ASIC backend experience
- Let us explore this in a special course
- 12 students join
  - Mostly BSc in their 4th semester
- Use an open-source design (Patmos)
  - Build all needed clue components
- Get a chip from Google/SkyWater ☺

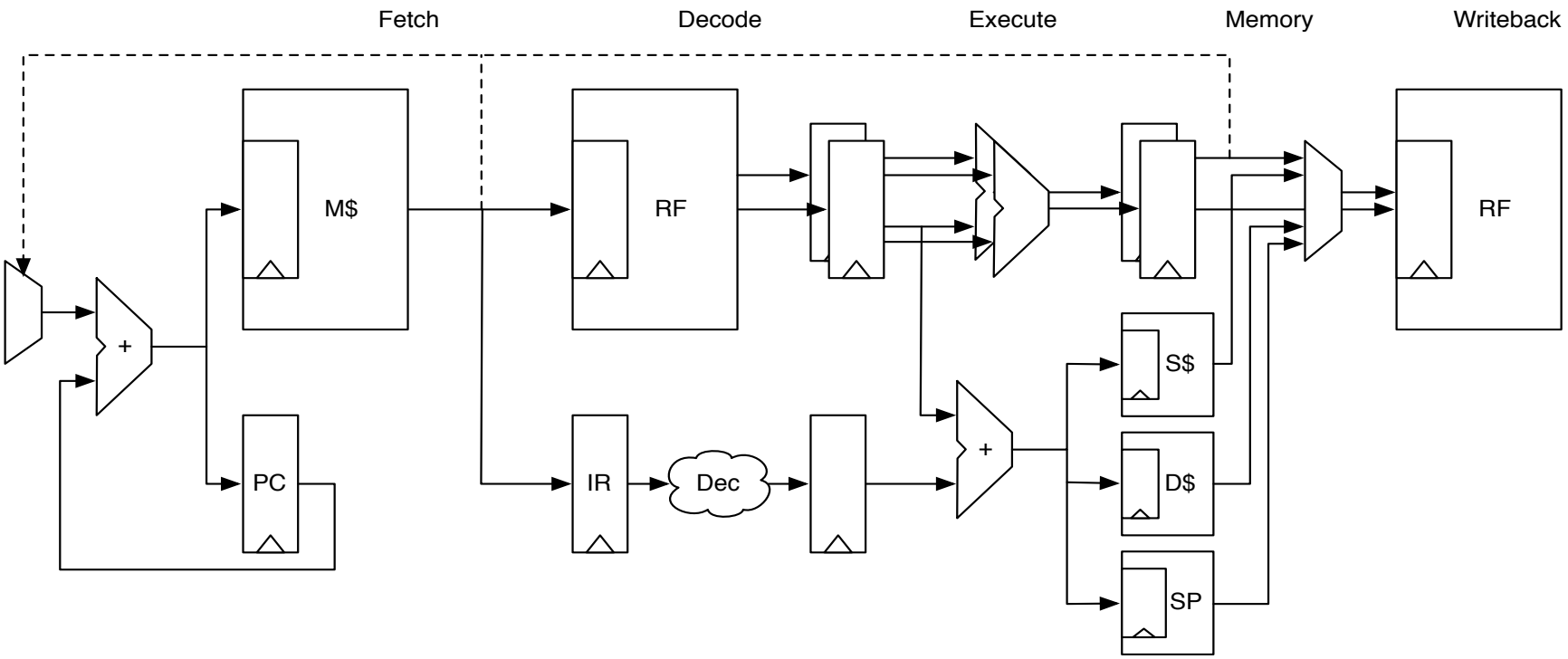
What Students Know

- They had Digital Electronics 1 and 2
- Basic digital electronics
  - Boolean algebra
  - A little VHDL and basic Chisel
  - Final project: a vending machine
    - FSM plus datapath
- Project is done with an FPGA board
  - They know how to use Xilinx Vivado

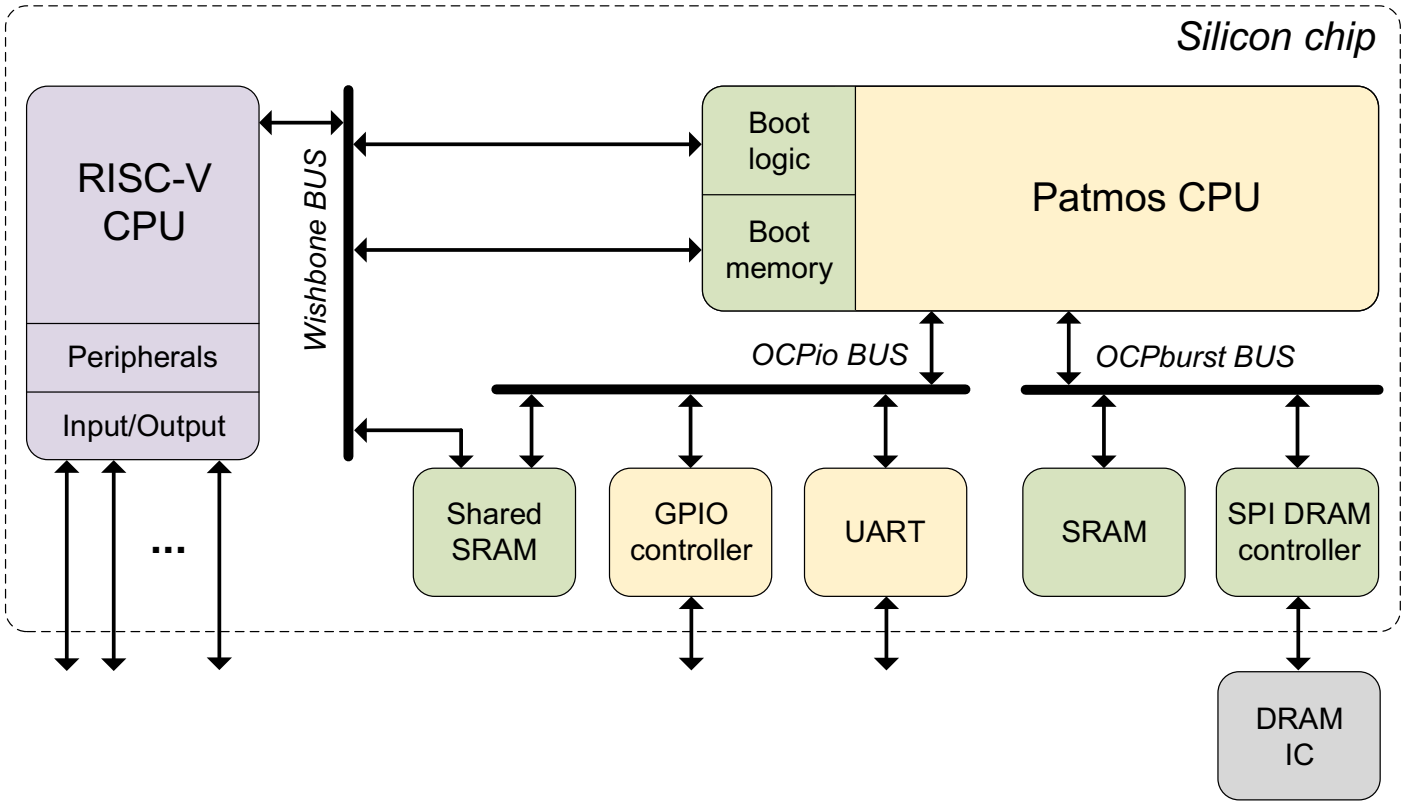
The Patmos Project

- A time-predictable processor for real-time systems
- Was part of a large EU funded project
  - As a multicore processor with a network-on-chip
  - All in open-source from the start on
- Initially written in VHDL
- I ported it during a UC Berkeley visit to Chisel
  - As an exercise to learn Chisel

Patmos Pipeline



The Design


Silicon chip
RISC-V CPU
Peripherals
Input/Output
...
Wishbone BUS
Boot logic
Boot memory
Patmos CPU
OCPio BUS
OCPburst BUS
Shared SRAM
GPIO controller
UART
SRAM
SPI DRAM controller
DRAM IC

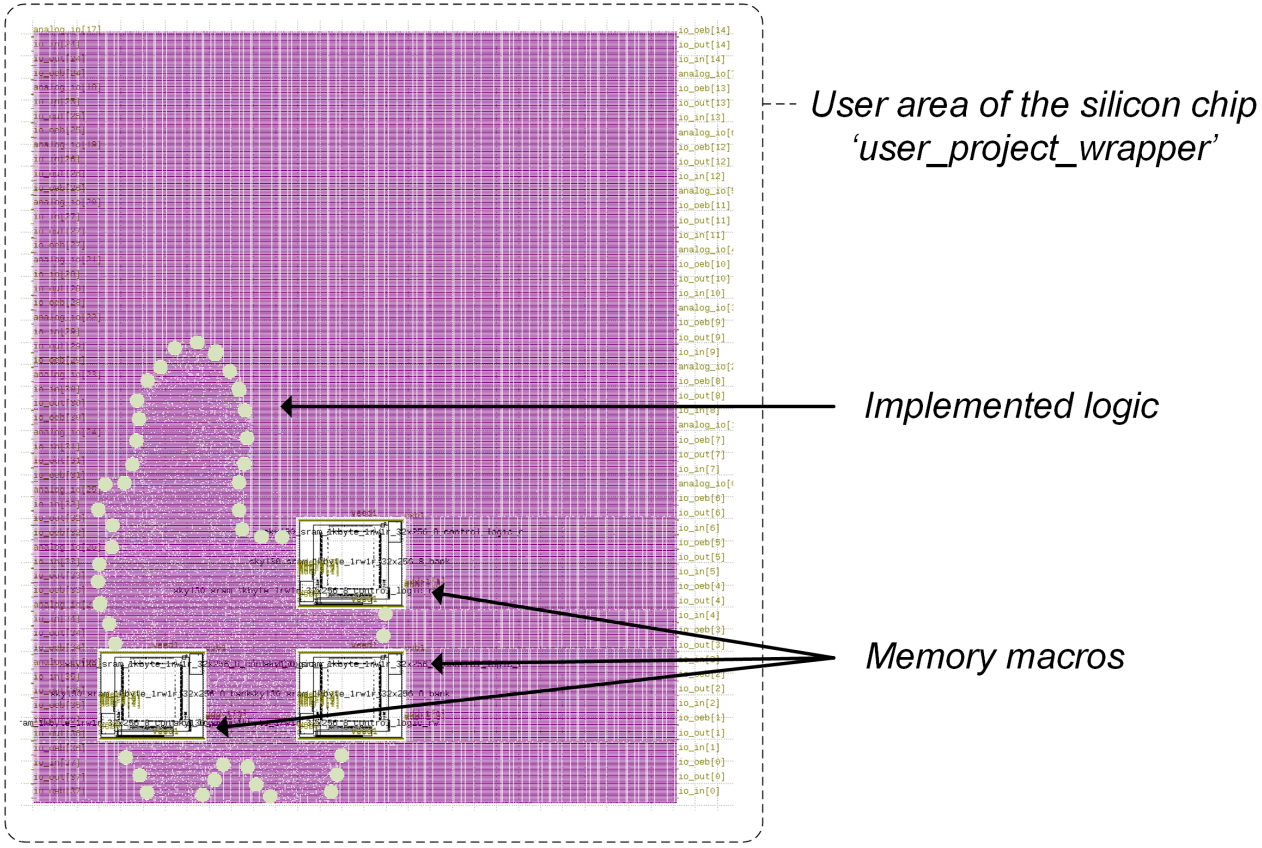
Work Groups

- General tool flow and server setup
- SPI Controller
- Memory controller with the SPI controller
- Loadable boot memory
  - Including setting the PC
- RAM compiler

Finishing

- After integration
  - We had many precheck errors
  - Consumed a lot of time to fix them
- Missed deadline for MPW 6 by hours
- Submitted later to MPW 7
  - We are now in position #3
  - Increases the chance in the lottery

Our Final Patmos Chip



What Did We Learn

- A chip is doable within one semester
  - With 4th semester students
- It is not as simple as FPGA synthesis
  - No “Play” button
- We should have run the hardening and precheck earlier
- Memories are a pain
- Installation was not so easy
  - Needed some help from a Slack channel

Summary

- The open-source move approaches hardware
- Complete flow from Chisel to chips is possible
- Sponsored by Google
- Produced by SkyWater on a MPW
- We managed to finish one chip in a semester
  - with 4th semester students
- It was quite fun to do it
- Getting a real chip was a strong motivation for the students