Computation of Lower and Upper Bounds for Switching Activity: A Unified Approach

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Abstract

Accurate switching activity estimation is crucial for power budgeting. It is impractical to obtain an accurate estimate by simulating the circuit for all possible inputs. An alternate approach would be to compute tight bounds for the switching activity. In this paper, we propose a non-simulative method to compute bounds for switching activity at the logic level. First, we show that the switching activity can be modeled as the Bayesian distance for an abstract two class problem. The computation of the upper and lower bounds for the switching activity is unified into a single function, $\psi(\alpha, p, \rho)$, where α is a parameter, ρ is the temporal correlation factor and p is the signal probability. The constraints on α for $\psi(\alpha, p, \rho)$ to be tight upper and lower bounds are derived. The proposed approach computes bounds for individual gate switching. Experimental results are obtained by taking spatial and temporal correlations into account. The computations are simple and fast.

1 Introduction

Low power designs are critical for portable and wireless systems. Until recently, designers were mainly concerned with area and throughput as the important design parameters. The addition of power as a third parameter to the design search space has consequently lead to the exploration of the tradeoffs between area, delay and power. Low power designs can be realized at various levels of the design cycle. Therefore, accurate estimation of power consumption at each level is necessary for the synthesis of these designs. However, power dissipation is an input dependent phenomenon and would require exhaustive simulation to get an accurate estimate. This becomes intractable for circuits with large number of inputs. Hence, the computation of tight upper and lower bounds for the switching activity provide a reasonable measure of the power consumption.

In CMOS circuits, the main source of power dissipation is the dynamic power which occurs due the charging and discharging of the node capacitances The dynamic power can be characterized as:

$$P_{dynamic} = \frac{1}{2} S C {V_{dd}}^2 f \quad (1)$$

where C is the capacitance of the node and V_{dd} is the supply voltage. Hence, the estimation of S is critical for the accurate and efficient estimation of power dissipation. However, accurate estimation of power dissipation is difficult due to its dependence on the input pattern applied, the delay model and the circuit structure. A good method is to obtain the upper and lower bounds for switching activity and tighten them as much as possible. The strategy adopted to get the bounds should be fast and simple. Lower bounds can also be used at higher levels of design abstraction to get bounds of area and power. A lower bound gives an indication of the minimum power requirement for a given circuit. Hence, it is natural to use the lower bound as a metric in designing power minimization algorithms.

2 Related Work

Many algorithms have been proposed for estimating the power dissipation at different design abstraction levels. Power estimation can be done for the average power dissipation or the worst case instantaneous power called peak power. Techniques for either of these can be broadly classified as non-simulative and simulative. The non-simulative techniques use probabilities to describe the set of logic signals. These logic signals are modeled as stochastic processes having signal and transition probabilities associated with them. The signal probability is defined as the probability of having a logic one and the transition probability represents the proportion of transitions on that signal. These are propagated from input to output to get a measure of the

average switching activity in a circuit. The simulative methods take care of the input dependence by proper choice of the input vectors. The idea is to simulate the circuit repeatedly. A stopping criterion is required when the power converges to average power. The main drawback of this approach is that it may take a lot of time for large circuits. A complete survey of the state of the art techniques in power minimization and estimation is described in [11, 8].

Some attempts have been made to compute bounds for power dissipation [3, 4, 6, 5, 7]. In [3, 4], entropy and informational energy have been used as measures of switching activity. It is shown that the switching activity is upper bounded by a function of entropy. This method is useful in computing the average switching activity of a RT level module. A method to obtain the entropy for dataflow graphs has also been described. In [3], a simplified model for the RT level structure has been used which characterizes it in terms of NAND gates. But this might be difficult in practice for large modules. Shanbag [6] uses the information transfer rate to obtain a power dissipation lower bound for digital signal processing algorithms. The Shannon's joint-source channel coding theorem provides a proof of achievability of the bound. A non-parametric, simulative method to estimate and bound the average power dissipation in CMOS VLSI circuits is described in [5]. Order statistics are used in the evaluation of the bounds. The stopping criterion for the simulation is a function of the desired percentage error with a specified confidence level. Simulation results show that it performs better than the normality assumption for the distribution of the power in a circuit. The work in [7] proposes a technique for estimating an upper bound on the transition density of each node by using an upper bound on the number of glitches in a circuit. It is very fast but the bound is not tight.

In this paper, we propose a unified approach to compute upper and lower bounds for the switching activity. The proposed bounds are derived using decision theoretic arguments. The switching activity is modeled as the Bayesian distance for a two class problem. The computation of upper and lower bounds is unified into a single function. The tight bounds computed for the benchmark circuits indicate that the approach can be used for estimates at the RT level similar to [3, 4]. These bounds can be used for redesigning early on in the design cycle to meet the power constraints. The bounds are computed for each gate for temporally correlated signals. The proposed non-simulative approach is simple and fast.

3 Models for Switching Activity

The Markov chain model for signal transitions has been used widely in probabilistic estimation of the switching activity [8, 11]. We briefly describe the Markov chain formulation of the switching activity followed by the switching activity computations based on classification errors using decision theory.

3.1 Markov Chain Model for Switching Activity

Markov models are used in general to model the memory of a stochastic process using finite state machines. A process with memory M depends on the previous M time units. It is characterized by the M lag transition probabilities. At equilibrium, the state probabilities converge to the *steady state probabilities*. Let $X(n) \in \{0,1\}, n \in [0,\infty)$ denote the signal value at the time instant n. Since, the switching activity for any line z is the probability of a transition, we get,

$$\begin{aligned} S &= P(X(n-1)=0, X(n)=1) + \\ &\quad P(X(n-1)=1, X(n)=0) \end{aligned}$$

For temporally independent signals, we get

$$\begin{aligned} S &= P(X(n)=1)P(X(n-1)=0) + \\ &\quad P(X(n)=0)P(X(n-1)=1) \end{aligned}$$

If $p = P(X = 1)$ is the signal probability at steady state, then

$$\begin{aligned} S &= p(1-p) + p(1-p) \\ &= 2p(1-p) \end{aligned} \tag{2}$$

3.2 Decision Theoretic Model for Switching Activity

Decision theory is concerned with guessing the unknown nature of an observation. If the observation is $X = x$, then its unknown nature, $Y = y$, is called a *class*. The probability distribution of the random pair $(X,Y) \in \Re^d \times \{0,\cdots,Q-1\}$ gives the probability of occurrence of the specific pairs where $\Re^d$ is the d-dimensional space over the reals, $\Re$ and Q is the total number of classes. A *classifier* is a function $g(x) : \Re^d \rightarrow \{0,\cdots,Q-1\}$ that maps the d-dimensional input space into one of the Q classes. A classification error occurs on X if $g(X) \neq Y$, and the *probability of error* for g is given by

$$L(g) = P(g(X) \neq Y) \tag{3}$$

For a two class problem, $P(Y=1|X)$ is the conditional probability of class-1 given the observation X. Figure 1 gives the correspondence between Markov chains and decision theory. From the mapping scheme in Figure 1, we see that the decision error gives the probability of a transition occurring on a line and hence is equivalent to the switching activity. For the classifier $g(X)=X$ and

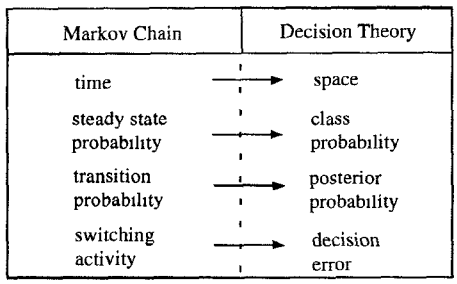

Figure 1: Mapping of Markov chain to decision theory

the two abstract classes $Y=\{0,1\}$, the classification error is given by

$$\begin{aligned} L(g) &= P(g(X)\neq Y) \\ &= P(X=0,Y=1)+P(X=1,Y=0) \\ &= p_{01}p(X=0)+p_{10}p(X=1) \end{aligned} \quad (4)$$

where p_{01} and p_{10} are the posterior probabilities for any line z given by

$$\begin{aligned} p^z_{01} &= P^z(Y=1|X=0) \\ &= \frac{P^z(X=0,Y=1)}{P^z(X=0)} \\ p^z_{10} &= P^z(Y=0|X=1) \\ &= \frac{P^z(X=1,Y=0)}{P^z(X=1)} \end{aligned}$$

For a specific choice of the priors, namely, $p(X=0)=\frac{p_{10}}{p_{10}+p_{01}}$ and $p(X=1)=\frac{p_{01}}{p_{01}+p_{10}}$,

$$L(g)=\frac{2p_{01}p_{10}}{p_{01}+p_{10}} \quad (5)$$

For temporal independence, $p_{01}=p_1$ and $p_{10}=p_0$, where $p_1=P(X=1)$ and $p_0=P(X=0)$. Since $p_0+p_1=1$, we write $p=p_1=1-p_0$. Hence, we get

$$L(g)=2p(1-p) \quad (6)$$

which is the Bayesian distance [13]. From equation (2) and the above equation, it is clear that Bayesian distance is equivalent to the switching activity, S. Modeling S as the Bayesian distance allows the use of decision theoretic methods for computation of bounds.

4 Computation of Bounds

In hypothesis testing the computation of bounds for the probability of error is a classical problem. Often, it is difficult to compute the exact probability of error. This is due to the fact that, the posterior probabilities are rarely known. Therefore, good upper and lower bounds for the probability of error are desired. A continuous and differentiable bound helps in optimizing the performance of the classifier. Many attempts in statistical decision theory have been made to compute such bounds [1]. Recently, a bound for the Bayes error is derived in [13]. In this paper, we extend the approach of [13] to compute tight upper and lower bounds for S. In [12], a model for switching activity has been proposed which accounts for temporal correlation. If ρ_i denotes the temporal correlation of line i, then the switching activity for line i is given by

$$S=2p_i(1-p_i)(1-\rho_i) \quad (7)$$

where ρ_i is given by

$$\rho_i=\frac{p^i_{00}-p^i_{10}}{\sqrt{(p^i_{00}+p^i_{10})(p^i_{01}+p^i_{11})}} \quad (8)$$

Let $f(p)$ be a continuous and differentiable function. For $f(p)$ to be an upper or a lower bound, it is required that $f(0)=f(1)=0$ and $f(\frac{1}{2}+p)=f(\frac{1}{2}-p)$, $0\leq p\leq 0.5$. Let $f(p)=0.5(sin\pi p)(1-\rho)$. For $0\leq p\leq 1$ and $|\rho|<1$, $f(p)\leq 2p(1-p)(1-\rho)$, hence it is a lower bound for S. This bound can be tightened further by weighting it using an exponential function. The exponential function is continuous, differentiable and can be made symmetric about $p=0.5$. The rate of decay or growth of this function can also be easily controlled. Therefore, we choose the exponential function to be $e^{\alpha[p-0.5]^2}$, where, the parameter α controls its behavior. In order to get tight bounds, we define

$$\psi(\alpha,p,\rho)=0.5(sin\pi p)(1-\rho)e^{\alpha[p-0.5]^2} \quad (9)$$

Theorem 1 *For* $0\leq p\leq 1$, $0.5(sin\pi p)(1-\rho)e^{\alpha_1[p-0.5]^2} < S \leq 0.5(sin\pi p)(1-\rho)e^{\alpha_2[p-0.5]^2}$, *for some* $\alpha_1 < 4ln(4/\pi)$ *and* $\alpha_2 \geq 4ln(4/\pi)$

The computation of the bounds require the computation of the signal probability. The motivation for computing the bounds is as follows: i) The switching activity

computed using Equation(7) approximates the actual switching activity. Its value may be slightly more or less than the empirical value. The lower and upper bounds obtained give an interval within which the empirical S may lie. ii) The lower bounds give an indication of the minimum power dissipation of a circuit for a given input signal probability and switching activity. Hence, it will be useful in power minimization techniques which use input reordering. iii) The bounds are useful in RT-level power characterization.

5 Experimental Results

The numerical computation of bounds was implemented in SIS [9]. Given the input signal and conditional probabilities, the output conditional probabilities of a logic gate can be computed [10]. The conditional probabilities are used to compute ρ for every node using Equation(8). The signal probability is computed using global BDDs [2] and hence takes care of the spatial correlations due to reconvergent fan outs. The bounds are computed using Equation(9) with input signal probability of 0.5 and switching activity 0.5 The results are shown in Figure 2. The columns indicate the switching value for different values of α. The values have been rounded off to the second decimal place. The results indicate that tight upper and lower bounds for the switching activity are obtained and that the bounds become looser when the value of α are further away from $4ln(4/\pi)$. The last column shows the average ρ value for each circuit. It is seen that the switching activity is low with higher temporal correlation.

Circuit	$\alpha = -0.5$	$\alpha = 0.5$	Actual S	$\alpha = 1.5$	$\alpha = 2.5$	ρ_{avg}
rd73	0 11	0 12	0.13	0.13	0.15	0.2
alu4	0.07	0.08	0.09	0.10	0.11	0.48
apex1	0.11	0 12	0 13	0.14	0 15	0.3
apex4	0.05	0.05	0.05	0.06	0.07	0.6
clip	0 13	0 15	0 15	0.16	0.18	0.17
misex1	0.28	0.29	0.30	0.31	0.32	0 11
misex3	0 03	0 03	0 03	0.04	0.04	0.74
table3	0.06	0.06	0.07	0.07	0.08	0 69
table5	0.07	0.08	0.08	0.08	0.09	0.65

Figure 2: Simulation results

6 Conclusions

In this paper, we show that switching activity is a two class decision theoretic problem. A unified method to compute upper and lower bounds for the switching activity at the gate level is presented. Since switching is an input pattern dependent problem, non-simulative methods which are fast and accurate are desirable. The proposed non-simulative technique is applied on some common benchmark circuits and the results indicate that tight bounds are obtained. The method can be used for module characterization and power analysis at the RT level of abstraction.

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