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A Genetic Framework For The High-Level Optimisation Of Low Power VLSI DSP Systems

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Abstract: This letter presents a technique for optimising CMOS based DSP systems for power. A Genetic Algorithm is used to reduce power, while tracking area and speed specifications, through the application of high level transformations. The algorithm searches for systems with the lowest power consumption within a large solution space. Results are presented which demonstrate the efficiency of the Genetic Algorithm as a power optimisation tool for complex VLSI systems.

Introduction: Power dissipation has become an increasingly important parameter in the realisation of VLSI systems. It is especially important in the rapidly expanding portable computing market where the limiting factor is the operating time provided by the battery. Various techniques have been developed that tackle power reduction at different levels of the VLSI design process [1][2][3], however decisions made at higher levels will have the greatest impact on power [1]. The most significant factor affecting power consumption in a CMOS device is the product [(supply voltage)^2 $\times$ effective capacitance] [4]. This demonstrates that reduction of supply voltage will have the largest impact on power. However, research has shown that this will induce delays in the device [5]. This reduction in throughput could be compensated for with the application of a number of high level transformations [5], thus allowing supply voltage reduction while keeping throughput constant. Even with a restricted set of transformations no time efficient algorithm can be developed to determine the lowest power solution [3]. The optimisation problem is further complicated by the fact that transformations

may reduce voltage while having an adverse effect on the effective capacitance. Hence any optimisation technique will need to track area and speed concurrently while optimising power.

Genetic Algorithms [6] (GAs) have proved successful in solving a number of VLSI design problems [7][8], and have shown a high degree of flexibility in handling multiple constraints [8]. In this paper a GA is developed to search for the optimal power solution of a system through the application of high level transformations. The GA successfully manipulates high level systems to produce systems with lower power requirements, while tracking area and speed constraints.

Implementation: Circuits are presented to the GA as Data-Flow Graphs (DFGs). These are encoded into the chromosome representation shown in figure 1. Each element within the DFG is an individual gene in the chromosome. High level transformations operate on the circuits to modify their power requirements. Transformations currently implemented include: *Retiming* [4], which is the process of moving delay elements around the DFG to minimise the longest computational (critical) path. *Pipelining* [4], which is the process of inserting delays in the DFG, also to minimise the critical path. This may have the disadvantage of increasing system latency. *Automatic Pipelining* [9], which is a specialised form of retiming. *Loop Unfolding* [10], which creates a parallel implementation of the DFG to increase throughput at the cost of an increase in area. Unfolding utilises the *postponing principle* [11], which has the advantage of lower area overhead [11]. It is initially applied at a relatively low rate, after a number of generations the rate is increased to improve the power reduction.

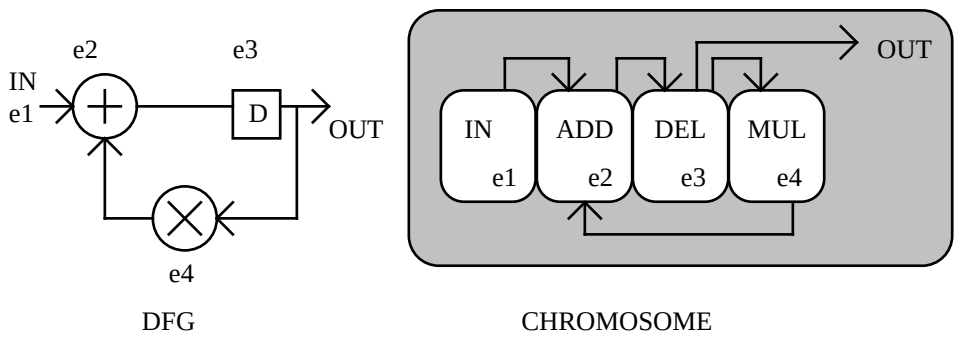

Fig. 1 *Chromosome Representation*

The system flowchart is shown in figure 2. A diverse initial population is created of randomly transformed copies of the original DFG. A fitness is allocated to each member of the population. This is determined by calculating the supply voltage and effective capacitance of the DFG. Area requirements are computed for the adders, delays and multipliers. The total required area is used to estimate the effective capacitance. The GA selects a member of the population for transformation using the probabilistic Roulette Wheel [6] method. A library of transforms is used from which transforms are selected at predetermined rates. (*Pipelining*=1%, *Retiming*=20%, *Unfolding*=1%, *Auto-Pipelining*=1%). These rates were calculated using a combination of design heuristics and experimental data. Repeated application of the transformations will form the new population of designs. Genetic evolution terminates when the design with required power specification is produced, that design with the highest fitness over all generations. The GA may produce multiple designs that satisfy the power requirements, giving greater flexibility in the implementation stage.

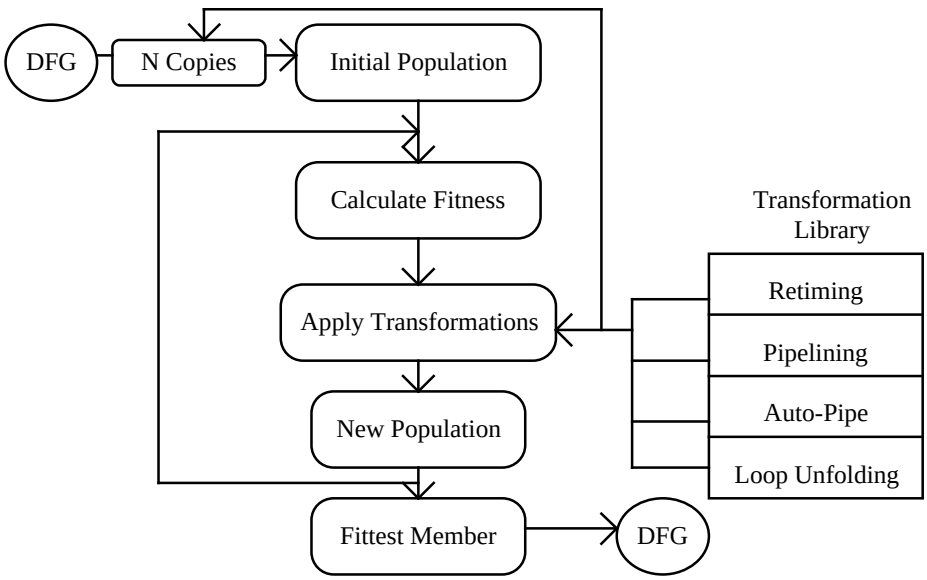

Fig. 2 *System Flowchart*

Results & Discussion: System performance is demonstrated with examples of recursive and non-recursive circuits of varying complexity. The circuits are an 8th order Avenhaus filter [5], a 2nd order IIR Lattice filter, a 3 tap FIR filter and an 8 tap FIR filter. Figure 3 illustrates the DFG obtained for the 3 tap FIR filter before the application of loop unfolding. The shortest

critical path has been achieved through pipelining, as in this example a multiplication has an execution time twice that of an addition.

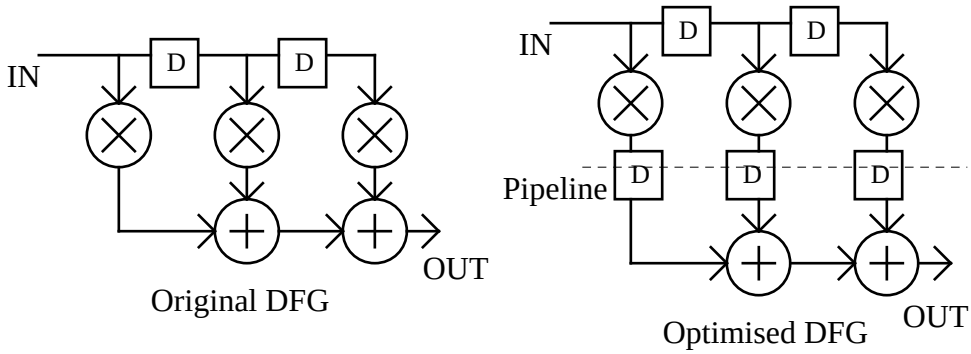

Fig. 3 *Three Tap FIR Filter*

Figure 4 illustrates the performance of the GA for the 8th order Avenhaus filter. The graph shows the fitness profile of the fittest member of the population during evolution. The results demonstrate an increase in fitness until a maximum value is reached. Loop unfolding is then applied to achieve the lowest power solution.

The discontinuity present in the fitness curve is specific to the synthesis problem, since for example a simple pipelining operation on a low fitness circuit may dramatically decrease the critical path, resulting in a sudden decrease in power consumption.

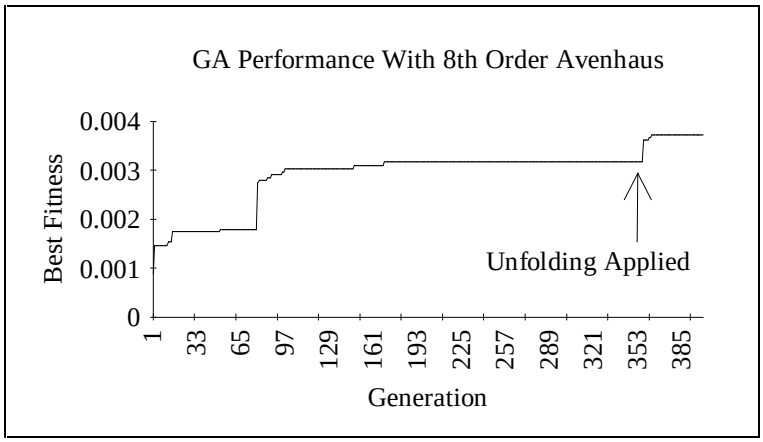

Fig. 4 *GA Performance With 8th Order Avenhaus Filter*

The results obtained for each of the example circuits are presented in Table 1. The comparative power is an estimation of the power consumption of the new circuit expressed as a percentage of the original power consumption. In all cases power was reduced.

	Percentage Power		
Circuit	**Before Unfold**	**After Unfold**	**Relative Size**
8th Order Avenhaus	28	24	2
2nd Order Lattice	65	62.8	2
3 Tap FIR	44.9	9.43	6
8 Tap FIR	20.54	7.9	16

Table 1 *Results For The Example Circuits*

Conclusion: The results demonstrate that the GA is capable of optimising circuits for power at the high level using a number of transformations. The variable application rates produced designs with good area/power trade-off. The concurrent tracking of power, area and speed shows the effectiveness of the GA method.

References

[1] Sing D., Rabaey M., Pedram M., Catthoor F., Rajgopal S., Sehgal N. and Mozdzen T.J., "Power Conscious CAD Tools And Methodologies : A Perspective", *Proceedings Of The IEEE*, Vol. 83, No. 4, pp. 570-594, April 1995

[2] Chandrakasan A.P., Sheng S. and Broderson R.W., "Low-Power CMOS Digital Design", *IEEE Journal Of Solid State Circuits*, Vol. 27, No. 4, pp. 473-484, April 1992

[3] Chandrakasan A.P. and Broderson R.W., "Minimising Power Consumption In Digital CMOS Circuits", *Proceedings Of The IEEE*, Vol. 83, No. 4, pp. 498-523, April 1995

[4] Arslan T., Erdogan A.T and Horrocks D.H., "Low Power Design For DSP: Methodologies and Techniques", *Microelectronics Journal*, (Accepted, to be Published)

[5] Chandrakasan A.P., Potkonjak M., Mehra R., Rabaey J. and Broderson R.W., "Optimising Power Using Transformations", *IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems*, Vol. 14, No. 4, pp. 12-3

[6] Davis L., "Handbook Of Genetic Algorithms", *Van Nostrand Reinhold*, New York, 1991

[7] Arslan T., Horrocks D.H. and Ozdemir E., "Structural Cell-based VLSI Circuit Design Using A Genetic Algorithm", *International Symposium On Circuits And Systems*, Atlanta, USA, 1996 (Accepted, To Be Presented)

[8] O'Dare M.J. and Arslan T., "Generating Test Patterns For VLSI Circuits Using A Genetic Algorithm", *IEE Electronics Letters*, Vol. 30, No. 10, pp. 778-779, May 1994

[9] Lucke L.E. and Parhi K.K., "High-Level Algorithm And Architecture Transformations For DSP Synthesis", *Journal Of VLSI Signal Processing*, Vol. 9, pp. 121-143, 1995

[10] Parhi K.K., "Static Rate-Optimal Scheduling Of Iterative Data-Flow Programs Via Optimum Unfolding", *IEEE Transactions On Computers*, Vol. 40, No. 2, pp. 178-195, Feb. 1991

[11] Huang S. and Rabaey J., "Maximising The Throughput Of High Performance DSP Applications Using Behavioural Transformations", Proceedings of EDAC-ETC-EUROASIC '94, Paris, France, pp. 25-30, March 1994.