A Low Power Pseudo-Random BIST Technique

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Abstract

Peak power consumption during testing is an important concern. For scan designs, a high level of switching activity is created in the circuit during scan shifts, which increases power consumption considerably. In this paper we propose a pseudo-random BIST scheme for scan designs, which reduces the peak power consumption as well as the average power consumption as measured by the switching activity in the circuit. The method reduces the switching activity in the scan chains and the activity in the circuit under test by limiting the scan shifts to a portion of the scan chain structure using scan chain disable. Experimental results on various benchmark circuits demonstrate that the technique reduces the switching activity caused by scan shifts.

1 Introduction

Low power electronics has become increasingly important with the advent of portable electronic devices such as laptop computers and cellular phones. Power dissipation is also important in VLSI designs such as microprocessors that contain very large numbers of very small devices. The power dissipation in CMOS circuits is directly proportional to the switching activity in the circuit. Thus, power optimization techniques at different levels of abstraction target minimal switching activity at circuit nodes to reduce power consumption.

Power and energy consumption of digital systems are considerably higher in test mode than in system mode [1]. This is because a significant correlation exists between consecutive test vectors applied to a circuit during its normal mode of operation, whereas in test mode this is not necessarily true. Reduced correlation between consecutive test patterns increases the switching activity, and hence the power consumption in the circuit.

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Another source of increased switching activity in a scan design during test mode is the use of scan chains to load values into the memory elements. This kind of access to the memory elements greatly reduces the effort for test generation. However, during scan shift operations, input values of the combinational logic fed by the scan chains change frequently, creating a large amount of switching activity in the circuit. Additionally, shifting contents of scan chains increases the switching activity in the elements of the scan chain.

High energy consumption due to increased switching activity in test mode may be critical for the battery life of devices that are periodically tested. Also, the peak power consumption is one of the factors that determine the thermal and electrical limits of components and the system packaging requirements. High peak power consumption causes several problems. Excessive heat generated by high switching activity requires more expensive packaging and cooling equipment. If not removed properly, the excessive heat can permanently damage the circuit. Increased electro-migration rates due to increased peak currents and temperature reduces the reliability of the circuit. Excessive power/ground noise (given by Ldi/dt) experienced during bare-die testing can result in rejection of good dies. Therefore, it is crucial to reduce peak power consumption during test.

Various techniques have been proposed to reduce power consumption during test application. Test vectors in a test set T are reordered for minimal power consumption in [2] and [3]. Wang et. al. [4] and Girard et. al. [6] employ two different LFSRs as pattern generators to reduce the switching activity at the circuit inputs. In another work, Girard et. al. [5] use a mapping technique to reduce switching activity at some circuit inputs, and a vector inhibition technique for pseudo-random BIST to filter out vectors that are not detecting any new faults [8]. The above mentioned techniques are applicable to combinational circuits.

Several test power reduction techniques were also proposed for scan circuits. In [2] power reduction in scan designs during the external application of a test

set was also considered. In [7] a vector inhibition technique is used to stop scan shifts for some vectors, as well as a toggle suppression technique to reduce switching activity due to scan shifts. In this work, toggle suppression is achieved by adding a NOR gate to each scan cell output and setting its output to 0 through a control signal during scan shifts. Although this technique is highly effective in reducing the average power, peak power reduction may not be guaranteed. For example, it is still possible to launch transitions at every circuit input if the scan chain contents are all 1's at the time control signal is activated or deactivated. Wang and Gupta [9] proposed a low-transition test pattern generator for pseudo-random BIST to reduce switching activity due to scan shifts. Again, this technique is effective in reducing the average power, but there is no control over the captured data and peak power may not be reduced. Whetsel [10] adopts a scan architecture that divides scan chains into multiple segments, and activates these segments one at a time using different enable lines to reduce power consumption due to scan shifts without increasing the test application time. The reduction in scan power is proportional to $(1 - \frac{1}{N})$ where N is the number of segments, however, since the whole scan chain will be active when the data is captured, peak power reduction may not be guaranteed in this scheme either. In [11] Sankaralingam et. al. describe a low power method that uses scan chain disabling. In this approach, tests in a given test set T are divided into groups and only changing portions of consecutive tests are shifted into the scan chains. Peak power consumption, however, is not necessarily reduced in this scheme since all of the chains are activated when a test from the next group in T is shifted into the scan chains. To reduce the peak power consumption, this technique should be modified such that the simultaneous activation of all scan chains is prevented at test group boundaries.

In this paper, we propose a low power pseudo-random BIST methodology for scan circuits based on scan chain disabling, that primarily targets peak power reduction. We assume that a circuit with multiple scan chains is given, and we do not modify the scan structure of the circuit. In the next section we describe the proposed BIST methodology. In Section 3, a scan chain selection method for scan disabling is discussed. Experimental results are presented in Section 4. Section 5 concludes the paper.

2 Proposed BIST Scheme

In this section, we describe a low-power pseudo-random BIST methodology based on scan chain disabling. The scan chain disabling methodology described in [11] is based on a given deterministic test set. In that work, a given test set is divided into groups, such that the tests in each group have compatible specifications in a subset of scan elements. When tests in a group are applied consecutively, the set of scan elements and the corresponding compatible values are not loaded again, and the elements are disabled during the capture cycle. In this work we develop a procedure

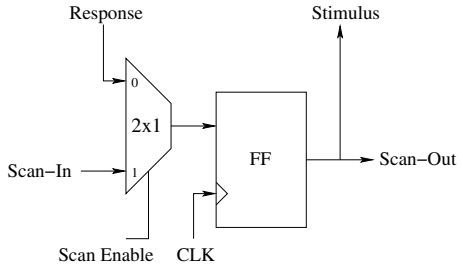

Figure 1. A scan element

suitable for pseudo-random test patterns with a given scan structure.

A widely used scan element in scan designs is shown in Figure 1. When the **Scan Enable** input is active, the flip-flop captures the data from the **Scan Input** (connected to the previous scan element), otherwise it captures the circuit response. It is necessary in this case to disable the clock signal to achieve scan chain disabling and such a capability is also assumed in [11].

If it is not desirable to disable the clock signals due to clock tree design considerations, e.g., clock skew, scan chain disabling can be achieved by using a modified scan element as shown in Figure 2.

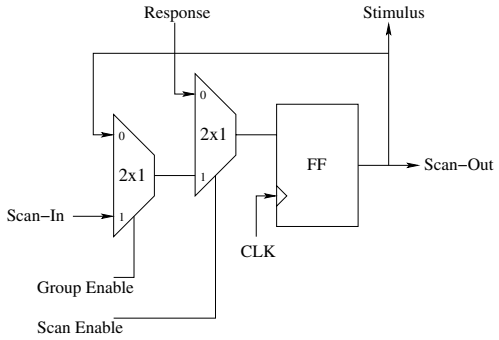

Figure 2. Modified scan element

To scan-in new data into this scan element, both the **Scan Enable** and **Group Enable** must be activated. When the **Scan Enable** input is not active, a response from the circuit is captured by the flip-flop. When the **Scan Enable** input is active but the **Group Enable** is not active, the flip-flop re-captures its own data. Hence, the need for disabling the **CLK** signal to hold the current scan chain status is eliminated.

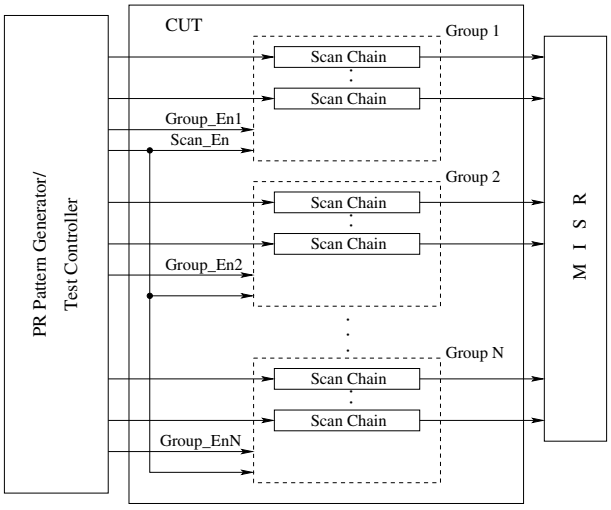

Figure 3. Proposed BIST scheme

The proposed scheme divides the scan chains of the design into N scan chain groups, where N is a preselected constant. A block diagram of the proposed scheme is given in Figure 3. As shown in this figure, each group has a different **Group Enable** signal in addition to the common **Scan Enable** signal. If the standard scan elements are used in the design, this input controls the **CLK** signals. If the modified scan elements are used, it corresponds to the **Group Enable** signal of the scan elements. Using the **Group Enable** signals, the test controller selects the scan chain group that will be loaded/unloaded during a particular scan cycle. The proposed scheme allows only one of the groups to be active (enabled) at any given scan cycle. Since only the scan chains in the active group will capture data and experience data shifts, switching activity in the logic caused by the data capture and scan shifts will be confined to the fanout cone of the active scan chains. This will allow reduction in the peak power consumption as well as average power consumption in the circuit under test.

Although disabling a subset of the scan chains ensures reductions in peak and average power consumptions, it may have an adverse effect on the fault coverage for two reasons:
1) Some of the circuit inputs (corresponding to disabled chains) will not be exercised by new input values. This will reduce the chances that new faults will be activated and propagated to the outputs.

2) Even if some of the faults are activated and propagated to the outputs, fault effects that are propagated to the inputs of scan elements corresponding to the disabled scan chains will not be captured. This may prevent some of the faults from being detected.

Therefore, under the proposed scheme it may be necessary to run the test for more *test cycles*. A test cycle is composed of a *scan cycle* in which a test input (stimulus) is shifted into (out of) the scan chains, plus a *functional cycle* in which the circuit is exercised with the test input and its effect is captured.

Implementing the proposed method needs a procedure to partition the set of scan chains into groups and a procedure to determine which group of scan chains is loaded/unloaded during a given test cycle. Next we describe the procedure we use to select disabled scan chain groups. In the next section we describe the procedure used to select groups of scan chains.

The scheme we propose divides the test session into N equal length phases. That is, if the whole test session consists of M test cycles, then the duration of each phase is M/N cycles. Within each phase, different scan chain groups are assigned different activity ranks. The frequency of scan shifts for different groups are determined according to this ranking. Suppose that the activity ranking of the scan chain groups is given as $G_1, G_2, \ldots, G_N$, G_N being the least active group. Then, after exercising G_1 for n_1 test cycles, the contents of G_2 is replaced once. G_1 is exercised for n_1 more test cycles before the contents of G_2 is replaced for a second time. After the contents of G_2 is replaced n_2 times, the contents of G_3 is replaced once and so on. These numbers are referred to as the *cycle lengths* for each activity group. The total number of test cycles required before replacing the contents of each activity group can be listed as follows:

$$\begin{array}{ll} G_1: & 1 \\ G_2: & n_1 \\ G_3: & n_2 \times n_1 \\ \vdots & \vdots \\ G_N: & n_{N-1} \times \ldots \times n_2 \times n_1 \end{array}$$

Occasionally changing the contents of the less active scan chain groups can help to activate, propagate and capture more faults in the heavily exercised regions. However, the activity created in the less active chains may still not be enough to detect the faults in the regions driven by those scan chains. Hence, at the end of each phase, the activity order of the scan chain groups are rotated such that the most active group becomes the least active, the second ranked group becomes the most active, the third ranked becomes the second and

so on as listed below:

$$
\begin{array}{rccccc}
Phase_1: & 1 & 2 & 3 & \ldots & N \\
Phase_2: & 2 & 3 & 4 & \ldots & 1 \\
\vdots & & & & \vdots & \\
Phase_{N-1}: & N-1 & N & 1 & \ldots & N-2 \\
Phase_N: & N & 1 & 2 & \ldots & N-1
\end{array}
$$

As a result all the chains are rotated through all the activity groups. This scheme achieves an effect similar to weighted random pattern generation with different weight settings, except that weights in this case correspond to activity levels.

3 Selection of Scan Chain Groups

In this section we describe the selection of scan chain groups. Grouping of the scan chains can affect the final test coverage, because certain chains may have to be active together for the detection of certain faults.

One way to determine the scan chain groups is to use COP [12] based testability analysis to calculate the effect of scan chain disabling. We aim at preserving the testability of the circuit as much as possible when scan chain disable is used, that is, the detection probabilities of the faults must be close to those in the original circuit when a group of scan chains is disabled. Initially, detection probabilities for all the faults are calculated by calculating the COP observabilities and controllabilities of all the circuit lines. Then for each scan chain pair (k, l) a weight $w_{k,l}$ is calculated as follows:

$$w_{k,l} = \sum_i \frac{Pd_{i_{new}}}{Pd_{i_{orig}}} \quad (1)$$

$Pd_{i_{new}}$ is the detection probability of fault i when only scan chains k and l are active, while $Pd_{i_{orig}}$ is the detection probability of fault i when all the scan chains are active. If the ratio $Pd_{i_{new}}/Pd_{i_{orig}}$ is equal to 1, then the detection probability of fault i is the same as in the original circuit when both of the scan chains k and l are activated together. This data is represented as a graph where nodes correspond to individual scan chains and the weight of the edge between two nodes k and l is $w_{k,l}$. To obtain N scan chain groups, this graph must be partitioned into N groups with (more or less) equal numbers of nodes. To minimize the loss of fault coverage due to scan chain disabling, we use the heuristic of maximizing the sum of the edge weights for edges between vertices in the same subset. This is because the edge weights reflect the number of faults that are likely to be detected when two chains are activated together. Viewed differently, we search for a partition such that the cut weights for the cuts defining the partition is minimum. An example is shown for $N = 2$ in Figure 4.

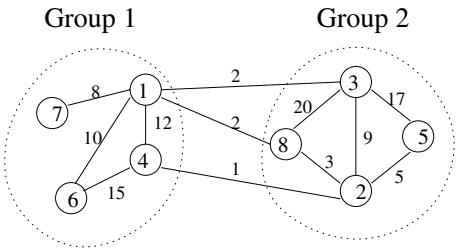

Figure 4. Partitioning of a graph

Partitioning a graph into N subgraphs with a minimum cut weight across the subgraphs is an NP-hard problem [13]. We use the following greedy algorithm to determine the partition:

```
form graph G;
FOR (i=1 to N) {
  from the unselected nodes select the
  pair with the highest edge weight;
  add the pair to group i;
  cnt_i = 2;
  while (cnt_i < |V|/N) {
    select a node such that the sum of the
    weights of the edges between the node
    and the already selected nodes in group i
    is maximum;
    add the node to group i;
  }
  optimize selection;
}
```

The optimization step in the procedure given above replaces an already selected node with an unselected node if the latter has a higher cumulative edge weight to the rest of the selected nodes. Optimization stops when no more improvement is possible.

4 Experimental Results

We have carried out experiments on full scan versions of various ISCAS89 benchmark circuits. We inserted multiple scan chains into these circuits using Mentor Graphics' DFTAdvisor tool, and then conducted experiments for $N = 1, 2$ and 3.

When $N = 1$ all the chains are kept active, i.e., the conventional BIST methodology is applied. In this case pseudo-random patterns are applied to the circuit until no more faults are detected by the last 1000 vectors. This is repeated for 5 different random pattern generator seeds. Average results of these runs are determined.

For $N = 2$ and $N = 3$, the scan chains are partitioned into N groups using the procedure given in the last section. The length of the test sessions for these cases are adjusted such that the total test energy

Table 1. Experimental results

		# of Test Vectors			Fault coverage (%)			%Power Red.(N=2)			%Power Red.(N=3)		
Circuit	SC	N=1	N=2	N=3	N=1	N=2	N=3	Avg.	Peak	Max Tr.	Avg.	Peak	Max Tr.
s9234	6	19893	37000	55250	85.50	85.64	85.49	46.32	32.40	45.33	63.93	45.91	60.67
s13207	15	28096	54500	80000	96.20	96.80	96.56	48.49	35.55	43.65	64.92	41.79	62.44
s15850	15	15124	29500	43250	91.59	91.71	91.80	48.81	30.94	43.27	66.24	42.01	62.18
s38417	30	43152	80500	120000	95.23	95.37	95.24	46.46	43.89	47.96	64.04	57.20	63.87
s38584	30	25303	49000	72000	95.24	95.24	95.19	48.36	22.13	47.34	64.94	28.57	63.55
Average		26314	50100	74100	92.75	92.95	92.86	47.69	32.98	45.51	64.81	43.10	62.54

consumed in these experiments for each circuit are the same as in the $N = 1$ case. The total test energy is approximated by the total *weighted switching activity* in the circuit during the test session. For each node, the weighted switching activity is given by the number of logic transitions times the number of fan-outs at that node. Logic transitions are calculated by logic simulation of the circuit for every clock tick during scan shifts and capture. Logic hazards are not considered.

During the experiments, several different cycle lengths that are powers of 2 are tried for each circuit and the best ones are selected. For $N = 2$, $n_1 = 2$ for all of the circuits except s13207 where it is equal to 4. For $N = 3$, (n_2, n_1) is (2,2) for the first two circuits, (4,4) for the third and (4,2) for the last two circuits.

The results for $N = 1, 2$ and 3 are given in Table 1. After the circuit name, the number of scan chains is given. Next we give the number of test vectors and the fault coverage obtained for each value of N. Next we give the reduction in average power and peak power for $N = 2$ and $N = 3$ compared to the case of $N = 1$. As discussed above, average power and peak power are indirectly measured by counting the number of weighted signal state changes. We also give the reduction in the maximum number of transitions in the scan chains under the column *Max. Tr.* (this is a measure of the peak power dissipated in the scan chains).

From Table 1, it can be seen that peak power during testing reduced by an average of about 33% when $N = 2$ is used and by an average of 43% when $N = 3$ is used. Furthermore the fault coverages achieved with $N = 2$ are always higher or the same (in one case) as those achieved with $N = 1$. Fault coverages achieved with $N = 3$ are higher for three circuits and lower for two circuits compared to the $N = 1$ case. Another important observation one can make from Table 1 is based on the reductions in the maximum number of transitions in the scan chain elements. The percentage reduction in these numbers is much higher than the percentage reductions in the peak power when signal transitions in the combinational logic are included. This implies that in evaluating procedures to reduce peak power during testing, it is important to consider the entire circuit rather than only the transitions in the scan chains.

Summarizing the above observations, one can conclude that the proposed method is effective in reducing the peak and average power during test, both in the combinational logic and the scan chains, without affecting the fault coverage. The test application time is increased approximately in proportion to the value of N. However in BIST environments increased test application time is expected to be acceptable. It is important to observe that the average power during test can be reduced in standard scan-BIST (i.e., $N = 1$) by reducing the clock frequency and hence increasing the test application time. However the peak power cannot be reduced if standard scan-BIST is used.

Next, we list average and peak power reduction results from [7] in Table 2 when a NOR gate is used at the output of scan elements for toggle suppression during scan shifts. As the results in Table 2 indicates, toggle suppression technique is very effective in reducing the average power. However, the peak power consumption almost remained the same for all circuits, except for circuit s9234 where it is in fact increased by more than 9%.

Table 2. Power reduction by toggle suppression[7]

Circuit	Peak Red.(%)	Ave. Red.(%)
s9234	-9.28	81.7
s13207	1.27	70.3
s15850	1.76	78.2
s38417	2.49	80.2
s38584	0.22	77.4

The clock power is also an important component of the total power consumption. If clock gating is used in the scheme we propose, the portion of the clock tree corresponding to disabled chains will not consume any power. It is reasonable to assume that the clock tree is distributed evenly among all scan chains, therefore the disabled portion of the clock tree will be proportional to $(1 - \frac{1}{N})$. That is, we can estimate that the clock

power will be reduced by one half for $N = 2$ and by two thirds for $N = 3$.

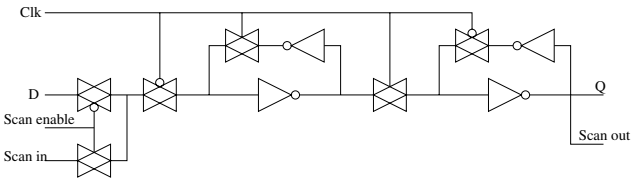

Figure 5. Implementation of the scan element in Figure 1

The proposed scheme does not affect the size of the scan elements if clock gating is used for scan chain disabling. If the modified scan elements are used, however, the size of each scan element will be larger by the area to one multiplexer. An implementation of the scan element of Figure 1 using inverters and transmission gates is given in Figure 5. Each of the transmission gates and inverters are made of two transistors, hence, the total transistor cost of this scan element is 20. If an additional multiplexer is used as proposed in the modified scan element, two more transmission gates will be needed, therefore for such an implementation, the area cost of the scan element will be increased by 20% assuming equal transistor sizes. The modified scan element also requires an additional control signal, therefore there is an additional routing overhead for the **Group Enable** signal.

5 Conclusion

We proposed a low-power BIST scheme that mainly targets peak power reduction, which can be a significant test concern especially for circuits employing built-in self test. Peak power reduction is achieved activating only a portion of the scan chains during data capture as well as scan shifts. Compared to conventional test schemes, significant reductions in peak and average power consumption are achieved. Experimental data also showed that the proposed BIST methodology can achieve test coverage similar to the conventional BIST schemes for the same test energy.

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