Low-Power Field-Programmable VLSI Processor Using Dynamic Circuits

Weisheng CHONG, Masanori HARIYAMA and Michitaka KAMEYAMA
Graduate School of Information Sciences
Tohoku University
Aoba-05, Aramaki, Aoba, Sendai, 980-8579, Japan
cwsheng@kameyama.ecei.tohoku.ac.jp

Abstract

This paper proposes a low-power field-programmable VLSI processor (FPVLSI) to overcome the problem of large power consumption in field-programmable gate arrays (FPGAs). A bit-serial pipeline architecture is used in the FPVLSI to reduce the complexity of interconnection blocks. Moreover, a dual-supply-voltage scheme is effectively used to scale down the supply voltage along non-critical paths to obtain low power consumption without degrading the overall speed performance. Its main drawback is the additional hardware cost of level converters to connect a low-supply-voltage module with a high-supply-voltage one. To solve this problem, a level-converter-less look-up table based on dynamic circuits is presented. The dynamic circuits are also useful to reduce glitch power that is one of the significant portions of the total power in FPGAs. The FPVLSI is designed based on a 0.18-μm CMOS design rule. The power consumption of the FPVLSI is reduced to 40% compared to that of the FPGA.

1 Introduction

Field-programmable gate arrays (FPGAs) are widely used to implement special-purpose processors. FPGAs are cost-effective and flexible because functions and interconnections of logic blocks can be directly programmed by end users [1]. One of the major disadvantages of FPGAs is their large power consumption mainly because of complex programmable interconnection blocks [2]. To overcome the problem, this paper proposes a field-programmable VLSI processor (FPVLSI) based on a bit-serial pipeline architecture. The bit-serial architecture greatly reduces the complexity of interconnection networks because bits for each data word are transferred through a single wire one bit at a time irrespective of the word length. For the bit-serial architecture, cells of the FPVLSI are required to perform operations in one of three modes: arithmetic/logic, memory and control ones. A shift-register-based look-up table is presented to realize these modes in an area-efficient way using the same hardware resource.

Dynamic power consumption is the focus of this paper. In CMOS VLSIs, lowering the supply voltage reduces dynamic power consumption at the cost of speed degradation. The multiple-supply-voltage scheme is a well-known technique to scale down the supply voltage along the modules in non-critical paths without degrading the overall speed performance [3]. The main problem of the typical multiple-supply-voltage scheme is the hardware cost of level converters. Level converters are required to eliminate direct current paths between power supply and ground when connecting an output of a low-supply-voltage cell to an input of a high-supply-voltage one [3]. To eliminate the overhead of level converters, this paper presents a level-converter-less multiple-supply-voltage cell that employs dynamic circuits. There are no direct-current paths in dynamic circuits.

Glitch power is one of the significant parts of the total power in FPGAs [4]. Glitches are unnecessary signal transitions caused by unbalanced delays of input signals to a cell. To eliminate glitches, the presented cell employs dynamic circuits that all input signals should be stable before computing an output signal.

The FPVLSI is designed based on a 0.18-μm CMOS design rule. The power consumption of the FPVLSI is reduced to 40% under conditions of the same area and the same processing time compared to that of the typical FPGA when performing a 16-point FFT. Moreover, the power consumption of the dual-supply-voltage FPVLSI is reduced to 48% compared to that of the single-supply-voltage FPVLSI.

2 Architecture of the FPVLSI

2.1 Overview of the FPVLSI Architecture

As shown in Fig. 1, the FPVLSI has a 2-dimensional cellular array structure based on a bit-serial pipeline architecture using multiple supply voltages. A cell consists of

Proceedings of the IEEE Computer Society Annual Symposium on VLSI Emerging Trends in VLSI Systems Design (ISVLSI'04)
0-7695-2097-9/04 $20.00 © 2004 IEEE

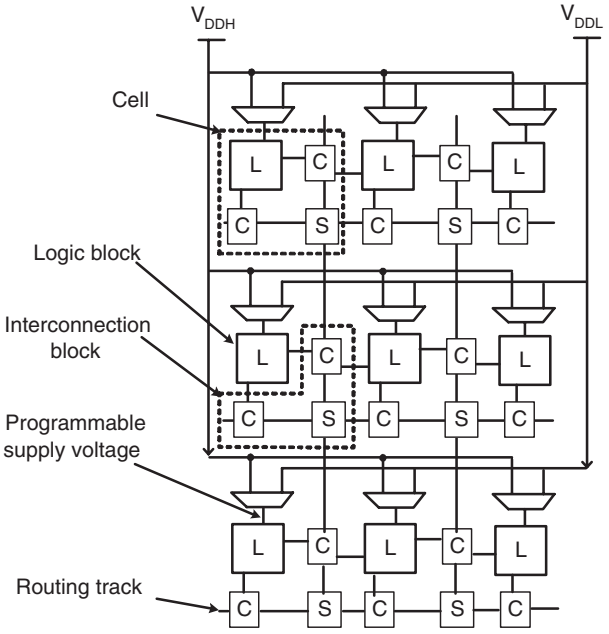


Figure 1. Architecture of the FPVLSI.

a logic block and an interconnection block that are programmable. The supply voltage for each logic block can be programmed to be a high one (V_{DDH}) or a low one (V_{DDL}). An interconnection block consists of two connection blocks and a switch block. The connection blocks interconnect their neighboring logic blocks to routing tracks. The bit-serial pipeline architecture is employed to obtain interconnection blocks with reduced complexity. The bit-serial architecture processes each data word one bit at a time. Each data word is also transmitted one bit at a time using a single routing track irrespective of the word length. Fine-grain pipeline and spatial parallelism are employed to increase the speed performance of the bit-serial architecture.

The use of multiple supply voltages is a well-known technique for low power consumption without degrading the overall speed performance. In this technique, a lower supply voltage is applied only to off-critical-path operations. Given a time constraint and a data flow graph (DFG) to specify an input behavioral description, there would be some operations in the DFG that could be slowed down by applying a lower supply voltage and the time constraint is still satisfied. Figure 2 shows that under the same speed constraint, off-critical-path operations (O_2 and O_3) and critical-path operations (O_1, O_4 and O_5) are supplied with low and high supply voltages, respectively. Figure 3 shows an allocation of the DFG of Fig. 2 into the FPVLSI. There are one critical path and two non-critical paths. Under the condition of using the same supply voltage, the non-critical paths are faster because their numbers of logic blocks and interconnection blocks are half of the

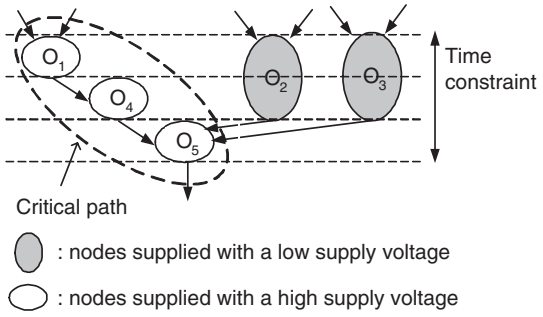


Figure 2. DFG for operations in a dual-supply-voltage scheme.

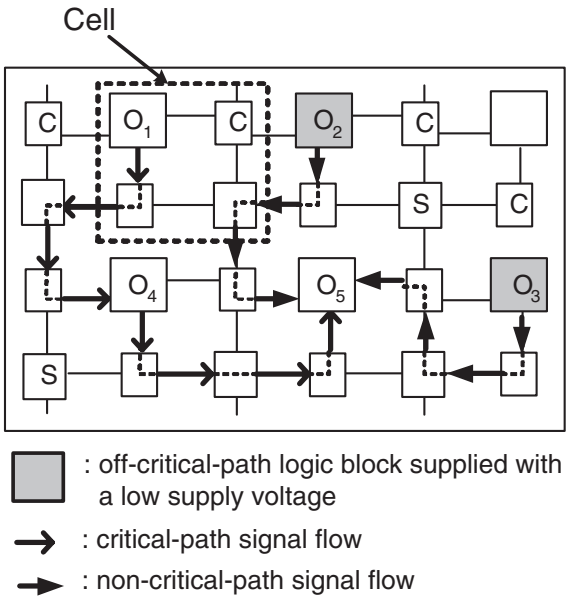


Figure 3. DFG allocation into the FPVLSI.

critical-path one. Therefore, a lower supply voltage is applied to the logic blocks along the non-critical paths. Since each logic block might be allocated with critical-path operations or off-critical-path ones depending on allocations, a fine-grain-programmable multiple-supply-voltage scheme is employed to allow each logic block to select the suitable supply voltage.

2.2 Shift-Register-Based Look-Up Table for Bit-Serial Computation

Figure 4 shows a structure of a logic block that consists of look-up tables and mode registers. Two look-up tables are required in a logic block to realize 3-input 2-output functions such as a full addition.

Three modes for bit-serial cells are arithmetic/logic,

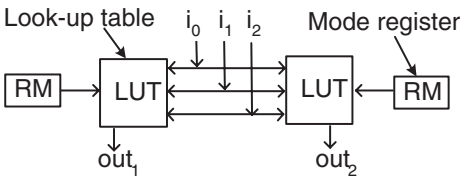


Figure 4. Structure of the logic block in the FPVLSI .

memory and control modes. The arithmetic/logic mode is for executing logic and arithmetic operations. The memory mode is used to delay or store intermediate results. The control mode is used to generate reset signals that show a division between data words.

A shift-register-based look-up table is presented to realize these modes using the same hardware resource to obtain area efficiency. Figure 5 shows that the multiplexer M_3 selects one bit from the shift register based on input signals of the look-up table (i_0, i_1 and i_2) and input signals from mode registers to multiplexers M_1 and M_2.

In the logic/arithmetic mode, the look-up table performs arbitrary 3-input 1-output functions by configuring the shift register based on truth tables of the functions. A configuration based on the truth table of an OR function is given as an example. The input signals from mode registers are '0' and '1' for multiplexers M_1 and M_2, respectively. A carry feedback path is also provided to perform carry-save operations for a bit-serial full adder.

In the memory mode, the input signal i_0 is shifted into the shift register and the multiplexer M_3 selects the (n-1)-th bit of the shift register to realize an n-bit shift register as shown in Fig. 6. The input signals from mode registers are zeros for both multiplexers M_1 and M_2.

Figure 7 shows that in the control mode, all of the bits in the shift register except the least significant bit are set to zeros. The (n-1)-th bit of the shift register is selected by the multiplexer M_3 and feedback to the shift register input to realize an n-bit one-hot counter. The input signals from mode registers are '1' and '0' for multiplexers M_1 and M_2, respectively.

3 Level-Converter-Less Look-Up Table for the Multiple-Supply-Voltage Scheme

There is area overhead of level converters in a multiple-supply-voltage scheme that uses static CMOS circuits. Let us consider a situation where a V_{DDL}-operating logic block is connected to a V_{DDH}-operating logic block as shown in Fig. 8(a). A direct current path exists in the look-up table of the V_{DDH}-operating logic block as shown in Fig. 8(b). A typical solution to the direct current path is to convert a low

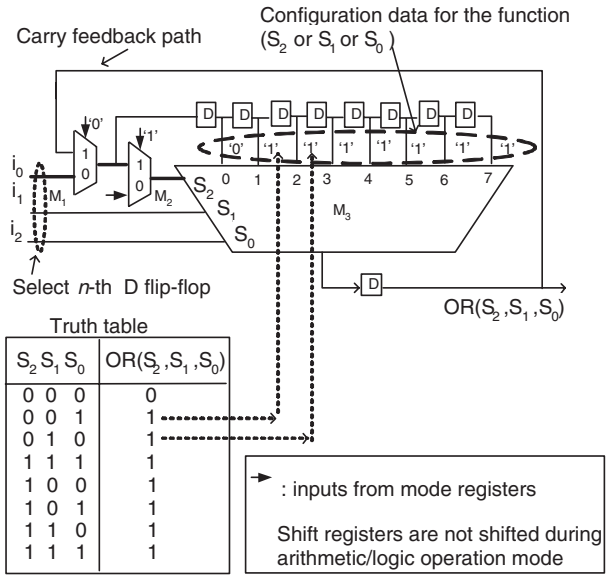


Figure 5. Look-up table in an arithmetic/logic operation mode.

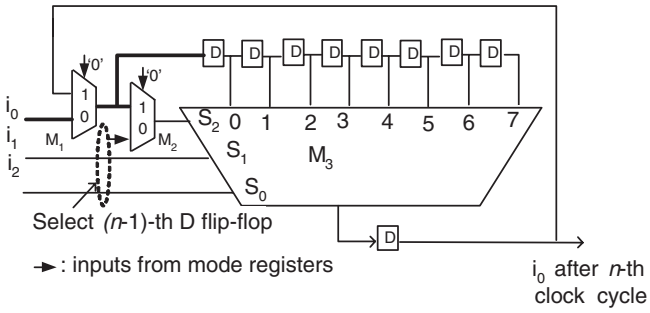


Figure 6. Look-up table in a memory mode.

swing input signal to a full swing one using a level converter as shown in Fig. 8(c). Fig. 9 shows that area overhead of level converters in the FPVLSI is large compared to that in an ASIC. In an ASIC, the number of level converters can be minimized because modules that require level converters are predetermined before the fabrication. In the FPVLSI, as shown in Fig. 9(c), level converters are required for each logic block since the voltage swing of its input signals is programmable and not predetermined before fabrication.

To overcome the overhead of level converters, dynamic circuits are employed to implement look-up tables of the logic blocks as shown in Fig. 10. A pull-up pMOS transistor and a pull-down nMOS transistor of the dynamic circuits are connected to an nMOS 8-to-1 multiplexer. Both transistors are controlled by a clock signal. The shift register of the look-up table employs static CMOS circuits. Direct current paths from power supply to ground are always turned

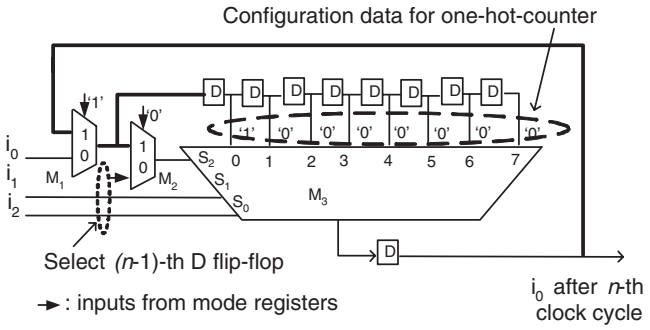


Figure 7. Look-up table in a control mode.

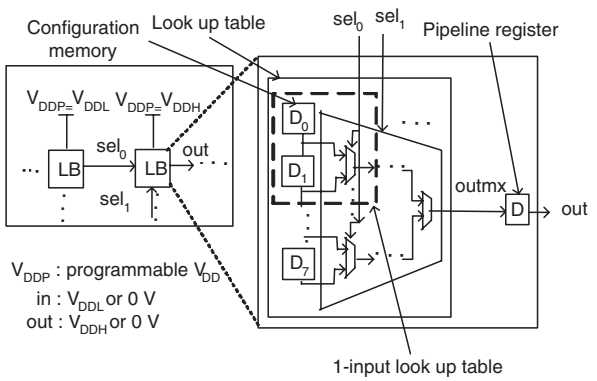
off by the clock signal. Therefore, level converters are not required. The dynamic circuit operates in two phases, $i.e$ pre-charge and evaluation phases. In the pre-charge phase, the output node of the look-up table is pre-charged to a selected supply voltage, *e.g.* V_{DDP}. The pre-charged node might be discharged during the evaluation phase depends on the input signals of the look-up table.

The employed dynamic circuits are also useful to reduce glitch power. There are no glitches in the presented look-up table because all input signals to dynamic circuits should be stable before the evaluation phase.

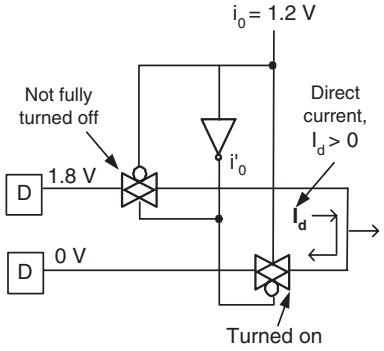
4 Evaluation

The FPVLSI is designed based on a 0.18-μm CMOS design rule. For comparison, an FPGA is designed based on the same rule. Logic blocks of the FPGA are based on static circuits. The functionality of a logic block in the FPVLSI is same with the one in the FPGA because both of them consist of two 3-input 2-output look-up tables. Features of the FPVLSI and the FPGA are summarized in Table 1. Chip area of the FPVLSI is same with the FPGA one, which is 5.5 $mm \times 4.2\ mm$. The delays are evaluated using HSPICE circuit simulations. Area of a cell in the FPVLSI is 67% smaller than the FPGA one. This is because compared to an interconnection block in the FPGA as shown in Fig. 11, the FPVLSI one has a lower complexity and a smaller area. The number of cells in the FPVLSI is three times larger than the FPGA one. Delay of an interconnection block in the FPVLSI is reduced to 44% compared to that of the FPGA. Delay of a logic block in the FPVLSI is 24% smaller than the FPGA one. This is because of smaller capacitive load of nMOS 8-to-1 multiplexers in a logic block of the FPVLSI.

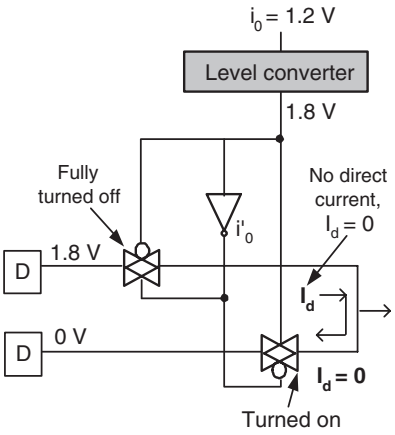
Let us evaluate the performance of the FPVLSI and the FPGA for a 16-point FFT computation with 1000 data sets, where each data set consists of 16 bits. Spatial parallelism is employed to process data sets in parallel by using processing units called FFT units. Fig. 12 shows that each FFT unit



(a) V_{DDL}-operating logic block drives a V_{DDH}-operating logic block.



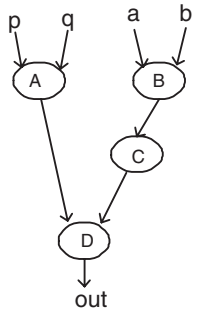
(b) Direct current in a 1-input look-up table.



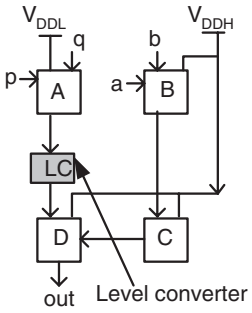
(c) Overhead of the level converters.

Figure 8. Overhead of direct current in the look-up table.

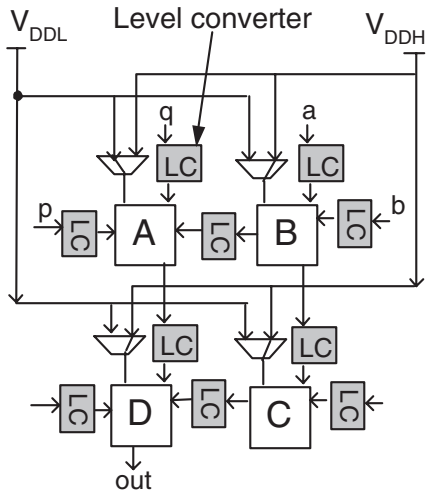
consists of four butterfly processing elements (BPEs) that are connected in series. For a single supply-voltage scheme, a comparison between the FPVLSI-based FFT implementation and the FPGA-based one is shown in Table 2. The same comparison for a dual-supply-voltage scheme is shown in Table 3. The number of FFT units in the FPVLSI is 18 times



(a) DFG



(b) Level converter in the ASIC and its minor area overhead.



(c) Large area overhead of level converters in a field-programmable device.

Figure 9. Area overhead of level converters in ASICs and field-programmable devices.

larger than that in the FPGA. This is because of a smaller area of each FFT unit in the FPVLSI. In the single supply voltage scheme using a 1.8V supply voltage, throughput of the FPVLSI is 1.64 times higher than that of the FPGA. The higher throughput allows the supply voltage to be reduced for low power consumption. Therefore, the power consumption of the FPVLSI (1.5V V_{DD}) is reduced to 82% of the one in the FPGA (1.8V V_{DD}). In the dual-supply-voltage scheme, non-critical paths of the FFT unit are exploited for further power reduction. The power consumption in the dual-supply-voltage FPVLSI (1.5V V_{DDH}, 0.9V V_{DDL}) is 40% compared to that of the FPGA (1.8V V_{DD}) and 48% compared to that of the single-supply-voltage FPVLSI (1.5V V_{DD}).

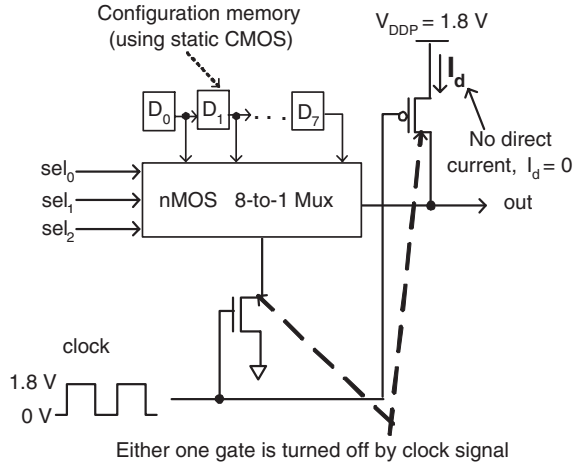


Figure 10. Level-converter-less look-up table for the multiple-supply-voltage sheme.

Table 1. Features of the FPVLSI and the FPGA.

Architecture	FVLSI	FPGA
CMOS technology	0.18-μm	0.18-μm
Chip size (mm^2)	5.5 $\times$ 4.2	5.5 $\times$ 4.2
Cell area (μm^2)	125 $\times$ 80	180 $\times$ 170
Number of cells	2288	736
Delay of an interconnection block (ns)	0.60	1.35
Delay of a logic block (ns)	0.16	0.21

5 Conclusion

The FPVLSI is proposed to realize special purpose processors with low power consumption. A bit-serial pipeline architecture is employed to reduce the power consumption of interconnection blocks. A level-converter-less multiple-supply-voltage scheme based on dynamic circuits is also proposed. The dynamic circuits also reduce the glitch power in the FPVLSI. In future work, static power consumption of the FPVLSI will be reduced by using a multiple-threshold-voltage scheme.

Acknowledgements

This work was supported by Industrial Technology Research Grant Program in 2002 from New Energy and Industrial Technology Development Organization (NEDO) of Japan.

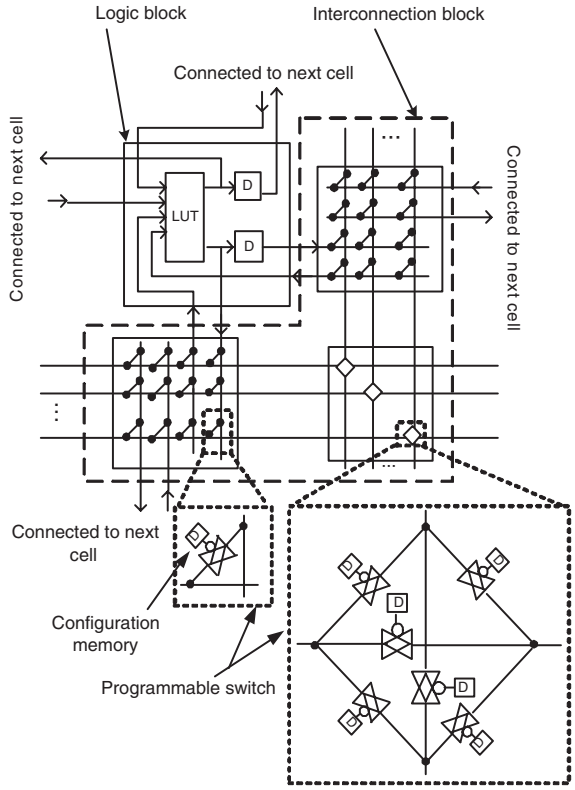


Figure 11. Complex interconnect block in a cell of the FPGA.

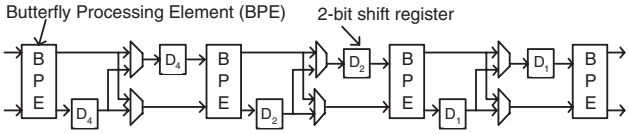


Figure 12. Block diagram of an FFT unit

Table 2. The performance comparison between the FPVLSI and the FPGA for a single-supply-voltage scheme

Architecture	FPGA	FPVLSI	FPVLSI
Supply voltage	1.8V	V_{DDH}:1.8V V_{DDL}:1.8V	V_{DDH}:1.5V V_{DDL}:1.5V
Normalized chip size	1	1	1
Normalized throughput	1	1.64	1
Number of FFT units per chip	1	18	18
Normalized power consumption	1	1.50	0.82

Table 3. The performance comparison between the FPVLSI and the FPGA for a dual-supply-voltage scheme

Architecture	FPGA	FPVLSI	FPVLSI
Supply voltage	1.8V	V_{DDH}:1.5V V_{DDL}:1.5V	V_{DDH}:1.5V V_{DDL}:0.9V
Normalized chip size	1	1	1
Normalized throughput	1	1	1
Number of FFT units per chip	1	18	18
Normalized power consumption	1 (1.21)	0.82 (1)	0.40 (0.48)

References

[1] S. D. Brown, R. J. Francis, J. Rose, and Z. G. Vranesic. *Field-Programmable Gate Arrays*, pages 1–4. Kluwer Academic Publishers, 1992.

[2] L. Shang, A. S. Kaviani, and K. Bathala. Dynamic Power Consumption in VirtexTM-II FPGA. In *Proceedings of the 10th ACM International Symposium on Field-Programmable Gate Arrays (FPGA)*, pages 157–164. ACM Press, 2002.

[3] F. Ishihara, F. Sheikh, and B. Nikolic. Level Conversion for Dual-Supply Systems. In *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pages 164–167. ACM Press, 2003.

[4] F. Li, D. Chen, L. He, and J. Cong. Architecture Evaluation for Power-Efficient FPGAs. In *Proceedings of the 2003 ACM/SIGDA Eleventh International Symposium on Field Programmable Gate Arrays*, pages 175–184. ACM Press, 2003.

[5] N. Ohsawa, M. Hariyama, and M. Kameyama. High-Performance Field Programmable VLSI Processor Based on a Direct Allocation of a Control/Data Flow Graph. In *IEEE Computer Society Annual Symposium on VLSI*, pages 95–100. ACM Press, 2002.

[6] N. Ohsawa, M. Hariyama, and M. Kameyama. Chip Design of a Field Programmable VLSI Processor Using Memory-Based Cells In *SICE Annual Conference*, pages 2225–2229. 2003.