An Adjacency-Based Test Pattern Generator for Low Power BIST Design

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Abstract

A new BIST TPG design that is comprised of an Adjacency-based TPG plus a conventional pseudo-random TPG (i.e. a LFSR) is presented in this paper. When used to generate test patterns for test-per-clock BIST, it reduces the number of transitions that occur in the CUT and hence decreases the average and peak power consumption during testing. Moreover, the total energy consumption during BIST is also reduced since the test length produced by the mixed TPG is roughly the same than the test length produced by a classical LFSR-based TPG to reach the same fault coverage. Note that this TPG design has been developed to deal preferably with strongly connected circuits with a small number of inputs.

1. Introduction

With the ever increasing complexity and density of today's VLSI circuits that make external testing more and more difficult, BIST has emerged as a promising solution to the VLSI testing problem. BIST is well known for its numerous advantages such as improved testability, at-clock-speed test of modules, reduced need for automatic test equipment, and support during system maintenance [1,2]. Moreover, with the emergence of core-based "system-on-a-chip" designs, BIST represents one of the most favorable testing method since it preserves the intellectual property of the design. In BIST, the generation of the test patterns is usually obtained from a Linear Feedback Shift Register (LFSR), which has the advantage of a compact size and the possibility to work as a signature analyzer as well.

The main motivation for considering power consumption during BIST is that power of a digital system is considerably higher in test mode than in system mode [3,4,5]. The reason is that test patterns cause as many nodes switching as possible while a power saving system mode only activates a few modules at the same time. Another reason is that successive functional input vectors applied to a circuit during system mode have a significant correlation, while the correlation between consecutive test patterns produced by an LFSR can be very low, thus increasing the switching activity in the circuit during self-test [6]. This extra power consumption due to test application may give rise to severe hazards to the circuit reliability. In addition, BIST may be iterated all over the system lifetime, and for remote applications, a high energy consumption may shorten the lifetime of the batteries.

Besides the energy/average power, the peak power consumption is another critical issue during the circuit design and test, since it determines the thermal and electrical limits of components and the system packaging requirements [7]. Excessive peak power during test can cause several problems. Firstly, this leads to an increased maximum current flow in the CUT which requires a more expensive package in consequence. Moreover, with increased peak currents, electromigration becomes more likely thus affecting the reliability of the system.

Recently, techniques to cope with the power and energy problems during BIST have appeared (a brief overview of these techniques is given in Section 2). Among these techniques, an efficient low power/energy BIST strategy based on circuit partitioning has been proposed by the authors [8]. Results on the ISCAS'85 [9] and ISCAS'89 [10] benchmark circuits showed that important power/energy reduction can be achieved at very low cost in terms of area overhead. Unfortunately, the same results could not be obtained on circuits of the MCNC'93 benchmark set [11]. These circuits have the peculiarity that they are strongly connected circuits with a small number of primary inputs. For these circuits, the partitioning technique does not succeed in reducing the power consumption during test application, or requires a prohibitive area overhead to reach a noticeable level of reduction in power and energy (for example, the area overhead is of about 19% for circuit alu4 with the partitioning technique).

Consequently, the goal of the technique presented in this paper is to minimize both power and energy consumption during pseudo-random testing of this type of circuits (strongly connected circuits with a small number of inputs - MCNC'93). The adopted strategy consists in using a mixed Test Pattern Generator (TPG) composed of an Adjacency-based TPG plus a conventional pseudo-random TPG (*i.e.* a LFSR) to generate test patterns in a test-per-clock BIST environment. Each test pattern

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generated by the mixed TPG is thus composed of two parts: a first one in which only one bit has changed compared with the previous test pattern of the test sequence, and a second one in which bits are randomly generated from the LFSR. The idea behind the use of such a structure is to reduce the number of transitions on primary inputs at each clock cycle of the test session, hence reducing the overall switching activity generated in the CUT. In applying partial adjacency tests to the CUT, the switching activity in a time interval (i.e. the average power) as well as the peak power consumption are minimized. Moreover, the total energy consumption during BIST is also reduced since the test length produced by the mixed TPG is roughly the same than the test length produced by a conventional LFSR-based TPG to reach the same or sometimes a better fault coverage. Experiments performed on the MCNC'93 circuits have shown a reduction in the average power consumption during test ranging from 33 % to 54 % with a hardware overhead ranging from 7.7 % down to 0.8 %. Reductions of the energy and peak power for these circuits are up to 57 % and 55 % respectively, with no loss of stuck-at fault coverage and no penalty on the circuit delay .

The rest of the paper is organized as follows. In the next section, we first discuss the energy and power modeling. Next, we review the existing techniques that cope with the power and energy problems during BIST. In Section 3, the basic principle of the proposed BIST strategy is described. In Section 4, the complete BIST TPG structure is detailed. Simulation results obtained from the MCNC'93 benchmark circuits are reported in Section 5.

2. Background and related work

2.1 Energy and power modeling

For the current CMOS technology, dynamic power is the dominant source of power consumption, although this may change for future developments of high scaled integration [12]. The average energy consumed at node *i* per switching is $½C_iV^2_{DD}$ where C_i is the equivalent output capacitance and V_{DD} the power supply voltage [13]. Therefore, a good approximation of the energy consumed in a period is $½C_is_iV^2_{DD}$ where s_i is the number of switchings during the period. Nodes connected to more than one gate are nodes with higher parasitic capacitance. Based on this fact, and in a first approximation, capacitance C_i is assumed to be proportional to the fanout of the node F_i [14]. Therefore, an estimation of the energy E_i consumed at node *i* during one clock period is $½.s_i.F_i.c_0.V^2_{DD}$ where c_0 is the minimum size parasitic capacitance of the circuit. According to this expression, the estimation of the energy consumption at the logic level requires the calculation of the fanout F_i and the number of switchings on node i, s_i. The fanout of the nodes is defined by circuit topology, and the switchings can be estimated by a logic simulator (note that in a CMOS circuit, the number of switchings is calculated from the moment the input vector is changed until the moment the internal nodes reach the new stable state, including the hazard switching). The product s_iF_i is named Weighted Switching Activity (WSA) of node *i* and represents the only variable part in the energy consumed at node *i* during test application. According to the above formulation, the energy consumed in the circuit after application of a pair of successive input vectors (V_{k-1},V_k) can then be expressed by:

$$E_{Vk} = ½.c_0.V^2_{DD}.\sum_i s(i,k).F_i$$

where *i* ranges all the nodes of the circuit and $s(i,k)$ is the number of switchings provoked by V_k at node *i*. Consider now a pseudo-random test sequence of length $Length_{test}$, where $Length_{test}$ is the test length required to achieve the targeted fault coverage, the total energy consumed in the circuit during application of the complete test sequence is:

$$E_{total} = ½.c_0.V^2_{DD}.\sum_{Vk}\sum_i s(i,k).F_i$$

Let us denote the clock period as *T*. By definition, the instantaneous power is the power consumed during one clock period. Therefore, the instantaneous power consumed in the circuit after application of vectors (V_{k-1},V_k) is $P_{inst}(V_k)=E_{Vk}/T$. The peak power consumption corresponds to the maximum of the instantaneous power consumed during the test session. It therefore corresponds to the highest energy consumed during one clock period, divided by T. More formally, it can be expressed as:

$$P_{peak} = \max_k P_{inst}(Vk) = \frac{\max_k (E_{Vk})}{T}$$

Finally, the average power consumed during the test session is the total energy divided by the test time, and is given as follows:

$$P_{ave} = \frac{E_{total}}{Length_{test}.T}$$

2.2 Related work

Techniques to cope with the power and energy problems during BIST have appeared recently. Except the techniques proposed in [3] and [15] that deal with the problem of power reduction during BIST at a higher level, the existing techniques can be classified into (i) those that apply to test-per-scan BIST schemes and (ii) those that apply to test-per-clock BIST schemes.

Several low power testing strategies have been proposed for scan-based BIST. Hertwig *et al.* in [16] propose to modify the scan cell design in such a way that the CUT inputs remain unchanged during shift operation. This novel design for scan path elements allows significant energy savings compared to a standard scan-based BIST scheme. Wang *et al.* in [17] present a low-transition

random pattern generation technique to reduce signal activity in the scan chain. A *k*-input AND gate and a T latch are used to generate high correlation between neighboring bits in the scan chain, thus reducing the number of transitions and hence the average power. Gerstendörfer *et al.* in [18] propose to combine the toggle suppression technique proposed earlier in [16] with the use of an additional logic in the scan path design for suppressing random patterns which do not contribute to increase the fault coverage. This technique avoids scan path activity during scan shifting at low cost in terms of area and performance.

In test-per-clock BIST, the outputs of a test pattern generator are directly connected to the inputs of the CUT, and a new test pattern is applied at every clock cycle. Hence, switching activity in the CUT can be reduced by generating test vectors from TPGs that cause less transitions at circuit inputs. In this sense, Wang *et al.* propose a BIST strategy based on two different speed LFSRs [6]. Their objective is to decrease the overall internal activity of the circuit by connecting inputs with elevated transition density to the slow speed LFSR. This approach reduces the average power and energy consumption with no loss of fault coverage. However, it is not guaranteed that the peak power consumption is reduced as well. Girard *et al.* in [19] present a test vector inhibiting technique to filter sets of consecutive non-detecting patterns of a pseudo-random test sequence generated by a LFSR. Important reductions in the average power and energy consumption are obtained with a low cost in terms of area overhead. An enhancement of this technique is proposed by Manich *et al.* in [20], where the filtering action is extended to all the non-detecting vectors of the pseudo-random test sequence. However, these techniques do not preserve the circuit from an excessive peak power consumption. Zhang *et al.* in [21] modify the LFSR by adding weight sets to tune the signal probabilities of the pseudo-random vectors in order to decrease the energy consumption and increase the fault coverage. However, the area overhead imposed by this TPG may be high.

3. Proposed BIST strategy

3.1 Basic principle

The term *Adjacency test* was first introduced in the context of pseudo-exhaustive BIST [22]. It means that only a single transition is applied at the primary inputs of the CUT at each clock cycle of the test session. In other words, it means that the Hamming distance between vectors of the test sequence is always one. Adjacency testing is particularly attractive for low power testing. In [23], the authors have shown the strong correlation which exists between the Hamming distance of vectors of a given test sequence and the switching activity induced in the CUT. They conclude that the lowest switching activity can be obtained from a test sequence in which test vectors have a Hamming distance of one. However, the switching activity generated in the circuit during test application has also a strong impact on the number of faults that can be activated and detected by the test sequence. To reach a high fault coverage in the shortest test time requires to use test patterns which stress the CUT and hence generate a lot of switching activity.

Consequently, it follows that conventional adjacency testing cannot be used in practice for stuck-at fault testing. Prohibitive test length may result. On the other hand, it can be interesting to take advantage of this kind of testing to reduce the switching activity in the CUT. For this reason, we propose in this paper to combine adjacency testing and conventional pseudo-random testing to trade off between the test length required to reach a target fault coverage and the power consumed during BIST application.

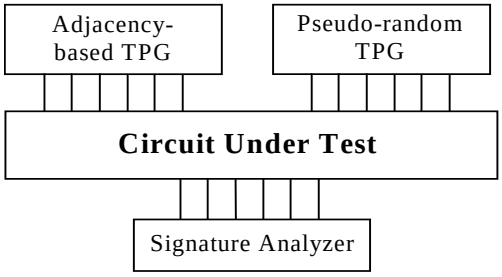

Figure 1: The adjacency-based BIST scheme

The adopted strategy consists in using a mixed TPG composed of an Adjacency-based TPG plus a conventional pseudo-random TPG (*i.e.* a LFSR). The basic scheme of the proposed BIST strategy is depicted in Figure 1. At each clock cycle, a test pattern is applied to the CUT. Each test pattern generated by the mixed TPG is thus composed of two parts: a first one in which only one bit has changed compared with the previous test pattern of the test sequence, and a second one in which bits are randomly generated from the pseudo-random TPG. Assume a CUT with *n* primary inputs: *k* of them will be driven by the adjacency-based TPG, *n-k* will be driven by the pseudo-random TPG. The idea behind the use of such a structure is to reduce the number of transitions on primary inputs at each clock cycle of the test session, hence reducing the overall switching activity generated in the CUT.

In order to provide important power/energy reduction, inputs of the CUT driven by the adjacency-based TPG are those that have a great impact on the internal switching activity generated in the CUT during pseudo-random testing. A gain function used to select the inputs which must be connected to the adjacency-based TPG has been determined and is described in the next sub-section. The remaining inputs are directly connected to the pseudo-random TPG.

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3.2 Selecting inputs driven by the adjacency-based TPG

If a transition at an input of the CUT propagates to the internal circuit, it will subsequently cause more transitions. Depending on the circuit structure, the transitions at some inputs cause more transitions at internal nodes than those at other inputs. Therefore, reducing the transition density at some inputs must be done by measuring the impact of this reduction on the total switching activity in the circuit. In the context of our study, it means that the transition density on internal nodes of the circuit must be used as a criterion to select inputs driven by the adjacency-based TPG, rather than the transition density on primary inputs only. For this purpose, a gain function, called the *induced activity function*, is calculated for each input of the CUT. This function measures the impact of reducing the transition density at a selected input on the total switching activity generated in the circuit. This function has already been used in [24] and is recall here for the reader's convenience.

Let $n_x(T)$ be the number of transitions at a circuit node x in a time interval of length T. Then, the *transition density* at node *x, i.e.* the average number of transitions per second at x, is defined as:

$$D(x) = \lim_{T \to \infty} \frac{nx(T)}{T} \qquad (1)$$

The transition density provides an effective measure of the switching activity in logic circuits. Now, consider a CUT with n primary inputs $p_1, p_2, ..., p_n$ which are driven by the mixed TPG. Assume that output lines of the mixed TPG (inputs of the CUT) are not correlated, so that the value applied to any input p_i of the CUT is independent of the value applied to any other input p_j, when $i \neq j$. The Boolean difference of the Boolean function implemented by node *x*, *val(x)*, with respect to input p_i is defined as:

$$\frac{\partial val(x)}{\partial pi} = val(x)\big|_{pi=1} \oplus val(x)\big|_{pi=0} \qquad (2)$$

where $\oplus$ denotes an exclusive OR operation. The transition density of a node x can be redefined in terms of the Boolean difference with respect to each input, $\partial val(x)/\partial p_i$, and the transition density of each input, $D(p_i)$, as:

$$D(x) = \sum_{i=1}^{n} P(\frac{\partial val(x)}{\partial pi}) D(pi) \qquad (3)$$

where $P(\partial val(x)/\partial pi)$ is the probability that the Boolean difference $\partial val(x)/\partial pi$ evaluates to 1. Hence, the portion of the transition density of node x due to the transition at a specific input p_i is given by:

$$Dpi(x) = P(\frac{\partial val(x)}{\partial pi}) D(pi) \qquad (4)$$

where *val(x)* is the Boolean function of node *x*. The sum of the transition densities of all nodes in the circuit that can be attributed to the transitions at input p_i is therefore [6]:

$$Dpi = \sum_{\forall x} Dpi(x) \qquad (5)$$

This function, which takes into account dependencies between internal nodes and input p_i, could be used as gain function in our problem. However, an important feature in CMOS technology is that power dissipation in a circuit depends on the load capacitance of internal nodes, which is itself related to the fanout of the nodes. Consequently, when two or more nodes in a CUT have the same transition density, the power induced by transitions on one node may be higher than that induced by transitions on the others, simply because the nodes may have different fanout values. For this reason, the induced activity function is calculated from both the transition density $Dp_i(x)$ on each node x in the circuit and the fanout $F_{an}(x)$ of the nodes. For each input p_i, this function Φp_i is given by:

$$\Phi pi = \sum_{\forall x} Dpi(x).Fan(x) = \sum_{\forall x} P(\frac{\partial val(x)}{\partial pi}).D(pi).Fan(x) \qquad (6)$$

This gain function Φp_i is computed for all inputs of the CUT and used as a criterion to select the inputs which are to be driven by the adjacency-based TPG. In other words, the k inputs which have the greatest Φp_i values are chosen to be driven by the adjacency-based TPG. The remaining inputs are driven by the pseudo-random TPG.

4. Complete BIST TPG structure

The proposed BIST TPG structure is presented in Figure 2. This structure is composed of a l-stage primitive polynomial LFSR (where l is equal to n-k) with a seed calculated from the procedure shown in [25]. This structure is also composed of a sequential block (grey box in Figure 2) providing the means to generate random adjacent vectors of bits. This block is composed of a mapping logic that transcodes a random m-bit vector coming from the LFSR into a k-bit vector (T_1, …, T_k) in which exactly one component has the value 1. More formally, we have $k=2^m$.

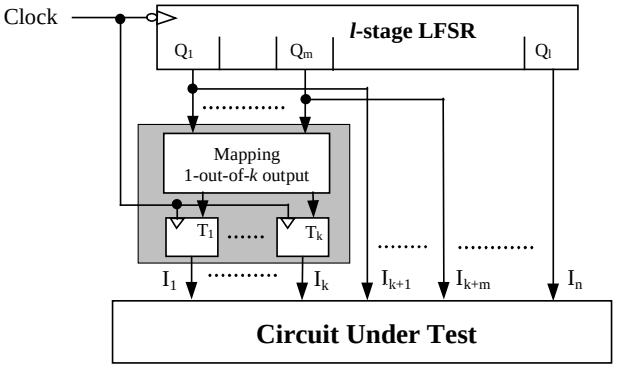

Figure 2: The complete BIST TPG structure

A register made of k T flip-flops is connected at the output of the mapping logic to create a single change of state (on the k outputs of the block) at each clock cycle of the test

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session. For example, if $T_i = 1$ and $T_1 = \ldots = T_{i-1} = T_{i+1} = \ldots = T_k = 0$ at time *t*, then a single transition on input I_i (among the first *k* inputs of the CUT) will occur at the time *t+1*. This structure to generate adjacency tests has been proposed in [26], in which more details can be found.

With respect to the basic scheme shown in Figure 1, it follows that the adjacency-based TPG is constructed from the first *m* stages of the LFSR plus the sequential block providing adjacent vectors of *k* bits. The pseudo-random TPG in Figure 1 is simply the *l*-stage LFSR itself. At each clock cycle of the test session, a test pattern is applied at the *n* inputs of the CUT: the first *k* values of the test pattern differ in exactly one bit position from the test pattern applied at the previous clock cycle, the last *n-k* values are new pseudo-random values provided by the LFSR. Partial adjacency tests are thus applied to the CUT at each cycle of the BIST session.

5. Simulation results and discussion

Benchmarking process described here was performed on the MCNC'93 circuits [11] on a Sun Enterprise 3000 with 256 MB of RAM. The goal of the experiments we performed is twofold: to measure the power and energy savings that our BIST strategy allows to obtain, and to measure the area overhead introduced by this strategy.

For all the experiments, the number of circuit inputs driven by the adjacency-based TPG is *k=8* and the number of outputs of the LFSR used by the mapping logic is *m=3*. These values were chosen after several simulation trials and represent TPG parameters which provide the best tradeoff between the test length required to reach a target fault coverage and the power consumed during BIST.

Circuit	Standard BIST		Adjacency-based BIST	
	Length	FC (in %)	Length	FC (in %)
apex6	8 501	97.75	9 816	98.23
table5	9 993	84.11	9 947	84.45
table3	9 861	97.66	9 868	96.37
apex1	9 664	98.23	9 879	98.20
t481	9 997	84.44	9 840	84.51
apex3	9 624	100	9 100	100
Cps	9 214	65.95	9 729	65.95
alu4	9 847	90.15	9 984	89.35
seq	9 985	77.15	9 910	76.95
misex3	9 999	91.96	9 976	90.42

Table 1: Test length and fault coverage comparison

First, results of the proposed BIST strategy in terms of test length and fault coverage are reported in Table 1. All experiments are based on pseudo-random pattern testing, and complete fault coverage cannot be expected for each circuit. The first part of Table 1 shows the test length and the fault coverage obtained from a classical LFSR as TPG. In the second part of Table 1, the same results (test length and fault coverage) obtained with the proposed Adjacency-based TPG are given for each benchmark circuit. Fault coverage calculations were performed with TestGen of Synopsys [27].

Regarding the above results, it should be noted that the fault coverage obtained with a standard BIST scheme is not affected by the proposed adjacency-based BIST scheme. The fault coverage is roughly the same than that obtained with a classical LFSR, with a test length which is not so far from the test length in a standard BIST scheme.

Cirt	Adjacency-based BIST					
	peak [μW]	power [μW]	energ. [ηJ]	peak reduct	power reduct	energy reduct
duke2	247	1.26	0.73	34.4	47.8	48.9
apex6	765	4.23	2.49	9.4	33.3	22.9
table5	195	1.54	0.91	27.9	36.8	37.6
table3	185	1.54	0.91	17.2	40.3	40.1
apex1	443.5	2.96	1.75	16.3	41.3	40
t481	289.5	3.19	1.88	55.1	34.1	35.1
apex3	391	2.8	1.52	17.5	54.8	57.5
Cps	404.5	3.72	2.17	19.1	40.4	37.1
alu4	880	13.5	8.08	11.5	40.0	39.2
seq	980	8.4	4.99	9.6	38.6	39.1
misex3	427	7.55	4.51	32.2	47.2	47.3

Table 2: Power and energy reduction

Now, results about the power and energy consumption improvement are discussed. Power consumption in each circuit was estimated by using PowerMill, a dynamic simulator provided by the Epic Technology Group of Synopsys [28], assuming a clock period of 60 nanoseconds (frequency equal to 16.6 MHz) and a power supply voltage of 5V. Experiments performed on each circuit have been done with technology parameters extracted from the HSPICE level 6 foundry model for a 0.8μm digital CMOS process. Results are summarized in Table 2 for the MCNC'93 benchmarks. For each circuit, we have reported the peak power, the average power, and the energy obtained with the proposed adjacency-based TPG. Peak power and average power are expressed in microWatts. Concerning energy, the values reported were obtained by performing the product between the average power and the test time (length×T). Energy is expressed in nanoJoules. The last part in Table 2 shows the reductions in peak power, average power and energy consumption (expressed in percentages) compared to a standard BIST scheme. These results on MCNC'93 benchmark circuits show that average power reduction of up to 54.8 %, peak power reduction of up to 55.1 %, and energy reduction of up to 57.5 % can be achieved by using the proposed adjacency-based BIST TPG. Note that the power consumed by the additional part of the adjacency-based TPG (mapping 1-of-n plus T flip-flops) has been considered in these results.

The overhead in gate count of the adjacency-based BIST scheme over the standard BIST one is presented in Table 3 for MCNC'93 benchmarks. This overhead is due to the area taken by the mapping logic inserted between the

CUT and the LFSR to allow generation of partially adjacent vectors. The second and third columns list the number of primary inputs and the number of gates (respectively) in each circuit. This number is expressed in terms of gate equivalents (GE). Column 4 gives the number of additional gates needed for each circuit. This number is obtained by summing the number of gates in the mapping logic with the number of XOR gates of the T flip-flops. Only the XOR gates of the T flip-flops have been counted in our evaluation (instead of the complete T flip-flops) because the size of the LFSR used as TPG (size *l*) is reduced compared with a classical pseudo-random generation (a *n*-stage LFSR would be used in this case), thus saving *k* D flip-flops. The last column in Table 3 shows the area overhead (in terms of gate count) imposed by our solution. These results show up that the area overhead needed to include the mapping logic is below 7.6 % for all benchmarks, and that this percentage decreases when the size of the circuit increases.

Circuit	# inputs	# gates (GE)	# add. gates (GE)	Area overhead
duke2	22	656	41.5	6.32 %
apex6	135	918	41.5	4.52 %
table5	17	1 026	79	7.69 %
table3	14	1 330.5	101.5	7.62 %
apex1	45	1 662	41.5	2.49 %
t481	16	1 850	86.5	4.67 %
apex3	54	1 971	41.5	2.10 %
Cps	23	2 209.5	41.5	1.87 %
alu4	14	4 483	101.5	2.26 %
Seq	41	5 186	41.5	0.80 %
misex3	14	6 720	101.5	1.51 %

Table 3: Area overhead of the proposed solution

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