An Effective Defect-Oriented BIST Architecture for High-Speed Phase-Locked Loops

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Abstract

We propose a new method of defect-oriented testing of PLL using charge-based frequency measurement BIST (CF-BIST) technique. As no test stimulus is required and the test output is pure digital, low-cost and practical implementation of on-chip BIST for a PLL is possible. Fault simulations using the 900MHz PLL from National Semiconductor Corp. show higher fault coverage than previous test methods.

1. Introduction

PLL systems have been conventionally tested using functional specifications, where the functionality of the circuit is verified at some pre-specified test points. This method can result in either excessive or insufficient testing of the circuit. Fault-based testing is an attractive alternative to functional testing, which targets the presence of physical defects in a PLL, thus providing a quantitative measure of the test process [6].

Studies on a number of analog circuits show that relatively simple tests can give high test coverage for common defects, and this can be achieved by using the defect-oriented testing approach [11]. At the same time it also became clear that these tests are not able to cover all faulty products caused by process parametric variations. However, as the result of the ever increasing functional complexity of mixed-signal ICs and the improved IC fabrication-process control, spot defects are the dominant yield limiter in a mature process and a dominant cause of customer rejects for a product in high volume production [1].

In this paper, we propose a new vectorless all-digital BIST technique for PLL based on defect-oriented testing, which uses existing analog components to reduce area overhead and for practical high-speed PLL applications. The proposed scheme can incorporates IEEE 1149.1 boundary scan architecture for easy access of the BIST output or use the existing scan path if available. The key advantage of this technique is that there is no change to the sensitive analog blocks. This ensures that the characteristics of the loop-filter, charge-pump, and VCO are not altered by using the proposed BIST scheme.

The paper consists of following sections. In section 2, the fundamental theory behind the proposed charge-based frequency measurement BIST (CF-BIST) technique is explained. Section 3 describes the CF-BIST structure. The detailed self-test procedure of CF-BIST is explained in section 4. In section 5, Monte-Carlo analysis is carried out to compute the variation in measurements due to tolerance for both fault-free and faulty cases, which shows the accuracy of the test signature analysis. Section 6 looks at the structural fault model and its simulation results. Finally, conclusions are drawn in section 7.

2. Fundamental Theory

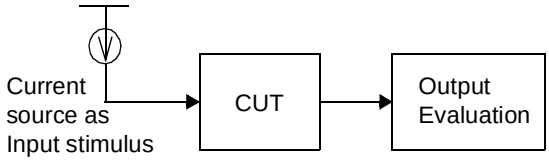

Figure 1. Fundamental theory of the proposed BIST technique

The fundamental theory of the proposed BIST technique for PLL is shown in figure 1. A constant current source is injected to the CUT (Circuit Under Test) as an input stimulus. The resulting signature output is measured and evaluated by the output evaluation block. The CUT in this case consists of analog circuitry with a relatively low input impedance. The output of the CUT is usually a voltage value which is the multiple of the input current injected and the impedance of the CUT circuit. Thus, any change in the impedance will affect the signature output of the CUT, where CUT impedance can be altered by any type of faults including physical defects.

This test theory can be adapted to a PLL for testing the entire PLL, by designating the loop-filter of the PLL as the CUT block. Thus, the relationship between the

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constant current input I to the corresponding voltage output V can be written as in equation (1) for a simple RC loop-filter, where t denotes the duration of time the input current is applied.

$$V = RI + \frac{1}{C} \cdot \int_{t} I dt \qquad (1)$$

Thus, a fault can be screened by comparing the magnitude of the output voltage V against a mask.

For a more practical realization, a PLL with a open loop configuration as in figure 2 is considered.

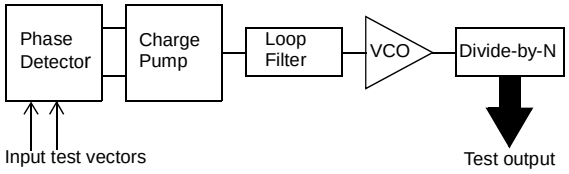

Figure 2. PLL test application of the proposed theory.

For a constant current source used in this test, we can utilize the existing charge-pump in the PLL which generates a perfect current source by digitally controlling the input of the charge-pump circuit. By using the existing charge-pump, there are three major advantages which also covers most of the previously addressed problems in building BIST for PLL:

- It eliminates the need for on-chip precision current source which will occupy relatively large die area.
- The charge-pump itself is tested for possible faults. This saves the overall test time by performing a single test for multiple of blocks.
- The sensitive loop-filter input node is not altered since the current source which is the output of the charge-pump is already connected to the loop-filter. This ensures the sensitive analog node is not loaded which is a common problem in previous PLL BIST techniques [4],[5],[8].

For the output voltage measuring device, we can use the existing VCO and the divide-by-N block to measure the output voltage signature of the loop-filter. The VCO generates an output frequency according to the loop-filter's output voltage, the VCO output is then fed to the divide-by-N block which acts as a frequency counter. Thus, by retrieving the binary data store in the counter, we can digitally read the output frequency of the VCO which represents the output signature of the loop-filter. The advantages of using the existing VCO and divide-by-N as a measuring device are:

- It eliminates the need for an on-chip precision voltage measuring device, which can take-up considerable die area.
- As the output voltage of the loop-filter is being measured, the VCO and divide-by-N blocks are also tested for possible faults.
- The VCO is tested without any change to its sensitive analog feedback loop.
- The test output is in a digital form, thus enabling the test controller and evaluation blocks to be constructed with only the digital parts.

While this method is simple, it can test all the analog blocks in a PLL for possible faults. The major advantage of this theory is that it uses mostly existing blocks for testing and measurement, thus minimizing the area overhead. Furthermore, the test output is transformed into a digital value which can be evaluated with relatively reliable digital circuitry.

3. Proposed CF-BIST structure

The proposed CF-BIST block diagram is shown in figure 3, where a controller/grabber block and a multiplexer are added to the existing PLL.

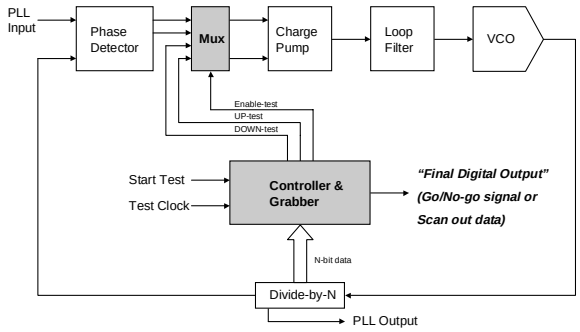

Figure 3. Proposed CF-BIST technique for PLL.

The multiplexer (mux) is added to the output of existing phase-detector block and provides input controls for stimulating the loop-filter. In normal PLL operation, the mux is set to bypass the phase-detector output signals. In test mode, the mux provides charge-pump control signals generated by the controller/ grabber block to the charge-pump input. The VCO will then oscillate according to the output voltage of the loop-filter. The oscillation frequency reflects the faults in the loop-filter, charge-pump, and the VCO. The deviation of the oscillation frequency from its nominal value indicates a faulty circuit in the loop.

3.1 Controller/Grabber Block

When the BIST system is active, the controller/ grabber block controls the multiplexer in the phase-detector to provide proper stimulus for the loop-filter. It consists of two sub-blocks which are the state-machine and the grabber, and the entire block consists of digital components, thus, it is highly reliable compare to analog counterparts.

3.2 Divide-by-N

The divide-by-N, which is used in a PLL to shift the

output frequency to the input dynamic range, is utilized as a frequency counter in the proposed BIST system. When the BIST system is in the self-test mode, the divide-by-N counts the output frequency of the VCO and the resulting digital value is grabbed and stored by the controller/grabber block. The digital frequency data stored in the controller/grabber block can be scanned out using the IEEE 1149.1 boundary scan path or any existing scan path available.

3.3 Test Clock Speed, Counter Bit Number Determination Algorithm

To determine the test clock frequency and the bit-width of the counter, three input specifications are needed for calculation:

- F_{max} Maximum VCO output frequency
- F_{min} Minimum VCO output frequency
- A Accuracy of the measurement in (%).

From F_{max} and the test duration T, the maximum counter output C_{max} is given by

$$C_{max} = \frac{T}{1/(F_{max})} \quad (2)$$

where T is the amount of time the counter is enabled for a measurement. If we include the resolution of the measurement A in equation (2), it gives the following relationship:

$$C_{max} - 1 = \frac{T}{\frac{1}{F_{max} - (F_{max} - F_{min}) \bullet A}} \quad (3)$$

where $(F_{max}\text{-}F_{min})A$ represents the minimum value of frequency that can be measured with the counter.

Combining equation (2) and (3) gives

$$C_{max} = \frac{F_{max}}{(F_{max} - F_{min}) \bullet A} \quad (4)$$

To count up to C_{max}, the counter must have at least C_B bits, where:

$$C_B = Integer(\log_2 C_{max}) + 1$$

The test duration T can be calculated using the following equation:

$$T = \frac{C_{max}}{F_{max}}$$

Therefore, the test clock frequency F_{test} is given below.

$$F_{test} = \frac{1}{T}$$

For example, if a PLL has following specifications:

- F_{max} = 900MHz
- F_{min} = 400MHz
- A = 0.01 (1% resolution in measurement)

Then from equation (4), C_{max} is 180 which yields the counter bit-width of 8 bits. Further through the procedure yields F_{test} to be 5MHz which is the test clock speed. Hence, 8bit wide counter and 5MHz test clock are the only information needed to construct the proposed CF-BIST structure.

In this section, the proposed CF-BIST structure and procedures to construct the BIST circuitry was explained. The detailed explanation of CF-BIST technique will be discussed in the following section.

4. CF-BIST Technique

In order to better understand the concept of CF-BIST technique, simplified schematic diagram of the charge-pump and the loop-filter (figure 4) is used. The charge-pump injects a constant current for a certain period of time to the loop-filter, creating a output voltage variation in the loop-filter. This is then converted in to a frequency value by the VCO. Finally, the divide-by-N which acts as a counter converts the frequency value into a digital data for a simple test output evaluation.

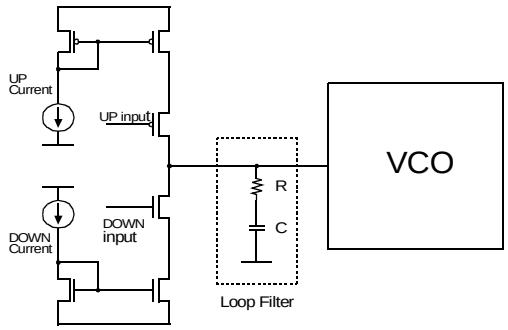

Figure 4. Simplified schematic of the charge-pump and the loop-filter.

The detailed test procedure is as follows:

STEP 1: DC reference count

1. *DC voltage generation*: A DC voltage is generated by closing both the up and down current transistors to form a voltage divider. The generated DC voltage should be around mid-point voltage. Since this mid-point value is used as a reference value instead of an absolute value, it is not necessary to be at the exact mid-range.
2. *Voltage measurement*: The generated DC voltage is converted to frequency by the VCO and counted by the divide-by-N block. The DC voltage value which is now in a digital form, is grabbed and stored in the controller/grabber block which is the reference-count (F1) in figure 5.

STEP 2: Discharge test

3. *Stimulus injection*: In order to discharge the loop-

filter, the up-current switch is opened while the down-current switch is kept closed. This down-current acts as the input stimulus for the loop-filter test.

4. *Voltage measurement*: At the end of the discharge period, the output voltage of the loop-filter is measured with the VCO and the counter. This value is stored in the controller/grabber block as down-count (F2) which can be scanned out using the scan path at the final test step.

STEP 3: Charge test

5. *Stimulus injection*: In order to charge the loop-filter, the down-current switch is opened while the up-current switch is kept closed. This up-current acts as the input stimulus for the loop-filter test.
6. *Voltage measurement*: At the end of the charge period, the output voltage of the loop-filter is measured with the VCO and the counter, and this digital value is grabbed and stored in the controller/ grabber block as up-count (F3) which will be used in the next step.

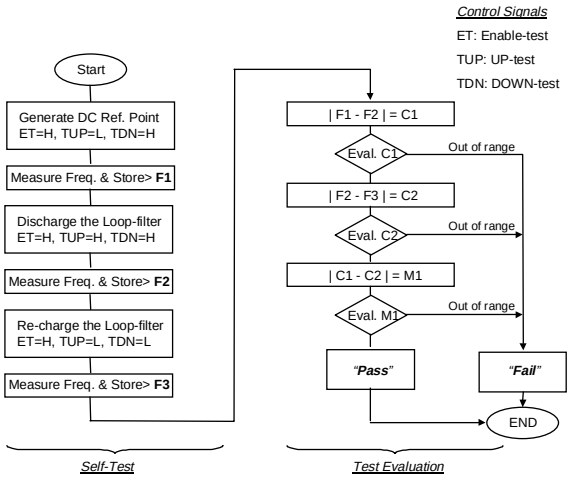

Figure 5. Overall self-test procedure.

In figure 5, a flow chart is drawn to help understand the overall test procedure. The control signals *ET*, *TUP* and *TDN* control the charge-pump which are generated by a state-machine in the controller/grabber block. *ET*, which is the test enable signal, should remain high during the test period. It sets the mux at the end of the phase-detector block in the test mode. *TUP* controls the UP-current switch in the charge-pump when *ET* is high. It is active-low, since the p-type MOS transistor is used for UP-current switch. TDN is the control signal for the DOWN-current switch which is the n-type transistor.

STEP 4: Test evaluation

7. *Scan out*: Using any existing scan path as in figure 6, the three stored digital values (F1,F2,F3) in the controller/grabber block are scanned out for test evaluations. Then, the |F1-F2| and |F3-F2| are evaluated for possible faults in the PLL blocks according to the flowchart in figure 5.

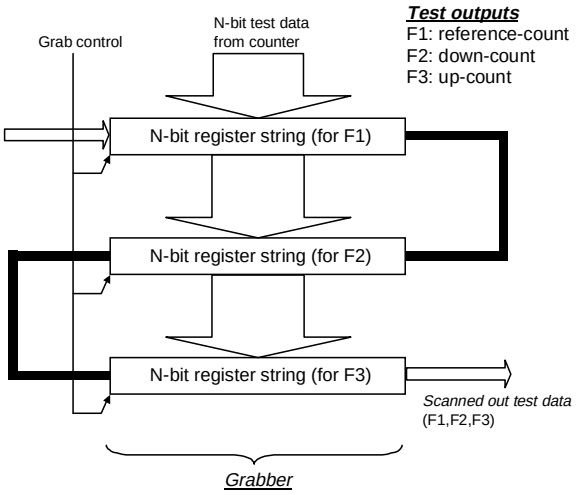

Figure 6. Grabber portion of controller/grabber block.

8. *Self checking*: An alternative way of evaluation, if a scan path is not available in the chip or the BIST has to incorporate the self-checking ability, is adding a subtracter and a comparator to form a self-checker in the controller/grabber block. This is shown in figure 7, where the subtracted values are compared with the preset values to make a go/no-go decision.

Figure 8 shows the overall timing of the controller/ grabber block, the signals shown are related to the multiplexer and the controller/grabber block. The only input signals are Test-clock and Start-test signals. The Enable-test and measure-&-store-enable signal are internal signals generated by the controller. The output signals are UP-test and DOWN-test which controls the up-current switch and the down-current switch of the charge-pump, respectively.

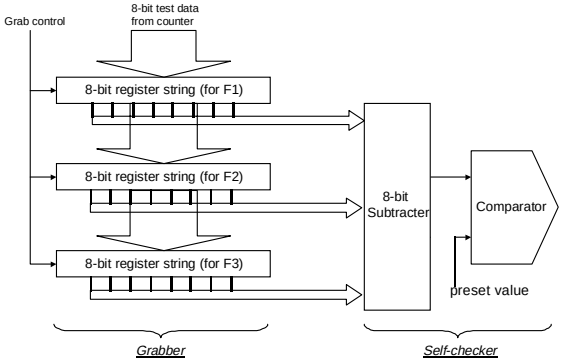

Figure 7. Grabber portion of the controller/grabber block with the self-checker block.

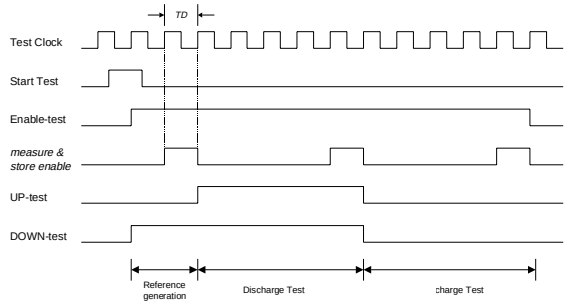

Figure 8. Timing diagram of CF-BIST.

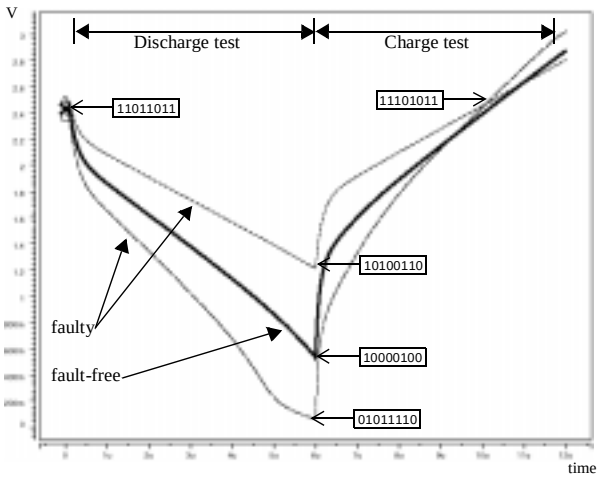

Figure 9. Output voltage of the loop-filter during the test using a real PLL.

Table 1: Final digital outputs and differences due to fault

Fault	Ref. count (F1)	Down count (F2)	Up count (F3)	|F1-F2|	|F3-F2|
Fault-free	11011011	10000100	11101011	87	103
Faulty case1	11011011	10100110	11101011	53	69
Faulty case2	11011011	01011110	11101011	125	141

In figure 9, example test simulations for faulty and fault-free cases are shown using the PLL provided by the National Semiconductor Corp. which has the operating range around 900MHz with a single 3.3 volt power supply. It shows the output voltage of the loop-filter as well as the actual measured frequency data at each measurement points. These binary data are evaluated using the above test evaluation process (STEP 4). Table 1 shows the calculated differences between F1, F2 and F3 which are used to make a final decision. For the faulty cases, the difference between F1 and F2 were 53 and 125, where in the fault-free case showed 87. Also, the difference between F2 and F3 measured 69 and 141 for the faulty cases, 103 for the fault-free case. The values of |F1-F2| and |F3-F2| for faulty case show more than 33% deviations from the fault-free case value. Therefore, table 1 and the graph shown in figure 9 clearly demonstrates the fault detectability of the proposed BIST technique.

5. Monte-Carlo Analysis

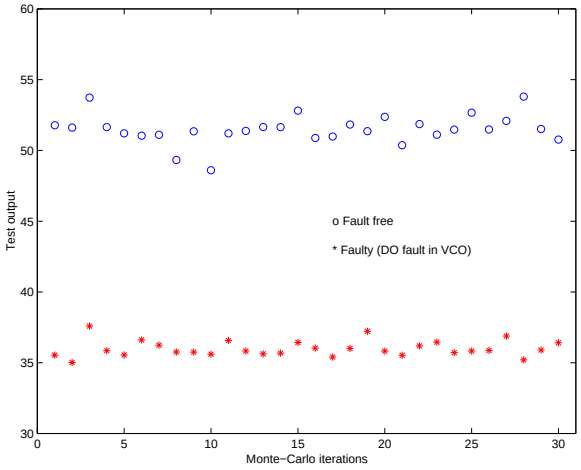

Figure 10. Monte-Carlo analysis for charge test for one DO fault in VCO.

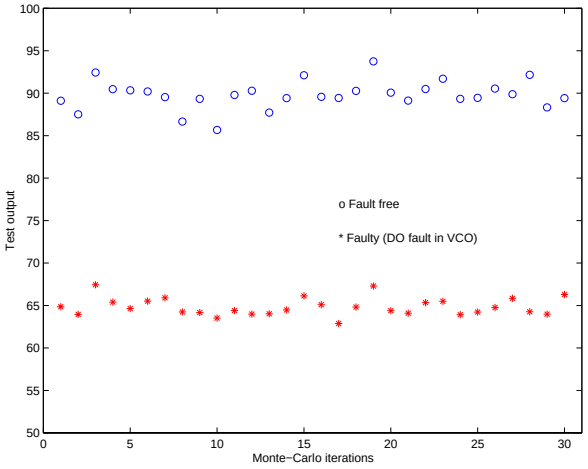

Figure 11. Monte-Carlo analysis for discharge test for one DO fault in VCO.

We have analyzed the effects of the process variations for the differences of the measured digital counts in two tests, which are charge test and discharge test. Figure 10 shows Monte-Carlo results for the charge test, both fault-free and faulty cases are displayed for comparison. In this case, we chose drain-open fault in VCO, since its test results showed the

least separation from the fault-free test results. Thus, it is the worst case for the Monte-Carlo analysis. As it can be observed in both figures 10 and 11, the output of the faulty case varies well within the tolerance window, which means that the fault stays detectable even with the presence of process variations.

6. Structural Fault Simulation

We have built a structural fault model of National's PLL which includes complete set of catastrophic (hard) faults, to demonstrate the effectiveness of CF-BIST technique in detecting structural faults.

The total number of structural faults (defects) was 395. These served as a practical fault model of the PLL for evaluating the proposed CF-BIST approach.

To demonstrate the efficiency of the proposed CF-BIST technique, all 395 faults were used and simulations were carried out to evaluate the fault coverage for each configuration. Table 2 presents the fault coverage results.

As it can be observed in table 2, the CF-BIST structure proposed in this report clearly shows the effectiveness of the fault test. Therefore, it provides a low-cost and highly-effective BIST solution for detecting structural faults.

Table 2: Fault coverage results

Fault Type	Fault coverage (%)
Drain-open (DO)	100
Gate-open (GO)	82.4
Source-open (SO)	100
Gate-to-drain short (GDS)	100
Gate-to-source short (GSS)	100
Drain-to-source short (DSS)	97.1
Resistor-open (RO)	100
Resistor-short (RS)	100
Capacitance-short (CS)	100
Overall	**96.5**

7. Conclusion

A new PLL BIST technique, which exploits the defect-oriented testing of analog and mixed-signal circuits based on the charge-base frequency measurement methodology, is proposed. The proposed technique has been compared with previously announced PLL BIST techniques, which clearly showed the advantages of the proposed BIST method. Fault simulation results showed higher fault coverage than previous test methods. The proposed BIST scheme is applied to a CMOS 0.25μm PLL without any alteration to the existing analog blocks. The CF-BIST uses existing blocks to perform the test and the test output is pure digital, thus, a low-cost practical on-chip BIST scheme for a PLL is possible.

Acknowledgment

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