Low-Power Design Using Multiple Channel Lengths and Oxide Thicknesses

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Two CMOS design techniques use dual threshold voltages to reduce power consumption while maintaining high performance. Simulation results show power savings of 21% for one technique at low activity, and for the other, 19% at high activity and 38% at low activity.

With the increasing use of portable and wireless electronic systems, reducing power consumption has become an important design concern. Power dissipation affects performance and battery life, and greatly affects packaging, reliability, and heat removal costs.[1,2]

In digital CMOS circuits, total power consumption has static and dynamic components. Modern technologies scale down feature sizes to achieve high density, high performance, and low power. Scaling down the supply voltage can reduce both static and dynamic power consumption. However, a commensurate decrease in transistor threshold voltage (V_{th}) is necessary to satisfy performance requirements. Such scaling increases subthreshold leakage current (I_{sub}), as "The leakage current problem" sidebar explains.

Using a dual-V_{th} design can reduce I_{sub}.[3] The idea is to use higher threshold voltage for transistors on noncritical paths to reduce static power, and low-threshold transistors on critical paths to maintain performance. There are several different ways to achieve a higher threshold voltage. Traditionally, researchers have achieved multiple V_{th} values by adjusting the channel doping concentration and modifying the body bias.[4,5] Here, we consider two other techniques, multiple-channel-length CMOS (M_LCMOS) and multiple-oxide-thickness CMOS (M_{ox}CMOS), to tune a transistor's threshold voltage. We developed a dual-V_{th} design algorithm that could handle these two techniques as well as the traditional multiple-channel-doping/multiple-body-bias (M_DM_BCMOS) technique. We then compared the effectiveness of the three techniques in simulations conducted with IEEE International Symposium on Circuits and Systems (ISCAS) benchmark circuits.

Dual-V_{th} CMOS circuit

Researchers have considered the dual-V_{th} approach as a promising way to address the leakage problem in high-performance CMOS circuits. Because the subthreshold leakage current has an exponential relationship with the threshold voltage, increasing V_{th} significantly reduces I_{sub}, along with static power consumption. However, as a transistor's threshold voltage increases, the equivalent *On* resistance also increases, thereby increasing the gate's propagation delay. Dual-V_{th} CMOS circuits assign low threshold voltage to the transistors on the critical paths to maintain high performance, and assign an optimum high threshold voltage to the transistors on noncritical paths to reduce leakage power. But assigning the high V_{th} to all the transistors on noncritical paths is not possible, because the critical path could change and critical delay might increase.

Figure 1 shows an example of a dual-V_{th} CMOS circuit. Dark-shaded gates represent those on the critical paths. Figure 1a represents the original, single-V_{th} circuit with a threshold voltage of 0.2 V. Figure 1b shows the dual-V_{th} CMOS circuit with low V_{th} of 0.2 V and high V_{th} of 0.4 V. The dual-V_{th} design preserves the critical paths and critical delays.

Dual-V_{th} CMOS technologies

Here we compare different dual-V_{th} CMOS techniques based on MiniMOS simulations of 0.25-micron CMOS technology.[6] For all simulations, the transistor's

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base-case channel length was 0.25 micron, and the oxide thickness was 5.0 nm.

We can express a transistor's threshold voltage as[7]

$$V_{th} = V_{T0} + \gamma[(|-2\phi_F + V_{SB}|)^{1/2} - (|2\phi_F|)^{1/2}]$$
$$V_{T0} = V_{FB} - 2\phi_F - Q_{B0}/C_{ox}$$
$$V_{FB} = \phi_{ms} - Q_{ox}/C_{ox} - Q_I/C_{ox}$$

where V_{TO} is the 0-bias threshold voltage, γ is the body-effect coefficient, ϕ_F is the Fermi potential, and V_{SB} is the bias of the source and body. Q_{B0}, Q_{ox}, and Q_I are the fixed charge in the depletion region, the fixed charge at the oxide-silicon interface, and the threshold-adjusting implanted impurities. C_{ox} is the oxide capacitance, and ϕ_{ms} is the work-function difference. Because of source and drain charge sharing for short-channel devices, V_{th} roll-off occurs when scaling the channel length. We can adjust V_{th} by implanting threshold-adjusting impurities, varying V_{SB}, altering the channel length, or modifying the oxide thickness.

Multiple channel doping, multiple body bias

The traditional M_DM_BCMOS technique lets us achieve dual threshold voltages by adjusting the channel doping densities, as in Figure 2.

Achieving dual thresholds requires two additional masks—a commonly used approach for modifying threshold voltages. However, the threshold voltage can vary between dies. Even within a die, the threshold-voltage variation can be significant for scaled technologies. Hence, for dual-threshold designs, the low and high thresholds should be far enough apart to be distinguishable under process variation.

Given a MOSFET's body effect, another way to vary V_{th} is to adjust the body bias. However, if the transistors' thresholds are tuned individually, the transistors might not be able to share the same

The leakage current problem

Scaling down the supply voltage can benefit both static and dynamic power consumption. However, it also increases the subthreshold leakage current (I_{sub}), as the following equation shows:

$$I_{sub} = Ae^{q/n'kT(VG - VS - VT0 - \gamma' VS + \eta VDS)}(1 - e^{-qVDS/kT})$$

where A is a constant, q is the electronic charge, n' is the transistor's subthreshold swing coefficient, k is Boltzmann's constant, T is the temperature, V_{T0} is the 0-bias threshold voltage, γ' is the linear body-effect coefficient, and η is the drain-induced barrier-lowering (DIBL) coefficient. Moreover, as circuits progress further into the deep-submicron region, the gate-oxide thickness becomes thinner to reduce short-channel effects. As a result, gate-oxide tunneling current, which is negligible in current process technology, can be significant.

We can model gate-oxide tunneling leakage J_n as

$$J_n = AE_{ox}^2 \exp\left(\frac{-B[1-(1-(V_{ox}/\Phi_b))^{3/2}]}{E_{ox}}\right)$$

where E_{ox} is the electric field, V_{ox} is the voltage across the gate oxide, Φ_b is the barrier height, and A and B are constants. Results from the Medici simulation in Figure A show that gate-oxide tunneling leakage is comparable to subthreshold leakage for 90-nm process technology and below. The reduction of the supply voltage alone is not enough to counteract these effects. Hence, other techniques are necessary to achieve lower leakage current while maintaining performance.

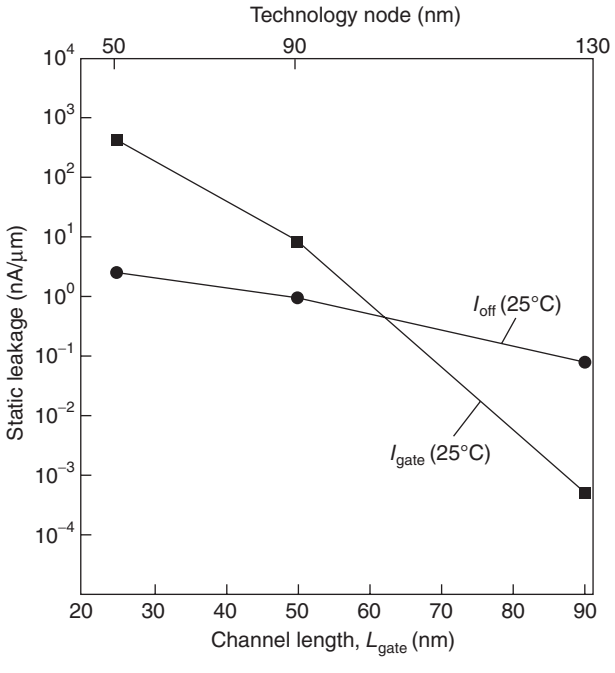

Figure A. Static leakage for different technologies.

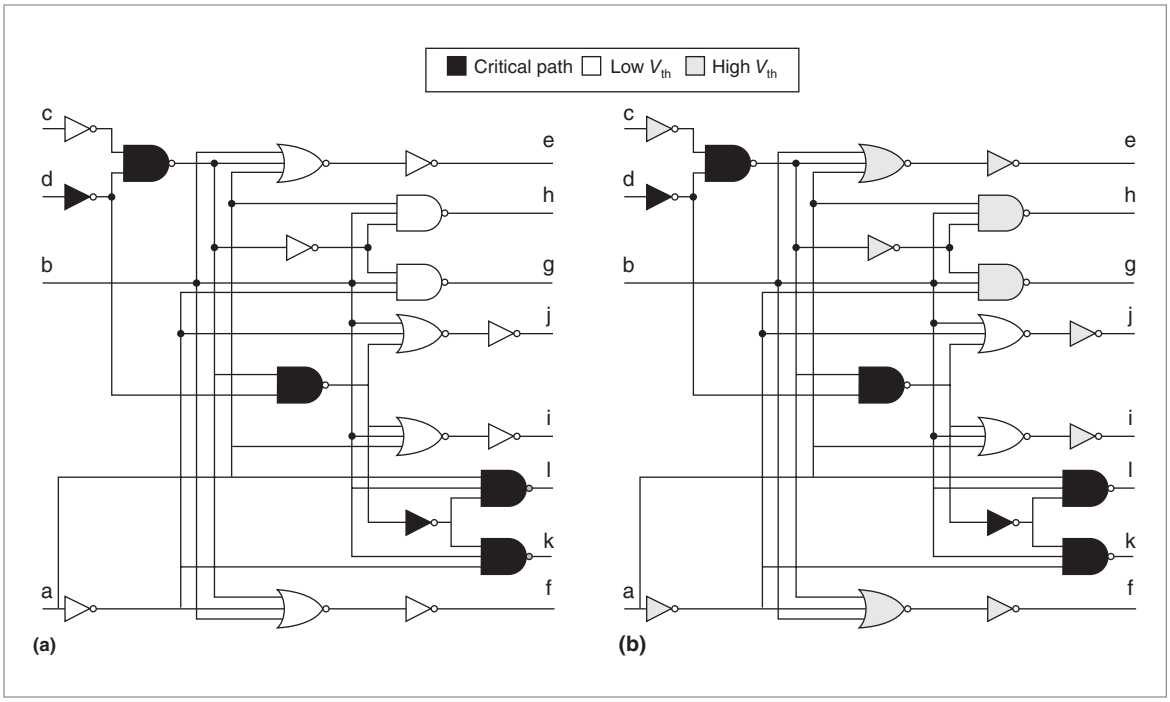

Figure 1. Example circuit: original, single-V_{th} (a) and dual-V_{th} (b) CMOS circuits.

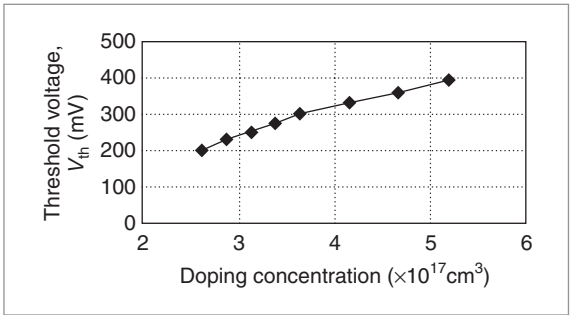

Figure 2. V_{th} at different channel doping densities.

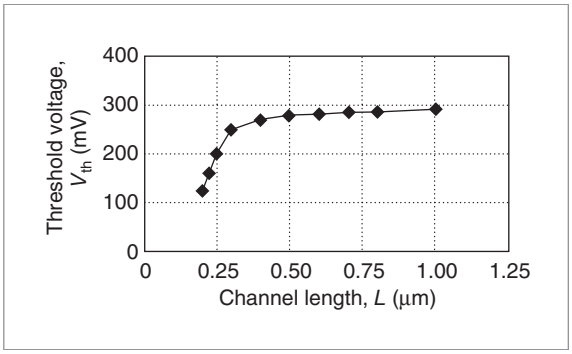

Figure 3. V_{th} roll-off for NMOS.

well; hence, triple-well technology could be necessary.[8]

Multiple channel length

For short-channel transistors, the threshold voltage decreases with the decrease in channel length (V_{th} roll-off). Figure 3 illustrates how feature-size scaling decreases threshold voltage.

M_LCMOS uses short-channel transistors on critical paths, and an optimal long-channel length on noncritical paths. However, for transistors whose feature size is close to 0.1 micron, Halo doping profiles are necessary to suppress the short-channel effect.[9] For such doping profiles, the V_{th} roll-off can be sharp, and controlling the threshold voltages near the minimum feature size for such technology can be difficult. Thus, this technique might not be suitable for scaled technologies using Halo.

Multiple oxide thicknesses

M_{ox}CMOS uses large gate-oxide thicknesses for off-critical paths, and thin gate-oxide thicknesses for critical paths. Using larger gate-oxide thicknesses gives a transistor a higher threshold voltage. However, suppressing the short-channel effect requires increasing the transistor's channel length to give the device a good *aspect ratio*.[10] The aspect ratio is the ratio between the transistor's lateral and vertical dimensions, and it measures short-channel immunity. We can express aspect ratio *AR* as

$$AR = \frac{L}{\sqrt[3]{t_{ox}\left(\varepsilon_{si}/\varepsilon_{ox}\right)}\sqrt[3]{d}\sqrt[3]{X_j}}$$

where L is the channel length, t_{ox} is the oxide thickness, ε_{si} and ε_{ox} are the permittivities for silicon and oxide, d is the depletion depth, and X_j is the junction depth. Altering the gate-oxide thickness along with the channel length has both positive and negative effects on the circuit's performance and power consumption. Thus, a careful analysis is necessary. Figure 4 gives the threshold voltage at different t_{ox} values for constant AR.

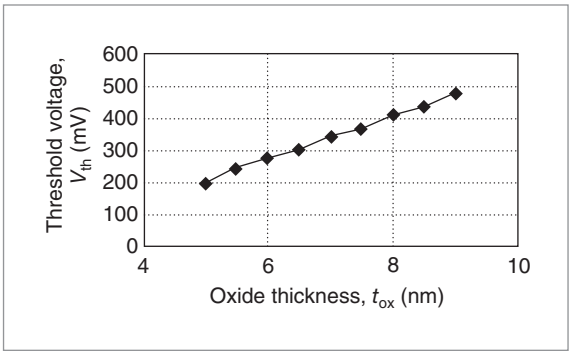

Figure 4. V_{th} at different oxide thicknesses.

The process technology for multiple-oxide-thickness design is complicated. However, a larger oxide thickness can reduce gate capacitance. This reduction can then reduce both dynamic power and subthreshold leakage power. Moreover, the thicker oxide can reduce gate-oxide tunneling leakage. Recently, Chang et al. presented a multiple-oxide-thickness process technology.[11]

Dual-V_{th} CMOS design algorithm

We have presented a dual-V_{th} design methodology that assigns different threshold voltages to transistors in static CMOS circuits to achieve the best leakage savings under given delay constraints.[3] However, this algorithm is suitable only for conventional dual-V_{th} CMOS circuits using M_DM_BCMOS. Here, we present a design algorithm that is suitable for M_LCMOS and M_{ox}CMOS designs as well.

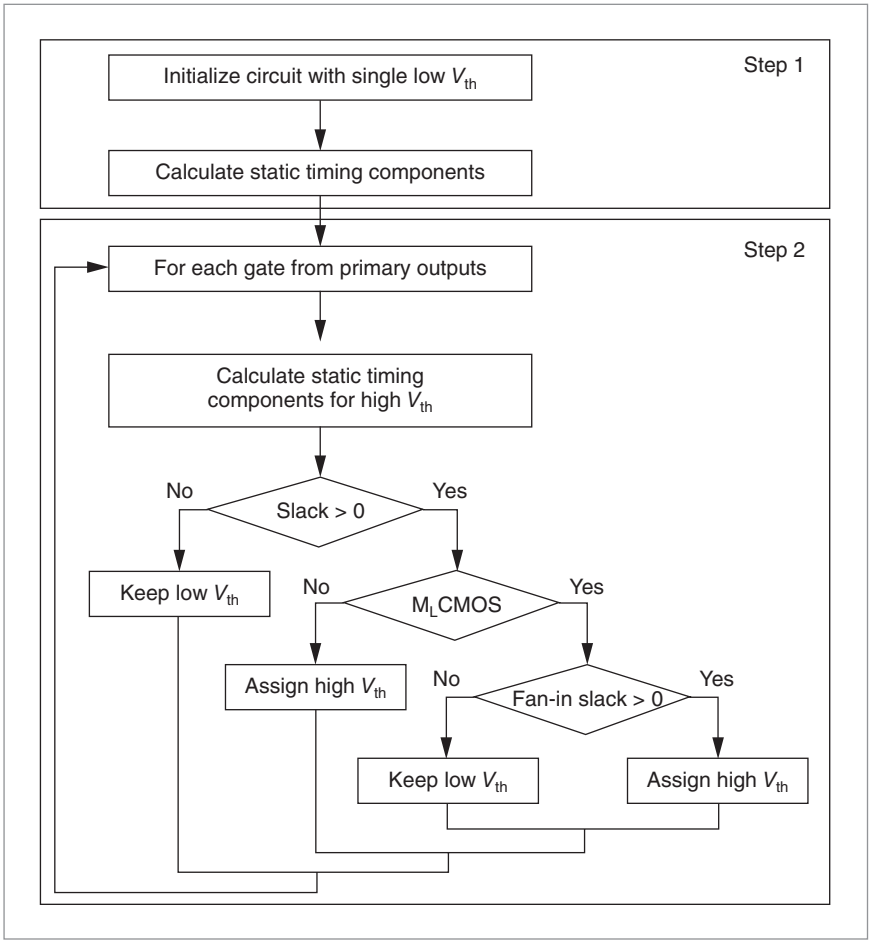

Figure 5. Dual-V_{th} CMOS design algorithm.

Figure 5 gives a general flowchart for this dual-V_{th} CMOS design algorithm. The algorithm starts by initializing all of a circuit's gates with a single low V_{th}. During initialization, the algorithm forward traces the circuit, level by level. It then calculates each gate's propagation delay, arrival time, departure time, and slack. (A gate's slack is the amount of time the gate can be slowed down without affecting circuit performance.) The algorithm determines the critical delay and critical paths by back tracing the circuit from the primary outputs.

The next step is to assign a high threshold voltage to gates on noncritical paths under the given delay constraints. The algorithm does this by back tracing the circuit, level by level. If the algorithm must assign such a voltage to a gate, that gate's propagation delay increases, thereby reducing the slack. For M_DM_BCMOS and M_{ox}CMOS, if the new slack is positive, the algorithm can assign the high V_{th} to the gate without affecting the crit-

ical delay. However, for M_LCMOS, changing the gate length also affects the propagation delay of all fan-in gates. Thus, the algorithm can assign a high V_{th} to a gate only when the new slack of that gate and the slack of all its fan-in gates are positive.

It is then possible to estimate the circuits' dynamic and static power using the methods that Roy and Prasad described.[10] The optimal high V_{th} and corresponding optimal channel length and oxide thickness for each circuit corresponds to the high V_{th} that gives the lowest total power consumption.

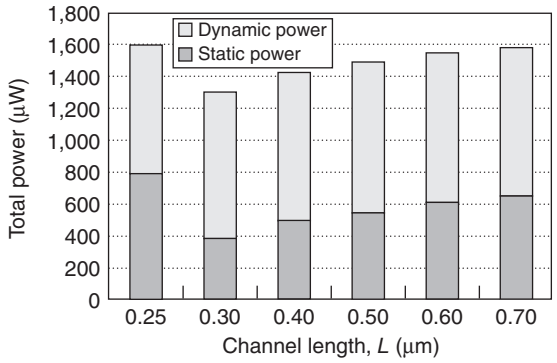

Figure 6. Total power at different long-channel lengths.

Implementations and results

We implemented the dual-V_{th} CMOS design algorithm in C under the Berkeley Student Information Systems (SIS) environment. We used technology mapping to map the circuits with a library containing, for simplicity, only NAND gates, NOR gates, and inverters. Threshold voltages are based on the MiniMOS simulations mentioned earlier. We tested the design methodologies on ISCAS benchmark circuits with a supply voltage of 1.0 V. For all experiments, the nominal channel widths for PMOS and NMOS transistors were 10.5 microns and 3 microns.

Conventional dual V_{th}

M_DM_BCMOS is the traditional dual-V_{th} design tech-

Table 1. Total power savings for M_LCMOS, where α is the input switching activity, L_2 is the larger channel length, and ΔP is the power savings between the single- and dual-length designs.

			Static power			Dynamic power			Total power		
Circuit no.	α	Optimal L_2 (μm)	Single length (μW)	Dual length (μW)	ΔP (%)	Single length (μW)	Dual length (μW)	ΔP (%)	Single length (μW)	Dual length (μW)	ΔP (%)
C432	0.03	0.30	269.5	204.0	24.3	103.4	108.8	–5.2	372.9	312.7	16.1
	0.30	0.30	268.4	204.4	24.0	654.6	687.4	–5.0	923.0	891.8	3.4
C499	0.03	0.30	643.5	439.9	31.6	1,193.6	1,240.8	–4.0	1,837.1	1,680.7	8.5
	0.30	0.25	643.5	643.5	0	4,359.3	4,359.3	0	5,002.8	5,002.8	0
C880	0.03	0.30	478.8	203.2	57.6	335.0	404.7	–20.8	813.8	607.9	25.3
	0.30	0.25	477.4	477.4	0	2,053.5	2,053.5	0	2,531.0	2,531.0	0
C1355	0.03	0.30	655.8	485.2	26.0	1,035.8	1,071.2	–3.4	1,691.7	1,556.5	8.0
	0.30	0.25	655.7	655.7	0	3,592.1	3,592.1	0	4,247.8	4,247.8	0
C1908	0.03	0.30	792.1	387.1	51.1	823.1	916.5	–11.3	1,615.2	1,303.6	19.3
	0.30	0.25	792.1	792.1	0	3,265.3	3,265.3	0	4,057.3	4,057.3	0
C2670	0.03	0.30	1,126.2	510.7	54.7	557.1	659.3	–18.3	1,683.3	1,170.0	30.5
	0.30	0.25	1,126.0	1,126.0	0	3,437.0	3,437.0	0	4,563.1	4,563.1	0
C3540	0.03	0.30	1,559.5	697.2	55.3	805.3	919.9	–14.2	2,364.9	1,617.1	31.6
	0.30	0.30	1,559.4	697.0	55.3	4,481.9	5,115.6	–14.1	6,041.3	5,812.6	3.8
C5315	0.03	0.30	2,420.3	1,006.5	58.4	1,695.5	1,992.8	–17.5	4,115.8	2,999.3	27.1
	0.30	0.25	2,420.4	2,420.4	0	10,098.3	10,098.3	0	12,518.7	12,518.7	0
C6288	0.03	0.30	3,245.8	2,472.9	23.8	1,503.9	1,589.7	–5.7	4,749.8	4,063.6	14.5
	0.30	0.30	3,246.1	2,472.9	23.8	5,090.2	5,363.0	–5.3	8,336.3	7,835.9	6.0
C7552	0.03	0.30	3,635.0	1,576.7	56.6	1,922.7	2,218.7	–15.4	5,557.8	3,795.3	31.8
	0.30	0.30	3,634.8	1,576.5	56.6	11,614.7	13,371.5	–15.1	15,249.5	14,947.5	2.0

nique. The low threshold voltage is assumed to be 200 mV. Because this technique raises the transistor's threshold voltage by changing the channel profile's doping density or the body bias, there is virtually no effect on the load capacitance. Hence, the circuit's dynamic power remains essentially the same, while the static power decreases, yielding a net decrease in total power consumption. The optimal high V_{th} is approximately 0.35 V, with 67% average savings in static power consumption. Total power savings at switching activities of 0.03 and 0.3 are 40% and 15%.

Multiple channel length

For M_LCMOS, minimum feature length L_1 is 0.25 micron, corresponding to the threshold voltage of 200 mV. Larger channel length L_2 varies from 0.25 micron to 0.7 micron. The simulation occurs at different input switching activities α.

Figure 6 shows the static, dynamic, and total power of benchmark circuit C1908 at different channel lengths with $\alpha = 0.03$. With larger L_2, although the savings in static power is greater, fewer transistors can go into L_2, because of a higher increase in node delay. Dynamic power also increases, because of larger capacitances. Hence, an optimal L_2 must exist that gives the lowest total power consumption. For the circuit in Figure 6, the optimal L_2 is 0.30 micron, which translates to $V_{th} = 246$ mV, with 19.3% savings in total power.

Table 1 gives the results of applying this technique to the ISCAS benchmark circuits. At low switching activity, the average optimal L_2 is 0.3 micron. The average savings in static power consumption is approximately 44%, the average increase in dynamic power is 12%, and the total power consumption decreases by an average of 21%. At high switching activity, because of the large increase in dynamic power, the total power for some circuits cannot improve. Thus, M_LCMOS is more suitable for low-activity circuits in which the increase in dynamic power is smaller than the static power reduction.

Multiple oxide thicknesses

For M_{ox}CMOS, lower oxide thickness t_{ox1} of the transistor based on the MiniMOS simulations is 5.0 nm (V_{th} = 200 mV). Figure 7 shows the total power and its different components for benchmark circuit C1908 at different high oxide thicknesses t_{ox2}. The optimal t_{ox2} for this circuit is 6.5 nm, which translates to $V_{th} = 304$ mV. This gives a 37% savings in total power: 68% savings in static power, and 6% savings in dynamic power at low switching activities.

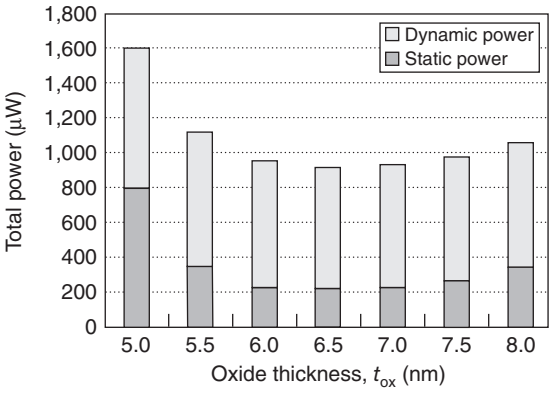

Figure 7. Total power at different high-oxide thicknesses.

Table 2 shows the results of applying M_{ox}CMOS on the ISCAS benchmark circuits. Static power decreases by an average of 60%, and dynamic power decreases by about 6%. Total power consumption improves by approximately 38% and 19% at low and high switching activities, respectively. Thus, M_{ox}CMOS can reduce total power consumption at both low and high switching activities because both dynamic power and static leakage power decrease with increased t_{ox}.

To explore the power consumption trend for future technology, in which gate tunneling leakage will become more significant, we applied M_{ox}CMOS to ISCAS benchmark circuits using the 70-nm Berkeley Predictive Technology Model provided by the Device Group at the University of California, Berkeley (http://www-device.eecs.berkeley.edu/~ptm). Parameters such as V_{DD} and t_{ox} follow the guidelines set by the 2000 *International Technology Roadmap for Semiconductors*.[12] For this technology, the supply voltage is 0.9 V, and the low oxide thickness is 1.2 nm. Oxide thickness t_{ox2} ranges from 1.2 nm to 2.8 nm. Simulation results show that M_{ox}CMOS can reduce the circuits' static power and dynamic power by an average of 60% and 20%, with a 70% decrease in gate tunneling leakage. Total power can decrease by approximately 46% at low switching activity, and 35% at high switching activity. These results show that M_{ox}CMOS is very effective in reducing power consumption for scaled CMOS technologies.

Efficiency comparison

Table 3 compares the power savings and process complexity for the three power optimization techniques. For M_DM_BCMOS, the circuit's dynamic power component remains the same while static power

Table 2. Total power saving for M_{ox}CMOS with L = 0.25 μm, where α is the switching activity, t_{ox2} is high oxide thickness, and ΔP is the power savings between the single- and dual-oxide-thickness designs.

			Static power			Dynamic power			Total power		
Circuit no.	α	Optimal t_{ox2} (nm)	Single oxide thickness (μW)	Dual oxide thickness (μW)	ΔP (%)	Single oxide thickness (μW)	Dual oxide thickness (μW)	ΔP (%)	Single oxide thickness (μW)	Dual oxide thickness (μW)	ΔP (%)
C432	0.03	6.0	269.5	158.7	41.1	103.7	101.2	2.4	373.2	260.0	30.3
	0.30	6.0	268.4	157.4	41.3	652.8	637.6	2.3	921.2	795.1	13.7
C499	0.03	6.0	643.5	362.0	43.8	1,189.4	1,174.0	1.3	1,832.9	1,536.0	16.2
	0.30	7.5	643.5	362.0	43.8	4,420.9	4,318.0	2.3	5,064.4	4,679.9	7.6
C880	0.03	8.0	478.8	94.7	80.2	348.5	303.8	12.8	827.3	398.5	51.8
	0.30	8.0	477.4	93.2	80.4	2,114.6	1,849.6	12.5	2,592.1	1,942.8	25.0
C1355	0.03	7.0	655.8	393.0	40.1	1,034.4	1,022.8	1.1	1,690.2	1,415.8	16.2
	0.30	7.5	655.7	392.9	40.1	3,556.0	3,459.9	2.7	4,211.7	3,852.9	8.5
C1908	0.03	6.5	792.1	253.6	68.0	816.2	763.9	6.4	1,608.3	1,017.6	36.7
	0.30	7.0	792.0	253.6	68.0	3,235.2	3,032.8	6.3	4,027.3	3,286.4	18.4
C2670	0.03	8.0	1,126.2	299.6	73.4	555.7	502.4	9.6	1,681.9	802.0	52.3
	0.30	8.0	1,126.2	299.8	73.4	3,410.1	3,080.4	9.7	4,536.2	3,380.2	25.5
C3540	0.03	6.5	1,559.4	394.4	74.7	805.6	741.7	7.9	2,365.1	1,136.0	52.0
	0.30	7.0	1,559.4	394.0	74.7	4,455.5	4,089.2	8.2	6,014.9	4,483.3	25.5
C5315	0.03	7.5	2,420.3	573.4	76.3	1,733.6	1,573.3	9.2	4,153.9	2,146.7	48.3
	0.30	8.0	2,420.4	573.5	76.3	10,287.5	9,277.7	9.8	12,707.9	9,851.2	22.5
C6288	0.03	6.0	3,245.8	2,147.1	33.9	1,512.7	1,477.4	2.3	4,758.5	3,624.5	23.8
	0.30	6.0	3,245.1	2,146.9	33.9	5,103.2	4,987.9	2.3	8,349.3	7,134.9	14.5
C7552	0.03	6.5	3,635.1	939.1	74.2	1,943.9	1,781.7	8.3	5,579.0	2,720.8	51.2
	0.30	8.0	3,634.8	938.9	74.2	11,677.5	10,674.5	8.6	15,312.3	11,613.4	24.2

Table 3. Comparison of the three power optimization techniques.

Technique	Static power	Dynamic power	Process complexity
M_DM_BCMOS	Decreases	Stays the same	Medium
M_LCMOS	Decreases	Increases	Low
M_{ox}CMOS	Decreases	Decreases	High

decreases, yielding a net decrease in total power consumption. For M_LCMOS, increasing the length increases the threshold voltage, because of V_{th} roll-off, but the gate capacitance also increases. As a result, dynamic power consumption increases. For low-activity circuits, the increase in dynamic power is smaller than the leakage savings, and hence, total power consumption decreases. M_{ox}CMOS, on the other hand, raises the threshold voltage by increasing the oxide thickness yet keeping the device aspect ratio reasonable, yielding a net reduction in capacitance and dynamic power consumption. Thus, it appears that M_{ox}CMOS is the most effective technique, especially for high-activity circuits, because both static and dynamic power consumption decreases. Moreover, this technique helps suppress gate tunneling leakage for future process technology. However, more complex and advanced technology is necessary for multiple t_{ox}.

OPTIMIZING POWER without any delay penalty makes these techniques very promising for scaled technologies. Future work could focus on the multiple-oxide-thickness technique, from both the process and design sides, to further reduce power consumption as designs move further into the deep-submicron region. ■

Acknowledgments

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