Fixed-Load Energy Recovery Memory for Low Power

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Abstract

This paper proposes an energy recovery SRAM that achieves significant dynamic power savings by recovering energy stored in large bit line capacitors. Memory load to power-clock during write is kept fixed by precharging non-selectively after each write cycle. Load during read is also kept fixed by not driving the bit lines with power-clock for read. A simple power-clock generator control scheme that exploits the fixed-load characteristics of the energy recovery memory is introduced to achieve substantially reduced total system power dissipation. The power-clock control scheme reduces system dissipation by preventing the replenishing operation of the power-clock generator while not writing and thus does not require energy transfer between the memory and the power-clock.

Hspice simulations of a full custom 128x256 energy recovery SRAM core show over 4.77x more efficient write operations in comparison with its conventional counterpart at 2.5V, 250MHz. Simulations with a power-clock generator show that disabling power-clock replenishing, whenever memory does not write, achieves savings over 1.47x on total system power over that of a system without the power-clock control.

1. Introduction

Managing power dissipation has become a major goal in designing modern processors for both desktop and mobile applications. Power dissipation of large on-chip static memories, widely used due to their high speed and density, can be quite large [3, 9]. Energy recovery memories achieved reduced memory power dissipation by recovering energy stored in memory capacitors using a special time-varying power source called, the power-clock `PC`, that is generated by a power-clock generator. Multi-phase power-clock energy recovery memories accomplished significant power savings at a cost of design complexity and increased operation latency [1, 4, 5, 6, 7, 8]. An energy-recovery SRAM with a single-phase power-clock was presented in [2]. That memory achieved considerable energy efficiency with reduced power-clock routing complexity. An energy recovery driver with synchronizing circuitry was implemented to support single cycle operations while recovering charges from both word and bit line capacitors.

In this paper, we propose an energy recovery static memory that is an enhancement of the single-phase power-clock SRAM [2] which had tight timing constraints due to the fact that both word line and bit lines are driven by power-clock while providing single-cycle operations. To relax the timing constraints, our memory recovers energy from the bit line capacitors only which dominate total memory dissipation. A novel energy recovery driver, owing its simplicity to the relaxed timing constraints, maintains substantial power savings by recovering energy from the bit lines efficiently.

For a resonant energy recovery system, it is important to keep cycle-to-cycle load variance to minimum to prevent large perturbation on the power-clock. The load for write of our energy recovery memory is kept fixed regardless of data pattern by precharging non-selectively after each write cycle. The load for read is also kept fixed by disconnecting the memory from the power-clock and precharging conventionally with small read precharge transistors.

A typical power-clock generator continuously monitors the power-clock and replenishes it as the voltage falls below some level to maintain the correct operation of the circuits driven by the power-clock. This replenishing involves large power-clock driver and is very dissipative. We propose a simple power-clock control scheme `PCC` which exploit the fixed-load characteristic of our memory to reduce total system power. By disabling the replenishing operation of the power-clock generator when memory is not writing large power savings can be achieved while maintaining the correct memory operations.

Hspice simulations of a 128x256 SRAM in 0.25μm TSMC process show that our energy recovery mem-

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ory achieves 4.77x more energy efficient write operations, in comparison with a conventional counterpart at 2.5V, 250MHz. Simulations with an operation set of 50% read and write show 2.42x savings over conventional memory. PCC, which enables the replenishing of the power-clock only during write, achieves over 1.47x savings in total system power over that of a system with same configuration except the PCC.

The remainder of this paper has five sections. Section 2 describes our novel energy recovery driver. Fixed-load characteristics of our memory and power-clock control is described in Section 3 and the architecture and operations of our energy recovery SRAM are explained in Section 4. Hspice simulation results are presented in Section 5 and Section 6 concludes with a summary of our contribution.

2. Energy Recovery Driver

This section describes the structure and operation of our energy recovery driver. The efficiency of an energy recovery driver depends on the potential difference the moving charges experience during the current flow. Hence, the driver becomes more efficient as the driver output tracks the gradually swinging power-clock more closely. Figure 1 (a) shows the schematics and output waveforms of our proposed energy recovery driver. Dotted lines denote power-clocks and solid lines denote driver outputs. This driver comprises a pair of load driving pass transistors (MP1 and MN1), two evaluation transistors (MP2 and MN2), two pairs of driver activation blocks controlled by feedback from the driver output (MP3,MN4 and MN3,MP4), and a pair of inverters (inv1 and inv2) driving the pass transistors.

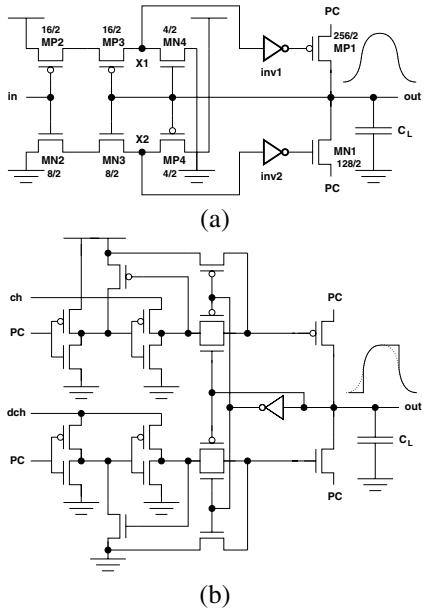

Figure 1. Schematics of energy recovery drivers and corresponding output waveforms. (a) Our energy recovery driver and (b) energy recovery driver from [2].

The activation blocks serve the most important role of allowing the driver output to track the power-clock while preventing unnecessary switching. Since energy-recovery drivers are powered by oscillating power-clocks, the output of the driver also oscillates even when the driver input remains unchanged. Hence, this mechanism to prevent the idle switching increases driver efficiency.

The driver charge path has two modes of operation depending on the level of the driver output. If out is low and PC increases above Vth, MP1 is turned on to charge the driver output. Since MN4 is turned off and MP3 is turned on, assuming in is low, a pull-up path is formed from Vdd to X1. Hence, through inv1, MP1 is turned on to charge the load in an energy recovery manner. As PC and out reaches full rail, MP3 is turned off and MN4 is turned on pulling down X1 to Gnd, hence turning MP1 off. If out is at high level, MP1 remains turned off regardless of in to prevent unnecessary swing of driver output. Since MP3 is turned off and MN4 is turned on, X1 is clamped down causing MP1 to remain turned off.

The driver discharge path is a dual of the driver charge path and has two modes of operation depending on the level of the driver output. If out is high PC decreases below high-Vth, MN1 is turned on to discharge the driver output until PC and out reaches lowest peak value, assuming in is high. If out is low, MN1 remains turned off regardless of in, preventing unnecessary dissipation.

Overdriving MP1 and MN1 with additional voltage levels supplied to inv1 and inv2 achieves more efficient switching by providing full gradual swing as both MP1 and MN1 are turned on at each peak of the power-clock waveform.

	no. of trs	area	cont. delay
our e.r.driver	12 ea	43x717 λ^2	0.13ns
e.r.driver from [2]	20 ea	54x889 λ^2	0.34ns

Table 1. Comparison of implementation overhead of energy recovery drivers.

Figure 1 (b) shows the schematic of energy recovery driver from [2]. It has complex synchronizing circuitry to meet timing constraint, resulting large overhead and less tolerance to power-clock variance. In comparison with this driver, our proposed driver has lower overheads as shown in

Table 1. Delays through the control circuitry in the drivers are also shown for comparison.

3. Fixed-load and Power-Clock Control

This section describes fixed-load characteristics of our energy recovery memory and a simple power-clock control scheme to reduce power-clock generator dissipation by exploiting the fixed-load characteristics.

$$\omega^2 = 2\pi f^2 = \frac{1}{LC_o} \quad (1)$$

$$E_C = \frac{1}{2} C_o {V_{PC}}^2 \quad (2)$$

Equations 1 and 2 describe an energy recovery memory system in resonance. Here ω and f are angular frequency and system operation frequency, respectively. Co is memory capacitor and L is power-clock generator inductor. E_C is the energy stored in the memory and V_{PC} is the peak voltage of power-clock. Assuming the energy stored in the LC tank is conserved, it is evident that the variation in the memory load causes variation in both frequency and amplitude of the power-clock.

Perturbation on the power-clock waveform not only affects the memory operation but also increase total system power by forcing the power-clock generator to correct the perturbation. One approach to relieve the effect of the memory load variance on the power-clock is to add a large stabilizing capacitor C_s to the LC network such that the load variance in the memory does not affect total load of the power-clock substantially. Following Equations 1 and 2, frequency and voltage variance due to load variance can be calculated as below.

$$\omega_2 = \omega_1 \sqrt{\frac{(C_{o,1} + C_s)}{(C_{o,2} + C_s)}} \quad (3)$$

$$V_{PC,2} = V_{PC,1} \sqrt{\frac{(C_{o,1} + C_s)}{(C_{o,2} + C_s)}} \quad (4)$$

From Equation 3 and 4, the stabilizing capacitor for a given energy recovery memory can be chosen to meet target frequency and voltage variance. However, one fact to note here is that the Q factor for LC network decreases with the square root of the capacitance increase thus limiting the maximum size of the C_s.

To prevent load variance during write, write load of our energy recovery memory is kept fixed regardless of data pattern by precharging bit line pairs non-selectively after each write cycle. Load during read is also kept fixed by precharging the bit line pair after read conventionally without interacting with power-clock. The fixed-load characteristic of our energy recovery memory results reduced power-clock perturbation and thus reduced power-clock generator dissipation by reducing the needs for power-clock replenishing.

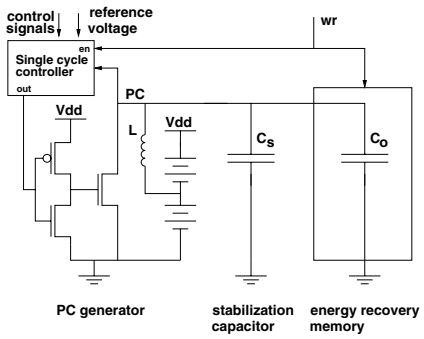

Figure 2. Configuration for PCC.

Fixed-load characteristics of our memory can be exploited further to reduce total system power dissipation. Since our memory does not interact with power-clock while not writing, the replenishing of the power-clock can be halted without affecting correct operation of the memory. The energy will oscillate between the stabilization capacitor and the inductor in the power-clock generator until next memory write operation comes. Figure 2 shows application of this power-clock control scheme PCC to an energy recovery memory system, consisting of an energy recovery memory and a resonant power-clock generator from [10]. This load aware power-clock control reduces total system power significantly as will be shown in Section 5.

4. Architecture and Operation

This section describes the architecture, operation modes for fixed-load of our energy recovery SRAM.

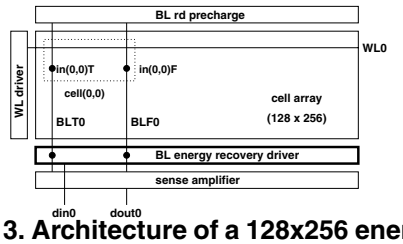

Figure 3. Architecture of a 128x256 energy recovery SRAM.

As can be seen in Figure 3, our energy recovery SRAM, which uses conventional 6T SRAM cells, has a similar architecture to that of a conventional SRAM. Except for the bit line energy recovery drivers, every component of our memory is the same as its conventional counterpart. This modification ensures efficient energy recovery from the bit lines which dissipate a majority of total memory

power with minimal overhead. Driving less dissipative word lines with conventional drivers enables relaxed timing constraints, providing simpler and efficient bit line driver design.

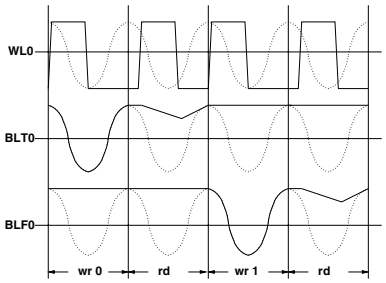

Figure 4. Waveforms of bit/word lines for write0, read, write1, and read operations.

Figure 4 shows the timing relationship of memory modules achieving single-cycle latency memory operations. Write operations occur in a manner similar to that of conventional SRAMs. First, the bit line `BLT0` storing "0" is pulled down by the bit line energy recovery driver. Then, word line `WL0` is asserted by conventional word line driver to store data into the cells. After data storage, the pulled down bit line is precharged back to high level by the bit line energy recovery driver.

Read operation is same as that of a conventional SRAM. After equalization of the bit line pair, the word line `WL0` is asserted resulting voltage difference on the bit line pairs. Then the sense amplifier is enabled and data is read out. The bit lines pulled down by the cells are precharged back conventionally by small read precharge transistors. Applying energy recovery to precharge after read is not effective in reducing energy, since the dissipation from the additional circuitry can outweigh the energy savings from precharging the small voltage in an energy recovery manner.

5. Simulation Results

We have designed a full custom energy recovery 128x256 SRAM using MOSIS design rules for the 0.25μm TSMC process. For comparison, we designed a conventional SRAM with the same components, except for the bit line drivers. Power dissipation of our memory is compared with that of its conventional counterpart and the effect of introducing the `PCC` is studied.

5.1. Simulation with Ideal Power-Clock

This section describes result of Hspice simulations on our energy recovery memory with an ideal power-clock of 100% efficiency. Power dissipation of our memory is compared with that of its conventional counterpart.

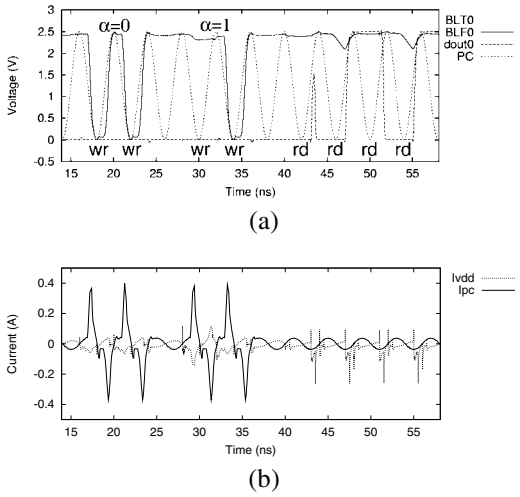

Figure 5. Hspice simulation of energy recovery SRAM. (a) Waveforms of bit line pair, data out and power-clock. (b) Waveforms of Vdd current and power-clock current.

Figure 5 (a) shows the waveforms of our energy recovery memory performing 4 cycles of write and 4 cycles of read operations at 2.5V, 250MHz with ideal power-clock. To assess the effect of data switching during write operations, 2 writes of same data and 2 writes of exact opposite data are performed. As can be seen, our energy recovery memory functions correctly under simulation conditions. Figure 5 (b) shows waveforms of currents from both Vdd and power-clock nodes. It shows that same amount of current flows back to the power-clock, during write, independent of the data switching factor. It also shows that memory does not draw power from the power-clock during read.

Operation of the conventional SRAM is shown in Figure 6 (a), performing same operation as that of our energy recovery memory. The effect of conventional driving on power is evident in Figure 6 (b) showing the Vdd current waveform. It shows that a large amount of current is drawn out during write to pull up bit lines to full Vdd without any recovery. Smaller current flows during read to precharge the bit line that was pulled down slightly below Vdd by the read out cells.

Table 2 compares the power dissipation of our energy recovery memory with that of its conventional counterparts. As can be seen, our memory is much efficient during write, achieving 4.77x savings over its counterpart, while dissipating same amount for same conventional read operations. For an operation set of 50% write and read our energy recovery memory achieves over 2.42x power savings over conventional memory.

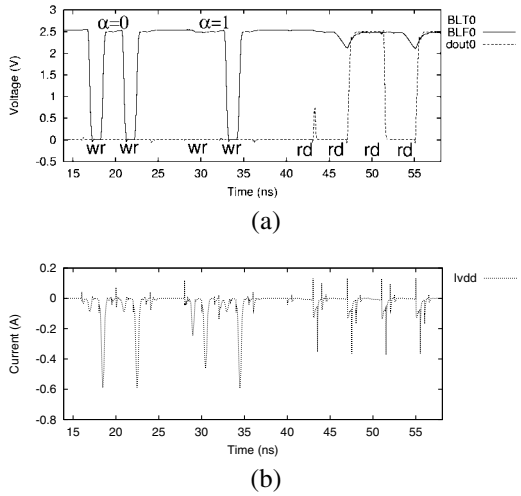

Figure 6. Hspice simulation of conventional SRAM (a) Waveforms of bit line pair, data, out and power-clock. (b) Waveforms of Vdd current.

	write		read
	$\alpha = 0$	$\alpha = 1$	
conv. SRAM	0.73 nJ/cyc	0.75 nJ/cyc	0.24 nJ/cyc
e.r. SRAM	0.14 nJ/cyc	0.17 nJ/cyc	0.25 nJ/cyc

Table 2. Comparison of energy dissipation of conventional and energy recovery SRAM (energy per cycle at 2.5V, 250MHz).

5.2. Simulation with Power-Clock Generator

This section describes the results of Hspice simulations on our energy recovery memory with a power-clock generator from [10]. The effect of the power-clock control exploiting the fixed-load characteristics is compared with the one without the scheme. Memory loads for write and read of memory is calculated from Hspice simulations and were 109.12pF and 55.10pF respectively. Values for the required stabilization capacitors and power-clock inductor were first calculated using Equation 3 and 4 with target maximum power-clock variance of 15%. Then their values were tuned for least power-clock variation under the influence of the replenish operation of the power-clock generator. The chosen C_S and L for simulations are listed in Table 3.

Figure 7 (a) shows the waveforms of our energy recovery memory with a power-clock generator without PCC. This power-clock generator is enabled periodically to replenish

without PCC		with PCC	
C_S	L	C_S	L
1.28nH	225pF	1.28nH	220pF

Table 3. Stabilization capacitor and power-clock inductor

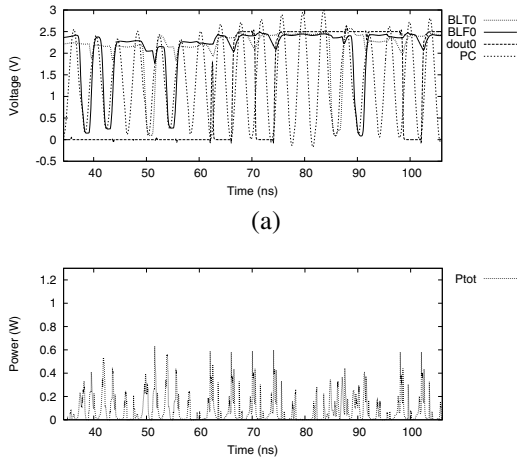

Figure 7. Hspice simulation of our energy recovery SRAM with power-clock generator. (a) Waveforms of bit line pair, data out and power-clock. (b) Total system power (memory + PC generator).

dissipated energy on the power-clock tree. The memory operation pattern is 2 cycles of writing same data ($\alpha = 0$), 2 cycles of writing opposite data ($\alpha = 1$), 4 cycles of read, 2 cycles of writing opposite data ($\alpha = 1$) followed by 2 cycles of read.

Figure 7 (b) shows dissipation of total system, including the memory and the power-clock generator. It can be seen that the system dissipates more during read operations due to the power-clock replenishing countering the variance in the load.

Figure 8 (a) shows the waveform of our energy recovery memory with a power-clock generator under PCC, performing same set of operations as the one without PCC in the previous paragraph. For this experiment, replenishing the power-clock was enabled only during the write cycles.

Figure 8 (b) shows dissipation of total system, including the memory and the power-clock generator. It can be seen that the system dissipates less during read operation due to the PCC.

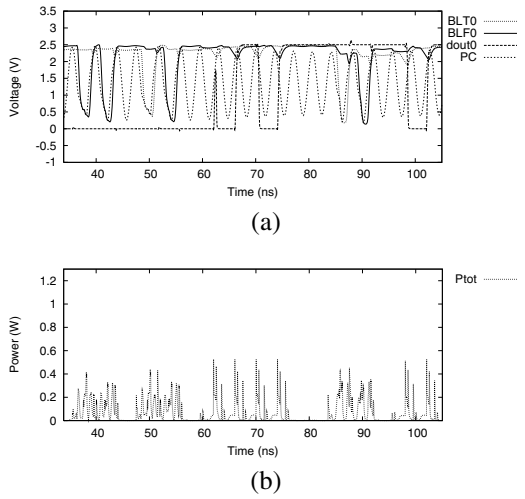

Figure 8. Hspice simulation of our energy recovery SRAM with power-clock generator with PCC (a) Waveforms of bit line pair, data out and power-clock. (b) Total system power (memory + PC generator).

	total system dissipation
conv. SRAM only	6.57 nJ
e.r.SRAM only (+ ideal PC)	3.30 nJ
e.r.SRAM + PC gen.	6.00 nJ
e.r.SRAM + PC gen. w/ PCC	4.08 nJ

Table 4. Comparison of total energy dissipation of various memory configurations (energy dissipation.

Table 4 compares the effect of PCC on total power dissipation of an energy recovery system, including an energy recovery memory and a power-clock generator over 12 cycles of operation, including 2 cycles of writing same data ($\alpha = 0$), 4 cycles of writing opposite data ($\alpha = 1$), and 6 cycles of read, at 2.5V, 250MHz. As can be seen, exploiting the fixed-load variance of our energy recovery memory achieves 1.47x savings on total system power to that of without any power-clock generator control schemes. Furthermore, the energy recovery system with controlled power-clock generator shows to be 1.61x more efficient than conventional memory even without the contribution from its own conventional clock generator.

6. Conclusion

This paper describes a single-cycle energy recovery SRAM with a single-phase power-clock that achieves substantially lower power dissipation than conventional SRAM. A novel energy recovery driver reduces memory dissipation by recovering energy from the bit lines efficiently. Memory load for write and read operations are kept fixed to minimize the perturbation on power-clock and thus the power-clock generator dissipation. Simple power-clock control scheme exploiting the fixed-load characteristic of our energy recovery memory achieves reduced total system power.

Simulations of 128x256 SRAMs show that our energy recovery memory achieves 4.77x more efficient write operations. Memory operation based power-clock control enabled over 1.47x savings in total power dissipation of system, including an energy recovery memory and a power-clock generator over same system without any power-clock control schemes.

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