A VERY LOW-POWER FLASH A/D CONVERTER BASED ON CMOS INVERTER CIRCUIT

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Abstract

A/D converter (ADC) is a basic device in digital signal processing systems. For high-speed applications, a flash ADC type is often used. Due to require many analog comparators, the chip complexity and power dissipation become very high. Moreover, the accuracy of dividing resistors requires very high for reference voltage if the converting resolution is high. In this study, we develop a new kind of flash ADC based on a simple CMOS circuit. By adjusting the ratio of channel length and width, the transition threshold of the CMOS inverters is various to detect input analog signal. Then their results are encoded to the digital code. The advantages are that the ADC circuit does not need any resistor and use simple CMOS inverters rather than analog comparators. The new 8-bit ADC chip only used 634 transistors. The power dissipates 0.9mW using 0.35um process when it operates at 100MHz.

KEYWORDS: A/D converter, CMOS inverter, flash

1. INTRODUCTION

Recently, the digital multimedia applications become more and more popular due to its functionality rich. However, all human interactive signals, such as video, music, are analog signals. For digital signal processing, an A/D converter is a basic component for digitizing the analog signal. Basically, an A/D converter chip has partial analog circuit and partial digital circuit [1-4]. Since this kind of chip belongs to a mixing-mode type, the design and implementation need to be very carefully. The main problem is that the analog circuit is easily interfered by the digital circuit. The converting resolution would be greatly degraded as the digital noise is induced to the analog circuit.

In the past 50 years, there were many methods presented to realize the chip of A/D converter. The design methodology is split with the charge capacitor, successive approximate, and flash type. In generate, the circuit complexity and the converting speed must be tradeoffs for practical application. As for a very low speed device, such as digital voltage meter, the simple charge capacitor is enough to satisfy the speed requirement with low circuit complexity. In the successive approximate A/D converter, the converting speed is inverse proportion of the resolution. The typical application is for the audio system. As for high-speed applications, such as video and communication systems, only the flash ADC can meet the converting speed. However, the circuit complexity is very high since there require many analog comparators. Hence the power consumption would become very high. Actually, for portable systems, the low-power consumption keeps as low as possible.In this paper, we aim to design a flash A/D converter with low-power consumption to apply on video systems. In input voltage detection, a low-power CMOS inverter is designed rather than the analog comparator. The results show that the circuit size can be efficiently reduced and the power dissipation also can be saved.

2. DESIGN FOR FLASH A/D CONVERTER

In the typical flash A/D converter, we require $(2^N - 1)$ comparators if the resolution is N bits. Since each comparator used different reference levels (v1,v2,…), we need to use resistors to divide the reference voltage. Thus the number of resistors requires 2^N.I n general, the architecture has some drawbacks, as described following. The converting accuracy is limited at the section resister. Since the resister is always implemented with semi-conductor materials, we hardly achieve high accuracy resistor value in a chip due to process deviation. Moreover, the resister value is proportion to the line length, thus the resistor is always designed at low value to keep small chip size. Obviously, the reference voltage must supply enough power driving to reduce the loading affection since the input current is high in low value resistors. Moreover, the analog comparators must be designed with high gain in order to detect the input voltage in small change and increase the noise margin. Hence the circuit complexity becomes high. The input signal is connected to the input of all comparators in parallel. The input signal requires large driver since the input capacitor is equal to the summation of the input capacitor of all comparators. In practical applications in a system, the shortcoming of the conventional flash A/D converter is to require large input signal driving, high reference accuracy and high driving reference voltage. This will cause the power dissipation highly.

In this study, we have a novel ideal that employs CMOS inverters rather than analog comparators. First we draw the characteristics of CMOS inverter. The basic CMOS is combined with one P-MOS and one N-MOS [1]. If the input voltage arrives one threshold, the output state is changed. The threshold is dependent on the βp and βn, which can be given by

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$$Vin_{threshold} = \frac{VDD + Vtp + Vtn(\beta n/\beta p)^{1/2}}{1 + (\beta n/\beta p)^{1/2}} \quad (1)$$

$$\beta n = k1 \times \frac{Wn}{Ln}; \quad \beta p = k2 \times \frac{Wp}{Lp} \quad (2)$$

where, k1 and k2 is constant, Vtp and Vtn is the threshold value of PMOS and NMOS, respectively. The βp and βn values can decide the center transfer point at the CMOS inverter. If the ratio of βp and βn is decreased, the transited threshold becomes low. Otherwise, the transited threshold becomes high if the ratio of βp and βn is increased. The βp and βn can be controlled with adjusting the length (L) and width (W) of P-MOS and N-MOS respectively. Based on this concept, we design various length/width ratios of CMOS inverters to change their thresholds. Each CMOS inverter has its specified threshold. Then all input of CMOS inverter is tried together to detect the analog input level. The basic architecture of the proposed flash A/D converter is shown in Fig. 2. We define Zu=Ln/Wn and Zp=Lp/Wp. Change the ratio of Zu and Zp, we can obtain various transited voltage of CMOS inverter to quantize the input level.

In this paper, we aim to design an 8-bit ADC chip for applying in high-speed video systems. First, 4-bit ADC is designed based on the CMOS inverter. Thus 16 CMOS inverters are tried in parallel to detect the input signal level. By changing the ratio of Zu and Zp for each inverter, we can achieve the expected transited voltage with (1). The inverter output is array from MSB to LSB. For MSB bit, the Zu/Zp value should become large to increase the transited threshold. Alternatively, for LSB bit, the transited threshold is very low, thus we need to decrease the Zu/Zp value. The detailed design for each CMOS inverter is described in the later section. Only the input voltage arrives the specified voltage, the output becomes low. For the later digital encoding circuit designed compatible to the conventional flash ADC chip, each output of detected inverter is added to an inverter. Thus the output will be high as the input analog level arrives the transited point of inverter. The function of inverter is like to the comparator of a conventional flash ADC chip. With this approach, we do not require the analog components, such resistors and analog comparators. The circuit complexity shall be greatly reduced. Since the CMOS inverter only dissipates the power during the state transition, the power consumption becomes very low. Since the input signal is detected with the various width/length ratio of CMOS inverter, the reference voltage and splitting resistors all can be saved. In additional, the input signal does not need high driving current because the inverter has very high input impedance.

From the previous mention, one can achieve 15 bits to present the detected result for analog input signal. In order to reduce the I/O pins, we must encode the 15-bit to 4-bit binary code. If the inverter array outputs A14~A0, we encode to 4-bit with B3~B0, as shown in Table-1, where A14 and B3 is MSB. The encoder can be implemented with XOR circuit. We find that B3 is equal to A7, and B2 can be obtained with XOR of A3, A7 and A11. Further, we find B2 is the sub-term of B1, and B1 is also the sub-term of B0. The logic function can be given by

B3=A7,

B2=A3⊕A7⊕A11,

B1=A1⊕A3⊕A5⊕A7⊕A9⊕A11⊕A13=B2⊕A1⊕A5⊕A9⊕A13,

B0=A0⊕A1⊕A2⊕A3⊕A4⊕A5⊕A6⊕A7⊕A8⊕A9⊕A10⊕A11⊕A12⊕A13⊕A14=B1⊕A0⊕A2⊕A4⊕A6⊕A8⊕A10⊕A12⊕A14. (3)

First, we implement B2 with two XOR gates. Then B1 is realized with the result of B2 and four XOR gates. In the same way, B0 is achieved with B1 output and eight XOR gates. Thus the encoder is designed with 16 XOR gates.

To design the 8-bit ADC chip, the proposed 4-bit ADC is doubly used with the same core. The architecture is shown in Fig. 2, which combines two 4-bit ADC, one 4-bit DAC and one differential amplifier. In the coarse 4-bit, we can achieve from the first-step 4-bit ADC core to present MSB bits. To obtain the fine LSB bit, the residual voltage from the differential of the input level and the result of first step is as the input of the second step 4-bit ADC. To use the same 4-bit ADC module, the residual voltage is amplified by 16 times with the differential amplifier. The second 4-bit ADC input voltage is

$$Vin2 = 16 \times (Vin - Vo_{(MSB)}). \quad (4)$$

Vo(MSB) is the first step 4-bit output after DAC converting to analog voltage. We design the differential amplifier uses OPA (operation amplifier) module. To keep enough bandwidth, the amplifier uses two stages cascade, where the gain of each stage is 4.

3. CHIP REALIZATION

To realize the ADC chip, we used the TSMC 0.35um process. First, the 4-bit ADC is implemented based on the Fig. 2 architecture. The 4-bit ADC is easily realized since all circuit are digital. This process is suggested with 3.3V as MOS supply voltage. The detectable range for input voltage is 0.4~2.4 in our design. The 16 transited points of each inverter and its Zu/Zp are listed at the Table-1. The detected step for input signal is about 0.14V by the change the ration of Zu/Zp of each inverter in experiments. The transited curve for 15 inverters is illustrated in Fig.3. The results of inverter are sent to the digital encoder with (3). Then we can achieve the expected output code in the specified input voltage. Table 2 shows the relationship of input analog voltage and the output code. The 4-bit ADC core is simulated by Hspice, the results are shown in Fig. 5. The input signal uses a ramp waveform, and we can obtain the binary counter code in the output. The results meet our expectation. According to the circuit, the layout for 4-bit ADC core is drawn. After DRC, LVS and ERC checking, the 4-bit core had prototyped with CIC (chip implementation center, Taiwan) education process. The sample had been tested in success. The maximum frequency for 4-bit ADC core can achieve about 150MHz.

Based on the 4-bit ADC core, the 2-step architecture is implemented for 8-bit ADC chip. We further implement one two stages OPA and one 4-bit DAC circuit. The 8-bit ADC chip had been designed by consisting of two 4-bit

ADC core, one OPA and one 4-bit DAC. The simulation for the function 8-bit ADC also can meet our expectation. The layout is shown in Fig. 5. To keep high flexible design in the prototype, the input and output pins of each core are independently connected to the chip I/O. We can check each module function and so this chip sample can be easily tested. If the four modular are successfully tested, we can connect the I/O pin in off-chip to obtain an 8-bit ADC chip. Table 3 lists the chip features of the proposed 8-bit ADC chip. Since we use inverters rather than the comparators and split resistors, the power dissipates very low. The total power consumption is only 0.9 mW when operating 100MHz. The circuit only uses 634 gates and the chip core size is very small.

Next, we compare the other ADC chips with various parameters. The results are listed in table 4. Most of flash ADCs use analog comparator to detect the input signal level. With the resistor to divide the voltage, each comparator has different reference voltage. In our ADC chip, we use CMOS inverters rather than comparators. The advantage is that the circuit size can be greatly reduced and the speed can be promoted. The CMOS inverter has high input impendence and low power consumption. Hence our ADC chip requires low input driving current and dissipates small power. The ADC chip is designed for video systems, and so the conversion speed with 100MHz is enough for all video systems, included HDTV (high-definition TV), although our speed is lower than that of the completing ones. The critical path in our chip is to compute the B0 in (3) and bandwidth of the differential amplifier. If for higher speed system applied, we can add the pipelined stage to reduce XOR operation time and increase the product of gain and bandwidth for the amplifier. Since each ADC chip design in different resolution, conversion speed, process and supply voltage, comparing the power dissipation parameter is unfair. To normalize the power dissipation, we define the normalized power factor (NPF) as

$$NPF = \frac{Chip\ Power\ Dissipation}{\mathrm{Re}\,solution \times speed \times process \times volatge} \times 1000$$

The reason for NPF is that as the resolution is higher, the chip power dissipation becomes high too. The MOS power consumption is almost linearly increased corresponding to the speed and voltage. Moreover, when the process scale is down, the power dissipation will be reduced too. From the NPF results, our chip indeed has lower power consumption than others.

4. CONCLUSIONS

This paper proposed a novel flash ADC architecture based on the CMOS inverter. First, we design 4-bit ADC core and then expanded to 8-bit with two-step architecture. The 4-ADC core actually is full digital circuit, and so it is easily implemented. The great advantages are that the input capacitor can be been reduced and input impedance becomes very high. Hence the input signal driver power can be reduced and the converting speed can be promoted. Moreover, the reference voltage and resister can be saved. The 8-bit ADC is designed with 2-step structure based on 4-bit ADC core. Comparison with other ADC core, this chip can achieve very low power dissipation and use small silicon area. With low power dissipation, small circuit core and high speed, the proposed 8-bit ADC chip can be applied on low-cost video systems.

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TABLE 1 The transited point of 15 inverters

Inverter	Zp/Zn	Vinv（V）
TR0	1100	0.5
TR1	55.55	0.64
TR2	9.25	0.78
TR3	4.09	0.92
TR4	1.74	1.06
TR5	1.15	1.2
TR6	0.6	1.34
TR7	0.308	1.48
TR8	0.2	1.62
TR9	0.114	1.76
TR10	0.0784	1.9
TR11	0.0516	2.04
TR12	0.0268	2.18
TR13	0.0132	2.32
TR14	0.0042	2.46

TABLE 2 The input and output of 4-bit ADC core

Input Signal（V_i）	Output Encoded Bits			
	B3	B2	B1	B0
$V_i < 0.5V$	0	0	0	0
$0.5V \le V_i < 0.64V$	0	0	0	1
$0.64V \le V_i < 0.78V$	0	0	1	0
$0.78V \le V_i < 0.92V$	0	0	1	1
$0.92V \le V_i < 1.06V$	0	1	0	0
$1.06V \le V_i < 1.2V$	0	1	0	1
$1.2V \le V_i < 1.34V$	0	1	1	0
$1.34V \le V_i < 1.48V$	0	1	1	1
$1.48V \le V_i < 1.62V$	1	0	0	0
$1.62V \le V_i < 1.76V$	1	0	0	1
$1.76V \le V_i < 1.9V$	1	0	1	0
$1.9V \le V_i < 2.04V$	1	0	1	1
$2.04V \le V_i < 2.18V$	1	1	0	0
$2.18V \le V_i < 2.32V$	1	1	0	1
$2.32V \le V_i < 2.46V$	1	1	1	0
$2.46V \le V_i$	1	1	1	1

TABLE 2. Chip Feature of Proposed ADC chip

Output Resolution	8 bit
Process	0.35um
Supply Voltage	3.3V
Input Range	0.4V~2.4V
Accuracy	1 LSB
Core Size	386um * 497um
Max Speed	100MHz
Input Pad/Output Pad	18/10
Transistor/Gate Count	634 MOS
Max Power Dissipation	0.895mW
Package Type	SB28

Table 3. Comparisons with other ADC Chips

	Stojcevski [2]	Hsu [3]	Proposed
Detection Component (Number)	Comparator (6)	Comparator (63)	CMOS Inverter (30)
Input Resistors	16	64	0
Input Driving Current	High	High	Very Low
Reference Voltage	Need	Need	no need
Input Multiplex	4:1 and 2:1	0	0
Resolution (bits)	4	6	8
Supply Voltage	2.5V	2.5V	3.3V
Process	0.25um	0.25um	0.35um
Speed	400MHz	500MHz	100MHz
Power Dissipation	1.68mW	261mW	0.895mW
NPF	1.68	139	0.96

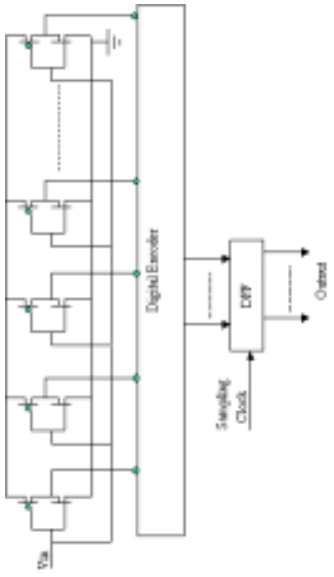

Fig.1 The architecture of proposed ADC chip

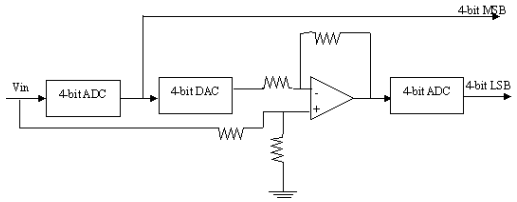

Fig.2 A two-step ADC architecture

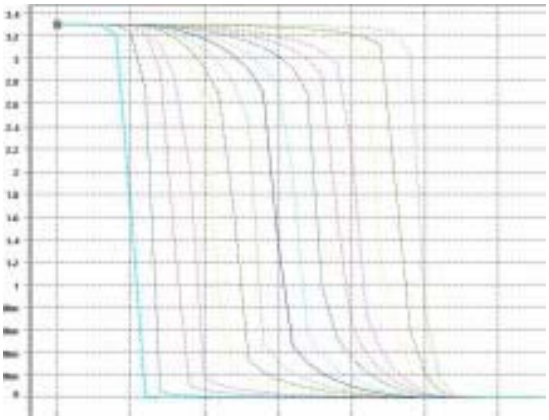

Fig.3 The transfer curve of 15 inverters.

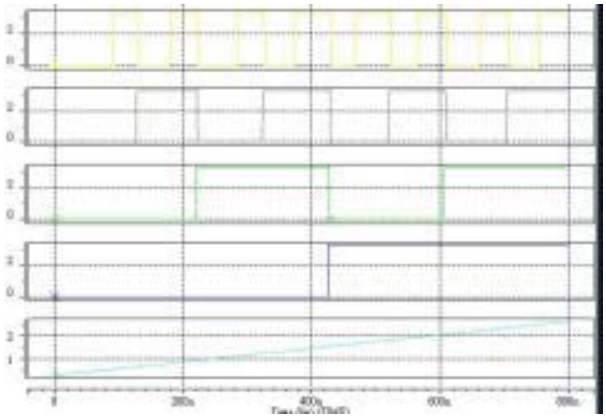

Fig. 4 The simulation result of 4-bit ADC

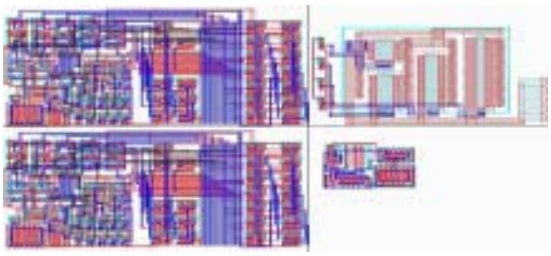

Fig.5 The layout of the proposed ADC chip