Low-power, low-voltage BiCMOS comparators for ~200MHz, 8bit operation

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Abstract

Two novel BiCMOS latched comparators operating at 3.3V with 8bit resolution are presented. They achieve ~200MHz operation and exhibit lower power consumption than the conventional architecture. The first resembles a conventional bipolar latched comparator, with a variable load resistance which changes its value three times during the acquisition cycle. It achieves the highest speed and the lowest power consumption. The second includes a differential amplifier which unbalances a ground-referenced latch by current mirror action. It may be adapted to even lower supply voltages and exhibits negligible kick-back effects.

1 Introduction

In recent years applications such as wireless telecommunications or hard disk drivers have created an increasing demand for Analog to Digital Converters with high speed (above 100MHz), medium resolution (6-8 bit) and low power consumption. The last requirement, together with the trend towards submicron technology, may require operation with a supply voltage below 5V (typically 3.3V).

The well known bipolar latched comparator, shown in fig.1, has been successfully used [1, 2] since the earliest designs of high speed A/D converters operating without Sample and Hold. However, low power consumption cannot be achieved without sacrificing the sampling frequency. Some further important improvements, aiming at raising the sampling frequency [3, 4], are also power hungry and cannot be easily adapted to reduced supply voltages.

This work presents two novel architectures of latched comparators which take advantage of BiCMOS technology, overcoming these limitations. The first one uses a variable active pMOS load instead of the resistors used in the circuit of fig.1. By dynamically controlling the load throughout the conversion period, a true power saving may be achieved without lowering the sampling frequency. The second comparator makes use of current mirroring for unbalancing a ground referenced latching stage; the solution eliminates kick-back effects, making the comparator very suitable for low-voltage application, and reduces power consumption. Both comparators are compatible with 8 bit resolution on a ± 0.5V differential range and achieve a clock frequency of about 200MHz, while operating with a single supply of 3.3V$\pm$10%. In order to reduce the power consumption of the digital part, the comparators are interfaced to CMOS logic. Simulation results are reported and compared with simulations of the conventional architecture.

2 Two novel architectures

The main design constraints for a latched comparator are listed below.

- The *regeneration time*, that is the time needed by the latch to achieve a sufficient voltage separation at the two output nodes, for an assigned initial voltage difference between nodes O1 and O2.
- The *recovery time*, that is the time employed by the differential amplifier for restoring a correct differential output voltage, after the end of the latched state. It can be reduced by increasing the load resistance.
- The *bandwidth*, i.e. the differential amplifier's analog bandwidth which, if it is not sufficiently large, introduces third harmonic distortion in the flash converter. Both bandwidth and recovery time can be improved by lowering load resistance [5].

The basic circuit of fig.1 was improved by cascoding [3] or load resistor splitting [4]. In particular, the latter solution increases the resistance seen by the latch, thus reducing the regeneration time; however neither solution easily operates with a single 3V supply.

In the first proposed circuit, the **variable load latched comparator** of fig.2, pMOS transistors M1 and M2 replace the load resistors. By controlling the voltage V_b at the pMOS gates, the most convenient

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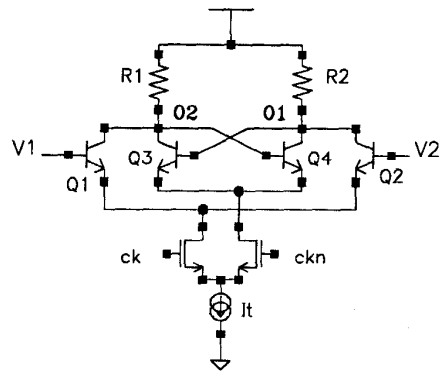

Figure 1: Circuit diagram of the **bipolar latched comparator.**

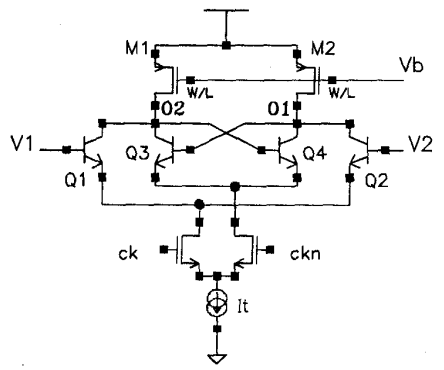

Figure 2: Circuit diagram of the **variable load latched comparator.**

load resistance R_L may be obtained during each phase of the conversion period: a high resistance during regeneration, a low resistance during the tracking phase, in order to achieve fast recovery and high bandwidth.

Let us first consider the regeneration phase. The behavior of the latch at the very beginning of regeneration and for small differential input voltages $v_{IN} = v_1 - v_2$, may be described by eq.1 [6],

$$v_{O2} - v_{O1} = A_V \, V_{IN} \, exp(\frac{t}{\tau_{reg}}) \qquad (1)$$

Here, A_V is the gain of the comparator in tracking mode and τ_{reg} is the regeneration time constant, approximated by $C_T g_m R_L/[g_m(g_m R_L - 1)]$ where g_m is the transconductance of Q3-Q4, R_L is the load resistance and C_T is the effective capacitance seen at the

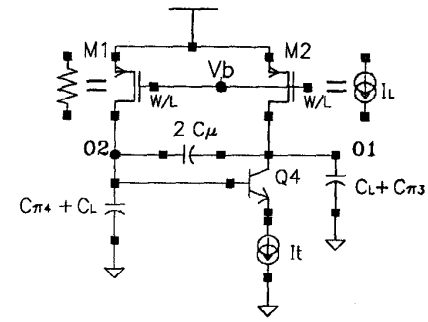

Figure 3: Simplified circuit diagram for transient analysis.

output nodes [6]. By driving transistors M1 and M2 with a small V_{sg}, the term $g_m R_L$ may be made large enough to approach the asymptotic minimum of τ_{reg}, C_T/g_m.

However, this linear theory no longer holds after the time t' when one of the BJTs, for example Q3, turns off and M2 becomes saturated. Fig.3 shows a simplified circuit of this situation. As long as M1 is non-saturated, the voltage at node O2 is nearly constant, some tens of millivolts under Vdd, while at node O1 the voltage changes approximately as:

$$V_{O1}(t) = V_{O1}(t') - \frac{I_T - I_L}{C_L + 2C_\mu + C_{\pi 3}}(t - t') \qquad (2)$$

where C_μ and C_π are the base-collector and base-emitter capacitances of Q3 and Q4 and I_L is the saturation current of M2. V_{O2} remains constant as long as the value I_L is not reduced below a minimum value I_{Lmin}, which may be approximately derived by current balance at node O2 and MOS transistors I-V equation: $I_L > I_{Lmin} \approx 2\, I_T\, C_\mu/(C_L + 4\, C_\mu + C_{\pi 3})$. Eq. 2 shows that the aperture $V_{O2} - V_{O1}$ at the end of regeneration increases as I_L is reduced. On the other hand, if I_L is too small (smaller than I_{Lmin}), M1 enters the saturation region, V_{O2} decreases with V_{O1}, eq. 2 does not hold any more and simulations show no increase in the final aperture $V_{O2} - V_{O1}$ over the value achieved with I_{Lmin}. Considering also that, the lowest the final value of V_{O2}, the longest the recovery, and the convenience of having one of the two output nodes at Vdd for interfacing to the subsequent CMOS logic, there is no interest in reducing I_L below I_{Lmin}; this places an upper bound on V_b.

Let us now consider the signal acquisition phase. At first the comparator has to reset an initial difference of several hundreds of millivolts between nodes

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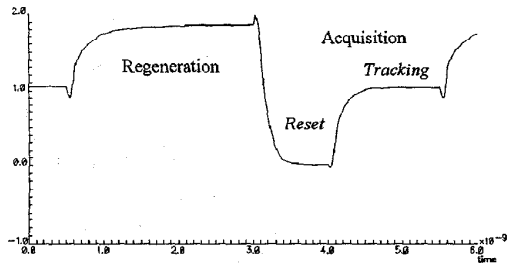

Figure 4: The voltage waveform at the gates of M1-M2.

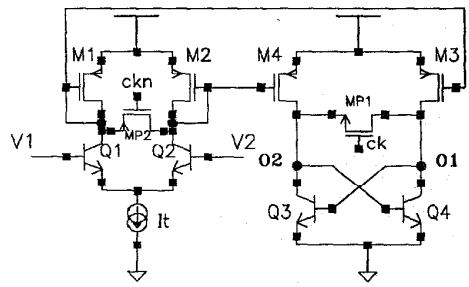

Figure 5: Circuit diagram of the **current mirroring latched comparator.**

O1 and O2 to the final value $A_V V_{IN}$. The recovery time (i.e. the the time needed for the comparator to set $V_{O1} = V_{O2}$ when $V_{IN} = 0$) depends almost linearly upon R_L [6]. In the proposed comparator the acquisition phase is split into a reset phase and a tracking phase. During reset the gates of M1 and M2 are pulled to ground for about 1ns to minimize R_L and thus reduce the recovery time. After that, R_L is set to obtain the desired gain (typically around 2) and bandwidth. By the dynamic reset operation, the same tracking performance may be achieved with a higher R_L and a smaller I_T, thus reducing the power consumption.

In [6] a simple time varying load driven by ckn was proposed. The three level waveform of V_b used here (fig.4) has the advantage of obtaining the most convenient load during each of the three phases: regeneration, reset and tracking. A suitable circuit for generating this waveform, with voltages referenced to the positive supply, was designed using the same technology.

The contribution of the pMOS loads to the comparator's input offset voltage is:

$$V_{os} = V_{th}[\frac{\Delta K}{K} + \frac{\Delta V_{Tp}}{(V_{sg} + V_{Tp})}] \qquad (3)$$

where $K = K'\frac{W}{L}$ and $(V_{sg} + V_{Tp})$ is referred to the tracking phase. Due to the fact that M1 and M2 are nonsaturated during the tracking phase, high immunity to V_{Tp} mismatch in the MOS load was achieved.

The second comparator architecture proposed in this work is the **current mirroring latched comparator**, shown in fig.5. In this circuit the voltage difference at the input is converted into a difference of currents flowing through M1 and M2. By the action of current mirrors M1-M3 and M2-M4, this current difference unbalances the latching stage. For small input voltages, the behavior during the first phase of regeneration is similar to the previous one. Later on however, the output latch regenerates with a higher slew rate than in the **variable load** case. In fact the emitters of Q3-Q4 are connected straight to ground and the discharge of the output capacitance is not limited by the tail generator. After regeneration, the comparator is reset by equalizing the output voltages using the pass transistors MP1 and MP2; MP1 was sized as discussed in [7] to properly reset the latch.

The contribution of the pMOS loads to the offset voltage may be approximated by:

$$V_{os} = V_{th}[2\,\Delta V_{Tp}\sqrt{\frac{K}{I_T}} + \frac{\Delta K}{K}] \qquad (4)$$

where the symbols have the usual meaning. The ΔV_{Tp} contribution to V_{os} decreases with the $\frac{W}{L}$ of M1-2, while the bandwidth of the differential stage increases. Thus, the MOS transistors of the load have to be sized so as to obtain a sufficient immunity to ΔV_{Tp} without sacrificing bandwidth. Power consumption is greater for this comparator than for the first one (fig.2), since both stages are active during the entire conversion period. Nevertheless, this circuit dissipates less power than the conventional scheme of fig.1 and can be adapted to a current mode, folding A/D converter [8]. For such applications the first stage may be removed or shared between many latches.

This architecture allows further reductions of the supply voltage, since no switches are present in series with the tail current generator. Moreover the input transistors are biased during the entire clock period, and this reduces kickback effects without resorting to "high clocking" architectures [5], unsuitable for low voltage operation.

In order to reduce the power consumption of the complete A/D converter, both comparators are directly interfaced to CMOS logic by a MOS follower and a CMOS flip-flop, unlike traditional designs which make use of ECL logic. Since the flip-flop is reset at the beginning of the regeneration phase, it may

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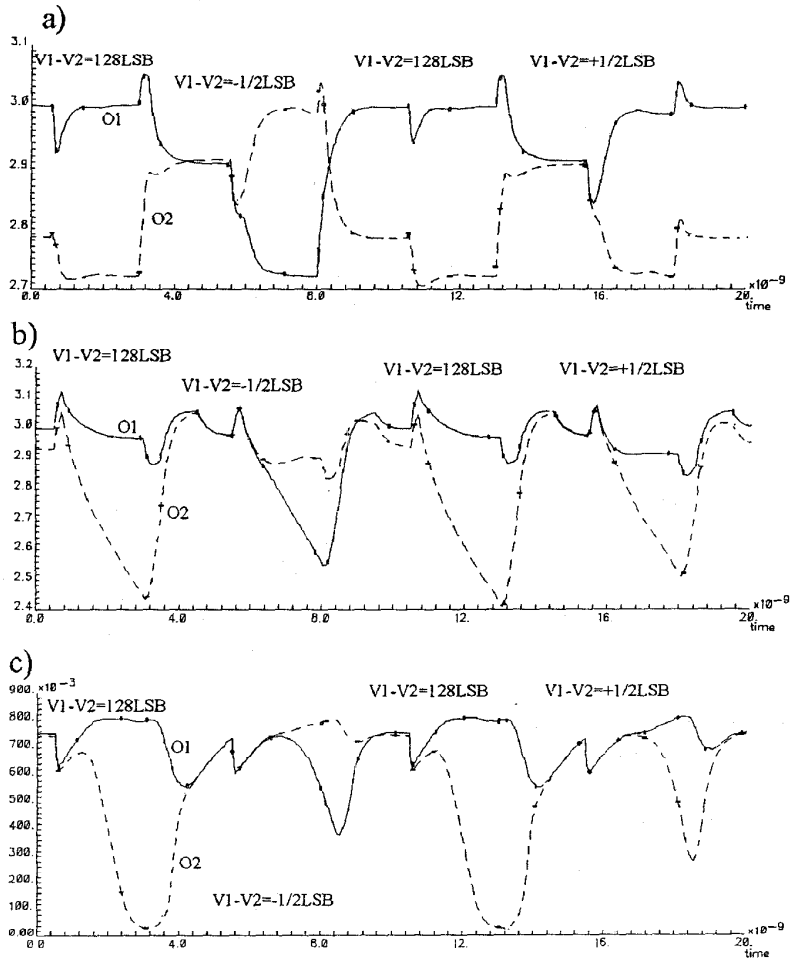

Figure 6: Output voltage waveforms: (a) conventional comparator, (b) **variable load comparator**, (c) **current mirror comparator**.

disturb the latched comparator by parasitic coupling, with the risk of bit errors. For this reason its design is critical. A current starved, dynamic circuit provided the best performance.

3 Implementation and results

The proposed comparators were designed in AMS 1.2um BiCMOS technology and simulated using SPECTRE. All the parasitic capacitances and the load represented by the interface to the CMOS logic were included. Fig.6 shows the voltage waveforms at the outputs V_{O1} and V_{O2} of the conventional latched comparator (a), of the **variable load latched comparator** (b) and of the **current mirroring latched comparator** (c). All were simulated with an input waveform of 200MHz changing between 128LSB (0.5V) and $\pm 1/2$LSB (± 1.95mv), which is the worst case operating condition within the input range of a differential A/D converter. These simulations were performed with nominal device parameters. The resistances and $\frac{W}{L}$ values are reported in tab.1.

In order to achieve a comparable voltage aperture $V_{O2} - V_{O1}$ at the end of regeneration (about 300mv for (a) and (c) and 340mv for (b)) the conventional comparator drains a tail current of $200\mu A$, the **variable load comparator** requires just $40\mu A$ and the **current mirroring comparator** a total of $80\mu A$ for the two stages. With the worst case parameters (2σ), the **variable load comparator** achieves a clock fre-

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	conv.	variable load	current mirr.
$R1 = R2$	$1.5K\Omega$		
$M1 = M2$		25/1.3	15/3
$M3 = M4$			15/3
$MP1$			5/1.2
$MP2$			9.6/1.2

Table 1: Resistance and $\frac{W}{L}$ values for the three comparators.

quency of 200MHz by increasing the tail current to $70\mu A$. This corresponds to 220MHz with nominal parameters. The degradation is more severe for the **current mirroring comparator**, which achieves only 165MHz at $120\mu A$ with the worst case parameters. These performance degradations are mostly due to a significant variation of the K' parameters of the MOS transistors for this specific technology. Since the levels of the V_b waveform are adapted by in-chip references, the **variable load comparator** is less sensitive to the decrease of the transconductance of the pMOS transistors.

4 Conclusion

Two novel BiCMOS comparator's architectures for high frequency (~200MHz) and-low power, low-voltage (3V) operation were presented. The **variable load** architecture allows a great reduction of the power dissipation with respect to the conventional circuit, and seems very attractive for achieving the highest speeds. The **current mirroring** architecture is very suitable for converter designs using current-mode interpolation and/or folding techniques. Moreover it fits well low voltage designs since fewer devices are stacked and kick-back effects are eliminated. First silicon is expected within the year.

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References

[1] Y. Yoshii, K. Asano, M. Nakamura and C. Yamada. "An 8 Bit, 100Ms/s Flash ADC". *IEEE Journal of Solid-State Circuits*, 19(6), December 1984.

[2] H. Reyhani and P. Quinlan. "A 5 V, 6-b, 60Ms/s BiCMOS flash ADC". *IEEE Journal of Solid-State Circuits*, 29(8), August 1994.

[3] M. Inoue, H. Sadamatsu, A. Matsuzawa, A. Kanda and T. Takemoto. "A Monolithic 8-Bit A/D Converter with 120 MHz Conversion Rate". *IEEE Journal of Solid-State Circuits*, 19(6), December 1984.

[4] B. Peetz, B.D. Hamilton and J. Kan. "An 8-bit 250 Megasample per Second Analog-to-Digital Converter: Operation Without a Sample and Hold". *IEEE Journal of Solid-State Circuits*, 21(6), December 1986.

[5] R. van de Plassche. *Integrated Analog-to-Digital and Digital-to-Analog converters*. Kluwer Academic Publishers, Netherlands, 1994.

[6] P.J. Lim and B.A. Wooley. "An 8-bit 200-MHz BiCMOS Comparator". *IEEE Journal of Solid-State Circuits*, 25(1), February 1990.

[7] G.M. Yin, F.Op't Eynde and W. Sansen. "A High-Speed CMOS Comparator with 8-bit resolution". *IEEE Journal of Solid-State Circuits*, 27(2), February 1992.

[8] M.Flynn and D.Allstot. "CMOS Folding ADCs with Current-Mode Interpolation". In *Proc. 1995 ISSCC*, 1995.

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