A Low Power 1.8 V 4-Bit 400-MHz Flash ADC in 0.18μ Digital CMOS

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Abstract

This paper is devoted to the design and implementation of high speed, low power, low voltage flash analog-to-digital convertors (ADC). A 4-bit flash ADC, with a maximum acquisition speed of 400 MHz, is implemented in a 1.8 V analog supply voltage. The large input signal dynamic range is handled using a fast switching common mode jump circuit, implemented with complementary pass transistors, which eliminates the need for high input-common-mode-range (ICMR) preamplifier based comparators. The measured INL/DNL is 0.4/1.1 LSB. The Signal-to-noise-plus-distortion ratio (SNDR) obtained at 12.5 MHz input is 21.25 dB. The spurious-free dynamic range (SFDR) is 27.6 dB and power consumption is only 30 mW. Design and simulations results are presented in dual-poly 0.18μ pure digital CMOS technology.

1. Introduction

Analog to digital convertors (ADCs) are of the most important mixed signal circuits as they interface with the real world analog signals and the digital signal processing and computing world. With the ever-increasing need for faster digital conversion and reduced supply voltage for deep-subμ CMOS technologies, the design of low voltage, high speed ADCs becomes increasingly vital, as it can often lead to a bottleneck in the performance of high speed analog and mixed signal integrated circuits (ICs). Furthermore, portable battery operated circuits, which are gaining wide popularity, require low power consumption to be viable. In this paper, the three driving digital forces of low supply voltage, low power and high speed have been addressed in the design of a high-speed, low-voltage 4-bit flash ADC which is power efficient. A general optimization has been done to achieve the lowest power consumption possible for the 1.8 V V_{DD}, 400 MHz A/D converter. The used architecture and the design of the building blocks are shown in the first part of the paper. Next the various design issues and the implemented solutions are presented. The digital error correction technique employed, which is very important for high conversion rate, is discussed and finally simulation results in dual-poly 0.18μ pure digital CMOS technology are presented.

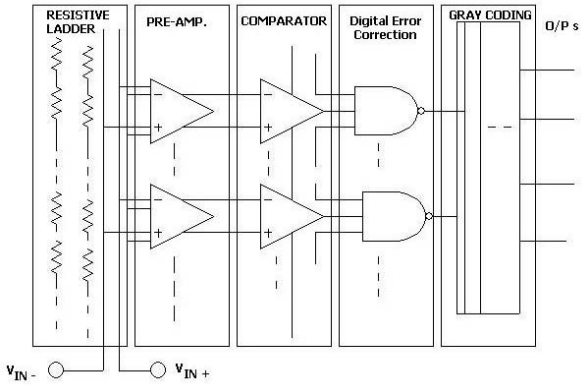

Figure 1. Block Diagram of the ADC Architecture.

2. The Flash Architecture

The 4-bit ADC implemented has a flash architecture. The flash architecture is usually the fastest, owing to its simplicity of design and parallelism employed.[1]-[4]. Fig. 1 shows the block diagram of the flash ADC. Because of the difficulty of implementing a high-speed sample-and-hold, the input is applied directly at the gates of the pre-amplifiers. The first stage is the bank of pre-amplifier based comparators, which compare the input signal with a set of 2^4 reference voltages, generated by a resistive ladder driven by V_{REF}. The resulting thermometer code is passed on to the digital error correcting circuitry, after which the output is converted to

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Table 1. Shows the primary target specifications.

Parameter	Specification
Conversion rate	400 MSamples/sec
Analog Input Range	$>$ dc to 10MHz
DNL	$<$ 0.5 LSB
INL	$<$ 1 LSB
SNDR	$\sim$ 25 dB
ICMR	$>$ 0.4- 1.4 V
Power	$<$ 30mW

gray code by a ROM line. Though the flash architecture is fast, it suffers from exponential increase of comparators with bit-resolution and therefore large die area and power. For our design, after reviewing recent works, we set certain primary target specifications, which are shown in Table 1.

3. Static Design of the Flash ADC

The most important task of the ADC is the correct comparison between the input level and the reference voltage level, the correct operation of a flash converter depends on the accurate definition of the reference voltages sensed by each comparator. The offset voltage arising in the comparator is random in nature, depending on the mismatch characteristics of the process, and directly adds to the reference voltages. Thus the first step in the static design is to calculate the offset voltage standard deviation that guarantees a high probability of correct design, i.e. high design yield [5]. Consider that the offset voltages of all the comparators are independent variables that follow a normal distribution. A Monte Carlo simulation can be used to estimate the design yield as a function of the offset voltage standard deviation. The results of the Monte-Carlo simulation is shown in Fig. 2.

4. Building blocks of the Flash ADC

Fig. 3 shows the schematic of one of the $2^4 - 1 = 15$ slices of the flash convertor. One slice of the ADC consists of a double-differential pre-amplifier, where the inputs are level shifted by a common-mode jump circuits to resolve the problem of finite ICMR of the pre-amp., followed by a discrete time track and latch comparator circuit. The comparator used here is a very fast regenerative comparator. The latch is a positive feedback device which amplifies any voltage difference across its

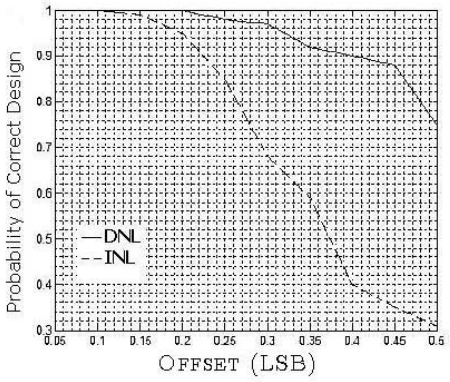

Figure 2. Shows the Probability of correct design vs offset of the comparator.

nodes exponentially. The time constant of the latch, in both set and reset phases is roughly,

$$T = \frac{C_{gs5} + C_{gs6}}{g_{m5} + g_{m6} - g_{ds5} - g_{ds6}} \quad (1)$$

, where C_{gsi} is the gate to source capacitance and g_{mi} is the transconductance of the i_{th} transistor. Both the NMOS and PMOS regeneration loops contribute with g_m and with C_{GS} to the definition of this time constant. If the size of the PMOS loop are relatively large compared with the size of the NMOS loop, the regeneration speed is strongly reduced because the PMOS transistors add too much capacitance to the regeneration nodes and add only a limited transconductance. Generally for optimal performance the ratio size of the NMOS and PMOS loops should be in their inverse ratio of carrier mobilities [1]. The outputs of the comparator are buffered and fed to the digital error correcting circuit before being given to the thermometer-to-gray logic convertor, which uses a pre-charged ROM line with speed-power optimized pull-down devices.

5. Design Issues of the Flash ADC

This section discusses the procedural design steps that were followed in the design the above blocks of the ADC's i_{th} slice. It follows a top-down design approach and considers global optimization of power and speed, wherever critical and possible.

5.1. Reference Ladder Resistance

To generate the reference voltages, a resistive reference ladder has been used on chip. Because of the

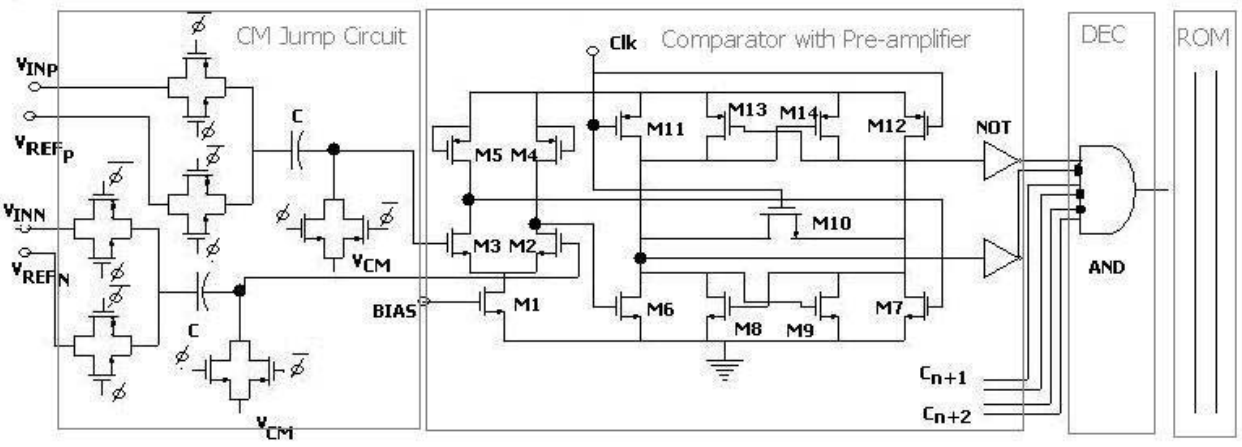

Figure 3. Shows the schematic of one of the 15 ADC slices.

well-known problem of ladder charge feed-through, the resistance value, R_{Ladder} of the ladder has to be small. A small resistance gives, on the other hand, high power consumption. The feed-through from the input to the midpoint of the ladder (which is the worst case) can be calculated by [11]

$$\frac{V_{MID}}{V_{IN}} = \frac{\pi}{4} f_{in}.R_{Ladder}.C_{in} \tag{2}$$

, where C_{in} is the total capacitance from the input to the resistive ladder and f_{in} is the input frequency. With this formula, the maximum ladder resistance was calculated for which the feed-through did not degrade the performance. This maximum ladder resistance gives rise to certain minimum power consumption in the reference ladder. The total ladder resistance of the ladder was approximately 320 Ω.

5.2. Switching Element

An NMOS switch operating in deep active region has an on-resistance, R_{ON}, given by

$$R_{ON} = \frac{1}{\mu_n C_{OX}(\frac{W}{L})_N(V_{gs} - V_{T_N})} \tag{3}$$

, where μ_n is the mobility of the electron and C_{OX} is the oxide capacitance per unit area. Thus we can see that the on-resistance of the NMOS switch decreases with increase in W/L of the device used. Thus many high speed applications prefer to use high values for W/L. Another important factor in the design of MOS switches is the channel charge injection factor. When on a MOS carries a finite amount of charge in its channel that under strong inversion conditions can be written as $Q_{CH} = WLC_{OX}(V_{gs} - V_T)$. When a MOS device turns off, the stored channel charge leaves the channel through the source and drain terminals introducing an error in the sampled voltage. If the injected charge is constant it appears as an error term; if it linearly depends on the input signal, then it appears as gain error and if it has a non-linear dependence on the input signal then this appears as a non-linear error. The non linear dependence actually arises from the fluctuation of the NMOS threshold voltage due to changes in the bulk-source voltage of the device. This is the limiting factor due to which very high values of (W/L) cannot be used for a MOS switch. To be on the safe side $\frac{Q_{CH}}{C} < 0.1LSB$ = 6 mV. To elucidate design constraints, a suitable starting value of C = 1 pF was chosen and then the W/Ls of the switches were calculated to satisfy both conditions. We have already seen that NMOS switches exhibit input-dependence resistance. This is a very important issue as it leads to signal dependent switching or distortion caused by the switches implemented by the pass transistors. The on-resistance of a MOS switch working in the linear region is given by eq. 3. This suggests that the resistance of the pass switch depends directly on V_{gs} of the MOS transistor, and hence the switching time const, $T_s = R_{ON} * C$ becomes a direct function of V_{gs}. In order to get over this problem, we used transmission gates as switches which comprise of both PMOS and NMOS transistors in parallel. The on-resistance of such switches are relatively constant. Another advantage of using transmission gate is that the input range of the switches increases to almost rail to rail as opposed to the case when only NMOSs are used. Yet another advantage of a CMOS switch is that the charge injection of the NMOS is partially canceled by the charge injection of the PMOS. Complete cancelation is not possible as the magnitude

of the charge depends on the $V_{gs} - V_T$ of each of the devices, which may not be equal to each other for the same input signal.

5.3. Comparator design

The comparator was made of two parts. A pre-amplifier and a discrete time track and latch circuit. The pre-amplifier stage should be wide-band and provide sufficient gain to overcome comparator offsets. It should also recover from large overdrive within one clock cycle. An open-loop low gain-stage amplifier with high gain-bandwidth product is used, which is suitable for high speed overdrive recovery. The input referred offset of the amplifier should also be minimal i.e. < 0.25 LSB, for the ADC to give satisfactory performance. While many comparator stages go for multi-stage pre-amplifiers followed by latches, we have only single stage pre-amplification followed by an output latch primarily due to two reasons : firstly more stages imply more power consumption - we were working on a tight power budget to ensure that the power consumed by a comparator should not exceed 1 mW, and secondly, multiple stages add to the input referred offset of the comparator. The implementation of double differential input comparators can be done using two major existing topologies - the first being a double-differential amplifier with tail current source, which converts the input voltage difference to a current equal to $g_m.[[V_{IN_P} - V_{REF_P}) - [V_{IN_N} - V_{REF_N})]$, where g_m is the transconductance of the device and V_{REF_p} and V_{REF_N} are reference voltages generated by the resistor degeneration of some constant voltage, V_{REF}. To implement such a circuit we need to make sure that the input pre-amplifiers are always in the linear range and g_m is constant for all V_{IN}. This poses a major problem in reaching high input common mode range (ICMR). The common method to overcome this is by using PMOS and NMOS double-differential pairs in parallel to increase ICMR, but this would require five to six times the current required for a single NMOS double-differential input pair. Another disadvantage is the increase of input referred offset arising due to the mismatches in V_T and βs of the four input transistors as opposed to two in case of single differential input pair. This is quite unacceptable for a low power ADC design. The other way out is using a common mode jump circuit which creates a voltage equal to $(V_{IN_P} - V_{REF_P} + V_{CM})$ and $(V_{IN_N} - V_{REF_N} + V_{CM})$ at the positive and negative inputs of the comparator, respectively. The common mode jump circuit is shown in Fig. 4.

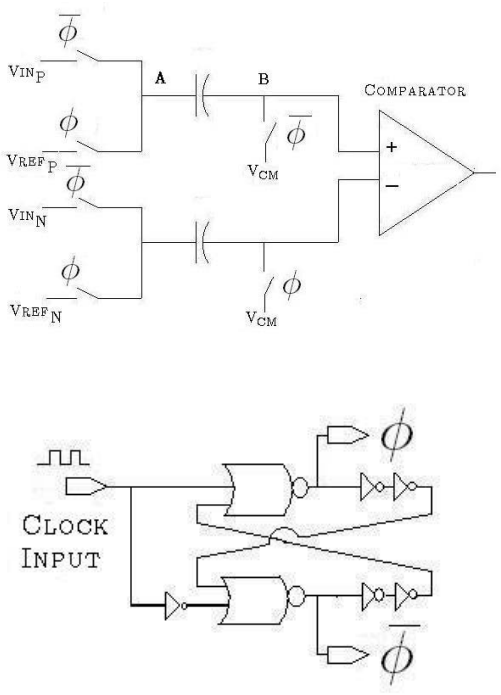

Figure 4. Shows the common mode jump circuit(top) and clock generation circuit(below).

5.3.1 Common Mode Jump circuit

A differential comparator circuit is expected to compare $V_P = V_{IN_P} - V_{REF_P}$ against $V_N = V_{IN_N} - V_{REF_N}$. Even if we consider V_{IN_P} and V_{IN_N} sinusoids from 0.4 to 1.4 V, V_P and V_N fall outside the common mode range of the input pre-amplifiers (viz. $V_{ON} + V_{gs_N}$ to $V_{DD} - V_{ds_P} + V_{T_N}$). If the PMOS load is diode connected the above reduces to $V_{DD} - V_{ds_P} + V_{T_N}$ i.e some 100 mV above V_{DD}. To overcome the above problem we raise V_P and V_N by fixed common mode voltage say V_{CM}. To do that we use the circuit in Fig. 4. It also shows the circuit used for generating the non-overlapping clocks.

The working of the above circuit is as follows. In clock phase ϕ the capacitor C gets charged to $V_{REF_P} - V_{CM}$. In phase $\overline{\phi}$, the left side of the capacitor is connected to V_{IN_P}, the other side, in order to maintain charge conservation would jump to $V_P = V_{IN_P} - V_{REF_P} + V_{CM}$. There are two issues to consider in the above circuit. First is that, this would limit the size of the input NMOS transistor of the pre-amplifier, as the transistor would add some input capacitance C_{in} (mainly the $C_{gs} = \frac{2}{3}WLC_{OX}$) to the input node. In this case, simple analysis shows that the sampled volt-

age, V_S, at the input node would be given by,

$$V_S = V_P(\frac{C}{C - C_{in}}) - V_{CM}(\frac{C_{in}}{(C - C_{in})}) \quad (4)$$

For this to be equal to V_P we need $C_{in} < 0.01 * C$. Increasing C will increase the charging time of the capacitor. Hence we need to limit the size of the input transistors.

Therefore, $C_{in} = 0.01 * C$ and $V_C = 1.01 * V_P - 0.01 * V_{CM}$. Since V_{CM}= 900 mV, this brings an error of about 9 mV ($\sim$ 0.15 LSB). To be on the safe side we restricted C_{in} to about 50 fF, for C = 1 pF.

This gives a starting constraint for the dimensions of M2. From [3] we have seen that for proper overdrive recovery, the bandwidth requirement of a one-pole pre-amplifier is given by

$$F_{-3dB} = -\frac{1}{2\pi t_{REC}} ln\{1 - \frac{1}{1 + \frac{\Delta V}{V_{eff}}}\} \quad (5)$$

Where $t_{REC} \sim \frac{0.01}{F_S}$. ΔV= 1 LSB and $V_{eff} = V_{gs} - V_{T_N}$ of the input pair.

This shows that a higher value of V_{eff} will require a lower value of 3dB frequency for the pre-amplifier. We start with typical values of V_{eff} i.e. (200 mV, 300 mV, 400 mV, 500 mV) and calculate the F_{-3dB} required for each. We chose a suitable value of $V_{eff} \sim$ 400 mV, so as to not overshoot the power budget, which was $\sim$ 100 $\mu A * V_{DD}$. For the architecture of the pre-amplifier chosen F_{-3dB} is given by

$$F_{-3dB} = \frac{1}{2\pi} \frac{1}{(g_{m4} + g_{ds2})C_L} \quad (6)$$

The pre-amp designed has unity gain bandwidth of about 10 GHz and dc gain of 6.2 dB. Since $g_{ds2} \ll g_{m4}$ we can neglect g_{ds2}. Assuming a maximum load of 100 fF from the 2^{nd} stage, we calculated the W/L ratio of M4 from g_{m4}. For the latch,

$$T_{reg}(\sim \frac{0.01}{F_S}) = \frac{2}{3} C_{OX} \sqrt{\frac{WL^3}{2K'I}} \quad (7)$$

Choosing a suitable value of I from the above equation we get W/L ratio for M8 and M9. The ratio of W/L values of PMOSs M13 and M14 with NMOSs M8 and M9 is approximately taken equal to the inverse ratio of their carrier mobilities [1].

6. Digital Error Correction

Digital error correction is an important aspect in the design of ADC with very high sampling speed. This is because when switching time reduces to become comparable to the clock skew and other parasitics induced delays, coupled with un-favorable offsets, improper comparison might take place and ADC output might be incorrect. In such case, bubbles are introduced, which is a situation when a 1 is found above a 0 in the thermometer code. In our design we take care of first order bubble error detection using a regular combinatorial circuit involving three-input AND gates which address the ROM line. The ROM line in turn is used to convert the thermometer code to gray or binary code. The circuit detects single bubble errors without introducing any significant delay in the signal path.

6.1. Meta-stability errors of the Comparator

Another problem observed in ADCs is that of meta-stability. Meta-stability designates the ability of a comparator to be completely balanced for a short period of time when the applied input signal difference is very small. In a flash converter, this means that when the input signal is very close to one of the reference voltages, that comparator might be unable to toggle fast enough to a valid logic level. Therefore, the logic gates driven by that comparator output might interpret the input as different levels. As a consequence, zero, one, or two ROM lines might be selected, leading to severe errors in the digital output code. To resolve this problem to certain extent, we used Gray coding. Here the adjacent code bits vary by only one bit therefore any comparator output which is undecided can be regenerated to either 1 or 0 with 50% probability of error in 1-bit, which is only an LSB error. However if the encoding had been binary, the an undecided comparator output could have created a huge error in the digital code generated. Thus, the problem of meta-stability is also resolved to great extent.

7. Results

The simulations were run on the CADENCE IC design platform, which is an industry standard and the implementation was done in 0.18μ CMOS9T technology. The digital supply voltage used is 1.8 V, which is among the lowest reported [1]. Poly-to-poly capacitors were used as they show less voltage instability. The performance of the ADC is shown in Fig. 5. The DNL is 0.4 LSB and INL is 1.1 LSB. The SFDR is 27.6 dB and SNDR at 12.5 MHz is 21.25 dB, which is very close to the maximum possible 24 dB, for a 4-bit ADC. HDB2 for input mixed signal (IMS) is 66dB. The power consumption was optimized to a low value of 30 mW. The results satisfies almost all our initial target specification

except for INL which is higher by 0.1 LSB. Some of the important performance parameters are shown in Table 2. The IC is being fabricated by National Semiconductor Corporation, USA.

Table 2. Shows the performance parameters of the ADC

Parameter	Achieved Value
Supply Voltage	1.8 V
Technology	0.18μ CMOS9T
I/P Diff. Range	2 V_{PP}
Ladder Resistance	320 Ω
Sampling Rate	400 MHz
Conversion Rate	1 code block/clk cycle
DNL	0.4 LSB
INL	1.1 LSB
Power Dissipation	20 mW
SNDR at 12.5 MHz	21.25 dB
SFDR	27.6 dB
HDB2 of IMS	66 dB
HDB3 of IMS	24 dB
Pre-amp.(PA) Gain	6.2 dB
PA Unity GBW	10 GHz
PA Settling time	1 ns

8. Conclusion

In this paper, the systematic design and the simulation results of a low-voltage high-speed CMOS ADC have been presented. The maximum sampling speed is 400 MHz and the SNDR at 12.5 MHz is 21.25 dB. The analog supply voltage is only 1.8 V. Several design issues have been discussed and used in the optimization procedure of the ADC. It has been shown that low-voltage, low power design of high-speed ADCs is feasible in sub-μ pure digital CMOS technologies. These have immediate applications in very high speed, multi-bit $\Sigma\Delta$ modulators, disk-read channels and several other mixed-signal applications.

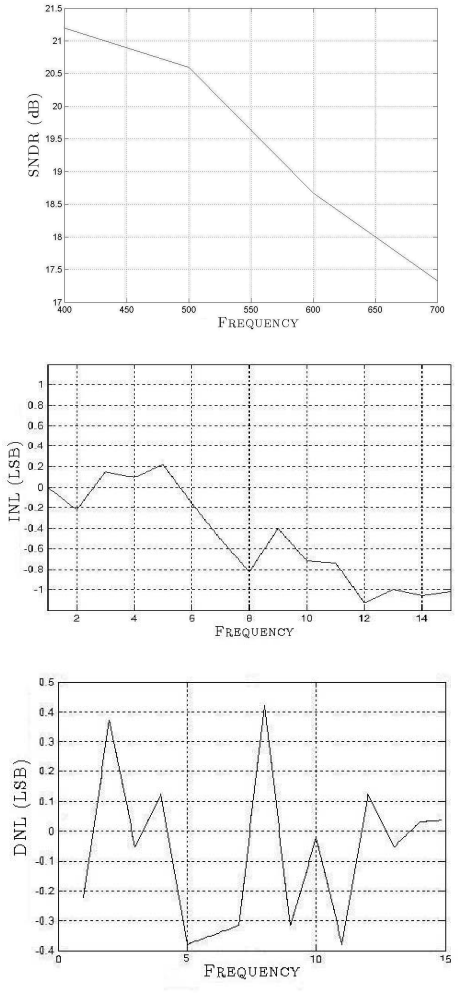

Figure 5. Shows the SNDR (top), INL (middle) and DNL(bottom) of the ADC with frequency (in MHz).

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