

Design and Analysis of a Low-Power Energy-Recovery Adder

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Abstract

In this paper, an 8-bit energy-recovery adder design is evaluated through SPICE simulation for energy dissipation and delay time, and is compared against a supply-voltage-scaled adder. The experimental results indicate that the energy-recovery adder outperforms the supply-scaled version for a wide range of frequencies.

1. Introduction

As the density and the operating speed of CMOS VLSI chips increases, their power dissipation becomes of utmost importance since it imposes restrictions on their design and their performance. It is well known that the dominant factor of the energy, E , dissipated in CMOS when a capacitance, C , is charged from 0 to a voltage V or discharged from V is:

$$E = \frac{1}{2}CV^2 \quad (1)$$

The prevalent approach to reduce this dissipation is to scale down the supply voltage V [1], which is attractive due to its simplicity because of the requirements for static logic structures and dc power supplies. However, it restricts the design style since when V approaches the threshold voltage V_t , dynamic structures are infeasible and, more importantly, the circuit performance is poor. Furthermore, the minimum energy dissipation is limited by the threshold voltage V_t .

Energy recovery is another approach for reducing the energy dissipation [2] [3] [4], where signals such as clocks are to directly drive the capacitive loads through charge-steering logic blocks (e.g., pass gates, transmission gates, etc.). The ideal energy dissipation, E_{ER} , of an energy-recovery circuit when a capacitance, C , is charged from 0 to a voltage V or discharged from V , through a circuit of resistance R , during time T , from a constant current source is [5]:

$$E_{ER} = PT = I^2RT = \left(\frac{CV}{T}\right)^2RT = \left(\frac{RC}{T}\right)CV^2 \quad (2)$$

Unlike the supply-scaled approach, energy-recovery is arbitrarily scalable since the energy dissipation is proportional to the inverse of the charging time T . Theoretically,

asymptotically-zero energy dissipation is possible for infinitely large T . Although energy recovery requires a different logic synthesis and special-purpose power supplies that are a new challenge to design, it is compatible with a variety of design styles.

For this paper, we compare, under the same conditions, the practicality of these two approaches (i.e., energy recovery and supply scaled) by applying them to the design of a pipelined adder suitable for a microprocessor datapath, a program counter, etc. First, we describe the experiment set-up along with the design of the supply-scaled adder (SSA). Then, we present the energy-recovery adder (ERA), we analyze the simulation results, and finally, we draw the conclusions.

2. Experimental Set-Up

In this section, we describe the set-up of the experiment. The adders are compared while their throughput is held constant. Specifically, we reduce the voltage supply in the SSA and we increase the charging time in the ERA which both imply lower operating frequency and less energy dissipation per cycle. Both adders operate from a two-phase, non-overlapping clock as shown in Figure 1, which also indicates which operations are performed in each phase. The two clock phases are assumed to be symmetrical, i.e., they have the same width. The non-overlap gap is held constant at 5ns. Each output of both adders drives a 100fF load capacitance. The SSA used in this experiment is a static CMOS circuit from Chandrakasan et. al. [1], which can operate at reduced supply voltages (Figure 2). Pass-gate logic was excluded from the comparison because it does not operate at low supply voltages. Conventional input and output CMOS latches were added to operate the SSA with a two-phase, non-overlapping clock. The latches are set up so that the addition starts at the rising edge of ϕ_2 . The rising and falling edges

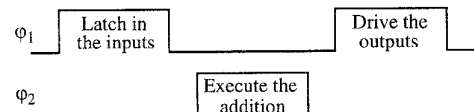


Figure 1. The two-phase, non-overlapping clocking scheme.

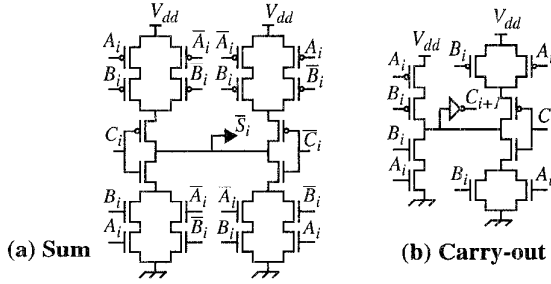


Figure 2. Transistor schematics for the SSA building blocks. are set to 0.5ns. All the nFETs are of minimum size and the pFETs are sized by the ratio of the mobilities, so that the total circuit capacitance is minimized for equal rising and falling transition times.

3. Description of the Energy-Recovery Adder

The ERA operation relies on (a) stretching the phase rising and falling edges, i.e., increasing the charging time T , (b) bootstrapping, to operate at the highest possible gate voltages, and (c) using pass transistor logic.

Figure 3 illustrates the clock scheme which has different phase shapes than the one of Figure 1. The phase width t_w is exploited in such a way that the maximum possible charging time T is achieved. The time t_h is kept minimal (i.e., 2ns to 3ns) and T is equal to $(t_w - t_h)/2$.

The ERA is organized as a bit-sliced carry propagate adder. All the inputs are fed to the circuit in dual-rail form. Each bit slice consists of four dynamic input latches, a block (i.e., *Sum*) that produces the sum bit S_i , and a block (i.e., *C-out*) that generates the carry-out C_{i+1} and its inverse \bar{C}_{i+1} . A pair of *Sum* and *C-out* blocks constitutes a full adder circuit. At phase ϕ_1 , the inputs are latched, and during ϕ_2 , they drive the corresponding *Sum* and *C-out* blocks.

Figure 4 shows the schematic diagram of the energy-recovery dynamic latch, which also illustrates the bootstrapped action. A detailed presentation of bootstrapping can be found in Seitz et. al. [4] and in Glasser and Dobberpuhl [6]. The basic idea is to exploit the varactance of a MOSFET. The gate node of a pass transistor boots to a voltage greater than the channel voltage, and hence, the threshold voltage drop through the channel is avoided, so that a full voltage

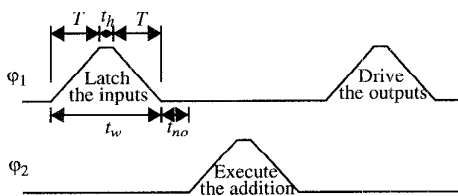


Figure 3. The ERA clocking scheme.

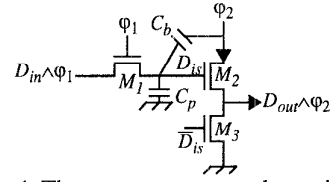


Figure 4. The energy-recovery dynamic latch.

swing signal passes from the drain to source of the pass transistor. Assume that the circuit operating voltage is V and that the node D_{is} is charged to at most $V - V_t$, where V_t is the threshold voltage of the transistor M_1 (the *isolation* transistor). When the positive edge of ϕ_2 occurs, the voltage of the node D_{is} is bootstrapped to at least $V + V_t$ due to the gate-to-drain capacitance C_b of the device M_2 (the *bootstrap* transistor) given that the ratio C_b/C_p is large enough. The output D_{out} is charged to voltage V . Two important factors affect the bootstrapping action: (a) the ratio of C_b to the parasitic capacitance C_p should be large, which entails that M_2 should be at least four times larger than M_1 , and (b) the body effect. The device M_3 is a minimum-size device which clamps the output low during ϕ_2 when D_{is} is at 0V. M_3 is driven by the complementary dual-rail input.

Figure 5 illustrates the energy-recovery logic circuits that evaluate the sum S_i , and the carry-out C_{i+1} of a full adder with the input data signals A_i and B_i , and the carry-in C_i . All the input data are fed to the adder from dynamic latches, which ensures that the input data are valid at ϕ_2 . These two circuits are similar since they are based on a 4-to-1 multiplexer function. The signals A_i , \bar{A}_i , B_i , and \bar{B}_i select one of the four possible paths that drive the output. In the sum case, first the addition result is isolated, and in the next phase (i.e., ϕ_1) the output capacitance is driven through the bootstrap device. In this case, an output clamp transistor is not necessary because the driven capacitance is modeled as a 100fF load capacitor and there is not any block of logic attached to the output. In contrast, the carry-out propagates between the adder bits and does not drive any output load capacitance. The main differences between these circuits are the bootstrap transistor, which is required only for the sum, and the transistor size. The devices that form the sum 4-to-1 multiplexer are minimum size, whereas the devices of the carry-out circuit are $24\mu\text{m}$ wide in order to reduce the resistance through the carry chain. The width of the carry-chain devices was determined by the number of stages (8)

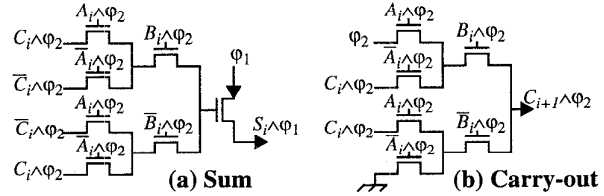


Figure 5. Transistor schematics for the ERA building blocks.

times the minimum transistor size ($3\mu\text{m}$). As one can notice, both C_i and \bar{C}_i are required to get the sum S_i ; another circuit very similar to the one shown in Figure 5(b) computes \bar{C}_{i+1} .

In comparing the ERA to the SSA design, there are advantages and disadvantages in terms of area (and hence driven capacitance) that can be immediately observed. The main disadvantage of the ERA is that the bootstrap device must be at least four times wider than the isolation device. On the other hand, the transistor count of the energy-recovery version is less than that of the conventional CMOS version. Excluding the latches in both cases, the ERA requires 19 nFETs, while the supply-scaled version needs 16 nFETs and 16 pFETs. Furthermore, the elimination of pFETs in the ERA circuit contributes to a compact layout, and thus, to a potentially faster circuit.

Generally, the delivered charge during each clock phase can be distinguished as either *recoverable* or *non-recoverable* due to the diode charge-trapping effect. The former includes the charge on the capacitance driven by a phase up to the isolation device, whereas the latter is basically due to the charge on the capacitance of the bootstrap nodes. Hereafter, we use the terms recoverable and non-recoverable for both the charge and the corresponding capacitance. The charge injected into the recoverable capacitance can be fully recovered by the end of the phase. On the other hand, a large fraction of the charge injected into the non-recoverable capacitance is trapped after the end of the phase and can not be recovered.

4. Simulation Results

In this section, we discuss the SPICE simulation experiments carried out for a $2\mu\text{m}$ MOSIS n-well process followed by a presentation and analysis of the results. To make the comparison fair, we measure the energy dissipated for the worst-case addition in terms of both power dissipation and latency for both circuits.

We first simulated the SSA by varying the supply voltage from $2V_t$ to $6V_t$, and measuring the propagation delay of the carry chain. From these delay times we set the phase widths t_w for the experiments. Subsequently, we measured the energy dissipation in the SSA by scaling the supply voltage and using the appropriate phase width and cycle time so that the circuit was operating at maximum speed.

For the ERA, two sets of simulations were done, with the voltage swing fixed at $5V_t$ and at $6V_t$. The charging time T was set so that the throughput of both adders was the same. This was accomplished by setting the charging time T equal to $(t_w - t_h)/2$, where t_h varied from 2ns to 3ns to match the phase widths and the cycle times of the two adders. In both cases, we measured only the energy dissipated for one spe-

cific addition even if a new addition was issued in the next cycle.

Figure 6(a) compares energy versus frequency for the two adders. The x-axis is the clock frequency, f , of the adders. Three trends are observable:

- (i) The ERA outperforms the SSA for almost all the cases in terms of energy dissipation per operation. Furthermore, the difference increases proportionally to the clock frequency.
- (ii) Although we expected the energy dissipation of the ERA to scale linearly with the charging time T , it scales down slower due to the charge trapped in the isolation nodes.
- (iii) The ERA dissipates less energy when the operating voltage is $5V_t$ because less charge is trapped in the isolation nodes.

To verify that the difference of the energy dissipation between the ERA and the SSA is due to the different approaches and is not a result of the different circuit capacitances, we also plot in Figure 6(a) the energy dissipation of the ERA without the effect of energy recovery (noted as *hybrid-ERA*). In this case, the energy dissipated in charging and in discharging the ERA capacitance are given by Eq. 2 and Eq. 1 respectively. Under the same operating conditions ($6V_t$, 28MHz), the total energy dissipation of the hybrid-ERA is about half of the SSA. If the ERA was powered conventionally, the actual dissipation would be about twice as much because of the two-fold overhead in delivering charge at a constant voltage. The dissipation of the ERA would be then about the same as the SSA under the same operating conditions.

As mentioning before, the addition is performed in three steps: (a) driving the dynamic input latches, (b) executing the addition, and (c) driving the output. Each of these operations requires a phase (see figure 3). To further investigate the individual steps, Figure 6(b) compares the energy dissipated per phase for the ERA.

The dynamic input latches have a very low ratio of recoverable to non-recoverable charge. Therefore, the bootstrap node capacitance dominates, and thus, most of the charge injected is trapped in the isolation node. We measured that roughly 66% and 69% (for V equal to $5V_t$ and $6V_t$ respectively) of the injected charge to the input dynamic latches is trapped. This implies that the energy dissipation of the input dynamic latches will not scale linearly with time, as shown in Figure 6(b).

The phase for the actual add operation indicates the effectiveness of energy recovery for logic in this example. According to Figure 6(b), the energy dissipation scales better in the adder than in the input dynamic latches. This is

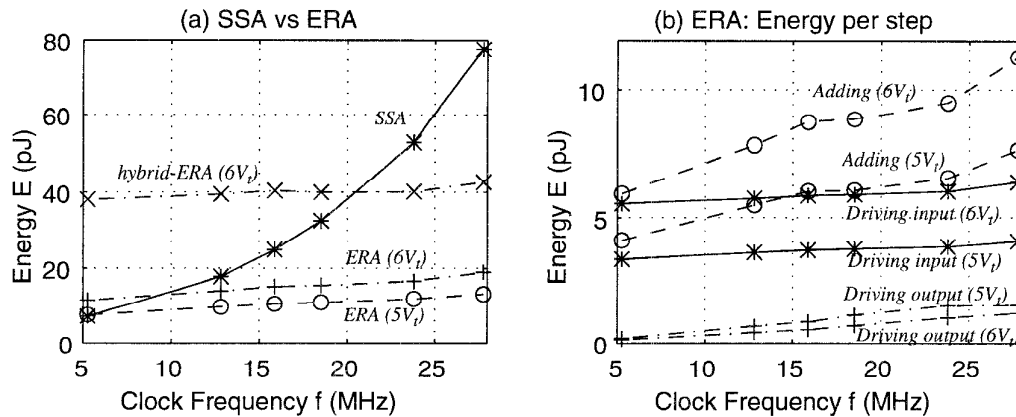


Figure 6: Comparison of (a) total energy dissipation for a worst-case addition and (b) energy dissipation per step.

expected since the recoverable charge dominates and the charge trapped is only about 12% of the total charge injected for the execution of this step.

Finally, for the last step, the energy dissipated is very low because there is no logic attached to the output other than a 100fF load capacitor and the entire injected charge is recovered at the end of the phase. In this case, where no charge is trapped, the energy dissipation *decreases* when the operating voltage increases, since the resistance across the bootstrapped device decreases (see Eq. 2).

There are some important comments to be stated regarding the results that we just described. First of all, in the general case, successive additions potentially reuse the same charge. Only when a bootstrapped node discharges, the trapped energy in the isolation nodes is lost. Furthermore, for a practical design where the inputs come from a data bus or block of combinational logic, the ratio of recoverable to non-recoverable charge would be significantly higher. The same fact affects also the output latches since, generally, they would drive another block (i.e., one or more input dynamic latches), and hence there would be some charge trapped which is not the case in the experimental circuit.

5. Conclusions

In this paper we compared the performance of an energy-recovery adder against a supply-scaled one in terms of energy dissipation and clock frequency. Although the energy dissipation of the ERA depends strongly on the ratio of recoverable to non-recoverable charge injected in the circuit, in this study it outperforms the SSA in terms of energy dissipation, especially for high frequencies. It is also of importance that the non-recoverable charge imposes a CV^2 limit higher than the asymptotically zero energy dissipation, which implies that the energy-recovery approach would perform better in circuits that exhibit a high ratio of recoverable

to non-recoverable charge (e.g., data bus drivers, register files, RAMs, etc.).

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