New Bulk Dynamic Threshold NMOS Schemes for Low-Energy Subthreshold Domino-Like Circuits

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Abstract

Dynamic threshold MOS circuits offer speed and energy saving advantages over the conventional subthreshold CMOS circuits; they are faster and consume less energy. In this paper a new Bulk Dynamic Threshold MOS scheme for NMOS transistors (B-DTNMOS) in Domino-like dynamic circuits is introduced. In this scheme the substrate of all the NMOS transistors is connected to the clock signal in dynamic circuits. The proposed scheme is shown to be 63% faster and has 37.2% energy savings compared to the regular subthreshold CMOS circuits.

1. Introduction

Energy-efficient VLSI design has been one of the most active research areas during the past decade. The continuing growth of portable devices market, such as notebooks cellular phones, and personal communications devices; the growing popularity of these devices has increased the demand of low-energy digital systems for longer operating times from their batteries. Nonetheless, moderate-performance devices such as pacemakers, wrest watches, hearing aids, and calculators have stronger demand for lower energy levels with a moderate-speed requirement.

Power consumption reduction can be achieved by several ways; the power consumption equation ($P = C_L V_{dd}^2 f$) shows that the most effective way to redusce power consumption is through reducing the supply voltage and this agrees with the continuing scaling down of the transistor size. Threshold voltage cannot be scaled down with the same rate due to the standby power considerations in static circuits and avoidance of failure in dynamic circuits [1]. Subthreshold circuit operation (sub-0.5V) is the logical result of the continuing downscaling.

Assaderaghi *et.al* in [1] introduced the Dynamic threshold-voltage MOSFET (DTMOS) in Silicon-On-Insulator (SOI) technology. DTMOS is implemented by connecting the gate of the MOSFET to its substrate to achieve the desired performance, which was shown to outperform the conventional CMOS logic in the subthreshold region in terms of speed and energy savings. The DTMOS technique can be applied to both NMOS and PMOS transistors in SOI technology since all transistors are isolated from each other and they don't share a common substrate. However, in the case to Bulk-CMOS technology, the standard DTMOS technique can only be applied to the PMOS transistors since every PMOS transistor has its own n-well; standard DTMOS technique cannot be applied to NMOS transistors in Bulk-CMOS technology because all NMOS transistors have a common substrate. To extend the application of the DTMOS to the NMOS in Bulk-CMOS technology triple-well has to be used [2]. This problem has prevented the use of DTMOS scheme widely in integrated circuits made in the conventional Bulk-CMOS technology. An example of implementing DTMOS technique on PMOS transistors in Bulk-CMOS process technology (DTPMOS) was introduced in [3].

In this paper, dynamic threshold MOS technique in Bulk-CMOS is extended to NMOS transistors where the common substrate is connected to the clock signal to achieve faster and more energy efficient circuits. This paper is organized as follows; section 2 discusses briefly the subthreshold circuit operation. Section 3 gives an introduction to the Dynamic Threshold MOSFET (DTMOS) technique. The proposed B-DTNMOS scheme is introduced in section 4. Simulation and experimental results are discussed in section 5. In section 6, DTPMOS technique is used along with the proposed B-DTNMOS scheme to further improve circuit operation. Section 7 concludes the work done.

2. Subthreshold circuit operation

Lowering the supply voltage to below the transistor threshold voltage so that the transistors will operate in the weak inversion domain ensures circuit operation in the subthreshold region. In this region, the subthreshold region, there is no conducting inversion channel, instead

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the operating current is the leakage current of the device, which gives a power consumption orders of magnitude lower than the regular strong inversion circuit. Unfortunately, the fact that the switching current is the leakage current indicates that the delay of the circuits operating in the subthreshold region is higher than the strong inversion mode of operation; however, the decrease in power consumption diminishes the drawback of increased delay, that results in a much lower energy rate for the subthreshold circuit. The subthreshold current equation is known to be:

$$I_{sub} = I_o(\frac{W}{L})e^{\frac{V_{GS}-V_T}{nv_t}} \quad (1)$$

V_T is the MOSFET threshold voltage

v_t is the thermal voltage $(= KT/q)$, and it is equal to 26mV at 300K

n is the subthreshold slope parameter

Subthreshold CMOS circuits behave differently if compared to the strong inversion CMOS circuits; they become more sensitive to voltage supply variations, temperature variations, and process parameters variations. However, they gain some favorable characteristics such as increased transconductance gain, due to the exponential relationship between the voltage and the current as seen in (1), and near-ideal static noise margin [2]. To overcome these limitations of the conventional subthreshold CMOS circuits, Dynamic Threshold MOS was introduced in [1].

3. Dynamic Threshold MOSFET (DTMOS)

In the Silicon-On-Insulator CMOS (SOI-CMOS) technology, the junction areas are small and the isolation between MOSFETs is high as compared to the Bulk-CMOS technology; these were the reasons behind using the Dynamic Threshold MOS (DTMOS) technique in SOI technology first. Figure 1 shows the SOI-DTNMOS as proposed in [1]. It's clear from equation (1) that if V_T increase then the leakage current will decrease and vise versa; so when the transistor is turned on we need to lower V_T to achieve higher current and higher driving capability, and when the transistor is turned off we need higher V_T to decrease the leakage current to save the power wasted while the transistor is in the off-state. Tying the gate of the MOS to its substrate gives us the desired performance. Equation (2) gives the threshold voltage expression for an NMOS transistor.

$$V_T = V_{T0} + \gamma(\sqrt{|-2\Phi_F + V_{SB}|} - \sqrt{|-2\Phi_F|}) \quad (2)$$

V_{T0} is the threshold voltage when $V_{SB} = 0$

γ is the body-effect coefficient

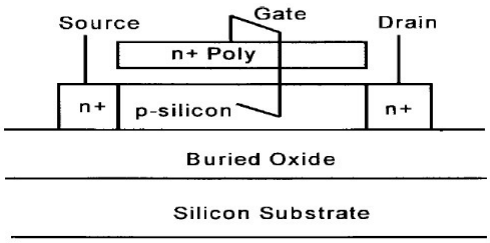


Figure 1. SOI Dynamic Threshold NMOS [1]

$2\Phi_F$ is the silicon surface potential at the onset of the strong inversion and it's equal to –0.6V for typical p-type substrates

V_{SB} is the source to body voltage

The following discussion explains the DTMOS operation for NMOS transistors, similar discussion can be done for PMOS transistors. Body voltage is high during the on-state, since the body is tied to the gate, and V_{SB} becomes low which forces γ to go low, thus raising the drain current, improving switching speed, and increasing the driving capability of the circuit. During off-state, body voltage returns to zero to return V_T to its normal value and V_T returns to its zero body bias value to decrease the drain current and save energy. In the off-state, both MOS and DTMOS have identical characteristics. Reduction of threshold voltage during the on-state is due to the reduction of body charges. Reduction of body charges leads also to a lower effective normal field in the channel and higher carrier mobility. The lower threshold voltage causes an increase of the inversion charge, which combined with the higher carrier mobility lead to a higher current drive in DTMOS [1][4].

The effective gate capacitance of a DTMOS is larger than the gate capacitance of a regular MOS, but the much higher driving current diminishes this problem and causes the DTMOS circuit to have less delay than the regular MOS circuits. DTMOS circuits are more robust against temperature and process parameter variations as compared to the conventional subthreshold CMOS circuits without losing the main advantage of the subthreshold circuits; namely, ultra-low-energy operation. Superiority of the DTMOS circuits over the conventional subthreshold CMOS circuits was proven in the literature [1][2][3][4][7]. Figure 2 shows the symbolic representation of the DTNMOS and the DTPMOS.

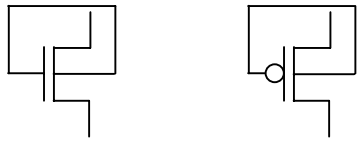


Figure 2. Dynamic Threshold NMOS (DTNMOS), and Dynamic Threshold PMOS (DTPMOS)

4. The proposed Bulk Dynamic Threshold NMOS (B-DTNMOS) scheme

In this section, a new Bulk Dynamic Threshold NMOS (B-DTNMOS) scheme for dynamic circuits is proposed. As discussed earlier, the main obstacle that prevented the implementation of DTMOS technique in Bulk NMOS transistors was the fact that all NMOS transistors share the same substrate; in other words, each NMOS transistor cannot have its own substrate bias independent of other NMOS transistors. In order to overcome this problem for a specific category of circuits, namely, dynamic circuits; the common NMOS substrate can be connected to the clock applied to the circuit. Connecting the clock to the common NMOS substrate will ensure the correct operation expected from DTMOS circuits. During the evaluate phase, clock is high, the body voltage becomes high forcing the threshold voltage to be low; lowering V_T increases the leakage (switching) current, improves speed, and enhances the driving capability of the circuit. During precharge phase, clock is low, the body becomes zero biased; thus returning the NMOS to its regular operation, meaning, lower leakage current and lower power dissipation. Figure 3 shows the proposed scheme applied to a 2-input AND gate in Domino dynamic circuit design style.

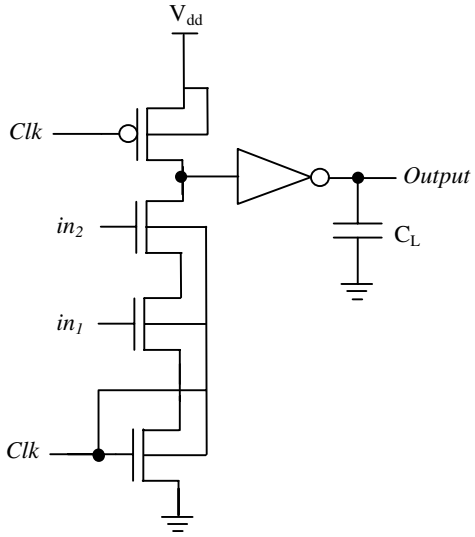


Figure 3. Domino implementation of a 2-input AND gate using the proposed scheme

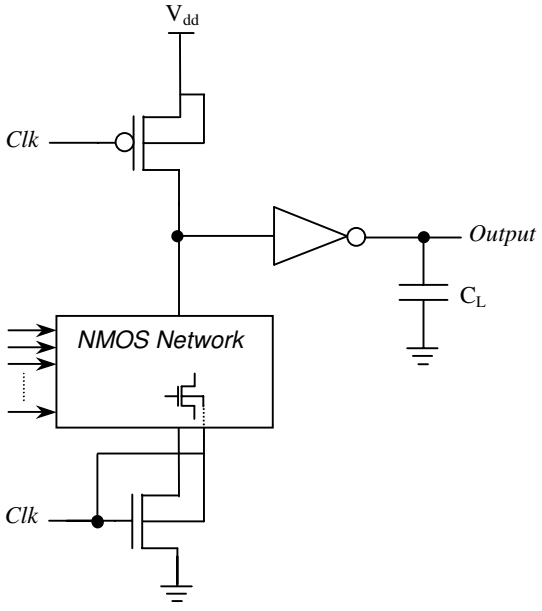
5. B-DTNMOS simulation and experimental results

To show the superiority of the proposed B-DTNMOS dynamic scheme over the conventional subthreshold dynamic MOS operation, for domino-like circuits, simulations were done on a 1-bit full adder cell in Domino design style. The full adder was implemented in both the conventional subthreshold Domino and the proposed B-DTNMOS Domino scheme. Figure 4 shows the Domino circuits implemented in both the conventional and the proposed schemes. HSPICE simulations were carried out for both the proposed and the conventional circuits using the TSMC 0.18 μm CMOS technology and using a comprehensive set of test patterns. The circuits were simulated using a 0.2V voltage supply and at different frequencies; {20, 50, 100, 150, and 200} MHz frequencies were used.

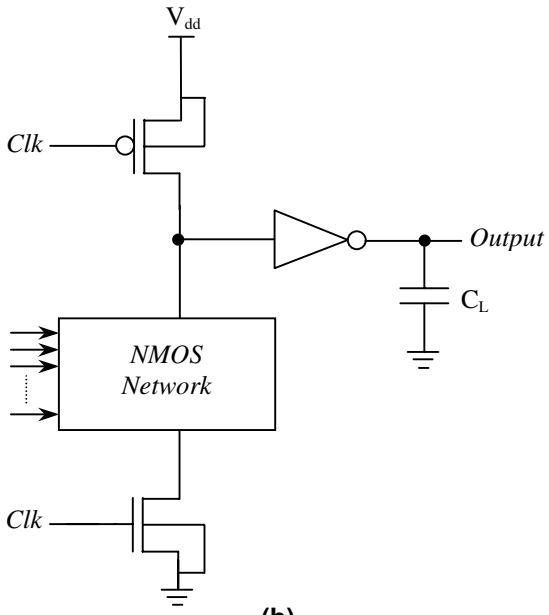
In table 1, the simulated delay of both circuits is shown. Figure 5 shows the simulation results of the B-DTNMOS Domino and the conventional subthreshold Domino in terms of energy and power consumption. Table 1 and Figure 5 both show that the proposed B-DTNMOS scheme outperforms the conventional scheme in both switching speed and energy efficiency; typically, B-DTNMOS Domino is 63% faster and has 37.2% energy savings over the conventional subthreshold Domino scheme at 200 MHz operating frequency.

Table 1. Delay comparison between proposed and conventional subthreshold Domino schemes

	Delay (e-10)
Proposed B-DTNMOS Domino	1.832
Subthreshold Domino	4.946



(a)



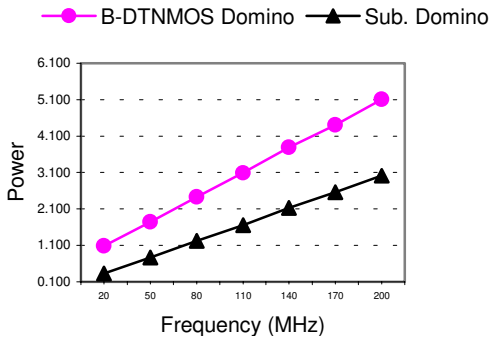
(b)

Figure 4. Domino circuit implemented using (a) proposed B-DTNMOS scheme (b) conventional scheme

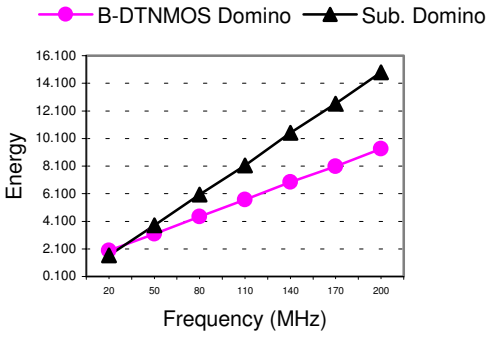
It is seen from figure 5 that B-DTNMOS domino consumes more power than the regular subthreshold domino; this is due to the increased leakage current during the evaluate phase. However, faster switching speeds gained overcomes this drawback to yield to more energy savings in the proposed B-DTNMOS. At low frequencies, below 50 MHz, energy consumption of B-DTMOS becomes comparable to the conventional subthreshold domino, or even higher if you go lower than 25 MHz. The power consumption difference between B-DTNMOS scheme and the conventional scheme increases as the clock frequency is lowered coming to a situation where the speed gain is matched by the power increase loss in the vicinity of 50 MHz; lowering the clock frequency beyond 25 MHz will result in more power dissipation difference, hence higher energy consumption in B-DTNMOS scheme. From the above discussion, the proposed B-DTNMOS scheme must be used for circuits operating above 50 MHz to give the desired performance.

6. Implementing B-DTPMOS with the proposed B-DTNMOS

Faster circuit operation with little increase in power consumption can be achieved if the proposed B-DTNMOS is implemented in dynamic circuits along with B-DTPMOS [3]; B-DTNMOS with B-DTPMOS will be called B-DTMOS hereafter. Figure 6 shows the Domino circuit configuration using B-DTMOS. In table 2, the delays of the conventional subthreshold Domino, proposed B-DTNMOS, and B-DTMOS are shown. Table 2 shows that B-DTMOS is 18.2% faster than B-DTNMOS and 69.7% faster than conventional subthreshold Domino



(a) Power vs. frequency



(b) Energy vs. frequency

Figure 5. Simulation results for the proposed B-DTNMOS Domino and the conventional Domino 1-bit full adder

Table 2. Delay comparison between B-DTMOS, B-DTNMOS, and conventional subthreshold Domino schemes

	Delay (e-10)
B-DTMOS Domino	1.499
B-DTNMOS Domino	1.832
Subthreshold Domino	4.946

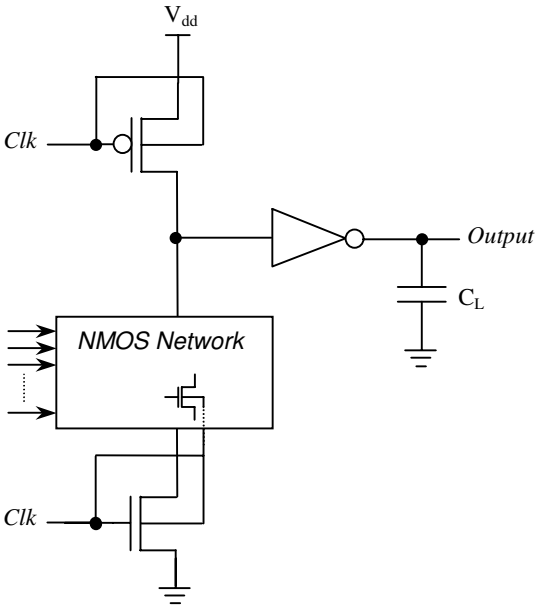
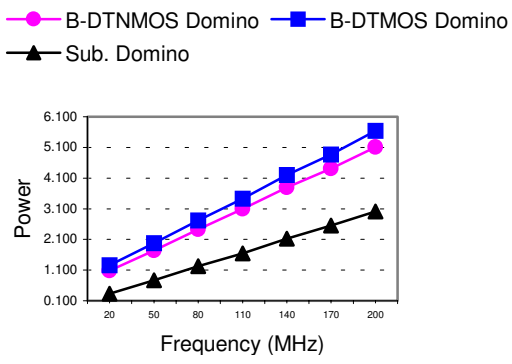
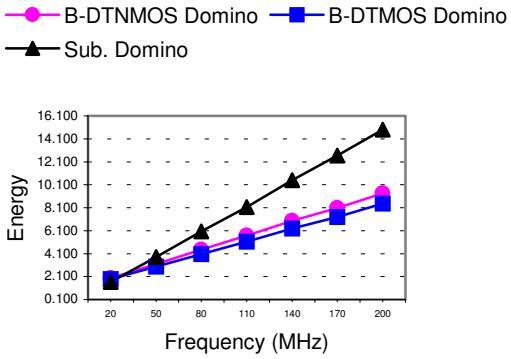


Figure 6. Domino circuit configuration using B-DTMOS scheme

Figure 7 shows simulation results, in terms of power consumption and energy dissipation, for B-DTMOS, B-DTNMOS, and conventional subthreshold Domino circuit configurations. Results show that B-DTMOS that it has a slight increase in power consumption if compared to B-DTNMOS; however, the speed gain overcomes this little shortage yielding to more energy savings. Typically, B-DTMOS has 9.5% energy savings more than B-DTNMOS, and 43.2% energy savings more than the conventional subthreshold Domino. A similar discussion, as the one in section 5, about the comparable energy levels at low operation frequencies can be made for the B-DTMOS.



(a) Power vs. frequency



(b) Energy vs. frequency

Figure 7. Simulation results for B-DTMOS, B-DTNMOS, and the conventional Domino 1-bit full adder

7. Conclusion

In this paper, a new scheme for implementing Bulk Dynamic Threshold N-MOSFET (B-DTNMOS) circuits in Bulk-CMOS technology was introduced. Connecting the system clock in dynamic circuits to the common p-substrate of all the NMOS transistors improves the switching speed and the driving capability of the Domino-like circuits at the cost of a little increase in power consumption if compared with the conventional subthreshold Domino scheme; however, the gained speed overwhelms this power increase yielding to a 37.2% energy savings for the proposed scheme. B-DTPMOS can be combined with the proposed B-DTNMOS to give even more faster operation and higher driving capability with an additional slight increase in power consumption to result in a 43.2% energy savings if compared to the conventional subthreshold Domino scheme. These results make the proposed scheme very favorable in implementing devices that use batteries in their operation where low-energy is the primary concern.

8. References

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