Power Bus Maximum Voltage Drop in Digital VLSI Circuits*

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Abstract

This paper presents a new input-independent method for finding the maximum voltage drop of power bus in digital VLSI circuits. The method relies on expressing the voltage at the power bus nodes in terms of gate currents using sensitivity analysis. Circuit timing information and circuit functionality are used to find maximum simultaneous switching and upper bounds on maximum voltage drop at a given node over a clock cycle. The effects of primary inputs(PIs) misalignment and statistical variation in the circuit delays on maximum voltage drop are automatically included in our method. HSPICE exhaustive simulation results on 3 by 3 and 4 by 4 multiplier are used to validate our work.

1 Introduction

Voltage drop (or surge) in the power bus (or ground bus) of digital VLSI circuits has become a very important issue in modern digital VLSI circuits design. In today's technology, more and more components are put in smaller and smaller area. This makes voltage drop on metal line a serious problem in high performance digital VLSI circuits. The voltage supply of each gate is not constant any more. The speed, noise margin and driving capability are all degraded due to this problem.

The voltage waveform at each node in the power bus is input dependent, it varies from one input vector pair to another. In order to verify that circuit will perform correctly for all input patterns, we can use the worst-case voltage drop waveforms as the supply voltages instead of a constant value. Then estimate the delay and other performances of the system. So a valid and tight upper bound voltage waveform for each node on power bus should be very attractive to every circuit designer.

However! solving this problem is extremely difficult. Firstly, there are 4^n, where n is primary inputs number, possible choices in primary input vector pairs space. It is very impractical to do the exhaustive simulation for the systems which have more than 10 primary inputs. Secondly, the worst-case voltage drop also related to the primary inputs signal misalignment and transition time difference. We will address this problem in more details in the section 6.

A number of techniques have been proposed in the past few years for estimating the voltage (IR) drop in VLSI digital circuit design. The basic idea has been to divide the problem into two parts: circuits part and the power and ground buses part. The circuit is first analyzed to obtain current waveforms drawn by the circuit components or gates at contact points to the bus, assuming constant specified supply voltage, V_{DD}. In general such an approach may require exhaustive simulation under all possible inputs in order to find worst case voltage drop at all nodes in the bus. Such exhaustive simulation could be extremely computationally expensive, if not practically impossible. Instead, the circuit is sometimes simulated for a small set of user specified inputs signals [8,9,10]. However. simulating the circuit for a small set of input signals does not guarantee worst-case voltage drop at the power bus nodes.

In contrast to input-dependent simulation based methods, input-independent fast techniques have been proposed to obtain upper bounds on the worst-case voltage drop. The aim is to obtain upper bounds much fast than input-dependent simulation based method. In [1, 2, 5, 6], all gates or modules in the circuit are assumed to draw maximum current at the same time. The DC current value are then applied to the power bus resistive model to compute upper bounds on maximum voltage drop at all the bus nodes. The technique has been applied in power bus design. Such an approach produces very pessimistic estimates of the voltage drop and wasteful power bus design. The main reason is that not all the gates in the design draw their maximum currents at exactly the same instant.

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An alternative approach($iMax$) has been proposed in [7] that apply timing analysis to obtain the time interval, called uncertainty interval, in which a gate could switch. A maximum current envelope of the gate is assumed to flow during its uncertainty interval. These current envelopes are then applied to the bus resistive model to compute a worst-case voltage waveform envelopes at all bus nodes. Such an approach gives tighter bounds compares to [1,2]. But the bounds can still be too pessimistic. The reason is that not all the gates in a given design switch in a given clock cycle. Even if they do switch, not all of them switch from low to high(LH) or high to low(HL) due to functional dependencies in the design.

In [9], the authors use genetic algorithm to derive an estimate of the maximum instantaneous current and the input vector pairs that cause maximum instantaneous total current flows. In [10], they use the same approach to find the input vector pairs that cause maximum average voltage drop of all the cells in the block. However, it can be easily shown that these input vectors are not necessarily the vectors that cause maximum voltage drops in the bus. In fact, it can be shown that voltage drop at different nodes in the bus are caused by different inputs.

In this paper we present a new approach to compute tight upper bounds on voltage drops in the power bus. We first express the voltage at bus nodes in terms of gate currents using sensitivity analysis. We then apply static timing analysis to obtain the uncertainty switching interval, as in [7]. We then formulate the maximum voltage drop at a node during a time sub-interval(determined by the overlap of the uncertainty intervals of the gates) as an optimization problem that takes into account the functional dependence in the design. The solution of the optimization problem gives the upper bound on the voltage drop in that sub-interval.

The paper is organized as follows. In section 2, the delay and current waveform model of standard cell in benchmark circuit are described. The static timing analysis is applied to get nodes switching interval and gates worst case current envelope. In section 3, the sensitivity analysis is introduced in details. We will consider adding constraint to get more tight upper bound. In section 4, the simulation results showing the primary inputs effect is presented. The exhaustive simulation results are used to validate out work. In section 5, we draw the conclusion.

2 Standard Cell Characterization

As an illustration, we implemented all the MCNC91 benchmark circuits on 0.35μ, 3V technology. Delay parameters and current waveform of each standard cell are characterized from HSPICE sirnulation results. We first describe the gate delay model, then the gate current waveform. The delay characterization method we use is based on the ones proposed in [12, 13, 14].

2.1 *Delay Model*

In [12], an analytical solution for the CMOS inverter output response to an input ramp is presented. The propagation delay is expressed as the sum of step response delay, as a function of load capacitance, and inputs slew rate dependent delay. Both dependencies are almost linear. For complex logic gate, the pin-to-pin delay can also be estimated using this approximation. The propagation delay of an LH output event for an input event at pin i is given by Eq(1):

$$\tau_{LH}^{i} = \alpha_{LH}^{i} + \beta_{LH}^{i} \times C_{load} + \frac{\gamma_{LH}^{i}}{s_{inHL}^{i}} \qquad (1)$$

where α_{LH}^{i} and β_{LH}^{i} are the cell intrinsic delay and the fanout delay for an LH event at the output of the gate due to an event at input i, respectively. s_{inHL}^{i} represents the input slew rate of pin i.Eq(1) gives a good estimation on pin-to-pin delay as long as the input slew is not too large [12]. This is also supported by HSPICE simulation results. Output HL transition delay parameters can be defined in the same way.

The slew rate is defined as the derivative of the voltage waveform at 50% VDD point. The transition time, T_{tr}(rising/falling), equals to $\frac{VDD}{slewrate}$. The gates output transition time depends on which input is active and the total load capacitance value. When input pin i is active, the output transition time T_{trout}^{i} of a gate can be represented by:

$$T_{trout}^{i} = T_{tr0}^{i} + \delta^{i} \times C_{load} \qquad (2)$$

T_{tr0}^{i} is the transition time when the output load equals to 0. 6" is the best fit coefficient. In fact, the output transition time is also a function of input transition time. The complete expression is:

$$T_{trout}^{i} = T_{tr0}^{i} + \delta^{i} \times C_{load} + \eta^{i} \times T_{trin}^{i} \qquad (3)$$

However, HSPICE simulation results show that the contribution of last term is usually smaller than 10%. In order to simplify the problem, we ignore the T_{trin}^{i} term.

2.2 *Current Waveform*

The gate will draw current from power bus when the output has LH transition and inject current into the ground bus when the output has HL transition. Here we explain the characterization of the current waveform drawn by the gate from the power bus. A similar waveform is constructed for the current injected into

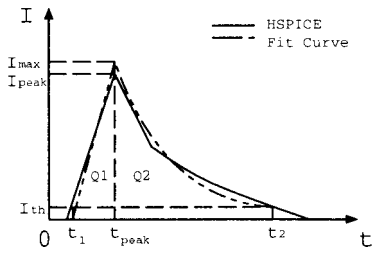

Figure 1: Current Waveform Parameters

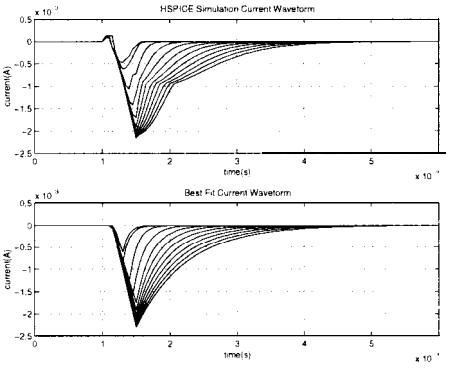

Figure 2: Fit Current Waveform with HSPICE

the ground bus. The shape of current waveform depends on the gate's input vector pair. Because we are interested in the worst case voltage drop on the power bus, it is necessary to find the maximum current envelope(MCE) of each gate. The MCE is not an actual current waveform but rather a envelope waveform that bounds all possible gate current waveforms. This model is different from the current waveform model in [14], which is dependent on the input pattern.

We first determine all the input vector pairs that will cause the gate output to have LH transition, then construct MCE through exhaustive simulation of the individual gate. A typical MCE waveform is shown in Fig. 1. Input transition occurs at time 0. I_{peak} is the MCE peak current value. t_{peak} is the time instant when I_{peak} occurs. Threshold current I_{th} is chosen to determine MCE duration time. At t_1 and t_2, MCE equals to I_{th}, the value of $t_{duration}$ is $t_2 - t_1$. In our work, I_{th} is chosen as 5% of I_{peak}. Because the tail of MCE decrease exponentially, we use exponential function to fit MCE instead of triangular waveform. The charge, which is simply the integration of MCE, can be expressed as:

$$Q = Q_0 + \kappa \times C_{load} + \lambda_i \times T^n_{trin} \quad (4)$$

Q_0 is the charge for intrinsic parasitic capacitance of standard cell. The second term is charge for load capacitance. The third term in the expression is due to short-circuit current. Different inputs have different λ_i. κ and λ_i are best fit parameters.

The duration time, $t_{duration}$, can be expressed as:

$$t_{duration} = t_{duration0} + \sigma \times C_{load} + \psi_i \times T^n_{trin} \quad (5)$$

$t_{duration0}$ is the duration time when output load equals to 0 and the input is a step function. σ and ψ_i are the best fit parameters. In [14], they only considered load capacitance in the duration time expression. We have found that the input transition can't be ignored for accurate estimation. Using NAND2 gate as example, a $100fF$ load capacitance difference will cause $434ps$ variation in duration time. The $0.5n$ difference at the input pin A's transition time will cause $156ps$ variation in duration time.

Similarly, we will also consider both load capacitance and input transition time effects on peak current occurring time instant estimation.

$$t_{peak} = t_{peak0} + max(\phi \times C_{load}, t^{sat}_{peak}) + \chi_i \times T^i_{trin} \quad (6)$$

When the load capacitance is very large, t_{peak} stops increasing with C_{load}. So we apply piecewise linear approximation. All the parameters are chosen to give the best fit with HSPICE simulation results.

As shown in Fig. 1, the effective maximum value for the fit current waveform, I_{max}, is determined by solving following equations:

$$\begin{cases} Q_1 = \frac{1}{2}(t_{peak} - t_1) I_{max} \\ Q2 = I_{max}(\int_{t_{peak}}^{\infty} e^{-\frac{(t - t_{peak})}{\tau}} dx) \\ Q = Q_1 + Q_2 \\ I_{th} = I_{max} e^{\frac{t_2 - t_{peak}}{\tau}} \end{cases} \quad (7)$$

The solution is:

$$\tau = \frac{t_{duration} - t_{peak}}{\ln 20} \quad (8)$$

and.

$$I_{max} = \frac{Q}{\tau + 0.5(t_{peak} - tl)} \quad (9)$$

Fig. 2 shows the NAND2 gate current waveforms obtained by our characterization method as compared to HSPICE simulation results. Different curves correspond to different load capacitance.

2.3 *Worst Case Current Envelope*

In a given circuit, each gate can only switch within a certain time interval. An interval at the output of a gate can begin or end at time t only if there is an interval beginning or ending at time $t - \tau^i$ at its input i. Using Eq(4) to (9), we can also find the gate possible transition MCEs. Because the gate may switch at any time instant within the interval, we can

derive the worst case current contribution of the gate due to the uncertainty interval by taking the envelop of all the transition MCEs. This is the basic idea used in the *iMax* algorithm in [7].

3 Maximum Voltage Drop Computation

After static timing analysis, the worst case current envelope of all the gates are available. The maximum IR voltage drop on the power bus can be determined by solving the linear power bus conductance matrix.

$$\mathrm{Yv} = \mathbf{i} \tag{10}$$

Y is conductance matrix of power bus network, v is the vector of bus node voltages, i is the vector of gate current sources connected to the nodes on the power bus. If a gate is connected to node j, then the jth element of i, I_j, is the worst case current envelope due to this gate. If no gate is connected to this node, I_j equals to 0. In [7], Eq(10) is solved to find an upper bound on the maximum voltage drop by applying the MCE of all the gates during their respective uncertainty interval. However, this upper bound can be shown to be too pessimistic.

Assume there are totally n nodes on the power bus, *m* of them are connected to the gates. The maximum IR voltage drop waveform of node j can be written in the form:

$$V_j(t) = \sum_{i=1}^{n} \varepsilon_{ij} I_i(t) \tag{11}$$

We define ε_{ij} as node j's sensitivity to gate i. Node j's sensitivity vector $\varepsilon_{\mathbf{j}}$ can be found in the following way:

$$V_j = \mathbf{e_j^T v} \tag{12}$$

where $\mathbf{e_j^T}$ is a unit vector,

$$e_{ij} = \begin{cases} 1 & \text{if } i = j \\ 0 & \text{else} \end{cases} \tag{13}$$

Using Eq(10) and (12):

$$V_j = (\mathbf{e_j^T Y^{-1}})\mathbf{i} \tag{14}$$

Let $\mathbf{e_j^T Y^{-1}}$ equal to the sensitivity vector $\varepsilon_{\mathbf{j}}^{\mathbf{T}}$. Then we just solve the following linear equation to find $\varepsilon_{\mathbf{j}}^{\mathbf{T}}$.

$$\mathrm{Y\&j} = \mathbf{e_j} \tag{15}$$

Here we used the fact that Y = $\mathbf{Y^T}$.

From Eq(11) we see that the voltage is related to the gate currents through the parameters ε_{ij}. The gate currents $I_i(t)$ may flow only during a subinterval of the clock cycle that is determined by the gate's uncertainty interval. Whenever the gate switches within that interval. We thus divide the clock cycles into intervals determined by the overlapping of the gate's uncertainty intervals. In each interval, Eq(11) together with the circuit functional relationships are used to formulate an optimization problem to determine which gate may switch simultaneously from

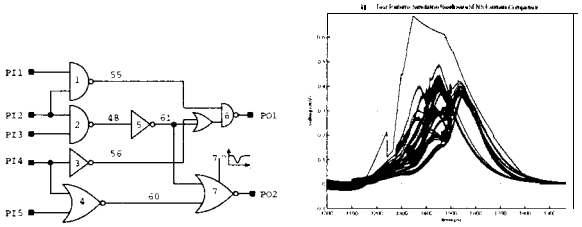

Figure 3: (a) C17 Benchmark Circuit (b) All Test Pattern Simulation Result

Low to High (or High to Low) which maximizes V,(t) within that interval. The optimization problem is mapped into a constraint graph optimization problem. An edge between two vertices in the constraint graph implies that the corresponding vertices can't simultaneously have contribution to the voltage drop on the specified node. Hence the problem of finding the maximum voltage drop contributed by a set of gates in an interval reduces to problem of finding a set of vertices in the constraint graph such that the sum of the weights on the vertices is maximum and there are no edges between any pair of the vertices. The algorithm details about how to solve constraint graph. and how to construct constraint graph from logic implication list can be found in [15,16].

4 Simulation Result

4.1 *Primary Input Effect*

One way to find the maximum voltage drop of one node is through exhaustive simulation. Run simulation for every possible input vector pair, and choose the maximum value at each time step. Usually, the signals at all primary inputs are assumed to have fixed slew rate and switch at the same time instant. But in practice primary inputs of a combinational block are connected to the output of some latches. Due to clock skew and load difference, the output signal of the latches may be misaligned and have different slew rates. This will affect the voltage drop on the power supply for each gate in the block and the total instantaneous peak current drawing by the power bus. This problem has never been addressed because there are infinite possibilities. Statistical techniques can be applied in this situation, but it will become very inefficient for the circuits with a large number of inputs.

Here we use benchmark circuit Cl7 as an example: the circuit is shown in Fig. 3(a). We will analyze the maximum voltage drop on node 7, the power supply connection of gate 7, using our simulator VMAX. The result is shown in Fig. 3(b). From $1300ps$ to $1600ps$, only gates 2, 6 and 7 have contribution to the volt-

age drop. We derived all the 52 possible input vector pairs (test patterns), which can cause nodes PO1, PO2 and 48 have low to high transition, from Cl7 binary decision diagram [17]. All the 52 test patterns simulation results are compared with VMAX estimation in Fig. 3(b). The worst test pattern which results the maximum instantaneous voltage drop is shown in Fig. 4. We can also use the algorithm in [8] to find this worst pattern. For comparison purposes, we also choose two other test patterns in Table 1 to do the optimization analysis.

Table 1: Three Test Patterns

Test Pattern	PI1	PI2	PI3	PI4	PI5
I	LH	HL	HL	LH	LH
II	LH	H	HL	LH	L
worst	L	HL	HL	LH	L

To account for the statistical variation, we run HSPICE optimization simulation by varying primary inputs' transition time and switching time instant. The optimization result for pattern I and II is shown in Fig. 4. The maximum misalignment is $0.5ns$.

The CPU time of VMAX to find maximum voltage waveform is 1.51 seconds. Cl7 regular simulation takes 3.2 CPU seconds for each test pattern. The average CPU time for Cl7 optimization simulation is 291.1 seconds for each test pattern.

4.2 Multiplier Exhaustive Simulation

We also implemented a 3 by 3 and a 4 by 4 multipliers using the same technology, with 102 and 200 gates, respectively. After exhaustive simulation, the maximum voltage drop of each node connected to gate is known. An arbitrary gate power supply node is then chosen from 3 by 3 multiplier. Its maximum voltage waveform envelope from exhaustive simulation result compared with VMAX result in Fig. 5.

From the figure, we can see that the maximum voltage drop predicted by VMAX is about 2.5 times larger than what is predicted by exhaustive simulation. The reason for this overestimation is the following. In computing the maximum voltage drop waveform, we assume that the gates that could switch in a given time interval, do switch simultaneously, that is, at exactly the same time. In practice: however: for a given gate delay assignment and a given primary input switching time alignment, these gates may not switch exactly at the same time. It is possible that by introducing gate delay statistics and by changing the primary input switching times, the voltage drop could approach the bound set by VMAX.

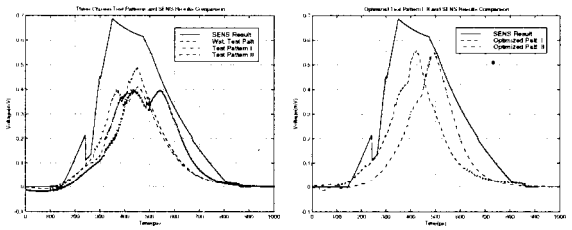

Figure 4: Primary Inputs Misalignment and Slew Effect

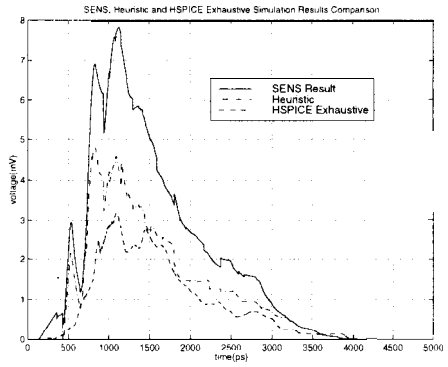

Figure 5: HSPICE Exhaustive and VMAX Comparison

Alternatively. one could assume that a certain fraction of simultaneous gate switching occurs. For example, if we assume that $1/3$ of the gate that are predicted by VMAX to switch simultaneously in a given interval do switch, one obtains a tighter upper bound as shown in Fig. 5. However, as mentioned above, such an upper bound may not hold if statistical variations are included.

The CPU time of VMAX to find maximum voltage drop waveform is 31.43 seconds. Heuristic method simulation takes the same amount of time. Because there are 6 primary inputs, we need to run HSPICE simulation 4096 times, each of them takes 73.2 CPU seconds. The total CPU time of exhaustive simulation is 2.99 x 10^5 seconds.

5 Conclusion

In this paper, we presented a sensitivity analysis based algorithm for estimating the maximum voltage drop on power bus. By using MCE as current model for standard cell and doing sensitivity analysis in our work, the primary inputs effects on worst case voltage are also included in the results. The simulator VMAX can estimate the worst case voltage waveform in a fast and accurate way. This waveform can be applied to the gates later in order to find the effect of voltage drop on power bus to circuit performance.

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