A Gated Clock Scheme for Low Power Scan Testing of Logic ICs or Embedded Cores

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Abstract

Test power is now a big concern in large System-on-Chip designs. In this paper, we present a novel approach for minimizing power consumption during scan testing of integrated circuits or embedded cores. The proposed low power technique is based on a gated clock scheme for the scan path and the clock tree feeding the scan path. The idea is to reduce the clock rate on scan cells during shift operations without increasing the test time. Numerous advantages can be found in applying such a technique.

1. Introduction

The System-on-Chip (SOC) revolution has brought some new challenges to both design and test engineers. Among these challenges, the power dissipation is one of the most important issues [1]. Generally, a circuit may consume more power in the test mode than in the normal mode due to the following reasons [2]. First, the design-for-testability (DFT) circuitry embedded in a circuit to reduce the test complexity is often idle during normal operations but may be intensively used in the test mode. Second, the test efficiency has been shown to have a high correlation with the toggle rate; hence in the test mode, the switching activity of all nodes is often several times higher than the activity during normal operations. Third, in a SOC, parallel testing is frequently employed to reduce the test application time, which may result in excessive energy and power dissipation. This increased test power may be responsible for cost, reliability, performance verification, autonomy and technology related problems. A survey of these problems is given in [3].

Until now, ad hoc solutions have been practiced in industry for considering test power. These solutions consist in oversizing power supply, package and cooling to stand the increased current during testing, or reducing the test operation frequency. Unfortunately, these solutions increase either hardware costs or test time, and may lead to a loss of defect coverage as dynamic faults may be masked. Thereby, a number of academic solutions have been proposed recently to cope with the power and energy problems during test. Test scheduling algorithms satisfying power constraints were presented in [4]. Low power BIST test pattern generators were proposed in [5-7]. Pattern suppression techniques [8,9] and circuit partitioning techniques [10] were also proposed. Low power ATPGs and vector ordering techniques were presented in [11,12] and [13,14] respectively. A static compaction technique to control power dissipation [15], a scan path segmentation technique [16], and an interleaving scan architecture for multiple-scan circuits [17] were also proposed.

The focus of this paper is on the problem of minimizing power dissipation during scan testing. There are three main sources of power dissipation during scan testing. One is the power dissipated when the outputs of logic gates in the circuit switch, which is referred to here as "logic power". Another is the power dissipated in the scan path during scan operation, which is referred to here as "scan power". The last one is the power dissipated in the clock tree each time the clock makes a transition, which is referred to here as "clock power". Therefore, the total power during scan testing includes the logic power, the scan power and the clock power. The previously proposed approaches have all focused on reducing the logic power and/or the scan power, but did not do anything to reduce the clock power. Results in [18] suggest that clock power is a significant component of the total power during testing. In this paper, we propose an approach that reduces logic power, scan power and clock power at once. The proposed low power scan architecture is based on a gated clock scheme for the scan path and the clock tree feeding the scan path. The idea is to reduce the clock rate on the scan cells during shift operations without increasing the test time. For this purpose, a clock whose speed is half of the normal speed is used to activate one half of the scan cells during one clock cycle of the scan operation. During the next clock cycle, the second half of the scan cells in the scan path is activated by another clock whose speed is also half of the normal speed. The two clocks are synchronous with the system clock and have the same but shifted in time period during scan operations. During capture operations, the two clocks operate as the system clock. The use of such a modified clock scheme lowers the transition density in the circuit under test (CUT), the scan path and

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the clock tree feeding the scan path during scan operations. Consequently, the switching activity in a time interval (*i.e.* the average power) as well as the peak power consumption are minimized. Note that the idea of reducing the clock rate without increasing the test time has already been proposed in [19] in the context of BIST.

Compared with existing low power scan architectures, our solution offers a number of advantages. The fault coverage and the IC test time are exactly the same as those achieved with a conventional scan architecture. This is because the test patterns derived with a standard scan architecture are directly reusable with the low power scan architecture. The area overhead is negligible and there is no penalty on the circuit performance compared with a conventional scan architecture. The proposed approach does not require any circuit design modification beyond standard scan testing and is very easy to implement. Reductions of logic power, scan power and clock power are up to 46%, 48% and 53% respectively for experimented ISCAS benchmark circuits. Note that the methodology described in this paper can be used for full scan cores or ICs having one or multiple scan chains.

The remainder of the paper is organized as follows. In the next section, we give some definitions about power and energy. In Section 3, we detail the new clock scheme proposed for low power scan testing. Section 4 describes the proposed low power scan architecture. Results obtained on the benchmark circuits are reported in Section 5.

2. Terminology

As discussed earlier, one of the current concerns, which may turn into a major engineering problem in the future of SOC development, is test power. As both the SOC designs and the deep-submicron geometry become prevalent, the hugeness of designs, the tightening of timing constraints, the rising of frequencies, and the lowering of applied voltages all affect the power consumption systems of silicon devices. These concerns involve energy, average power, peak power, instantaneous power and thermal overload. Below are some definitions [18].

Energy: the total switching activity generated during test application. Energy has impact on the battery lifetime during power up or periodic self-test of battery operated devices.

Average Power: the total distribution of power over a time period. The average power is given by the ratio between the energy and the test time. Elevated average power adds to the thermal load that must be vented away from the device under test. It may cause structural damage to the silicon (hot spots) or to the package.

Instantaneous Power: The value of power consumed at any given instant. Elevated instantaneous power may overload the silicon or package power distribution systems, and brown-out phenomena may occur.

Peak Power: the highest value of power at any given instant. The peak power determines the thermal and electrical limits of components and the system packaging requirements.

In the following, we propose an approach that reduces all components of the power involved during scan testing.

3. The low power scan architecture

3.1 Conventional scan architecture

Figure 1 illustrates a conventional scan architecture that an IC or a core can be configured into during test. In the normal functional configuration, the circuit can be a combinational or sequential logic. In the test configuration, it appears as shown in Figure 1. The scan architecture includes a scan path, the circuit under test (CUT), and the connections to the tester (scan input, scan output, control input). The scan path is formed by the connections between the scan input and the scan output of each scan cell.

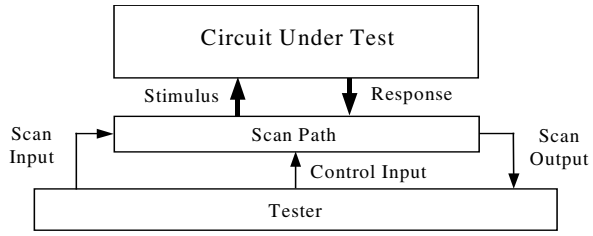

Figure 1: Conventional scan architecture

The tester provides a deterministic sequence of bits which are fed into the scan path. The content of the scan path serves as a test pattern for the CUT. A test pattern is applied every m+1 clock cycles, where m is the number of scan cells in the scan path. The response of the CUT is captured by the scan path in parallel, and is serially scanned out during the next m clock cycles to be loaded in the tester; the next test pattern is scanned in concurrently.

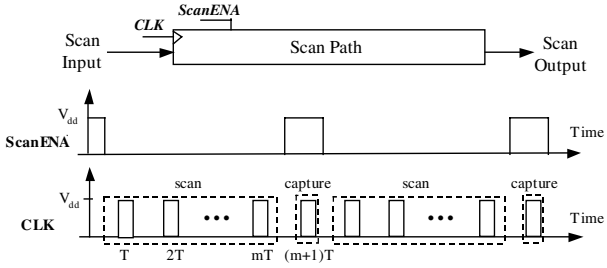

Figure 2: Timing waveforms of standard scan testing

As in any scan design, each scan cell in the scan path consists of a multiplexer connected to a D flip-flop. The D flip-flop is clocked by signal CLK. Signal CLK is the clock of the circuit in the system mode and has a period equal to T. The multiplexer is controlled by signal ScanENA and allows to drive either test response data from the logic circuit (Capture Mode) or shift data from

the scan input of the scan cell (Scan Mode) to the D flip-flop. Signal ScanENA is operated by the tester.

Figure 2 shows the timing waveforms of signals CLK and ScanENA provided by the tester during scan and capture operations. A logic zero on signal ScanENA in combination with signal CLK causes stimulus data to be shifted into the scan path while response data is shifted out from the scan path. A logic one on signal ScanENA in combination with signal CLK causes response data from the logic circuit to be captured into the scan path. According to this functioning, it clearly appears that most switching activity in the circuit occurs during scan shifting. In fact, it has been shown that for circuits with a long scan path, the shift operation contributes to more than 99% to the logic power dissipation during test [20]. Hence, average and peak power dissipation in a scan-based environment can be reduced by first reducing the switching activity during scan operation. This reduces both the logic power and the scan power. Next, the power dissipation can still be reduced by reducing the clock power in the clock tree feeding the scan path.

3.2 Proposed low power scan architecture

Today, several test synthesis tools exist that can automatically synthesize and insert scan architectures into ICs. The method described below provides a way of adapting synthesized scan architectures to achieve a low power mode of operation. The process of adapting scan architectures for low power operation is achieved by (1) simply modifying the clock scheme for the scan path and (2) inserting a single multiplexer to scan out test responses to the tester. As depicted in Figure 3 and Figure 4, the proposed low power scan architecture is based on a new clock scheme for the scan path and the clock tree feeding the scan path. The idea is to reduce the clock rate on the scan cells during shift operations without increasing the test time. For this purpose, a clock whose speed is half of the normal speed is used to activate one half of the scan cells (referred to as "Scan Path A") during one clock cycle of the scan operation. During the next clock cycle, the second half of the scan cells (referred to as "Scan Path B") is activated by another clock whose speed is also half of the normal speed. The two clocks are synchronous with the system clock and have the same but shifted in time period during scan operations (the clocks are phase shifted). During capture operations, the two clocks operate as the system clock CLK. The use of such a clock scheme lowers the transition density in the CUT, the scan path and the clock tree feeding the scan path during scan operations.

Let us consider again a CUT with *m* inputs. A scan path composed of *m* scan cells and driven by a clock CLK would be used in standard scan testing (Figure 2). Here, the conventional scan path is replaced by two new scan paths (Scan Path A and Scan Path B), each of them being composed of *m/2* scan cells and driven by one of the two clocks CLK/2 and CLK/2^{σ} (Figure 3). As one can observe in Figure 4, a shift operation is performed at each clock cycle of the scan operation. However, Scan Path A and Scan Path B are never active simultaneously. During the first clock cycle, a value provided by the tester is serially loaded into Scan Path A through the use of signal CLK/2. Scan Path B is in stand-by mode. During the next clock cycle, another value is serially loaded into Scan Path B through the use of signal CLK/2^{σ}. Scan Path A is in stand-by mode. As only half of the inputs may have a transition at each clock cycle, the average power consumed in the CUT is minimized. Moreover, the power consumed in the scan path is minimized since only half of the scan cells in the scan path may be activated in a given time interval.

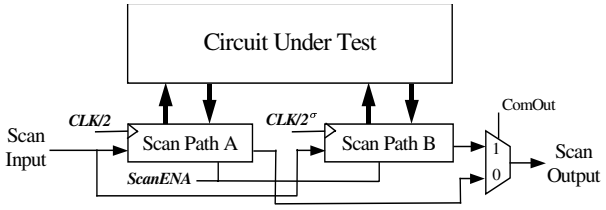

Figure 3: Proposed low power scan architecture

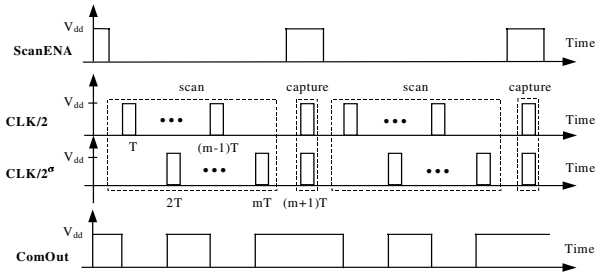

Figure 4: Timing waveforms of the proposed scan scheme

In the proposed low power scan architecture, the serial input of each scan path (Scan Path A and Scan Path B) are connected together and to the tester. The serial outputs of the two scan paths are connected to a multiplexer which drives either the content of Scan Path A or the content of Scan Path B to the tester during scan operations. As Scan Path A and Scan Path B must be scanned out alternatively during scan operations, the multiplexer has to switch at each clock cycle of the scan operations. Signal ComOut which controls the MUX has been designed to allow such a mode of operation. It is obtained from the test clock module described in Section 4.

3.3 Scan path adaptation

In a conventional scan architecture, the scan path receives stimulus frames from the tester and outputs response frames to the tester. In order to avoid having to modify these stimulus and response frames, and hence lessen the effort required to adapt a conventional scan architecture into the proposed scan architecture, the following scan path adaptation has to be applied.

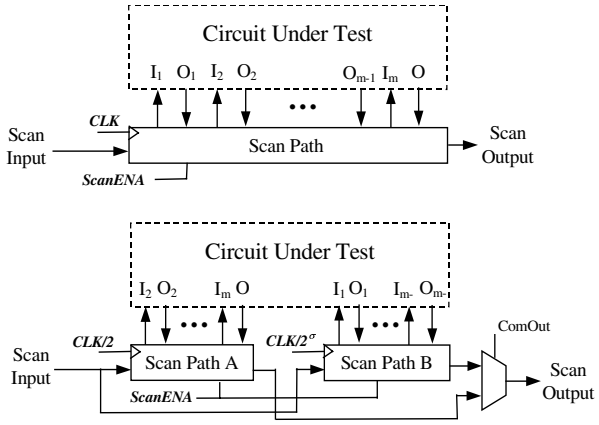

Figure 5: Scan path adaptation for low power

Let us consider the conventional scan path and its connections to the CUT shown on the top of Figure 5. When scanning in a deterministic test vector into the scan path, the first (last) value uploaded is the last (first) bit of the corresponding test vector. Similarly, when scanning out the test response from the scan path, the first (last) value downloaded is the last (first) bit of the test response vector. In the proposed low power scan architecture, the connections between the scan path and the CUT are as shown at the bottom of Figure 5, *i.e.* input I_1 is connected to Scan Path B, input I_2 to Scan Path A, input I_3 to Scan Path B, and so on until input I_m. Similarly, output O_1 is connected to Scan Path B, output O_2 to Scan Path A, output O_3 to Scan Path B, and so on until output O_m. As the bits provided from (to) the tester are alternatively loaded into (from) Scan Path A and Scan Path B during scan operation, this connecting scheme allows the deterministic test patterns calculated with a conventional scan architecture to be fully reusable with the low power scan architecture.

4. Design of the low power clock scheme

The complete low power scan structure proposed in this paper is depicted in Figure 6. This structure is first composed of a test clock module which provides test clock signals CLK/2 and CLK/2^σ from the system clock CLK used in the normal mode. Signal ScanENA allows to switch from the scan mode (=0) to the normal or capture mode (=1). Signal ComOut controls the MUX allowing to alternatively output test responses from Scan Path A and Scan Path B during scan operations. As two different clock signals are needed for the scan paths, two clock trees are used in the proposed scan scheme. These clock trees are carefully designed so as to correctly balance the clock signals feeding each part of the modified scan path. Finally, the two scan paths, Scan Path A and Scan Path B, stemmed from the segmentation of the original scan path, are connected to the CUT.

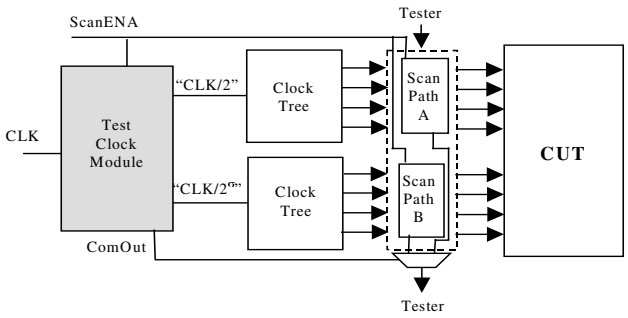

Figure 6: The complete low power scan structure

The test clock module which provides the control signal ComOut and the test clock signals CLK/2 and CLK/2^σ from the system clock CLK is given in Figure 7. This module is formed by a single D-type flip-flop and six logic gates, and allows to generate non-overlapping test clock signals (during the scan operation mode) as those represented in Figure 4. This structure is very simple and requires a small overhead of hardware. Moreover, it is designed with minimum impact on performance and timing. In fact, some of the already existing driving buffers of the clock tree have to be transformed into AND gates as seen in Figure 7. These gates mask each second phase of the fast system clock during shift operations.

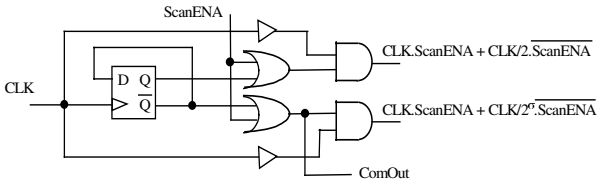

Figure 7: The test clock module

As two different clock signals are used by the scan paths, the clock tree feeding the scan paths has to be modified. In the proposed structure, two clock trees are therefore implemented, each of them with a clock speed which is half of the normal speed (CLK/2 and CLK/2^σ). Let us consider an example scan path composed of six scan cells and segmented into two scan paths in the proposed scan architecture. The corresponding clock trees in the test mode are depicted in Figure 8.a given below. Each of them has a fanout of 3 and is composed of a single buffer. During the normal mode of operation, the clock tree feeding the input register at the normal speed can therefore be easily reconstructed as shown in Figure 8.b. Note that using two clock trees driven by a slower clock (rather than a single one) allows to further drastically reduce the power consumption during scan testing. Since the clock tree usually requires a significant amount of power in a system, this reduction cannot be obtained by standard scan techniques targeting only the CUT and/or the Scan Path.

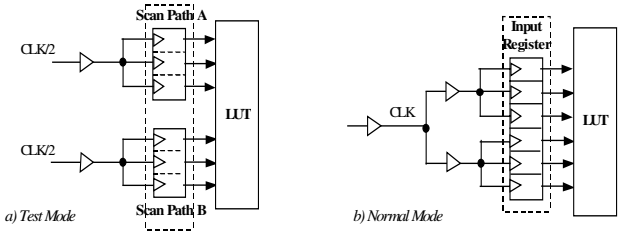

Figure 8: The clock tree in test mode and normal mode

The use of such a modified clock scheme lowers the transition density in the CUT, the scan path and the clock tree feeding the scan path. Saving in power consumption comes from the reduction of the switching activity in all these parts. Compared with existing low power scan techniques, our solution offers numerous advantages. The fault coverage and the IC test time are exactly the same as those achieved with a standard scan architecture. The area overhead, which is due to the test clock module and the routing area of the segmented scan path, is negligible. The proposed architecture does not require any further circuit design modification and is very easy to implement. It therefore has a low impact on the system design time and has nearly no penalty on the circuit performance.

5. Experimental results

The benchmarking process described here was performed on circuits of the ISCAS'85 and ISCAS'89 (full scan version) benchmark suites. Power consumption in each circuit was estimated by using PowerMill, a dynamic simulator provided by Synopsys [21], assuming a clock frequency equal to 200 MHz and a power supply voltage of 2.5 V. Experiments performed on each circuit have been done with technology parameters extracted from a 0.25μm digital CMOS standard cell library. The goal of the experiments we performed has been to measure the savings in logic power, scan power and clock power.

A first comment on these results is that biggest benchmark circuits have not been experimented. The reason is that the simulation time taken by PowerMill would be too long on these circuits. For example, experiments on circuit s15850 (which has 611 inputs in full scan version) have shown that 292 patterns are needed to achieve 100% of stuck-at fault coverage. The time taken by PowerMill to simulate one test pattern is 2448 seconds. This time is huge because PowerMill actually performs 612 simulations per test pattern during scan testing. According to that, 16 days of CPU time would be needed to completely simulate circuit s15850.

In the following experiments, deterministic test sequences provided by the ATPG tool "TestGen" of Synopsys [22] were used. *The test length and fault coverage of these sequences are not reported here because they are exactly the same as those obtained with a standard scan architecture*.

Now, results of the power savings achieved by the proposed technique are discussed. Results of the logic power are summarized in Table 1. For each circuit, we have reported the peak power and the average power, first with a standard scan structure (first part of Table 1) and next with the proposed low power structure. Peak power and average power are expressed in milliWatts. The last part in Table 2 shows the reduction in peak power and average power dissipation expressed in percentages. These results on benchmark circuits show that average power reduction of up to 46% and peak power reduction of up to 29% can be achieved with the proposed technique.

Circuit	peak [mW]	power [mW]	peak reduct	power reduct
c3540	142.3	10.5	16.7 %	33.9 %
c5315	214.2	15.5	29.0 %	33.8 %
c6288	295.3	42.8	9.2 %	20.5 %
c7552	437.9	23.3	13.2 %	40.1 %
s1196	68.3	2.2	7.6 %	33.1 %
s1423	80.2	2.7	14.2 %	46.7 %
s1488	82.7	4.6	-	26.9 %
s5378	266.7	8.6	7.7 %	37.5 %

Table 1: Power savings in the CUT (logic power)

An important comment on these results is that the peak power reduction appears to be irregular and sometimes poor. This is due to the fact that in some cases, the highest current in the CUT appears during application of the test pattern and capture of the corresponding response. As this operation is similar in both low power scan and standard scan testing, the reduction in peak power appears to be low. In fact, it is higher than it appears. The reason is that an elevated current consumed in a design can cause damage to the circuit if it occurs during more than one clock cycle. As the switching activity is reduced in the clock cycles preceding and following the capture clock cycle, the peak power in the proposed scheme is in fact much lower than the peak power in a standard scan.

Although the power consumed in the scan path is normally lower than the power consumed in the CUT, it may be attractive when testing circuits with a high number of inputs. In this case, the number of scan cells is high, and the scan power may represent a significant portion of the total power consumption. In order to evaluate the savings in scan power, we performed another set of experiments. The same electrical and technological parameters as those utilized to evaluate the logic power were used. Results are reported in Table 2. As can be seen, these results show that our low power technique reduces by roughly one half the average scan power. As we cannot handle sequential logic elements such as Dff with our version of PowerMill, the evaluation of the average scan power was performed from an estimated value of the power consumed in each scan cell during testing. This estimated value has been calculated by using HSPICE and by counting the average

number of transitions in a scan cell during one clock cycle of the test session. The peak power consumption has not been evaluated.

Circuit	Standard Scan	Low Power Scan Testing	
	Power [mW]	Power [mW]	Power Reduct
3540	0.16	0.09	43.3 %
c5315	0.54	0.30	43.9 %
c6288	0.07	0.04	41.2 %
c7552	0.66	0.34	48.0 %
s1196	0.11	0.06	46.3 %
s1423	0.29	0.15	45.7 %
s1488	0.03	0.02	32.0 %
s5378	0.67	0.38	42.9 %

Table 2: Power savings in the scan path (scan power)

Results reported in Table 2 show that average power reduction of up to 49% can be achieved by using the proposed low power technique. Even if the intrinsic values of the scan power are considerably lower as those of the logic power (this is due to the fact that we experimented circuits with few inputs), the percentage of reduction is undoubtedly an interesting information.

Circuit	peak [mW]	power [mW]	peak reduct	power reduct
c3540	64.9	0.87	-	24.3 %
c5315	270.0	4.19	21.1 %	48.8 %
c6288	55.9	0.83	-	6.1 %
c7552	169.1	3.84	53.6 %	53.0 %
s1196	26.36	0.31	25.7 %	64.7 %
s1423	100.4	1.08	-	49.5 %
s1488	100.40	1.08	-	49.5 %
s5378	362.4	5.22	-	34.1 %

Table 3: Power savings in the clock tree (clock power)

Reducing the clock power is an important issue since it represents a significant portion of the total power consumed during test [18]. The proposed low power technique reduces the switching activity in the clock tree as illustrated Section 4. In order to evaluate the savings in clock power, we performed a new set of experiments. Results are reported in Table 3. These results are based on a simple clock tree design with one buffer (or inverter) feeding 4 buffers in the next level. Note that this value is important from a design point of view but is not really important in our evaluations which have a comparison purpose. Actually, another value of the fanout would provide different intrinsic values of the power, but would provide roughly the same ratio between power in the proposed scheme and power in a standard scheme compared with those presented in Table 3.

These results on benchmark circuits show that average power reduction of up to 64% can be achieved in the clock tree by using the proposed low power technique. These percentages are evaluated in comparison with a standard scheme in which a single clock speed is used for the scan path. Note that results in terms of peak power reduction still appear to be irregular as those obtained for logic power.

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