Coping with Buffer Delay Change Due to Power and Ground Noise

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ABSTRACT
Variation of power and ground levels affect VLSI circuit performance. Trends in device technology and in packaging have necessitated a revision in conventional delay models. In particular, simple scalable models are needed to predict delays in the presence of uncorrelated power and ground noise. In this paper, we analyze the effect of such noise on signal propagation through a buffer and present simple, closed-form formulas to estimate the corresponding change of delay. The model captures both positive (slowdown) and negative (speedup) delay changes. It is consistent with short-channel MOSFET behavior, including carrier velocity saturation effects. An application shows that repeater chains using buffers instead of inherently faster inverters tend to have superior supply level-induced jitter characteristics.

Categories & Subject Descriptors:
J.6 [Computer-Aided Engineering]: Computer-aided design (CAD).

General Terms:
Algorithms.

Keywords:
Power and ground noise, differential mode noise, common mode noise, incremental delay change.

1. INTRODUCTION
This paper describes a new model for the change in buffer delay caused by both power and ground supply level variations and level variations between stages in sequences of repeaters. These delay changes are a large component of the total timing jitter for a signal where the jitter accounts for all noise sources such as substrate noise and coupling noise as well as power level noise. There is a substantial amount of previous work in this area, notably papers: [3][5][10]. However, for several reasons described below, we believe that the problem bears re-examination and an effort made to create a fast, simple model suitable for mass implementation in a modern design flow.

Growth in design sizes and scaling of interconnections have lead to the requirement for insertion of very large numbers of buffer/ repeaters in recent designs [1][7]. Because of their preponderance in number, use in heavily loaded nets, and use in clock and timing circuits, buffer delays account for a large percentage of all critical timing nets in a design. In some of these applications, total timing uncertainty (not just worst case delay) is important. At the same time, scaling of power supply levels and improving transconductance of devices have increased the sensitivity of buffers to supply level induced delays. Finally, increases in chip-level design scales and modern packaging strategies such as bump bonding have localized supply variations so that buffers in one set of supply levels are driving buffers in another zone with differing supply levels. Since power loading is logic switching dependent and supply sources are localized, power and ground levels need not be inversely correlated as is typical in wire bonded die.

Under such conditions, power level induced delay changes may either increase or decrease the effective delay of a buffer, and successive stages may or may not accumulate incremental delays. One must consider both power and ground levels at the signal source and at the current buffer to derive an equivalent delay change. This value can be substantially smaller than that predicted by superposing ground-bounce and power level changes [3][11][12]. Second, the delay effects of *common mod*e voltage shifts will be shown to be larger in scale to equivalent differential mode changes. (Differential mode voltage shifts are the commonly studied model). Lastly, changes in power distribution and clocking strategies and the potential for future changes, create the need for a timing model which is independent of common assumptions about power level noise sources. We *do* assume that large scale power level changes result from ensemble effect of many devices and occur at a somewhat slower time scale than the typical switching changes in buffers.

In the following, we analyze the effect of P/G noise on buffer delay, and present linear, closed-form formulas for the corresponding incremental changes in delay based on a short-channel transistor model. The expressions simultaneously model both the power supply and ground levels, resulting in positive (slowdown) or negative (speedup) delay changes. They are suitable for estimation of both upper and lower bounds on signal arrival time. Furthermore, they are shown to be largely independent of the buffer load circuit structure, increasing their applicability. These expressions are suitable for inclusion in timing analysis tools and to statistical delay estimators due to their rapid evaluation. Lastly, the expressions make no assumptions about the specific shape of the P/G noise waveform.

The paper is organized as follows: sections 2-3 defines P/G noise, buffer delay nomenclature and illustrate P/G induced buffer delays. Section 4 presents the new model. Section 5 demonstrates the accuracy and fidelity of the model. Applications of the model and concluding remarks are presented in sections 6-7.

2. BUFFER DELAY CONVENTIONS
A *buffer* is a chain of tapered inverters. Here, we consider buffers consisting of one or two inverters.

2.1 Variation of V_{dd} and V_{ss}
We use V_{dd}, V_{ss}, V_i (input), etc. to represent voltages related to ideal power and ground levels, and V_{dd}', V_{ss}', V_i', etc. to represent corresponding values in the presence of power and ground noise. ΔV_{dd} and ΔV_{ss} denote the variation of power and ground levels, respectively.

$$\Delta V_{dd} = V_{dd}' - V_{dd} \quad \text{(power noise)} \tag{1}$$

$$\Delta V_{ss} = V_{ss}' - V_{ss} = V_{ss}' \quad (V_{ss} = 0) \text{(ground/ noise)} \tag{2}$$

In wire-bond packaging styles, a dominant supply level noise source is bond wire inductance in the package. Neglecting I/O current drives, the power and ground noise of the chip due to simultaneous switching typically follow an inverse pattern, and ΔV_{dd} is often symmetric to ΔV_{ss}. However, in modern bump-

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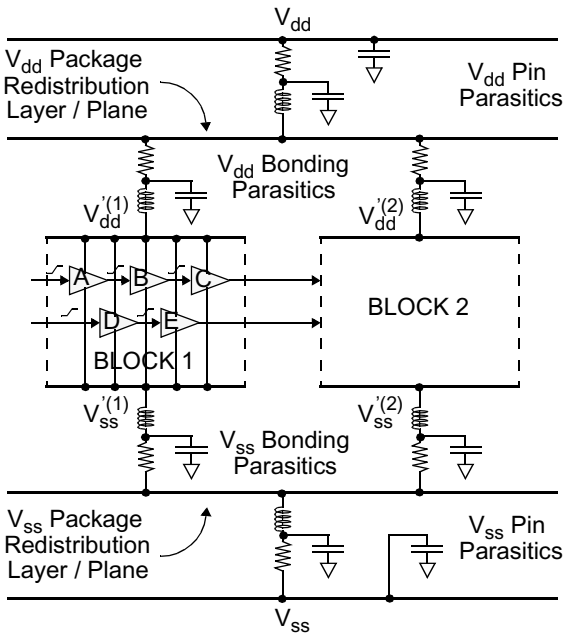

Figure 1. Power distribution: bump-bond packaging

bonded and low-inductance package styles, the package distributes power over the whole area of the chip (figure 1). Every bump connects to a local power/ground network. To save chip metallization area and improve density, chip global power distribution metal is reduced in lieu of thicker package distribution layers. Increasing design scales causes an increase in long wire loading, and in more wires connecting between different power domains. Logic-level-dependent currents flow between such blocks, causing asymmetric power and ground noise within a block. This noise is increased by the inclusion (within a bump block) of long wire repeater buffers which are often added in a post placement timing optimization step.

Figure 1 shows a simple equivalent circuit for bump-bond packaging. Each block is defined by the subcircuit supplied by a pair of bumps (V_{dd}/V_{ss}). Suppose that the cells A to E have transitions. Switching of the buffers A, B and D has a symmetric effect on the power and ground noise ($\Delta V_{dd}^{(1)}$ and $\Delta V_{ss}^{(1)}$), because they drive loads (consisting largely of parasitic interconnect capacitance) within the same block. On the other hand, switching of the C and E buffers has a non-symmetric effect on $\Delta V_{dd}^{(1)}$ and $\Delta V_{ss}^{(1)}$, because they drive loads which are outside of block 1, causing different switching currents to flow through the power and ground ports of block 1. Since wires leaving a block are likely to be physically long, these currents are proportionally large.

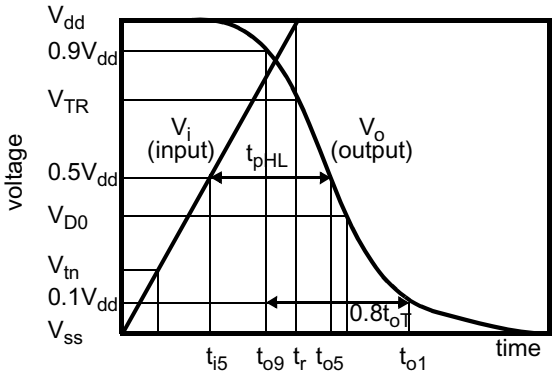

Figure 2. Notation for delay and slope for ideal V_{dd} and V_{ss}

2.2 Incremental buffer delay change

We define a buffer's *ideal* delay as the time interval between its input and output voltage reaching 50% of the power level. Figure 2 illustrates this definition. t_{pHL} is the high-to-low delay when the input of the inverter has a rising transition. Input and output transition times are t_r and t_{oT} respectively. Other time values are: t_{i5}, t_{o5}, t_{o1} and t_{o9}, which are times when the input or output voltage reaches 50%, 10%, and 90% of V_{dd}, respectively.

$$t_{pHL} = t_{o5} - t_{i5}\,,\; t_{oT} = (t_{o1} - t_{o9})/0.8 \qquad (3)$$

Figure 3 illustrates the delay and slope with P/G noise. The disturbed output voltage points are defined as follows:

$$V'_{o1} = V'_{ss} + 0.1(V'_{dd} - V'_{ss})\,,\; V'_{o9} = V'_{ss} + 0.9(V'_{dd} - V'_{ss})$$

$$V'_{o5} = V'_{ss} + 0.5(V'_{dd} - V'_{ss})$$

The disturbed high-to-low delay and slope are given by:

$$t'_{pHL} = t'_{o5} - t'_{i5}\,,\; t'_{oT} = (t'_{o1} - t'_{o9})/0.8 \qquad (4)$$

An alternative delay, $t'^{(2)}_{pHL}$, shown in figure 3, measures the delay referenced to the *disturbed* power and ground level V'_{o5}. In this paper, we will use t'_{pHL} in our analysis and results. Results for other definitions of delay change are similar but are omitted due to space limitations.

With a rising transition at the input, the changes of delay and output transition time are defined as follows:

$$\Delta t_{pHL} = t'_{pHL} - t_{pHL}\,,\; \Delta t_{oT} = t'_{oT} - t_{oT} \qquad (5)$$

3. EFFECT OF P/G NOISE ON BUFFER DELAY

Changes of power and ground levels affect signal propagation through an inverter in several ways.

3.1 Differential mode noise

We define *differential mode noise* (DMN) ΔV_{dif} as:

$$\Delta V_{dif} = V'_{dif} - V_{dif} = \Delta V_{dd} - \Delta V_{ss}$$

where

$$V'_{dif} = V'_{dd} - V'_{ss} \text{ and } V_{dif} = V_{dd} - V_{ss}$$

Differential mode noise ΔV_{dif} may be positive or negative, depending on the directions and amplitudes of ΔV_{dd} and ΔV_{ss}. The voltage difference (V_{dif}) between power supply and ground levels determine how fast the buffer charges/discharges its capacitive load.

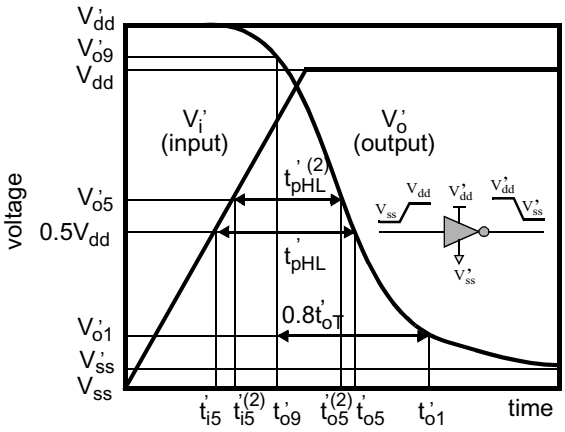

Figure 3. Notation for disturbed delay and slope

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Observation1: The buffer delay change is *linearly dependent* on the differential mode noise (DMN) as will be shown in section 4:

$$\Delta t_{pHL}\big|_{DMN} = -k_d \cdot \Delta V_{dif} = -k_d \cdot (\Delta V_{dd} - \Delta V_{ss}) \qquad (6)$$

where k_d is a positive constant dependent on the device and technology parameters, input transition times, and the gate load. Similar effects hold for both Δt_{pHL} and Δt_{pLH}.

3.2 Common mode noise

We define the *common mode noise* (CMN) ΔV_{com} as:

$$\Delta V_{com} = \Delta V_{dd} + \Delta V_{ss}$$

CMN modifies the effective switching threshold of the gate. This threshold shift changes the gate delay as illustrated in figure 4. Figure 4(a) shows an rising transition arriving at the buffer. Figure 4(b) illustrates the gate threshold shift and the corresponding delay change.

In figure 4(b), N and P are the original points when the nfet switches from cutoff to saturation region and pfet switches from saturation to cutoff, respectively. The corresponding switching times are indicated t_n and t_p. For noise of limited amplitude, the transistor thresholds (V_{tn} and V_{tp}) do not change significantly, so:

$$V'^{(N)}_{GS}\big|_{CMN} = V_i - V'_{ss} = V_{tn} > 0$$

$$V'^{(P)}_{GS}\big|_{CMN} = V_i - V'_{dd} = V_{tp} < 0$$

This causes a shift of the nfet and pfet switching points from *N* and *P* to *N'* and *P'*. The corresponding switching time shifts to t'_n and t'_p, respectively. We observe in figure 4(b) that:

$$\Delta V_{ss} > 0 \Rightarrow V^{(shift)}_{tn} > V_{tn} \Rightarrow t'_n > t_n \Rightarrow \text{increasing delay}$$

$$\Delta V_{dd} > 0 \Rightarrow V^{(shift)}_{tp} > V_{tp} \Rightarrow t'_p > t_p \Rightarrow \text{increasing delay}$$

And vise versa when power supply and ground level decrease.

Therefore, we make the following observation:

Observation 2: For an input with a rising transition, the dependency between the common mode noise (CMN) and the buffer delay change can be expressed by:

$$\Delta t_{pHL}\big|_{CMN} = k_{cr} \cdot \Delta V_{com} = k_{cr} \cdot (\Delta V_{dd} + \Delta V_{ss}) \qquad (7)$$

where k_{cr} is a positive constant determined by the device and technology parameters, input transition time, and the gate load. Similarly, for an input with a falling transition, the dependency between the common mode noise (CMN) and the buffer delay change can be expressed by:

$$\Delta t_{pLH}\big|_{CMN} = -k_{cf} \cdot \Delta V_{com} = -k_{cf} \cdot (\Delta V_{dd} + \Delta V_{ss}) \qquad (8)$$

where k_{cf} is a positive constant.

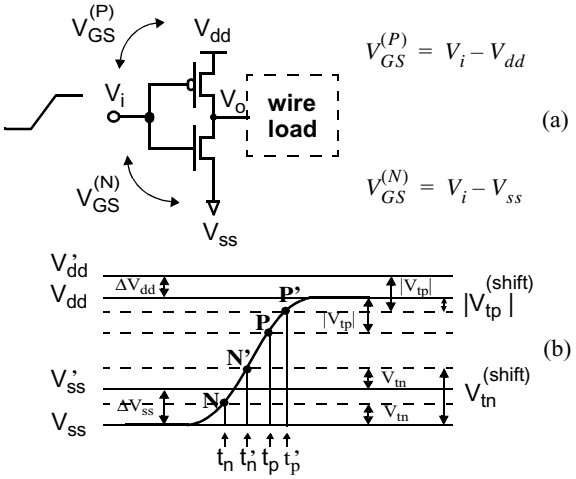

Figure 4. Threshold shift of an inverter

3.3 Loading effects

Both differential mode noise (DMN) and common mode noise (CMN) change buffer delays. Since the delay change can be of either sign, the noise sources need to be modeled together. Figure 5 shows alternative load configurations and the corresponding simulated delay change (both rising and falling transition) in 0.18μm technology. Note: $\Delta delay = 0$ when $\Delta V_{dd} = \Delta V_{ss} = 0$.

In figure 5 (a), the wire load of the inverter is a distributed RC tree network, including vias, extracted from the layout of a real circuit. In figure 5 (b), the wire load is simplified to an RC π-model. In figure 5 (c), the wire load is further simplified to a single resistor plus a single capacitor. In figure 5 (d), an effective loading capacitor is used to replace the inverter's output load. These simplified wire-load models in figures 5 (b)-(d) can be obtained using the methods described in [8]. The delay is measured when the input (V_i) and output (V_o / V_o' / V_o") voltage reach 50% of the ideal power supply voltage, respectively. The range for the power and ground noise is from -20% (-0.36 volt) to 20% (0.36 volt) of the power supply voltage, which is set to 1.8 volt for the selected technology. The range for the change of delay is from -30ps to 30ps. It is interesting to note that each of the four wire load models displays a linear relationship between the change of power/ground level and the change of inverter delay. Furthermore, the linearity improves when the change of power and ground level is smaller than 20%. In practical designs, the tolerable range for the power and ground levels is less than ±10%. Thus, the CMN and DMN induced delays can be superposed as noted below:

Observation 3: For a rising input transition and any of the wire load models described in figure 5, the incremental change of buffer delay is expressed as:

$$\Delta t_{pHL} = k_{1r} \cdot (\Delta V_{dd} + \Delta V_{ss}) - k_{2r} \cdot (\Delta V_{dd} - \Delta V_{ss}) \qquad (9)$$

A similar result applies to a falling input transition:

$$\Delta t_{pLH} = -k_{1f} \cdot (\Delta V_{dd} + \Delta V_{ss}) - k_{2f} \cdot (\Delta V_{dd} - \Delta V_{ss}) \qquad (10)$$

where k_{1r}, k_{1f}, k_{2r} and k_{2f} are positive constants dependent only on the input transition time, gate load, and the device technology parameters.

Observation 4: Buffer delay change is more sensitive to common mode noise than to differential mode noise in deep submicron designs, and may be dominated by common mode noise in some instances.

Observation 3 indicates that an appropriate simplified wire load model can be used for delay modeling of the buffer itself. With appropriate techniques [2][8], the distributed RC load of a gate can be simplified into the nearly equivalent π-model shown in figure 5(b). This π-model is further simplified into an effective capacitance load, shown in figure 5(d), by equating the average currents for the two load models. Such a capacitance model is inaccurate when the gate is behaving like a resistor [8]. This inaccuracy occurs primarily in the tail portion of the output waveform. However, for our purposes, the buffer delay is measured at the midpoint of the logic swing. Therefore, the inaccuracy in the gate delay (not the wire delay) caused by the effective capacitance model is relatively small.

The output voltage at node *o* in figure 5 (a) can be approximated by the voltage at node *o'* in figure 5 (b), *o"* in figure 5 (c) and *o"'* in figure 5 (d):

$$V_o \approx V'_o \approx V''_o \approx V'''_o$$

However, the voltage at node *q* is different from that of node *o*:

$$V_q \neq V_o$$

The simplified wire load model is only used to characterize the interconnect's driving point (node *o*) delay, not the receiving node (node *q*) delay. A variety of techniques exist [3] in order to model the interconnect delay. In this paper, we focus only on the buffer delay which is typically half of the total wire delay for optimized long wires.

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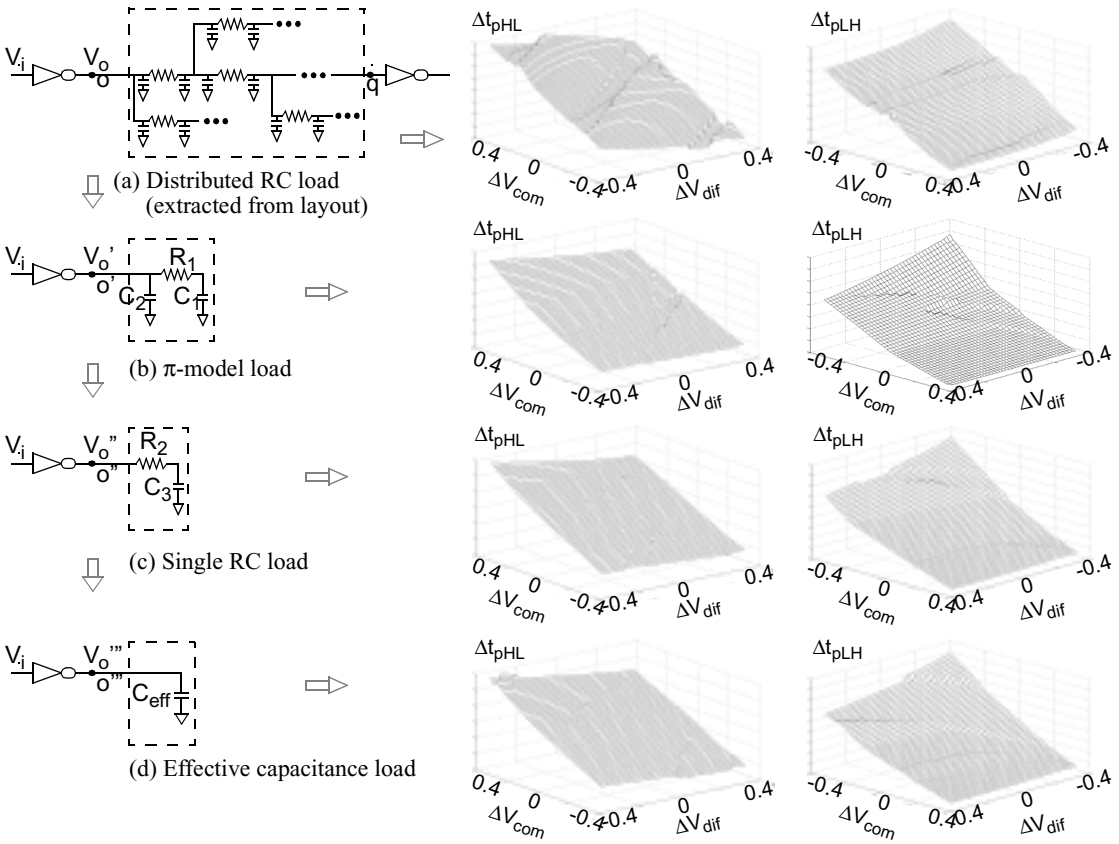

Figure 5. Buffer delay change for different load models

Power and ground noise amplitudes can either be correlated or largely independent depending on the relative magnitude of the power distribution parasitics and the relative number and activity of signals crossing between power distribution blocks. Such noise contributes to the local buffer/inverter delay in a complex way which can either increase or decrease the signal delay. For application in performance estimation, optimization or analysis it is useful to develop simple models which can be quickly evaluated and which can be linked to theoretical device models.

4. THEORETICAL MODEL

In deep submicron circuits, carrier velocity saturation effects predominate. To capture these effects, we use a short channel alpha-power law MOSFET model [9]. This model is based on four parameters: α (velocity saturation index), V_{tn} (threshold voltage), I_{D0} (drain current at $V_{GS} = V_{DS} = V_{dd}$), V_{DO} (drain saturation voltage at $V_{GS} = V_{dd}$). Note, *n* and *p* subscripts denote parameters related to nfet and pfet transistors, respectively. We assume that for a given transistor with a given loading capacitance, the above four values remain unchanged given a small disturbance of power supply and ground levels. Below, we present an abbreviated derivation of the model.

Referring to notations given in figures 2 and 3, we have:

$$t_{i5} = t_r/2 \tag{11}$$

$$t_{o5} = (C_L V_{dd})/(2I_{D0}) + (v_T + \alpha)/(1+\alpha)\cdot t_r \tag{12}$$

$$t_{i5}^{'(1)} = t_r/2 \tag{13}$$

$$t_{o5}^{'(1)} = [C_L/(I_{D0}k_{v1})]\cdot(V_{dd}/2 + \Delta V_{dd}) + t_\alpha^{'} \tag{14}$$

where

$$t_\alpha^{'} = t_r \cdot \left(1 - \left(1 - \frac{\Delta V_{ss}}{V_{dd}} - v_T\right)/(1+\alpha)\right),\ v_T = V_{tn}/V_{dd}$$

$$k_{v1} = \left(\frac{V_{dd} - \Delta V_{ss} - V_{tn}}{V_{dd} + \Delta V_{dd} - V_{tn}}\right)^\alpha \approx 1$$

From equations (11) - (14) and equations (3), (4) and (5), we obtain the incremental change of buffer delay:

$$\begin{aligned}\Delta t_{pHL} &= k_{1n}\cdot\Delta V_{com} - k_{2n}\cdot\Delta V_{dif} \\ &= k_{1n}\cdot(\Delta V_{dd} + \Delta V_{ss}) - k_{2n}\cdot(\Delta V_{dd} - \Delta V_{ss})\end{aligned} \tag{15}$$

The change of delay can also be expressed as:

$$\Delta t_{pHL} = k_{3n}\cdot\Delta V_{dd} + k_{4n}\cdot\Delta V_{ss} \tag{16}$$

where

$$k_{1n} = \frac{t_r}{2V_{dd}(1+\alpha)} + \frac{C_L}{2I_{D0}},\ k_{2n} = \frac{t_r}{2V_{dd}(1+\alpha)} - \frac{C_L}{2I_{D0}}$$

$$k_{3n} = k_{1n} - k_{2n},\ k_{4n} = k_{1n} + k_{2n} \tag{17}$$

Similar equations are derived for Δt_{pLH} with α, V_{tp}, I_{D0}, V_{D0} from the corresponding pfet, and the polarity of k_{Ip} is reversed:

$$\begin{aligned}\Delta t_{pLH} &= -k_{1p}\cdot\Delta V_{com} - k_{2p}\cdot\Delta V_{dif} \\ &= k_{3p}\cdot\Delta V_{dd} + k_{4p}\cdot\Delta V_{ss}\end{aligned} \tag{18}$$

where

$$k_{3p} = -k_{1p} - k_{2p},\ k_{4n} = -k_{1p} + k_{2p} \tag{19}$$

Theorem 1: Equations (15) to (19) demonstrate that the incremental change of buffer delay is *linear* with respect to the power and ground variations.

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The coefficients k_{1n} and k_{1p} quantify the effect of common mode noise while k_{2n} and k_{2p} characterize the effect of differential mode noise on buffer delay. This theorem shows why the observations in sections 3.1 through 3.3 hold. k_{1n}, k_{2n}, k_{1p} and k_{2p} are equivalent to k_{1r}, k_{2r}, k_{1f} and k_{2f} defined in observation 3.

Finally, with h_3 and h_4 determined by technology parameters, the change of slope can be expressed as:

$$\Delta t_{oT} = h_3 \cdot \Delta V_{dd} + h_4 \cdot \Delta V_{ss} \quad (20)$$

5. MODEL VALIDATION

We validated our model in both 0.25μm and 0.18μm technologies. As mentioned in section 4.1, the alpha-power law MOSFET model relies on four parameters: α, V_{tn}, I_{D0} (drain saturation current), and V_{DO} (drain saturation voltage). We determined these values for each transistor through HSPICE simulation. We follow the method in [9] to extract α and V_{tn}.

The results in Table 1 show that the model provides accurate estimation, with less than 5% error relative to HSPICE over a ±20% supply variation range. The model is not as accurate in estimating the change of transition time ($\Delta \mathbf{t_{oT}}$). For delay estimation, this is acceptable because $\Delta \mathbf{t_{oT}}$ has only a second order effect on the delay of the next stage. Note that this modeling technique applies to arbitrary size inverters, loading capacitance, and input transition times. Comparison between the technologies show the trend of increasing sensitivity to supply level noise with scaling.

6. APPLICATION

An important feature of the model is relative lack of dependence on the circuit loading structure. This simplifies inclusion in a design flow as a modification to the existing delay calculation.

6.1 Delay change for clock buffers

To preserve duty cycle, clock buffer chain designs often presume equal input and output transition times. Thus:

$$t_r = \frac{0.9C_L}{0.8I_{D0}}V_{dd} + \frac{C_L V_{D0}}{0.8I_{D0}} \cdot \ln\left(\frac{10V_{D0}}{eV_{dd}}\right)$$

$$\Delta t_r = \frac{0.9C_L}{0.8I_{D0}}(\Delta V_{dd} - \Delta V_{ss}) + \frac{C_L V_{D0}}{0.8I_{D0}} \cdot \ln\left(\frac{V_{dd}}{V_{dd} + \Delta V_{dd} - \Delta V_{ss}}\right)$$

Substituting t_r and Δt_r into equation (15), we have:

$$\begin{aligned}\Delta t_{pHL} &= (C_L/I_{D0}) \cdot (f_{1n} \cdot \Delta V_{com} - f_{2n} \cdot \Delta V_{dif}) \\ &= (C_L/I_{D0}) \cdot (f_{3n} \cdot \Delta V_{dd} + f_{4n} \cdot \Delta V_{ss})\end{aligned} \quad (21)$$

where

$$f_{1n} = (f_{3n} + f_{4n})/2 \ , \ f_{2n} = (f_{4n} - f_{3n})/2 \quad (22)$$

When Δt_r is ignored, we have:

$$f_{3n} = 1 \ , \ f_{4n} = f_{01}/(1+\alpha)$$

If Δt_r is not negligible, we have:

$$\Delta t_{pHL} = (C_L/I_{D0}) \cdot (f'_{3n} \cdot \Delta V_{dd} + f'_{4n} \cdot \Delta V_{ss}) \quad (23)$$

where

$$f'_{3n} = f_{3n} + f_{03} \ , \ f'_{4n} = f_{4n} - f_{03}$$

where

$$f_{01} = \frac{0.9}{0.8} + \frac{V_{D0}}{0.8V_{dd}} \cdot \ln\left(\frac{10V_{D0}}{eV_{dd}}\right)$$

$$f_{02} = \frac{0.9}{0.8} - \frac{V_{D0}}{0.8V_{dd}} \ , \ f_{03} = \left(\frac{1}{2} - \frac{1-v_T}{1+\alpha}\right) \cdot f_{02}$$

For a falling transition, we have:

$$\Delta t_{pLH} = (C_L/I_{D0}) \cdot (-f_{1p} \cdot \Delta V_{com} - f_{2p} \cdot \Delta V_{dif}) \quad (24)$$

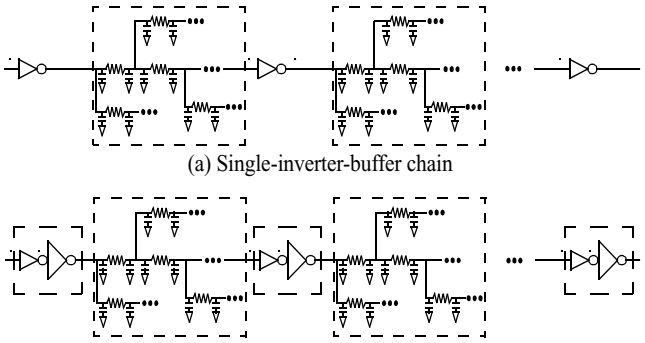
Note that equations (21) ~ (24) are independent of input slope. This result is used below to determine the cumulative jitter in a buffer chain.

6.2 Clock buffer chains

The linear relationship between the P/G noise and delay change can be used to analyze the delivered jitter for a chain of single-inverter-buffers and a chain of double-inverter-buffers, see fig. 6.

Assume the input is a rising transition. For one stage of a single-inverter-buffer, we have from (21):

$$\Delta delay^{(s)} = \Delta t_{pHL}^{(s)} = \frac{C_L}{I_{D0}^{(s)}} \cdot (f_{1n}^{(s)} \cdot \Delta V_{com} - f_{2n}^{(s)} \cdot \Delta V_{dif}) \quad (25)$$



(a) Single-inverter-buffer chain

(b) Double-inverter-buffer chain

Figure 6. Delay change for single-inverter chain v.s. double-inverter chain

Table 1: Model Validation for Delay and Slope

Parameter					0.25μm						0.18μm					
					Simulation		Our Method				Simulation		Our Method			
W_p/W_n (μm)	C_L (ff)	t_r (ps)	ΔV_{dd} (volt)	ΔV_{ss} (volt)	Δt_{pHL} (ps)	Δt_{oT} (ps)	Δt_{pHL} (ps)		Δt_{oT} (ps)		Δt_{pHL} (ps)	Δt_{oT} (ps)	Δt_{pHL} (ps)		Δt_{oT} (ps)	
10/5	100	100	-0.25	-0.250	-21.9	-4.2	-21	3.2%	-4.8	15%	-24.9	-10.7	-24.5	1.8%	-12.9	20%
10/5	100	100	0.00	-0.100	-4.7	0.2	-4.7	0.7%	0.2	1.1%	-6.2	-2.9	-6.0	4.0%	-2.6	12%
10/5	100	100	0.025	0.100	5.4	0.4	5.6	4.5%	0.4	0.7%	7.0	3.0	6.9	0.3%	3.1	6.2%
10/5	100	100	0.100	0.00	3.7	2.0	3.8	1.0%	2.0	1.8%	3.7	2.7	3.8	3.2%	2.9	8.0%
10/5	20	50	-0.500	0.025	-6.0	-1.7	-5.7	5.6%	-1.8	5.1%	-8.1	-6.9	-7.8	3.5%	-6.2	9.9%
10/5	20	50	0.500	0.100	8.6	2.7	8.2	4.7%	2.5	7.0%	9.7	1.6	10.2	5.0%	1.5	5.1%
5/5	100	100	0.250	0.100	14.1	5.4	14.4	1.6%	4.9	8.2%	17.3	3.6	16.5	4.9%	3.1	14%
5/5	100	100	0.500	-0.025	16.5	10.2	17.0	3.4%	10.2	0.8%	19.2	7.7	18.1	5.5%	7.2	6.7%
5/5	100	50	0.025	-0.250	8.3	-4.9	8.7	4.7%	-5.1	5.8%	8.5	1.7	8.9	4.9%	1.5	12%
10/10	100	100	-0.25	0.050	-4.7	-10.1	-4.6	1.1%	-11.8	17%	-4.7	-2.2	-4.5	5.1%	-2.3	3.2%

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For one stage of a double-inverter-buffer, we assume a tapered-buffer design. From (21) and (24) we have:

$$\Delta delay^{(d)} = \Delta t_{pHL}^{(d)} + \Delta t_{pLH}^{(d)} = C_L / I_{D0}^{(d)} \cdot [(f_{1n}^{(d)} - f_{1p}^{(d)}) \cdot \Delta V_{com} - (f_{2n}^{(d)} + f_{2p}^{(d)}) \cdot \Delta V_{dif}] \quad (26)$$

where the superscripts denote the parameters for single (s) and double (d) inverter buffers.

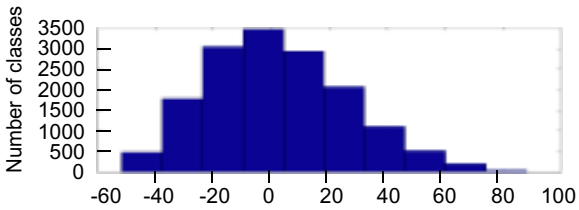
In deep submicron technologies, the buffer delay change is more sensitive to common mode noise than to differential mode noise. This has been experimentally demonstrated by our simulation results in figure 5, and theoretically shown by equation (15) which indicates $k_{1n} > k_{2n}$. In other words, we have

$$f_{1n}^{(s)} > f_{2n}^{(s)} \ , \ f_{1n}^{(d)} > f_{2n}^{(d)} \ , \ f_{1p}^{(d)} > f_{2p}^{(d)}$$

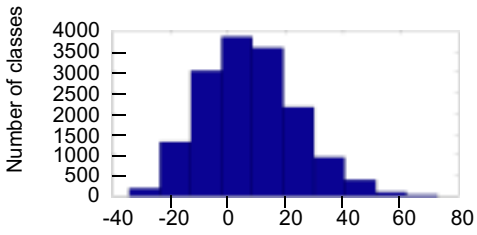
When the amplitude of the common mode noise is at least as large as that of the differential mode noise, the delay change of both buffer designs will be dominated by common mode noise. However, when $f_{1n}^{(d)}$ and $f_{1p}^{(d)}$ are comparable, the delay induced by common mode noise from (26) will cancel while the delay change given by (25) will be dominate. Hence, we make the following observation:

Observation 5: The delay of a double-inverter-buffer chain is less sensitive to the power/ground noise variations than that of a single-inverter-buffer chain.

Figure 7 shows simulation results of buffer delay change for the buffer chains shown in figure 6. The power/ground noise of each buffer in the chain is independent of the others and range over ±10% of V_{dd}. Inverter sizes are determined such that both buffer chains in figure 6 have a similar nominal delay (around 280ps). This is done to simplify comparison of the delay changes, because buffer chains with un-correlated delay would be difficult to compare. We choose similar wire loads for each stage. We randomly simulated 20000 combinations of P/G noise induced jitter. The statistics in figure 7 clearly show that the overall delivered jitter (total delay change of the buffer chain) for the double-inverter buffers is smaller. This provides us a new guideline for design: in terms of power/ground noise avoidance, the double-inverter buffer chain is a better choice. Double inverter buffers have slightly larger current requirements than inverters due both to tapering and to the domination of load capacitance by the interconnect, so the effect of additional current is minor. This result is effected by rapidly changing power levels primarily in the slow rise-time (RC dominated) extents of the interconnect. However, such effects should be similar for both styles of repeater.



(a) Delay change for a single-inverter-buffer chain (pS)



(b) Delay change for a double-inverter-buffer chain (pS)

Figure 7. Comparison of buffer delay change (histogram)

7. CONCLUSIONS

Maintaining signal integrity in deep submicron circuits is a difficult problem. Variations of power and ground levels play an important role because this type of noise significantly degrades circuit performance. Deep submicron circuits have decreased power supply level V_{dd} and decreased velocity saturation index α, leading to increased sensitivity of delay to P/G noise. Thus, despite the reduction of noise from lower inductance packaging, the relative magnitude of the delay changes is still a serious potential problem.

We studied the effects of differential and common mode power/ground noise on buffer delay. Using the α-power law MOSFET model, we derived general formulas to estimate the influence of power and ground noise on delay and slope. As our model does not rely on the circuit structure, it can be incorporated into any existing gate delay calculation techniques. It is simple and accurate. An application in clock buffer chain design shows that repeater chains using buffers instead of inherently faster inverters tend to have superior level - induced delay characteristics.

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