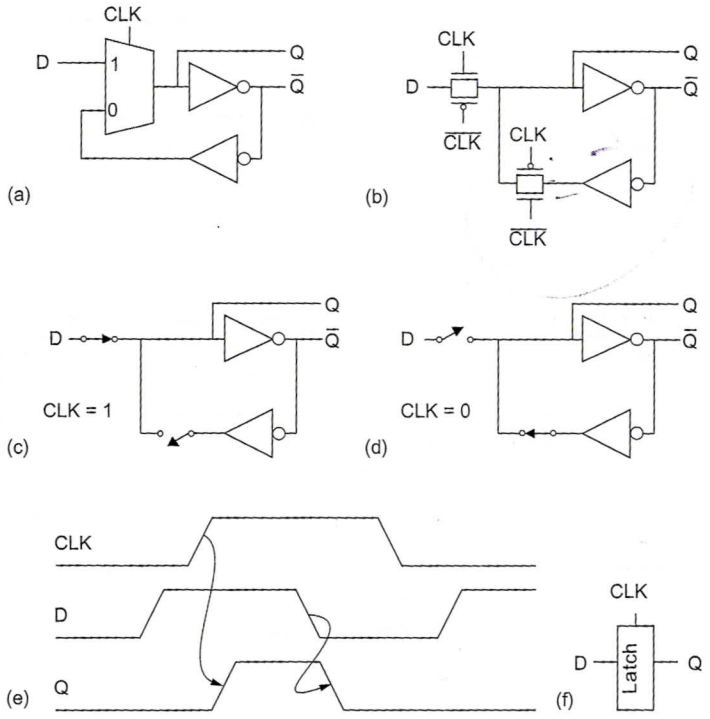

FIG 1.30 CMOS positive-level-sensitive D latch

(Figure 1.31(d)). When the clock transitions from 1 to 0, the slave latch holds its value and the master starts sampling the input again.

In summary, this flip-flop copies *D* to *Q* on the rising edge of the clock, as shown in Figure 1.31(e). Thus this device is called a positive-edge triggered flip-flop (also called a *D flip-flop*, *D register*, or *master–slave flip-flop*). Figure 1.31(f) shows the circuit symbol for the flip-flop. By reversing the latch polarities, a negative edge triggered flip-flop may be constructed. A collection of two or more *D* flip-flops sharing a common clock input is called a *register*. A register is often drawn as a flip-flop with multi-bit *D* and *Q* busses.

In Section 7.2.3 we will see that flip-flops may experience hold-time failures if the system has too much *clock skew*, i.e., if one flip-flop triggers early and another triggers late because of variations in clock arrival times. In industrial designs, a great deal of effort is devoted to timing simulations to catch hold-time problems. When design time is more important (e.g., in academic class projects), hold time problems can be avoided altogether by distributing a two-phase nonoverlapping clock. Figure 1.32 shows the flip-flop clocked with two nonoverlapping phases. As long as the phases do not overlap even with worst-case skews, at least one latch will be opaque at any given time and hold-time problems will never occur.

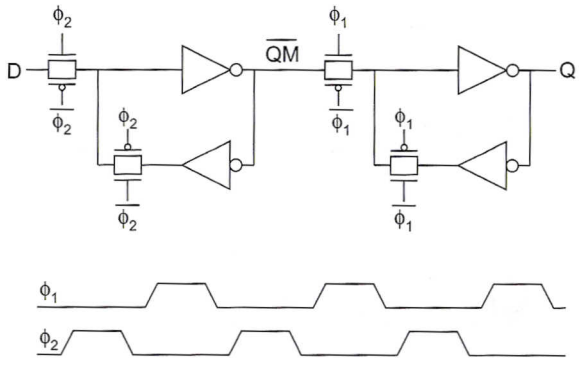

FIG 1.32 CMOS flip-flop with two-phase nonoverlapping clocks

1.5 CMOS Fabrication and Layout

Now that we can design logic gates and latches from transistors, let us consider how the transistors are built. Transistors are fabricated on thin silicon wafers that serve as both a mechanical support and an electrical common point called the *substrate*. We can understand the physical layout of transistors from two perspectives. One is the top view, obtained by looking down on a wafer. The other is the cross-section, obtained by slicing the wafer through the middle of a transistor and looking at it edgewise. We begin by looking at the cross-section of a complete CMOS inverter. We then look at the top view of the same inverter and define a set of masks used to manufacture the different parts of the inverter. The size of the transistors and wires is set by the mask dimensions and is limited by the resolution of the manufacturing process. Continual advancements in this resolution have fueled the exponential growth of the semiconductor industry.

1.5.1 Inverter Cross-section

Figure 1.33 shows a cross-section of the inverter from Section 1.4.1. In this diagram, the inverter is built on a p-type substrate. The pMOS transistor requires an n-type body region, so an n-well is diffused into the substrate in its vicinity. Note that it is also possible to design a CMOS process with an n-type substrate and p-wells to contain the nMOS transistors. As described in Section 1.3, the nMOS transistor has n-type source and drain regions and a polysilicon gate over a thin layer of silicon dioxide (SiO_2, also called *gate oxide*). The pMOS transistor is a similar structure with p-type source and drain regions. The polysilicon gates of the two transistors are tied together somewhere off the page and form the input *A*. The source of the nMOS transistor is connected to a metal ground line and the source of the pMOS transistor is connected to a metal V_{DD} line. The drains of the

ude Comparator

tor determines the larger of two binary numbers. To compare two and B, compute $B - A = B + \overline{A} + 1$. If there is a carry-out, $A \leq B$. A s that the numbers are equal. Figure 10.51 shows a 4-bit unsigned n a carry-ripple adder and 2's complementer. de is determined from the carry-out (C) and ding to Table 10.4. For wider inputs, any of the res can be used.

ed 2's complement numbers is slightly more of the possibility of overflow when subtracting fferent signs. Instead of simply examining the etermine if the result is negative (N, indicated t bit of the result) and if it overflows the range umbers. The overflow signal V is true if the gns (most significant bits) and the output sign sign of B. The actual sign of the difference use overflow flips the sign. If this sign is nega- Again, the other relations can be derived from d the Z signal.

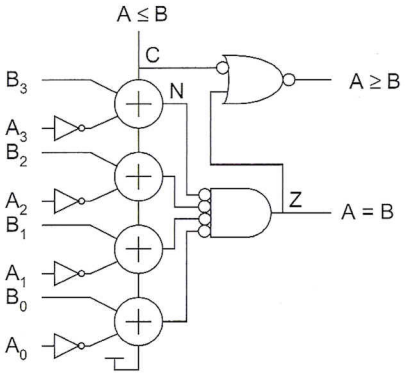

FIG 10.51 Unsigned magnitude comparator

Magnitude comparison

Unsigned Comparison	Signed Comparison
	Z
	$\overline{Z}$
$+ \overline{Z}$	$\overline{(N \oplus V)} + \overline{Z}$
	$(N \oplus V)$
	$\overline{(N \oplus V)}$
$+ Z$	$(N \oplus V) + Z$

Comparator

r determines if ($A = B$). This can be done more simply OR gates and a 1's detector, shown in Figure 10.52. done with a pseudo-nMOS or dynamic gate in which ere combined with a "wired-OR."

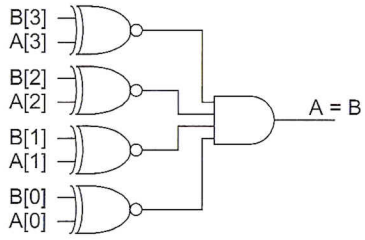

FIG 10.52 Equality comparator