

Basic Building Blocks

Exercise 1

Generate the VHDL model of a circuit that computes $y = a \cdot x$ where a is a bit and x, y are n -bit vectors.

Exercise 2

Generate several models of a 1-bit full subtractor (Boolean equations, truth table, LUT instantiation).

Exercise 3

Generate a generic model of an n -bit 8-to-1 multiplexer.

Exercise 4

Generate a generic model of an n -input address decoder.

Exercise 5

Design an n -bit magnitude comparator: given two n -bit naturals a and b , it generates a 1-bit output gt equal to 1 if $a \geq b$ and equal to 0 if $a < b$.