Architecture of digital circuits

Example (square root function)
Implement a circuit for the following integer square root algorithm:

```
1 r ← 0;
2 s ← 1;
3 while s ≤ x do
4 |   s ← s + 2 * (r + 1) + 1;
5 |   r ← r + 1;
6 end
7 sqrt ← r
```

Exercise 1
Let $S_n = \{x \in \mathbb{Z} : 0 \leq x < 2^n\}$ denote the set of all n-bit integers. A *carry-save adder* implements the transformation

$$\begin{cases} (x_1, x_2, x_3) \in S_n^3 \to (y_1, y_2) \in S_n^2 \\ x_1 + x_2 + x_3 = y_1 + 2 \cdot y_2 \end{cases}$$

A *7-to-3 counter* uses carry-save adder components to implement the transformation

$$\begin{cases} (x_1, x_2, x_3, x_4, x_5, x_6, x_7) \in S_n^7 \to (y_1, y_2, y_3) \in S_n^3 \\ x_1 + x_2 + x_3 + x_4 + x_5 + x_6 + x_7 = y_1 + 2 \cdot y_2 + 4 \cdot y_3 \end{cases}$$

These components are used in multiplication algorithms, where multiple-operand addition scenarios occur. Generate the following VHDL models of a 7-to-3 counter:

- a combinational circuit, made up of four carry-save adders;
- a data path including two carry-save adders and several registers where computation is performed over 3 cycles
- a data path including one carry-save adders and several registers where computation is performed over 4 cycles