PHY473R

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École polytechnique

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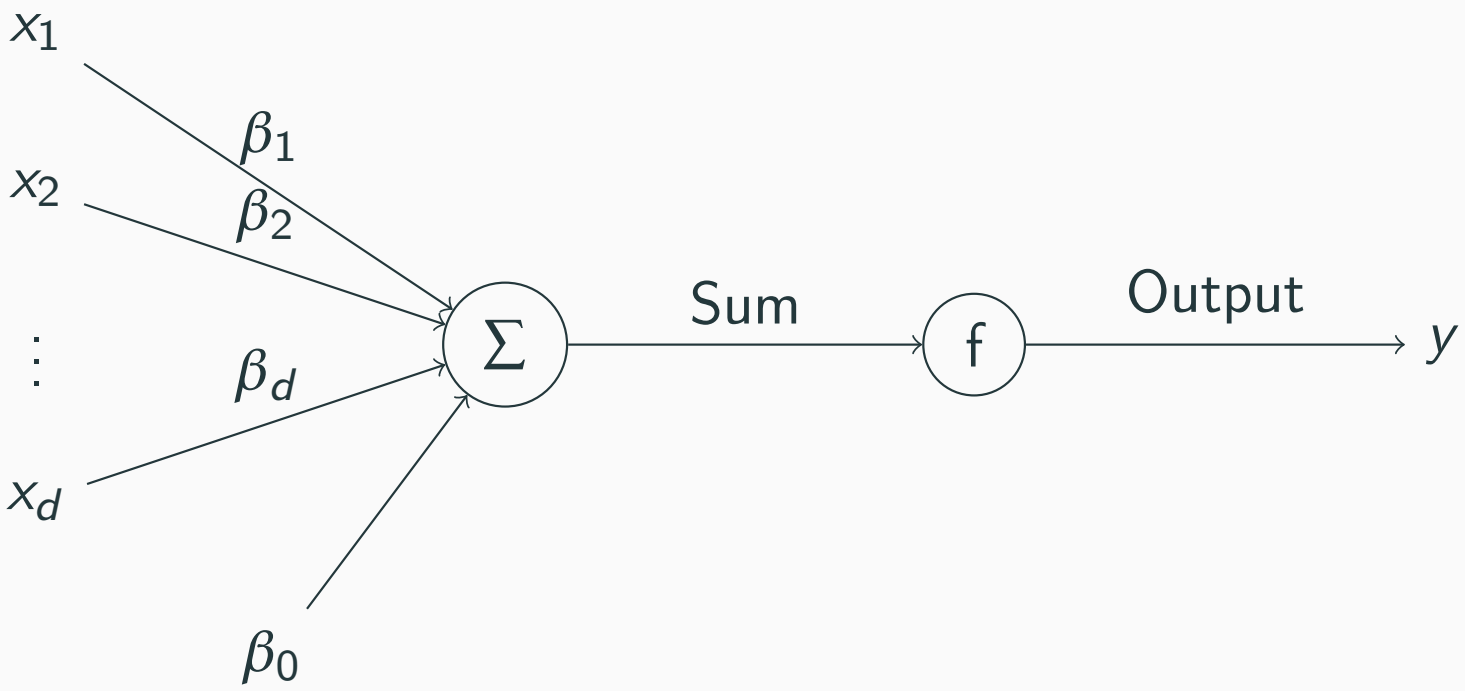
Question théorique: Implémentation d'un modèle de Machine Learning pour classification d'image en FPGA

Perceptron model



Output of the perceptron is given by:

$$y = f\left(\sum_{i=1}^{d} \beta_i x_i + \beta_0\right) \quad \text{in our case} \quad f(x) = \begin{cases} 0 & \text{si } x < 0, \\ 1 & \text{si } x \geq 0. \end{cases}$$

Perceptron model

Suppose that the data is linearly separable $\implies \exists$ hyperplane $x^\top \beta + \beta_0 = 0$ that separates the two classes of data. Therefore, for all test vector x, y(x) will be either positive or negative and the sign will give us the binary class of the input x.

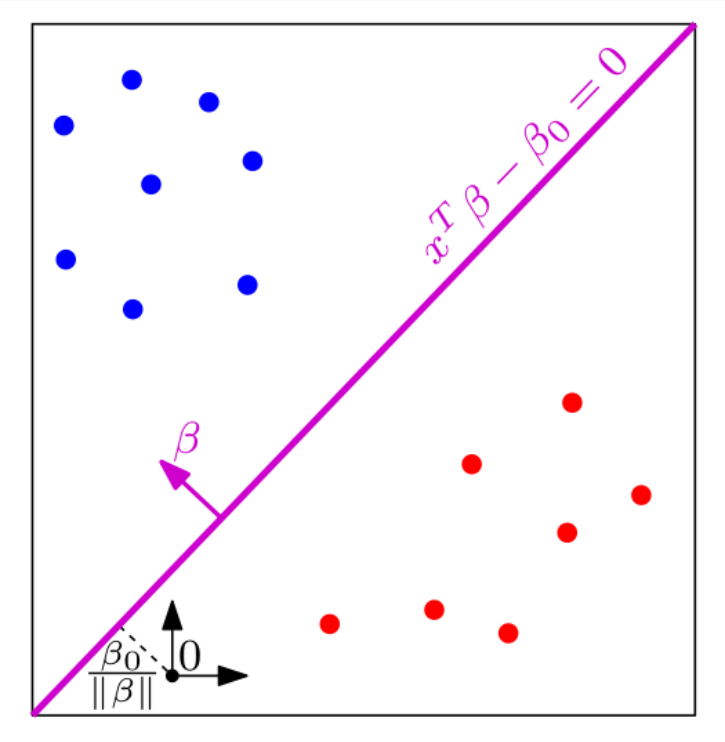


Figure 1: Separating hyperplane on linearly separable data

Transformation: image $\Longrightarrow$ vector

0	1	0	1
1	0	1	0
0	1	0	1
1	0	1	0

Flatten $\longrightarrow$

0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0

Tranining the model

Figure 2: MNIST dataset

Over **8000** to train our perceptron model (80% train/ 20% test).

Training the model

To fit the requirements of our FPGA project, we had to:

- Resize the images to 256x256.
- Transform them into black(0) and white(1) with pattern in white and background in black.
- Scale the weights, so we could approximate them with integers.
- Write the weights into a `.mif` file.

Résultats du modèle

Perceptron 0/1

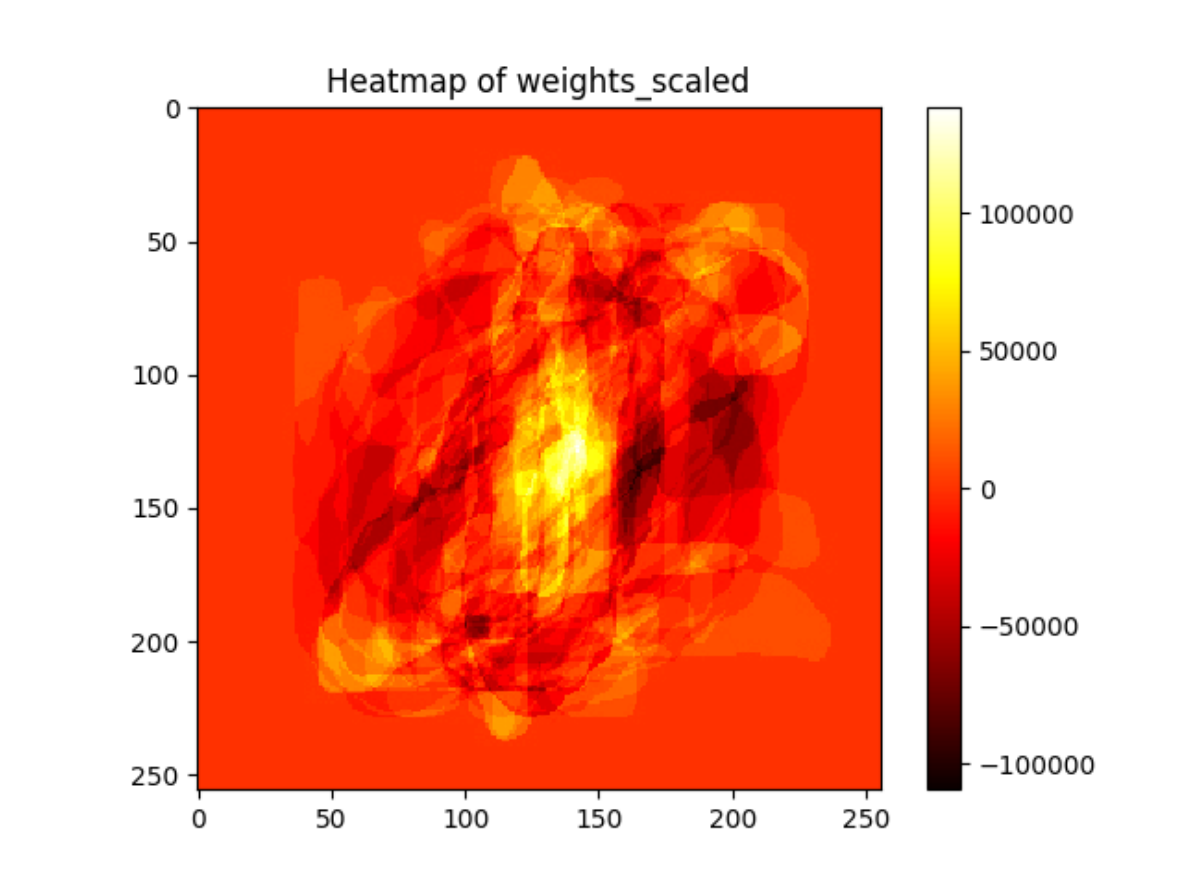


Figure 3: Heatmap for 0/1 perceptron

Accuracy on test data: 0,9989

Perceptrons 0/2 and 1/2

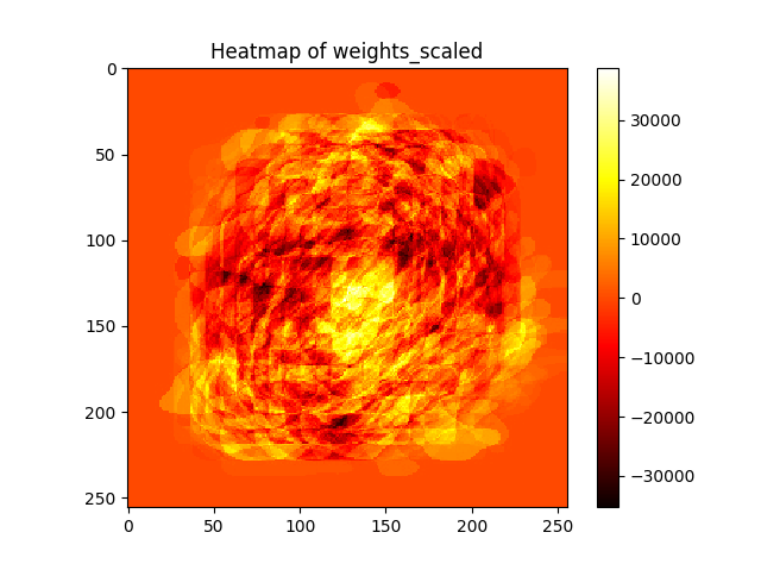


Figure 4: Heatmap for 0/2 perceptron

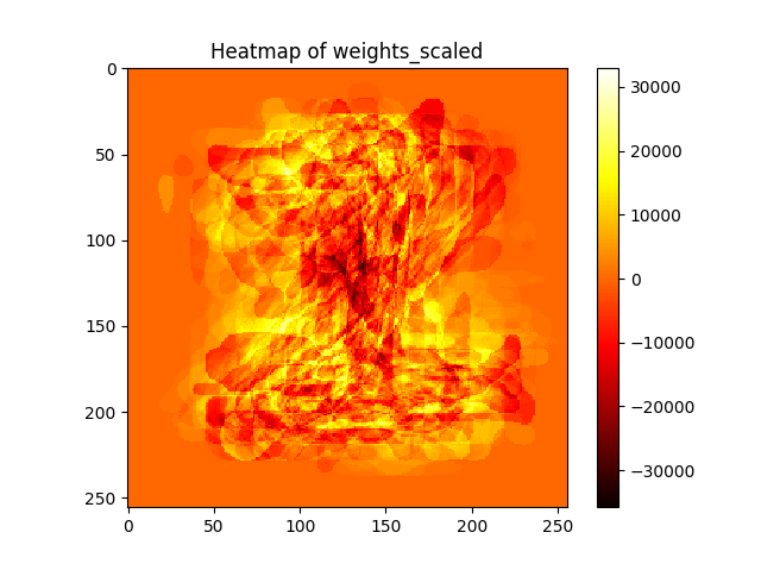


Figure 5: Heatmap for 1/2 perceptron

Design du circuit

Control Unit (State Machine)

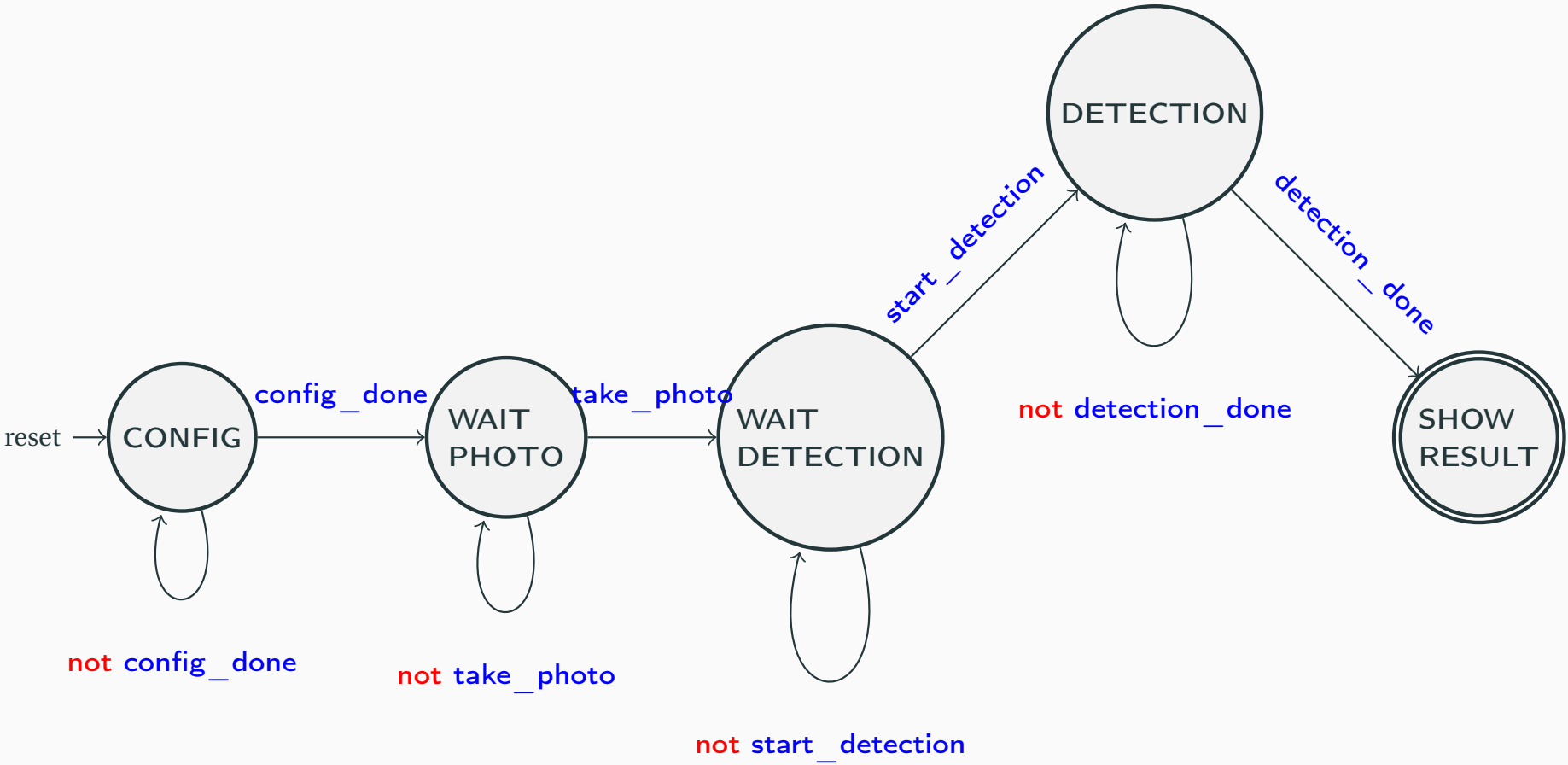
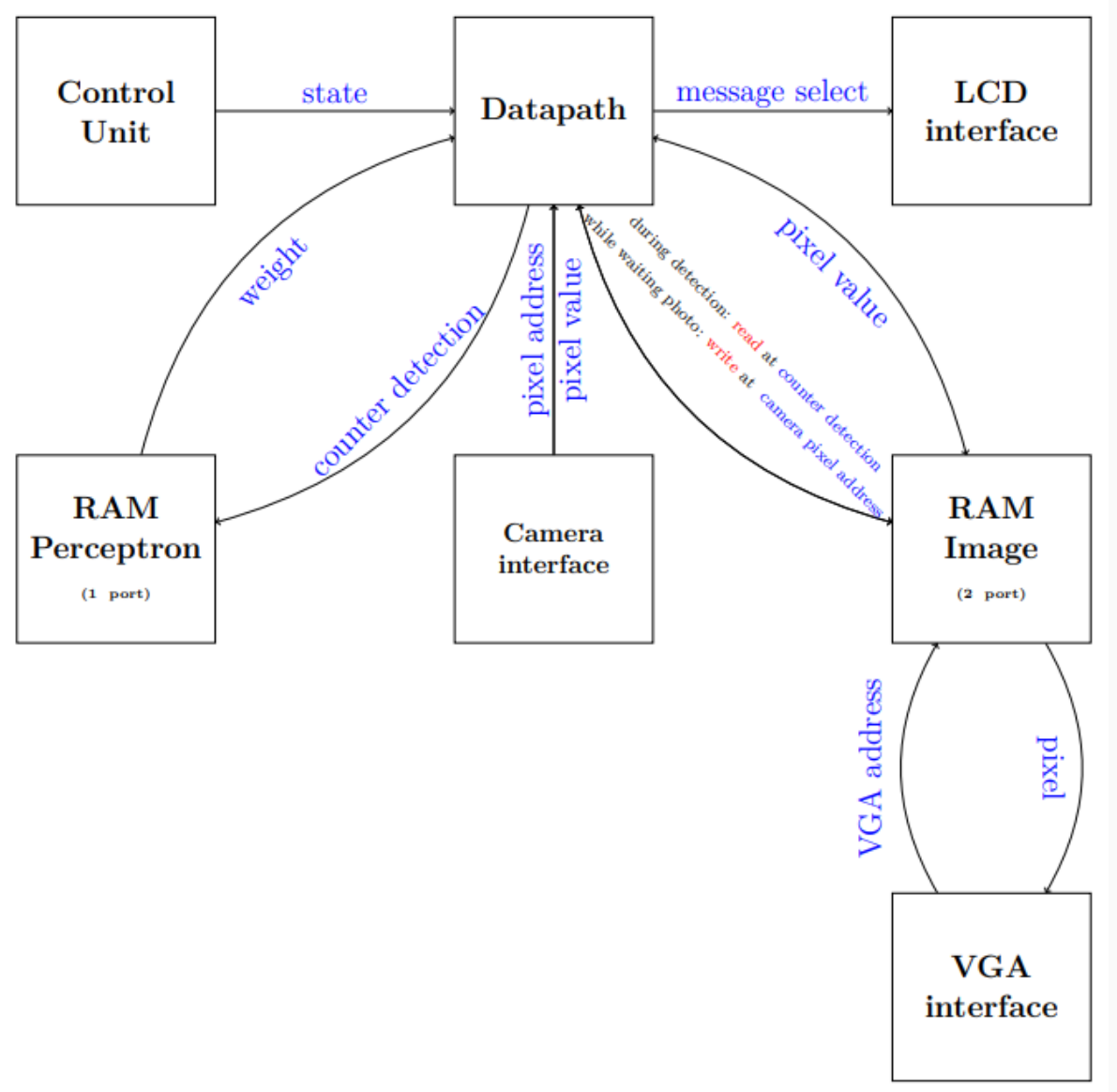


Figure 6: Control unit's state machine

Datapath


Control Unit
state
Datapath
message select
LCD interface
weight
counter detection
pixel address
pixel value
during detection: read at counter detection
while waiting photo: write at camera pixel address
pixel value
RAM Perceptron
(1 port)
Camera interface
RAM Image
(2 port)
VGA address
pixel
VGA interface

Demo!!