PHY_51059_EP
TP “SPICE electrical simulation”

Principle of TP:
Introduction:

The purpose of the « TP » is to achieve, through the study of the behavior of transistors and CMOS inverters, an introduction to the language of SPICE simulation.

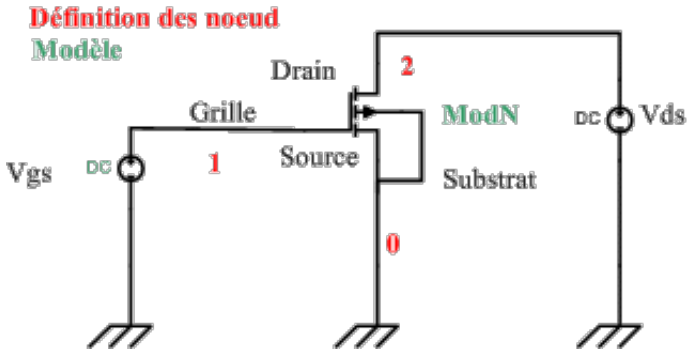
The subject, necessary for the implementation of TP and a summary of the main elements of the language files are available on the website of PHY_51059_EP in Moodle Ecole Polytechnique.
https://moodle.polytechnique.fr/course/view.php?id=20328

In this lab works, we ask you to write each a report containing your results and which must be filed in PDF format on the same website before Friday, December 20, 2024. This report will count as 20% of the final grade, if this improves the final grade, for the course PHY_51059_EP (Max [20% TP+80% writing exam; 100% writing exam]).

As part of the lab works, we will use the Spice OPUS software, you will find a free downloadable version of the software (Linux and Windows) and elements of documentation on the same Moodle website.
http://fides.fe.uni-lj.si/spice/

Introduction:

- Create in your home directory in a specific directory for this “TP”
- Store in that directory the files definition of technology (0.6 µm). These file “**cmostm.mod**” and “**cmosws.mod**” that found on the web site.
- You find a file such as "**nmos.cir**" corresponding to the simulation of a NMOS transistor with constant V_{DS}
- Copy this file in your working directory and open it with "**kedit**."
- The simulated pattern corresponds to the following figure:



the file is as follow

* transistor Nmos ********** * fichier techno .include cmosws.mod * dessin du circuit Vds 2 0 dc 3.3V Vgs 1 0 dc 1V M1 2 1 0 0 modn L=0.6U W=2.5U * simulation .dc Vgs 0 3.3v 50mV .end	Information displayed during loading not necessarily useful. The character "*" defined the beginning of a comment line Defined technology ie the models checking NMOS transistors and PMOS The simulation schema definition. Here 2 voltage sources "Vds" and "Vgs" and a NMOS transistor "M1". To see the syntax "Spice elements." ***Vx** Borne + Borne- Type valeur* ***Mx** Drain Gate Source Bulk Model ……* Type and simulation conditions. Here continuous simulation. “dc” via a Vgs voltage sweep of 0 to 3.3 V with steps of 50mV Symbol end of file

- Starting “**spiceopus**”.in a console previously positioned in the working directory
- Load File : « **SpiceOpus (c) 1-> source nmos.cir** »
  Execution File “**SpiceOpus (c) 2-> run**”

Warning: version not specified for modn MOSFET level=53 model, version 3.2.4 used. (Not important message)

- For the graph ***SpiceOpus (c) 3 -> plot abs(i(vds))***
- For voltage, indicate the node where we measure the voltage ***SpiceOpus (c) 4 -> plot v(2) v(1)***
- For the current, measurement is possible only on a voltage source ***SpiceOpus (c) 3 -> plot abs(i(vds))***
- Beware the current measurements are in receiver agreement to the source voltage (U and I in the opposite direction).
- The modification of axes (log) is done by the right mouse button

Part A: NMOS and PMOS transistors characterization

Our goal is to obtain the current/voltage functions Ids = f(V_{DS}, V_{GS}) for NMOS and PMOS transistors in a 0.6 micron CMOS process. The parameters defining the electrical behavior of the transistors are defined in the file « ***cmosws.mod*** ». *(File available on the web site to be copied in the working directory)*
The nominal values are V_{SS} = 0V and V_{DD} = 3.3 V.

Q1) Ids function of V_{GS}

Plot, for the two types of transistors, the graph Ids (V_{DS},V_{GS}) for V_{DS} constant = V_{DD}, and for V_{GS} varying between V_{SS} and V_{DD}. Define graphically the threshold voltages V_{tn} and V_{tp} of the two types of transistors.

Q2) Ids function of Vds

Plot, for the two types of transistors, the graph Ids (V_{DS},V_{GS}), for V_{GS} constant and for V_{DS} varying between V_{SS} and V_{DD}. These plots will be done for several values of V_{GS} (for example, V_{GS} = 1V, V_{GS} = 2V, V_{GS} = 3V, et V_{GS} = V_{DD}). Identify the linear and saturation domains for both types of MOS transistors.

For the simulations, the following sizing will be used:
- L_n = 0.6 µm / W_n = 3.0 µm
- L_p = 0.6 µm / W_p = 6.0 µm

Part B: CMOS inverter static characterization

Our goal is now to plot the static transfer function V_{out} = f(V_{in}) for the CMOS inverter. We want to analyze the value of the logic threshold V_l depending on the dimensions of the transistors W_n et W_p. We will only consider transistors with a minimum channel length, i.e. L_n = L_p = 0.6 µm.

We remind you that the logic threshold V_l of an inverter is the input voltage leading to V_{in} = V_{out}. (Cross section between the transfer function and the bisecting line).
This value is given by the following formula:

$$V_L = \frac{V_{t_n} + \sqrt{\beta}(V_{DD} + V_{t_p})}{1 + \sqrt{\beta}}$$

With $\beta = \frac{R_{N_{On}}}{R_{P_{On}}} = \frac{\mu_p}{\mu_n} \cdot \frac{W_P}{W_n} \cdot \frac{L_n}{L_p}$

Q3) Centered Inverter

Plot the static transfer function for a « centered » inverter,
- L_n = 0.6 µm / W_n = 3.0 µm
- L_p = 0.6 µm / W_p = 6.0 µm

Deduce the noise margin (i.e. the maximum noise acceptable) on the input low state and high state.

Q4) Decentered Inverter

Plot the static transfer function for a decentered Inverter with W_n = W_p = 3.0 µm (the equivalent resistance of the P transistor is two times greater than the resistance of the N transistor). Same question as Q3.

Plot the static transfer function for a decentered Inverter with $W_p = 12.0$ µm and $W_n = 3.0$ µm (the equivalent resistance of the P transistor is two times smaller than the resistance of the N transistor). Same question as Q3.

Q5) NAND2 transfer function

We now consider a centered NAND2 gate ($W_p = W_n = 6.0$ µm).
Plot the static transfer function of this NAND2 gate in the two following cases:

- The entries A and B of this NAND gate are connected to the same input signal which varies from V_{SS} to V_{DD}. This is a scenario in which the two inputs switches at the same time.
- The A input is at high state (voltage V_{DD}), and the B voltage varies from V_{SS} to V_{DD}. This corresponds to commutations which do not occur at the same time.

Deduce the noise margin on the input low state and high state.

Part C: dynamical characterization of the CMOS inverter

We now want to study the dynamic behavior of the CMOS inverter. The goal is to analyze the dependency of the propagation time between the input and output on several parameters:

- Parameters related to the technology: threshold voltages V_{tn} and V_{tp}
- Parameters related to the environment: temperature
- Parameters related to the design: output capacitance, sizing of the transistors (W_n, L_n, W_p, L_p)

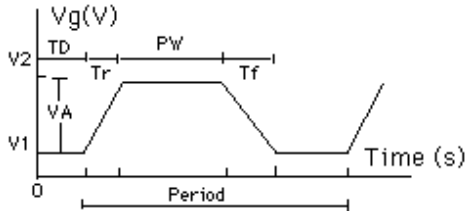
We just remind that the propagation time T_p is defined as the duration elapsed between:
-Time when the input crosses the voltage $V_{DD}/2$,
-Time when the output crosses the voltage $V_{DD}/2$.

There are two propagation times T_p (up->down) et T_p(down->up), corresponding to an upward transition for the input (i.e. downward transition for the output) and the opposite way. We will now systematically study both values.

For this dynamic simulation, we will use the transitory mode ".tran"
.tran simulation step time simulation lenght

The input signal IN is defined using a shape function described in the file containing the schematic (« pulse »). We will describe an upward transition followed by a downward transition.
Since the propagation times T_p (up->down) and T_p(down->up), depend on the shape of the input signal IN, and especially on the switching time of signal IN (duration of the transition of the input signal IN from V_{DD} to V_{SS}), the choice of this duration is very important.
We will use a typical value of 1ns. This choice corresponds to the switching time of the output signal of an inverter connected to the inputs of 3 identical inverters.

V_{name} N_1 N_2 pulse(V_1 V_2 T_D T_r T_f PW Period)
V_1 - initial voltage; V_2 - peak voltage; T_D - initial delay time; T_r - rise time; T_f - fall time; PW - pulse-wise; and Period – period



Q6) Output capacitance influence

Assuming that the conducting transistor of the inverter behaves as a resistance, the propagation times should be proportional to the output capacitance.
We consider a centered CMOS inverter for which the output S is connected to a charge capacitance C. This capacitance C modeled the sum of the capacitance of the input gates addressed by the signal S, plus the interconnection capacitance. We now use the following sizing for the inverter:
- L_n = 0.6 µm / W_n = 3.0 µm
- L_p = 0.6 µm / W_p = 6.0 µm

Measure the propagation time T_p(up->down) and T_p(down->up) for several values of capacitance C: 0.0pF, 0.1pF, 0.2pF, 0.5pF, 1.0pF
Plot the two Tp(C).

Q7) W and L Sizing Influence

Assuming that the conducting transistor of the inverter behaves as a resistance, the propagation time T_p(up->down) is proportional to the equivalent resistance of the N transistor, and the propagation time T_p(down->up) is proportional to the equivalent resistance of the P transistor. We select a charge capacitance of 0.5pF.
Measure the variation of the propagation times when the resistance of the N transistor is decreased by increasing W_n. Plot the graphs $T_p(W_n)$.
Measure the variation of the propagation times when the resistance of the P transistor is decreased by increasing W_p. Plot the graphs $T_p(W_p)$.

Q8) Temperature and threshold voltage Influence

We know that the equivalent resistance of the MOS transistors increases with temperature. The propagation times depend therefore on temperature.
The propagation time of CMOS gate also depend on the value of the threshold voltages V_{tn} and V_{tp} of the N and P transistors. These threshold voltages depend on the doping level and oxide thickness. Therefore, there is a dispersion of the threshold voltages.
The integrated circuits foundries usually warrantee that the threshold voltages V_{tn} and V_{tp} are within a range: ($V_{tnmin} < V_{tn} < V_{tnmax}$, and $V_{tpmin} < V_{tp} < V_{tpmax}$)
Foundries usually provide three sets of parameters for the simulation model of each N and P transistors:

- Parameters « typical »
- Parameters « worst case »
- Parameters « best case »

The parameters « best case » and « worst case » are referring to the propagation times.

Moreover, when designing a integrated circuit, the designer should take care that the circuit is working in the full range of temperature and threshold voltages. For example, for an automotive application, the circuit should work from -40°C (car start in winter) to +125°C (hot motor in summer).
To change the temperature, add the line at the beginning of the script file (2 possible solutions):

.option temp=XX (Celsius)
set temp=XX(Celsius)

Measure the variation of the propagation time for the reference inverter (W_n = 3.0 micron and W_p = 6.0 micron) for an output capacitance C of 0.5pF in the four following cases: [-40°C, ws] ; [+125°C, ws] ; [-40°C, tm] et [+125°C, tm], using the two parameters files « ***cmosws.mod*** » et « ***cmostm.mod*** ».
(File to be extracted from the web site and copied in the working directory)