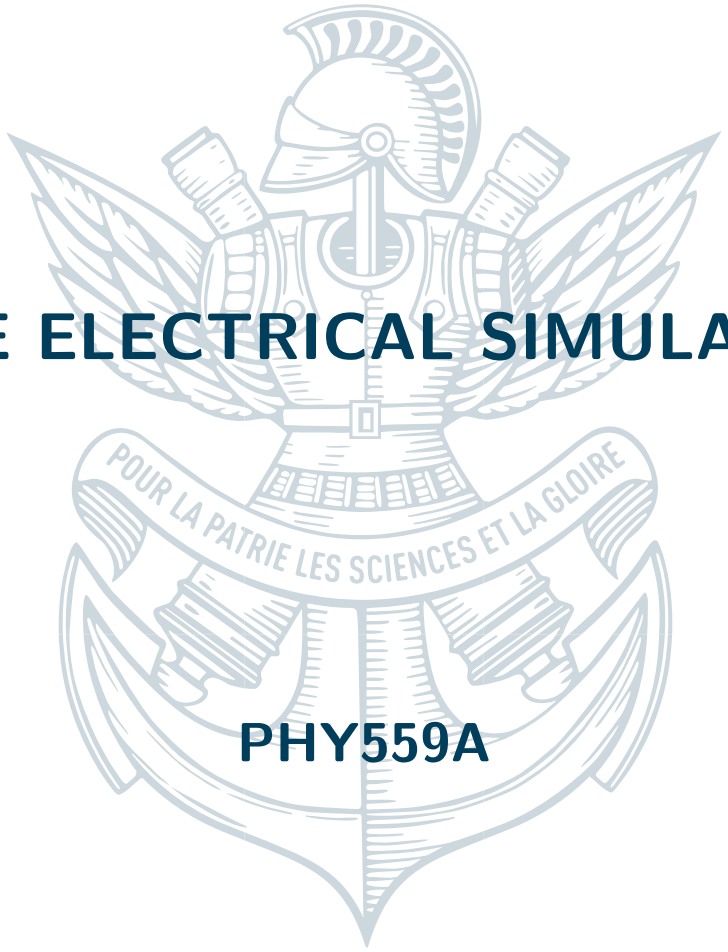

SPICE ELECTRICAL SIMULATION

PHY559A

November 18, 2024

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CONTENTS

1
NMOS AND PMOS TRANSISTORS CHARACTERIZATION

1.1 I_{DS} function of V_{GS}

Plot, for the two types of transistors, the graph $I_{DS}(V_{DS}, V_{GS})$ for V_{DS} constant $= V_{DD}$, and for V_{GS} varying between between V_{SS} and V_{DD}. Define graphically the threshold voltages V_{tn} and V_{tp} of the two types of transistors.

1.1.1 • NMOS transistor

We observe that $V_{DS} = V_{DD} \implies V_{DS} \geq V_{GS} - V_{tn} \implies$ the NMOS transistor is either cutoff or in saturation depending on the value of V_{GS}, thus

$$I_{DS}(V_{DS} = V_{DD}, V_{GS}) = \begin{cases} 0, & \text{if } V_{GS} < V_{tn} \text{ (cutoff)}, \\ \frac{1}{2} k_n \frac{W}{L} (V_{GS} - V_{tn})^2, & \text{if } V_{GS} \geq V_{tn} \text{ (saturation)}. \end{cases} \tag{1}$$

```
.include cmosws.mod

Vds 2 0 dc 3.3V
Vgs 1 0 dc 1V
M1  2 1 0 0 MODN L=0.6U W=3.0U

.dc Vgs 0 3.3 50mV
.end

```

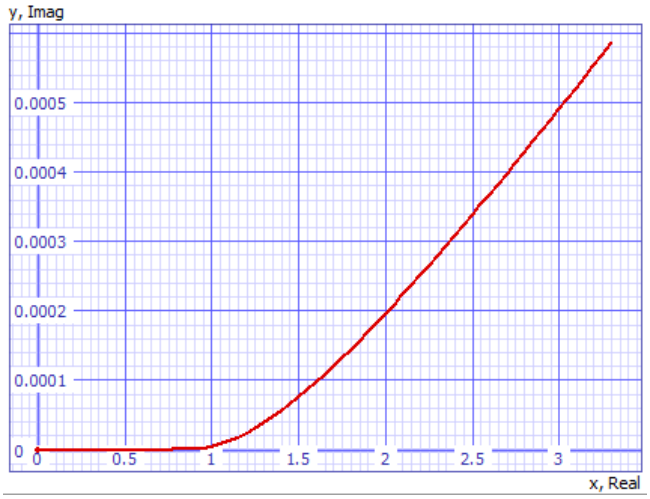


Figure 1: I_{DS} function of V_{GS} for NMOS transistor

We can define V_{tn} graphically as the limit value where I_{DS} becomes greater than 0. We get

$$V_{tn} \approx 0,87$$

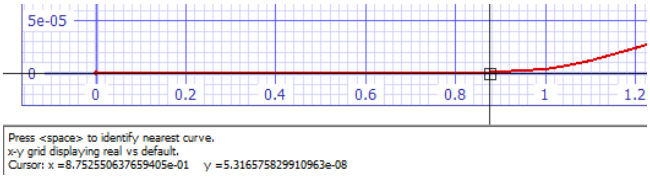


Figure 2: Determining V_{tn}

1.1.2 • PMOS transistor

In the PMOS transistor, to account for the reversed polarity we impose $V_{SD} = V_{DD} \implies V_{SD} \geq V_{SG} - V_{tp}$ where V_{tp} is negative.

Now, we expect

$$I_{DS}(V_{SD} = V_{DD}, V_{SG}) = \begin{cases} 0, & \text{if } V_{SG} < |V_{tp}| \text{ (cutoff)}, \\ -\frac{1}{2} k_p \frac{W}{L} (V_{SG} - |V_{tp}|)^2, & \text{if } V_{SG} \geq |V_{tp}| \text{ (saturation)}. \end{cases} \tag{2}$$

```
.include cmosws.mod

Vsd 2 0 dc 3.3V
Vsg 2 1 dc 1V
M1  0 1 2 2 MODP L=0.6U W=6.0U

.dc Vsg 0 3.3 50mV
.end

```

Now, we can observe a curve equivalent to that of the NMOS transistor.

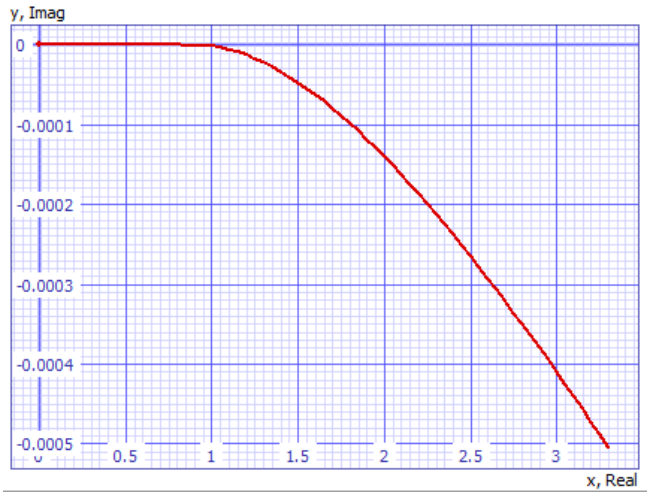


Figure 3: I_{DS} function of V_{SG} for PMOS transistor

We can identify $|V_{tp}|$ graphically as the limit value where I_{DS} becomes smaller than 0. We get

$$V_{tp} \approx -0,82$$

1.2 I_{DS} function of V_{DS}

Plot, for the two types of transistors, the graph $I_{DS}(V_{DS}, V_{GS})$ for V_{GS} constant, and for V_{DS} varying between between V_{SS} and V_{DD}. These plots will be done for several values of V_{GS}. Identify the linear and saturation domains for both types of transistors.

1.2.1 • NMOS transistor

We will use V_{GS} equal to $1V$, $2V$ and $3V$ (so we are never in the cutoff region because $V_{GS} > V_{tn}$).

Theoretically we expect

$$I_{DS}(V_{DS}, V_{GS} = \text{constant}) = \begin{cases} k_n \frac{W}{L}\left[(V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^2}{2}\right], & \text{if } V_{DS} < V_{GS} - V_{tn} \text{ (triode or linear)}, \\ \frac{1}{2} k_n \frac{W}{L}(V_{GS} - V_{tn})^2, & \text{if } V_{GS} \geq V_{tn} \text{ (saturation)}. \end{cases} \tag{3}$$

```
1       .include cmosws.mod
2
3       Vds 2 0 dc 3.3V
```

```
Vgs 1 0 dc 1V
M1  2 1 0 0 MODN L=0.6U W=3.0U

.dc Vds 0 3.3 50mV Vgs 1 3 1V
.end
```

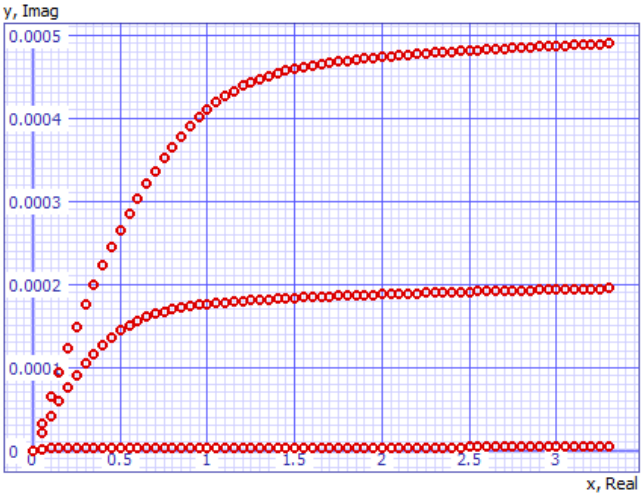


Figure 4: I_{DS} function of V_{DS} for NMOS transistor

1.2.2 • PMOS transistor

Once again for the PMOS, we make adaptions to account for reversed polarity.

We will use V_{SG} equal to $1V$, $2V$ and $3V$ (so we are never in the cutoff region because $V_{SG} > |V_{tp}|$).

Theoretically we expect

$$I_{DS}(V_{SD}, V_{SG} = \text{constant}) = \begin{cases} -k_p \frac{W}{L}\left[(V_{SG} - |V_{tp}|)V_{SD} - \frac{V_{SD}^2}{2}\right], & \text{if } V_{SD} < V_{SG} - |V_{tp}| \text{ (triode or linear)}, \\ -\frac{1}{2}k_p \frac{W}{L}(V_{SG} - |V_{tp}|)^2, & \text{if } V_{SG} \geq |V_{tp}| \text{ (saturation)}. \end{cases} \tag{4}$$

```
.include cmosws.mod

Vsd 2 0 dc 3.3V
Vsg 2 1 dc 1V
M1  0 1 2 2 MODP L=0.6U W=6.0U

.dc Vsd 0 3.3 50mV Vsg 1 3 1V
.end
```

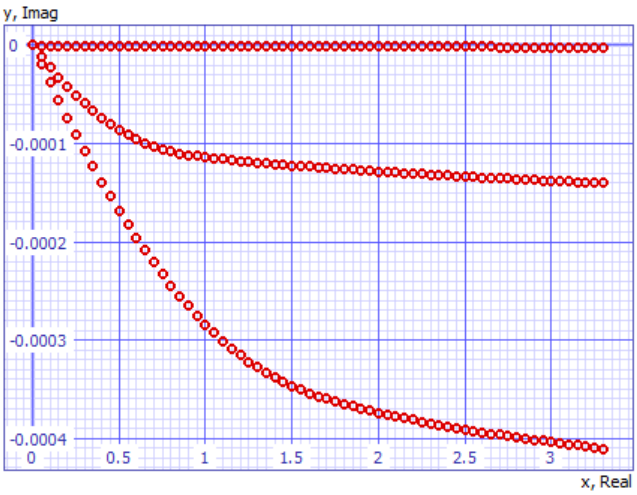
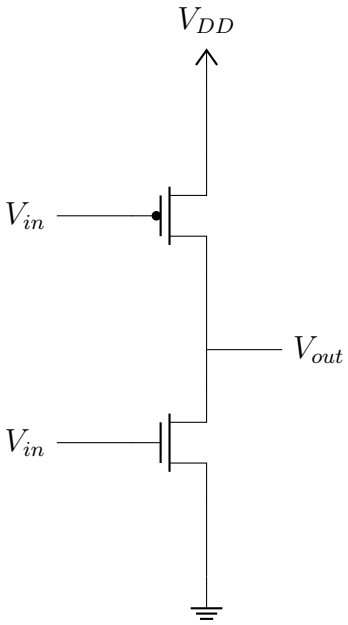


Figure 5: I_{DS} function of V_{SD} for PMOS transistor

2 CMOS INVERTER STATIC CHARACTERIZATION



2.1 Centered Inverter

Plot the static transfer function for a centered inverter. Deduce the noise margin on the input low state and high state.

```
.include cmosws.mod

Vin 1 0 dc 1V
Vdd 2 0 dc 3.3V
M1  3 1 0 0 MODN L=0.6U W=3.0U
M2  2 1 3 2 MODP L=0.6U W=6.0U

.dc Vin 0 3.3 50mV
.end

```

Figure 6: Transfer function for centered inverter

From the graphic, we have

- $V_{IL} = 0,92\text{V}$ (maximum V_{in} for which V_{out} is high)
- $V_{IH} = 2,3\text{V}$ (minimum V_{in} for which V_{out} is low)
- and we consider $V_{OL} = 0\text{V}$ and $V_{OH} = 3,3\text{V}$.

We conclude that

- $NML = V_{IL} - V_{OL} = 0,92\text{V}$
- $NMH = V_{OH} - V_{IH} = 3,3 - 2,3 = 1\text{V}$

We observe that $W_p = 2W_n$ did not give us a perfectly centered inverter, we expected $NML = NMH$.

2.2 Decentered Inverter

Plot the transfer function for a decentered inverter with

- $W_n = W_p = 3,0\mu m$
- $W_p = 12,0\mu m$ and $W_n = 3,0\mu m$

Deduce the noise margins on the input low state and high state.

For a lower value of W_p, the PMOS transistor has a smaller $g_m = \frac{\partial I_D}{\partial V_{SG}} = k_p \frac{W}{L}(V_{SG} - |V_{tp}|)$. Thus, the PMOS is less sensitive to variations in V_{SG} which makes the high-low transition slower. We expect $NML < NMH$.

Figure 7: Transfer function for decentered inverter with $W_n = W_p = 3,0\mu m$

We get from the graphic

- $V_{IL} = 0,85\text{V}$ (maximum V_{in} for which V_{out} is high)
- $V_{IH} = 2,22\text{V}$ (minimum V_{in} for which V_{out} is low)
- again we consider $V_{OL} = 0\text{V}$ and $V_{OH} = 3,3\text{V}$.

We conclude that

- $NML = V_{IL} - V_{OL} = 0,85\text{V}$
- $NMH = V_{OH} - V_{IH} = 3,3 - 2,22 = 1,08\text{V}$

Now for a higher value of W_p, the PMOS transistor has a higher $g_m = \frac{\partial I_D}{\partial V_{SG}} = k_p \frac{W}{L}(V_{SG} - |V_{tp}|)$. Thus, the PMOS is more sensitive to variations in V_{SG} which makes the high-low transition faster. We expect $NML > NMH$.

Figure 8: Transfer function for decentered inverter with $W_p = 12,0\mu m$ and $W_n = 3,0\mu m$

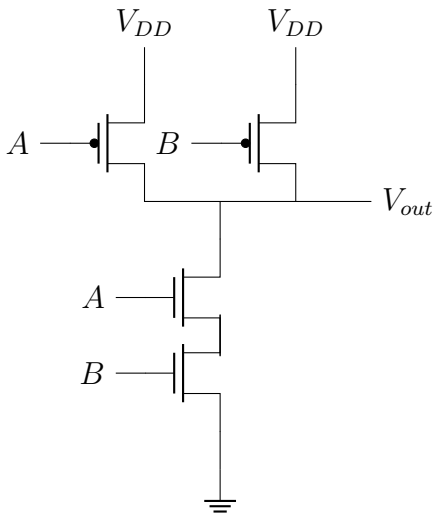
We get from the graphic

- $V_{IL} = 0,99\text{V}$ (maximum V_{in} for which V_{out} is high)
- $V_{IH} = 2,35\text{V}$ (minimum V_{in} for which V_{out} is low)
- again we consider $V_{OL} = 0\text{V}$ and $V_{OH} = 3,3\text{V}$.

We conclude that

- $NML = V_{IL} - V_{OL} = 0,99\text{V}$
- $NMH = V_{OH} - V_{IH} = 3,3 - 2,35 = 0,95\text{V}$

2.3 NAND2 transfer function



Plot the static transfer function of the NAND2 gate in the following cases:

- The entries A and B of this NAND gate are connected to the same input signal which varies from V_{SS} to V_{DD}. In this scenario the two inputs switch at the same time.
- The A input is at high state (voltage V_{DD}), and the B voltage varies from V_{SS} to V_{DD}. This corresponds to commutations which do not occur at the same time.

Deduce the noise margin on the input low state and high state.

2.3.1 • Simultaneous switch

We observe that $A = B = 0 \implies A \bar{\cdot} B = 1$ and $A = B = 1 \implies A \bar{\cdot} B = 0$. Thus, we expect the output graphic to look like an inverter and we can compute the margins like we did in the previous question.

```
.include cmosws.mod

Vdd 1 0 dc 3.3V
Vin 2 0 dc 1.0V
M1  1 2 4 1 MODP L=0.6U W=6.0U
M2  1 2 4 1 MODP L=0.6U W=6.0U
M3  4 2 5 0 MODN L=0.6U W=6.0U
M4  5 2 0 0 MODN L=0.6U W=6.0U

.dc Vin 0 3.3 50mV
```

```
.end

```

Figure 9: In red, we have inputs A and B. In green the output of the NAND2 gate.

We get from the graphic

- $V_{IL} = 0,97\text{V}$ (maximum A, B for which V_{out} is high)
- $V_{IH} = 2,32\text{V}$ (minimum A, B for which V_{out} is low)
- again we consider $V_{OL} = 0\text{V}$ and $V_{OH} = 3,3\text{V}$.

We conclude that

- $NML = V_{IL} - V_{OL} = 0,97\text{V}$
- $NMH = V_{OH} - V_{IH} = 3,3 - 2,32 = 0,98\text{V}$

2.3.2 • Non-simultaneous switch

Now we fix $A = 1$. For $B = 0$, we have $A \bar{\cdot} B = 1$ and for $B = 1$, we have $A \bar{\cdot} B = 0$. Thus, if we consider $V_{in} = B$ we have once again an inverter and we can compute the margins like we did previously.

```
.include cmosws.mod

Vdd 1 0 dc 3.3V
Va  2 0 dc 3.3V
Vb  3 0 dc 1.0V
M1  1 2 4 1 MODP L=0.6U W=6.0U
M2  1 3 4 1 MODP L=0.6U W=6.0U
M3  4 2 5 0 MODN L=0.6U W=6.0U
```

```
9       M4   5 3 0 0 MODN L=0.6U W=6.0U
10
11      .dc Vb 0 3.3 50mV
12      .end
13
```

Figure 10: In red, we have input B. In green the output of the NAND2 gate.

We get from the graphic

- $V_{IL} = 0,87\text{V}$ (maximum A, B for which V_{out} is high)
- $V_{IH} = 2,31\text{V}$ (minimum A, B for which V_{out} is low)
- again we consider $V_{OL} = 0\text{V}$ and $V_{OH} = 3,3\text{V}$.

We conclude that

- $NML = V_{IL} - V_{OL} = 0,87\text{V}$
- $NMH = V_{OH} - V_{IH} = 3,3 - 2,31 = 0,99\text{V}$

Comparing the margins calculated, we conclude that the simultaneous switch gives a more centered curve.

3
DYNAMICAL CHARACTERIZATION OF THE CMOS INVERTER

3.1 Output capacitance influence

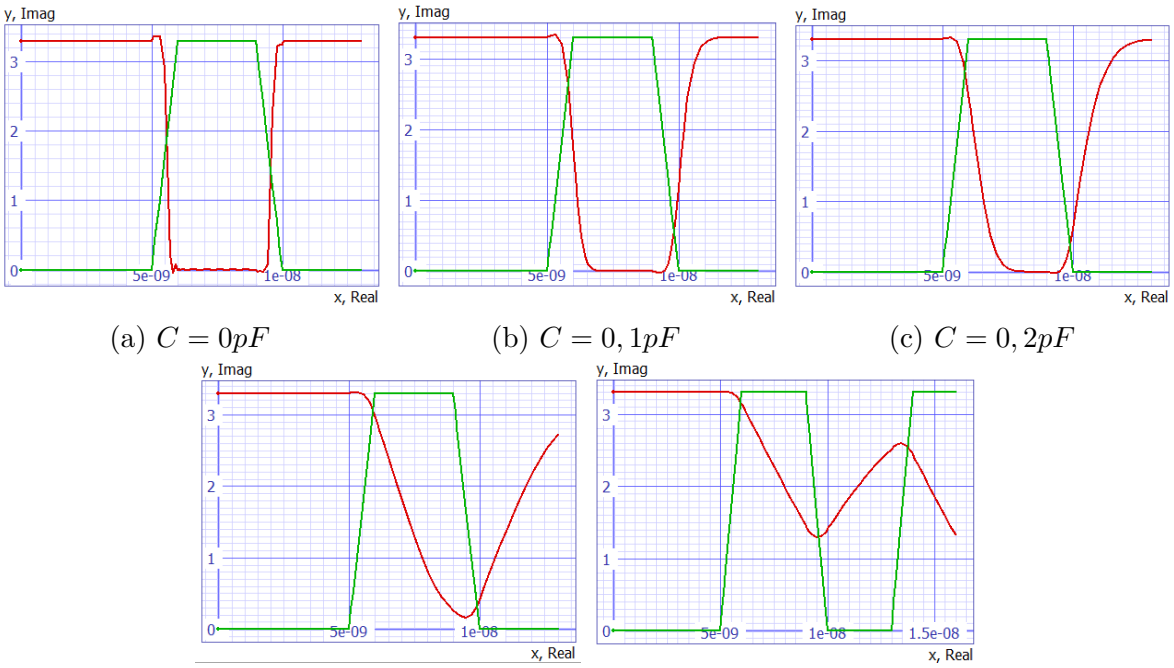
We consider a centered CMOS inverter for which the output S is connected to a charge capacitance C. This capacitance C modeled the sum of the capacitance of the input gates addressed by the signal S, plus the interconnection capacitance. We now use

- $L_n = 0,6\mu m$ and $W_n = 3,0\mu m$;
- $L_p = 0,6\mu m$ and $W_p = 6,0\mu m$;

Measure the propagation time $T_p(\text{up} \to \text{down})$ and $T_p(\text{down} \to \text{up})$ for C equal to $0.0pF$, $0.1pF$, $0.2pF$, $0.5pF$ and $1.0pF$.
Plot $T_p(C)$.

We modify the code for the centered inverter to introduce the capacitance C. I could not find support for *parameter sweep* in Spice Opus, so we must run the script with a different value of C to measure each propagation time.

```
1       .include cmosws.mod
2
3       Vin 1 0 pulse(0.0V 3.3V 5ns 1ns 1ns 3ns 8ns)
4       Vdd 2 0 dc 3.3V
5       M1  3 1 0 0 MODN L=0.6U W=3.0U
6       M2  2 1 3 2 MODP L=0.6U W=6.0U
7       C1  3 0 0.0pF
8       *C1  3 0 0.1pF
9       *C1  3 0 0.2pF
10      *C1  3 0 0.5pF
11      *C1  3 0 1.0pF
12
13      .tran 0.05ns 13ns
14      .end
15
```



(a) $C = 0pF$ (b) $C = 0,1pF$ (c) $C = 0,2pF$

(d) $C = 0,5pF$ (e) $C = 1pF$

Figure 11: Output V_{out} in red and input V_{in} in green for different values of C

C	$T_p(\text{up} \to \text{down})$	$T_p(\text{down} \to \text{up})$
$0pF$	$0,11ns$	$0,12ns$
$0,1pF$	$0,52ns$	$0,62ns$
$0,2pF$	$0,81ns$	$1,02ns$
$0,5pF$	$1,69ns$	$1,82ns$
$1pF$	$3,11ns$	$1,08ns$

Table 1: Propagation times measured in each plot

When we plot the propagation times, we observe a clear linear relation between T_p and C. We can use linear regression to plot $T_p(\text{up} \to \text{down})$ and $T_p(\text{down} \to \text{up})$. For high values of C however, it is importance to notice that because the capacitor never manages to fully decharge, $T_p(\text{down} \to \text{up})$ starts to decrease and we lose this linear behavior. The plot was made using *Python*.

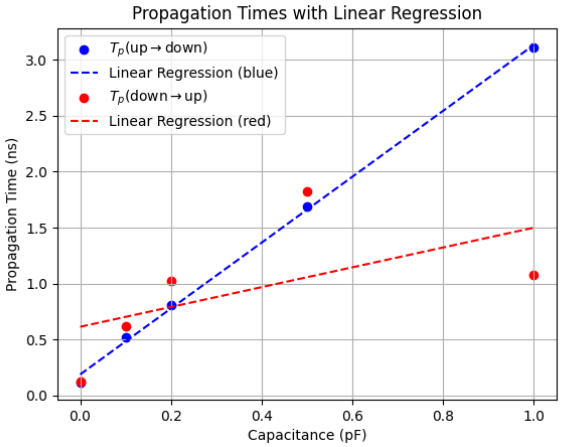


Figure 12: Propagation time T_p as function of capacitance C

3.2 W and L sizing influence

We select a charge capacitance of $0,5pF$.

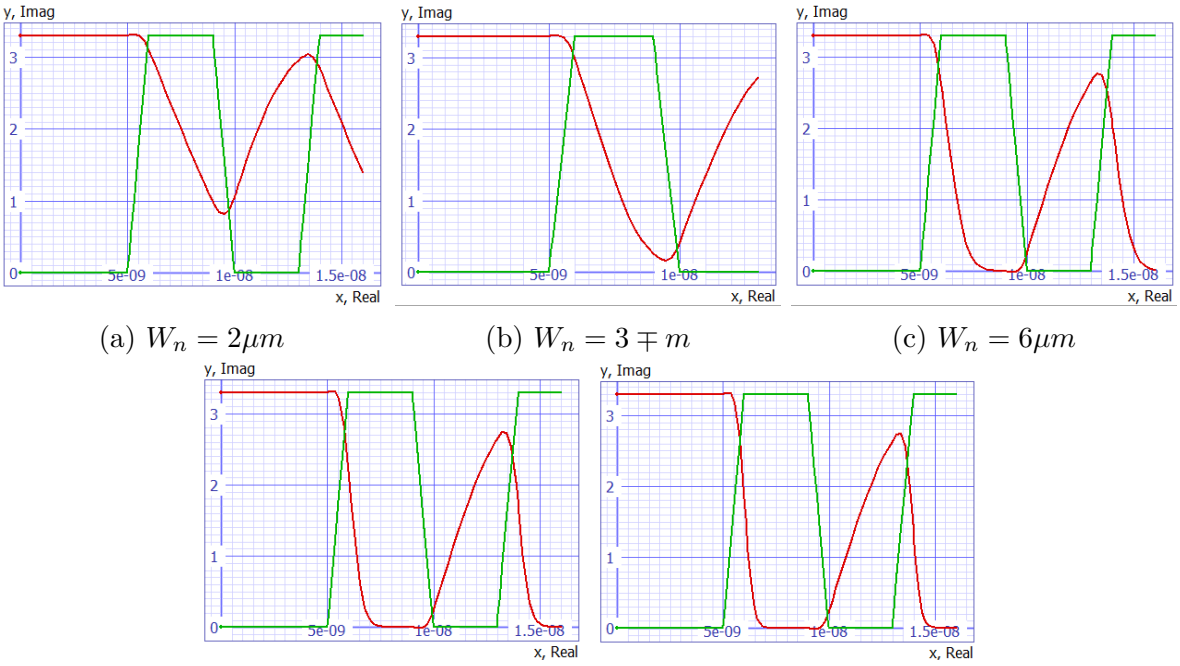
- Measure the variation of the propagation times when the resistance of the N transistor is decreased by increasing W_n. Plot the graph $T_p^{\text{up}\to\text{down}}(W_n)$.
- Measure the variation of the propagation times when the resistance of the N transistor is decreased by increasing W_n. Plot the graph $T_p^{\text{down}\to\text{up}}(W_p)$.

3.2.1 • T_p(up → down) function of W_n

The values of W_n chosen for simulation and measurement were: $2\mu m$, $3\mu m$, $6\mu m$, $9\mu m$, $12\mu m$. I tried $W_n = 1\mu m$ but for low values of W_n, the output does not even reach $\frac{V_{DD}}{2}$.

W_n	T_p(up → down)
$2\mu m$	$2,48ns$
$3\mu m$	$1,69ns$
$6\mu m$	$0,91ns$
$9\mu m$	$0,69ns$
$12\mu m$	$0,56ns$

Table 2: Propagation time measured for each value of W_n



(a) $W_n = 2\mu m$ (b) $W_n = 3 \mp m$ (c) $W_n = 6\mu m$

(d) $W_n = 9\mu m$ (e) $W_n = 12\mu m$

Figure 13: Output V_{out} in red and input V_{in} in green for different values of W_n

When we plot $T_p(\text{up} \to \text{down})$ as a function of W_n, we observe that $T_p(\text{up} \to \text{down})$ seems to decrease exponentially and for large values of W_n it approaches some constant. Therefore, the appropriate fit is

$$T_p^{\text{up}\to\text{down}}(W_n) = a \cdot e^{-bW_n} + c$$

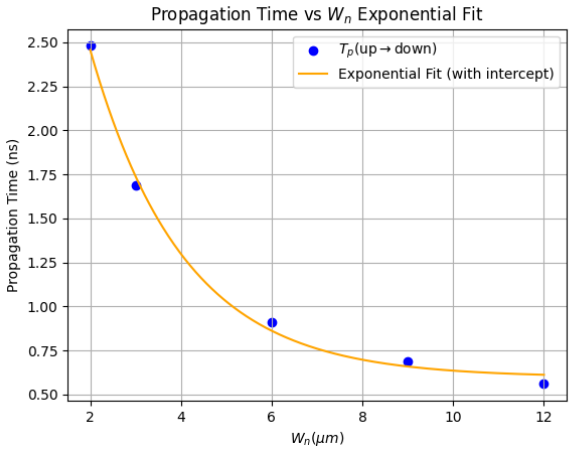


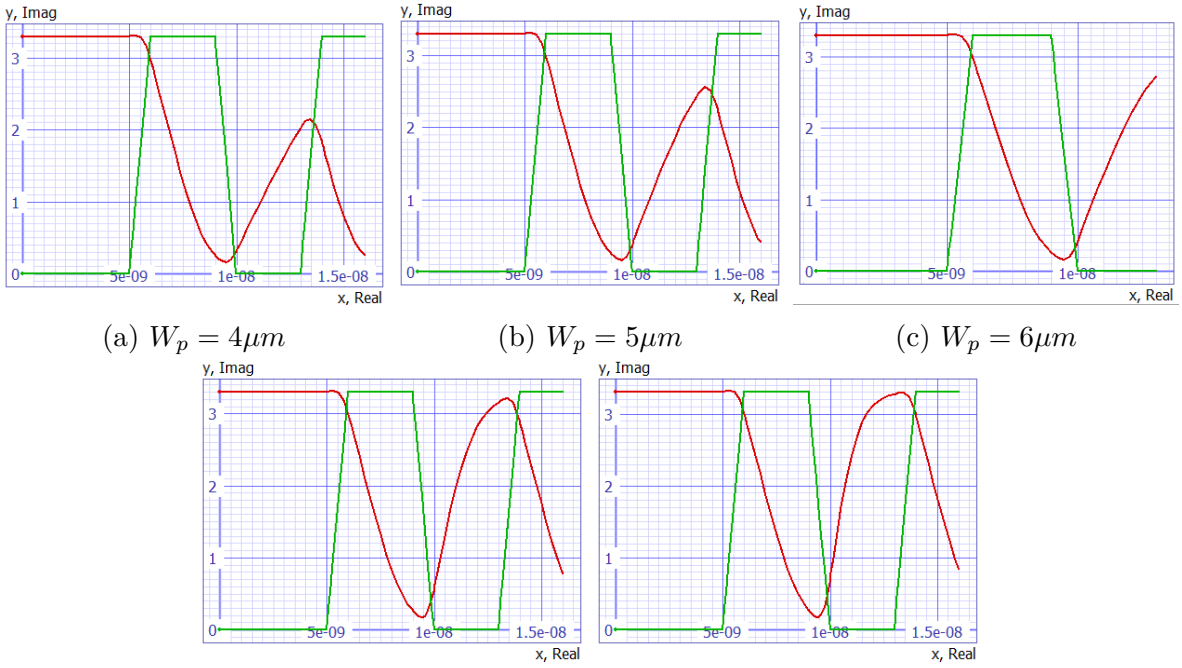
Figure 14: Propagation time $T_p(\text{up} \to \text{down})$ as function of W_n

3.2.2 • T_p(down → up) function of W_p

The values of W_p chosen for simulation and measurement were: $4\mu m$, $5\mu m$, $6\mu m$, $9\mu m$, $12\mu m$. I tried $W_p = 3\mu m$ but similarly to what we verified for W_n, for low values of W_p, the output does not even reach $\frac{V_{DD}}{2}$.

W_p	T_p(down → up)
$4\mu m$	$2,82ns$
$5\mu m$	$2,22$
$6\mu m$	$1,81ns$
$9\mu m$	$1,31ns$
$12\mu m$	$1,01ns$

Table 3: Propagation time measured for each value of W_p



(a) $W_p = 4\mu m$ (b) $W_p = 5\mu m$ (c) $W_p = 6\mu m$

(d) $W_p = 9\mu m$ (e) $W_p = 12\mu m$

Figure 15: Output V_{out} in red and input V_{in} in green for different values of W_p

Now, when we plot T_p(down → up) as a function of W_p, we observe that T_p(down → up) seems to decrease exponentially and for large values of W_p it approaches some constant. Therefore, the appropriate fit is

$$T_p^{\text{down}\to\text{up}}(W_p) = a \cdot e^{-bW_p} + c$$

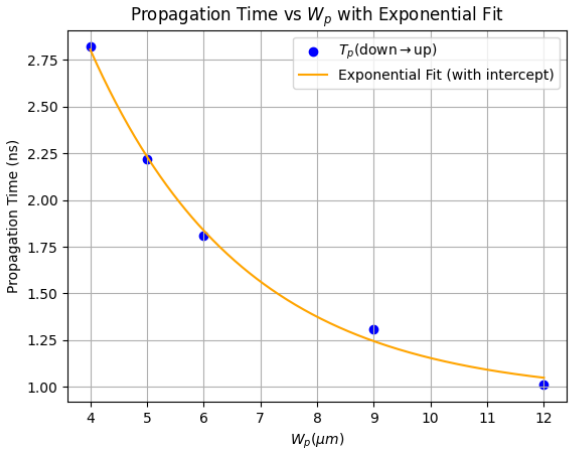
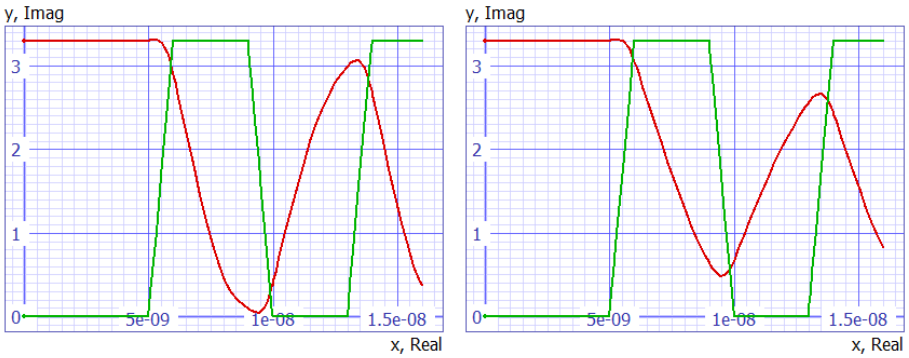


Figure 16: Propagation time $T_p(\text{down} \rightarrow \text{up})$ as function of W_p

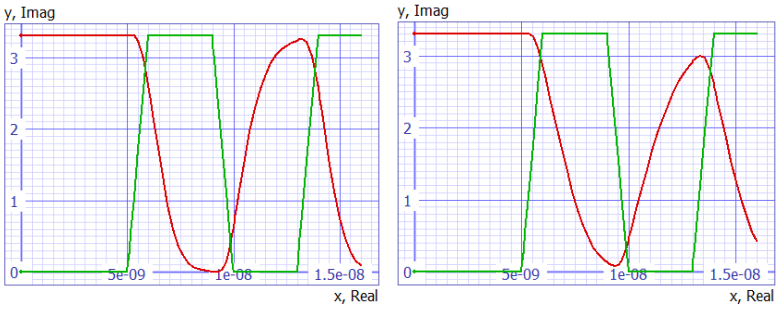
3.3 Temperature and threshold voltage influence

Measure the variation of the propagation time for the reference inverter($W_n = 3\mu m$ and $W_p = 6\mu m$) for an output capacitance C of $0,5pF$ in the four following cases:

- -40°C, worst case
- $+125$°C, worst case
- -40°C, typical
- $+125$°C, typical



(a) $-40°C$, worst case (b) $+125°C$, worst case



(c) $-40°C$, typical (d) $+125°C$, typical

Figure 17: Output V_{out} in red and input V_{in} in green in all 4 scenarios

	$-40°C$	$+125°C$
worst case	$1,43ns$	$2,07ns$
typical	$0,99ns$	$1,43ns$

Table 4: $T_p(\text{down} \to \text{up})$ measured in all 4 scenarios

	$-40°C$	$+125°C$
worst case	$1,61ns$	$1,91ns$
typical	$1,11ns$	$1,61ns$

Table 5: $T_p(\text{up} \to \text{down})$ measured in all 4 scenarios

We observe that $T_p(\text{down} \to \text{up})$ and $T_p(\text{up} \to \text{down})$ are bigger for the worst case parameters as expected. And they are also bigger at higher temperatures, which we also expected because heating causes the transistor's performance to deteriorate.