

# MICRO AND NANO ELECTRONICS EXPERIMENTAL DESIGN

PHY\_51173\_EP

December 2024

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## INTRODUCTION

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As the demand for energy-efficient and high-performance chips accelerates, the semiconductor industry faces an ever-growing challenge : scaling down transistors while minimizing power consumption and maintaining reliability. Although CMOS technology has been the cornerstone of microelectronics for decades, it is now approaching its physical and practical limits. As transistors are scaled down to nanometer dimensions, issues such as increased leakage currents, higher power densities, and reduced switching efficiency have become significant barriers. Furthermore, the variability in manufacturing at smaller scales and the rising cost of fabrication pose additional challenges. These limitations drive the search for alternative technologies capable of sustaining advancements in performance, efficiency, and miniaturization.

One promising solution is carbon nanotube field-effect transistors (CNTFETs), which leverage the unique properties of carbon nanotubes, such as their interesting electrical properties, nanoscale dimensions, and low-power operation. However, despite their theoretical advantages, the practical realization of CNTFETs faces numerous challenges, particularly in achieving consistent fabrication processes and scalable integration.

**This report presents our experimental project focused on the fabrication of CNTFET devices.** We will explain the underlying theory, outline the fabrication steps, and analyze the results obtained from the project.

We recorded videos explaining the experimental methodology for the *electron beam vapor deposition* and for CVD. We also have videos from our first SEM session with Prof. Costel. You can click on the links below :

- Molecular beam evaporation (metallic catalysts for CNT synthesis) part 1
- Molecular beam evaporation (metallic catalysts for CNT synthesis) part 2
- Chemical vapor deposition (CVD for CNT synthesis)
- Scanning electron microscopy (SEM, carbon nanotubes on silica) part 1
- Scanning electron microscopy (SEM, carbon nanotubes on silica) part 2
- Verification of photolithography results on SEM
- Characteristic curve for P type CNFET

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## CNTFET PRINCIPLE AND EXPERIMENT CORE IDEAS

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Carbon nanotubes (CNTs) are cylindrical structures composed of carbon atoms arranged in a hexagonal lattice, similar to graphene, but in a tube configuration. Not only do they have very remarkable mechanical properties, but they also have unique electronic properties that make some suitable for use in transistors. The electronic characteristics of CNTs, such as whether they behave as conductors or semiconductors, are highly dependent on their diameter and the way they are rolled. This property is described by the chirality of the nanotube, which defines its electronic band structure. Thinner CNTs with specific chiralities tend to exhibit semiconductor-like behavior, while wider CNTs can act as metals.

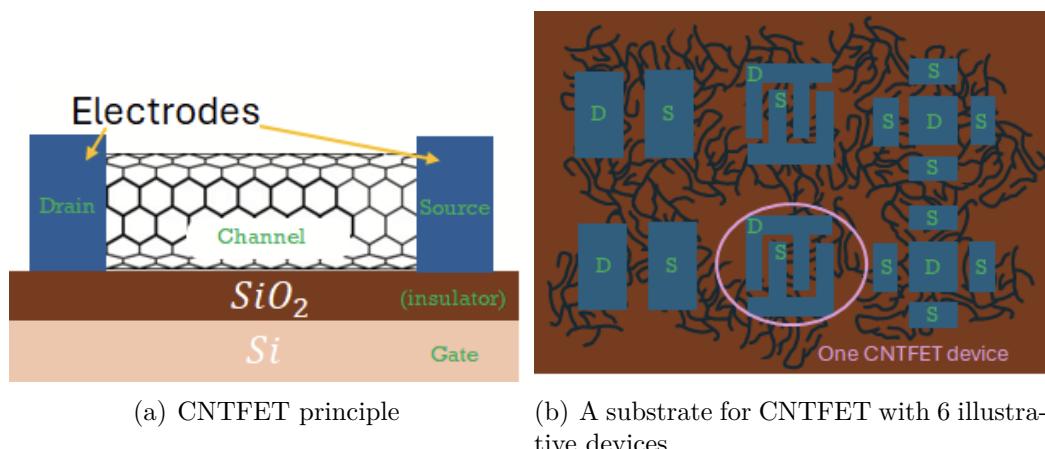


FIGURE 1 – CNTFET on a  $S_i$  substrate principle.

Carbon nanotube field-effect transistors operate on principles similar to those of CMOS transistors but leverage the unique properties of carbon nanotubes as the channel material. In a CNTFET, a semiconducting carbon nanotube replaces the traditional silicon channel used in CMOS devices. The gate electrode controls the flow of charge carriers (electrons or holes) through the carbon nanotube, modulating the current between the source and drain terminals. Like in CMOS transistors, applying a voltage to the gate creates an electric field that determines whether the channel is conductive or insulating. The accompanying subfigure 1(a) illustrates the basic principle, with the CNT forming the channel between the source and the drain, and a silicon dioxide layer acting as the dielectric insulator to separate the silicon gate. In our experiment, CNTFETs were integrated into substrates with multiple devices (pair of electrodes), as shown in the second subfigure 1(b). This configuration enables only one gate and one channel for the whole sample and thus does not enable scalability for a circuit involving multiple gates as it is, but it enables testing devices with various electrode configurations such as varying distance between the electrodes (we will discuss this more in depth in section 2.2.2).

The key advantage of CNTFETs lies in their combination of high electron mobility, small size, and low power consumption, enabling them to outperform traditional MOSFETs in critical areas. With ballistic electron transport in carbon nanotubes—where the mean free path can be up to 50 times longer than in silicon—CNTFETs experience minimal electron scattering, resulting in significantly reduced energy dissipation. This allows for operation at higher speeds with potentially up to 10 times lower energy consumption. Their nanoscale dimensions and low threshold voltage further enable faster switching (up to 3 times faster) and reduced parasitic losses. Additionally, CNTs exhibit exceptional thermal conductivity, preventing overheating and eliminating the need for extensive cooling systems. The high electron mobility of CNTs (over  $10,000, \text{ cm}^2/\text{V} \cdot \text{s}$ , compared to  $1,400, \text{ cm}^2/\text{V} \cdot \text{s}$  in silicon) supports efficient current drive even at small sizes, maintaining low resistance during operation.

# 1

## METAL CATALYST DEPOSIT ON THE SUBSTRATE

In the experimental setup, there were two chambers. The first step was fixing the silicon wafer on a platform by screwing in some metallic wires to hold the wafer in place. This step is important because we will rotate the wafer upside down before moving it into the second chamber for the deposition.

Then, we closed the lid to the first chamber and verified that the secondary pump was properly isolated from the first chamber. Then we turned on the primary vacuum pump until a pressure of  $10^{-2}$ mbar was reached. At this pump we activated the secondary pump to reach pressures under  $10^{-6}$ mbar.

After pressure was equalized in both chambers, we opened the valve connecting the chambers. Together with this valve, the first chamber effectively acts as a transition chamber which allows keeping a very low pressure of  $10^{-8}$  mbar in the second chamber. Then, we moved the silicon wafer into position in the second chamber before closing this connection again. For each deposition, we raised the wafer up the  $z$  axis, and then moved the crucibles into the right position.

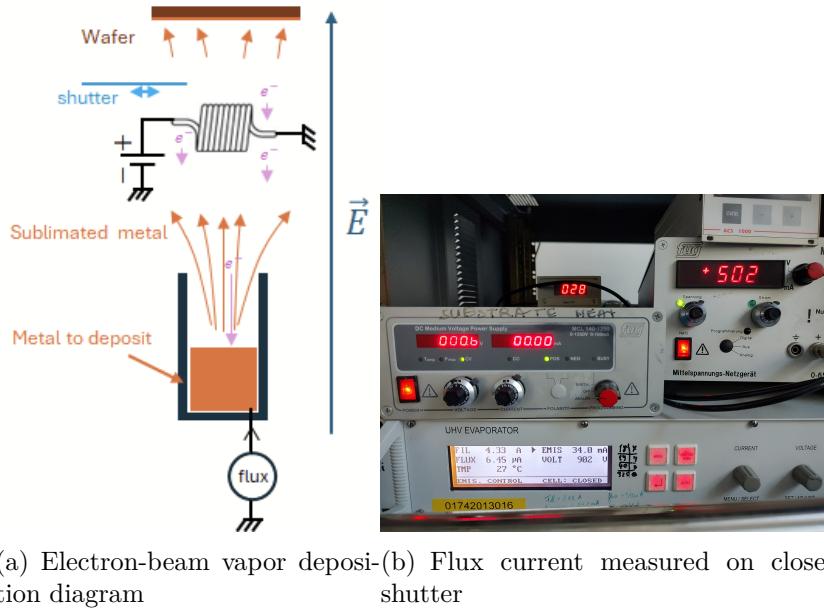
### 1.1 THEORY AND PROTOCOL

The conventional method to synthesize carbon nanotubes uses metallic catalysts. In the next section, we will discuss the importance of these metallic catalysts. But for now, let's focus on the deposition procedure.

In our project, we used a *electron beam vapor deposition* procedure to slowly deposit layers of a given metal with thicknesses in the nanometer range. For each wafer, we deposited two metal layers : first, a sacrificial layer of  $\text{Al}_2\text{O}_3$  and second, a layer of Fe (we also experimented with Co and Ni).

Figure 2(a) illustrates the setup inside the vacuum chamber. We aligned along the  $z$  axis : the crucible containing the desired metal, the shutter and the silicon wafer. To heat the crucible we utilized a metallic filament (made of tungsten because of its high melting temperature  $3422^\circ$ , good electrical conductivity and chemical inertia). By applying a high current on the filament, its temperature increases because of the Joule effect. When heated up, the filament emits electrons which are accelerated thanks to an electric field. Some of the electrons which have built up kinetic energy may then collide with the target metal contained in the crucible, which heats up the metal.

The process is done under vacuum (around  $10^{-8}$  mbar) which allows the electrons to reach the crucible with higher probability (do not collide with air), but also enables the metals not to liquefy but to be sublimated into a gas that will allow homogeneous deposition. The flow of



(a) Electron-beam vapor deposition diagram  
(b) Flux current measured on closed shutter

FIGURE 2 – Metal catalyst deposit principle

electrons coming to the crucible can be measured as a current called flux. Measuring this flux current, we can calculate the rate of deposition of the metal particles to determine when the desired thickness is reached and close the shutter.

There are two important calculations here :

- estimating the desired thickness to cover the wafer with the desired density of metal atoms ;
- and calculating the open shutter time for deposition, so we deposit the desired thickness.

### 1.1.1 • CALCULATING THICKNESS OF METAL LAYERS

We assume uniform deposition of the metal particles on the wafer.

We decided as a first reference to use a full monolayer of alumina and 0.1 monolayer of iron (see 1.1.2 to explain what we mean as less than 1 monolayer). These parameters allow good mobility of the iron atoms in the holes we will create in the sacrificial alumina layer.

Let  $n_A$  denote the number of atoms in the metallic layer,  $V_A$  denote the volume of a metallic atom,  $R$  denote the wafer radius and  $\epsilon$  denote the thickness of the layer. We can compute the volume of the layer in two ways

$$n_A \cdot V_A = \pi R^2 \cdot \epsilon \implies \epsilon = \frac{n_A \cdot V_A}{\pi R^2}$$

We suppose that the density of atoms in a monolayer is  $10^{16} \frac{\text{atoms}}{\text{cm}^2}$ . The silicon wafers we used had a radius  $R = 2.5\text{cm}$ , so the number of metallic atoms we want to deposit in each layer is

$$n_A = (6.25 \text{ cm}^2) \times \left( 10^{16} \frac{\text{atoms}}{\text{cm}^2} \right) = 6.25 \cdot 10^{16} \text{ atoms}$$

The atomic radius for an isolated alumina molecule is  $r_{\text{Al}_2\text{O}_3} = 215 \text{ pm}$  and for an iron atom  $r_{\text{Fe}} = 126 \text{ pm}$ . Thus, the volume of each deposited metallic particle, is

$$\begin{cases} V_{\text{Al}_2\text{O}_3} = \frac{4}{3}\pi r_{\text{Al}_2\text{O}_3}^3 = 4.16 \cdot 10^{-29} \text{ m}^3 \\ V_{\text{Fe}} = \frac{4}{3}\pi r_{\text{Fe}}^3 = 8.38 \cdot 10^{-30} \text{ m}^3 \end{cases} \quad (1)$$

Finally, we compute the thicknesses

$$\begin{cases} \epsilon_{\text{Al}_2\text{O}_3} = \frac{(6.25 \cdot 10^{16} \text{ atoms}) \cdot (4.16 \cdot 10^{-29} \text{ m}^3)}{\pi \cdot (6.25 \cdot 10^{-4} \text{ m}^2)} = 1.3 \text{ nm} \\ \epsilon_{\text{Fe}} = \frac{(6.25 \cdot 10^{16} \text{ atoms}) \cdot (8.38 \cdot 10^{-30} \text{ m}^3)}{\pi \cdot (6.25 \cdot 10^{-4} \text{ m}^2)} = 0.26 \text{ nm} \end{cases} \quad (2)$$

On our first wafer, we used

$$\begin{cases} \epsilon_{\text{Al}_2\text{O}_3} = 1 \text{ nm} \\ \epsilon_{\text{Fe}} = 0.15 \text{ nm} \end{cases} \quad (3)$$

On subsequent wafers, we tried variations of these parameters. We made a wafer with  $\epsilon_{\text{Al}_2\text{O}_3} = 4 \text{ nm}$  and several wafers with different iron thicknesses  $\epsilon_{\text{Fe}} = 0.1 \text{ nm}$ ,  $\epsilon_{\text{Fe}} = 0.075 \text{ nm}$ ,  $\epsilon_{\text{Fe}} = 0.05 \text{ nm}$ .

To test metals with lower reactivities, we tried to replace iron with cobalt and nickel but we did not observe nano tubes in these two samples. For further experimentation, one could try increasing the thicknesses  $\epsilon_{\text{Co}}$  and  $\epsilon_{\text{Ni}}$  to account for the smaller formed cluster sizes.

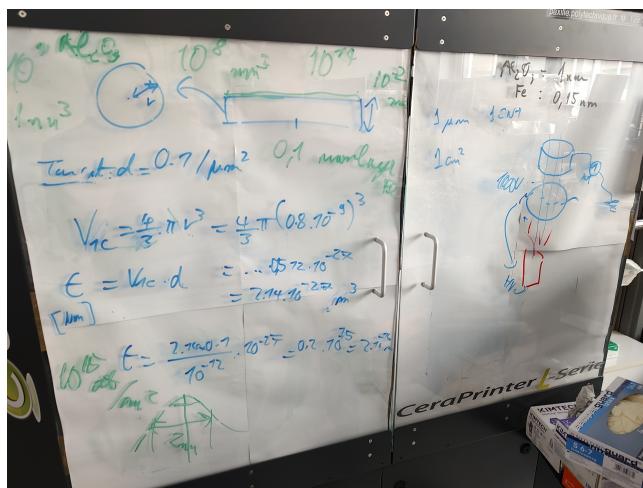


FIGURE 3 – Layer thickness calculation on our first sample with 1nm  $\text{Al}_2\text{O}_3$  and 0.15nm Fe.

### 1.1.2 • CALCULATING OPEN SHUTTER TIME

Using molecular beam of electron beam evaporation deposition procedures, there is a simple relationship linking target deposited thickness  $\epsilon$ , the flux  $I_{\text{flux}}$  and duration  $t$ . Indeed, we have

$$\epsilon = I_{\text{flux}} \cdot t \cdot C_{\text{evap}}$$

where  $C_{\text{evap}}$  is a constant value which is given for each metal for the specific setup we could use.

Materials	Al <sub>2</sub> O <sub>3</sub>	Fe
Crucible position (x,y,z) (mm)	(19.5, -6, -2)	(39, 5, -2)
Beam evaporation constant $C_{\text{evap}}$ (nm·μA <sup>-1</sup> ·s <sup>-1</sup> )	0.046	0.026

The deposition time is given by  $t = \frac{\epsilon}{I_{\text{flux}} \cdot C_{\text{evap}}}$ . Before starting deposition, we must first select the metal we want to deposit by displacing the movable crucible set to target coordinates to align the crucible with the wanted material with the setup. Immediately after opening the shutter, we used the flux value to compute  $t$ .

For example, a typical measurement for alumina is  $I_{\text{flux}} = 100\text{nA}$ . So, for  $\epsilon_{\text{Al}} = 1\text{nm}$ , we have

$$t_{\text{Al}_2\text{O}_3} = \frac{1\text{nm}}{100\text{nA} \cdot 0.046\text{nm} \cdot \mu\text{A}^{-1} \cdot \text{s}^{-1}} = 217\text{s} = 3\text{min}37\text{s}$$

after this time elapsed, we closed the shutter to stop the deposition.

### 1.1.3 • ABOUT SUB-NANOSCALE DEPOSITION

In the above computations, we assumed that matter deposition is continuous, with the ability to deposit a layer of any depth. However we have considered depositing as little as  $0.05\text{nm}$  of  $F_e$ , which at these scales make no real sense. Indeed for iron, as the atomic radius is  $r_{Fe} = 0.126\text{nm}$ , the height of a monolayer would be  $2r_{Fe} = 0.252\text{nm}$  which means that we would deposit a film of height below one monolayer. Thus, when we use the denomination  $0.05\text{nm } Fe$ , we in fact mean that we have deposited a fraction of the necessary atoms which would be needed to the first atomic layer, leaving a  $\frac{0.05}{0.252} = 20\%$  filled area.

## 2

# CARBON NANOTUBE GROWTH

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Here the experimental setup had only one chamber. However, the same procedure was followed to set the vacuum. First, we made sure the secondary pump was isolated to avoid contamination (if this step was not performed, it took a long time to get the secondary pump back to its pressure level). We also checked that the hydrogen and methane flows into the chamber were closed. Then, we turned on the primary pump to reach  $10^{-3}$ mbar. Then we activated the secondary pump to reach pressures below  $10^{-8}$ mbar, and then we isolated the pump again.

### 2.1 THEORY AND PROTOCOL

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In our project, we used a *chemical vapor deposition* (CVD) procedure to grow CNTs using metallic catalysts [1] [2]. As discussed in the introduction, the silica layer is an insulator, separating the active terminals of the CNFET from the silicon substrate. In addition, it also has important properties for CVD :

- The silica surface of a wafer has a very flat surface allowing for uniform deposition of the metal particles. Imperfections on the surface could cause aggregation of the catalysts in certain regions of the wafer, which could result in reduced cluster formation thus reduced CNT yield and non-uniform growth of CNTs.
- Silica is stable in the temperature range inside our vacuum chamber (up to  $800^\circ$ ).
- Silica does not chemically interact with the catalysts, the carbon structures or the gases used during the growth.

Now, before we discuss the CVD procedure and the formation of the nanotubes, let's discuss the chemical differences between graphene and carbon nanotubes to explain what needs to happen on the wafer to allow nanotubes to form.

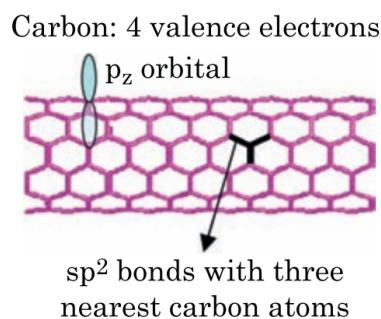


FIGURE 4 –  $sp^2$  hybridization in carbon nanotube structure

### Chemistry behind the formation of carbon nanotubes

In carbon, the  $2s$  and  $2p$  valence orbitals can interact to form hybridized orbitals. The different types of hybridization ( $sp$ ,  $sp^2$  or  $sp^3$ ) affect the bond angles between carbon atoms.

Let's consider methane for example. In methane, the  $s$  orbital and the three  $p$  orbital in the valence layer interact to form four hybridized  $sp$  orbitals. By symmetry, we see that this implies a tetrahedral structure, with carbon in the center and the hydrogen atoms in the vertices.

In both graphene and carbon nanotubes, we observe  $sp^2$  hybridization. Again by symmetry, this means we have three planar  $sp$  orbitals separated by an angle of  $120^\circ$  and an unhybridized higher-energy  $p$  orbital perpendicular to this plane (this orbital will curve to participate in the curved double bond we observe for each carbon in the structure). A graphene sheet is flat because the  $120^\circ$  angles in the hexagons match the angle separating the  $sp$  orbitals.

Thus, on our flat wafer, the deposition of carbon atoms will produce a perfectly flat graphene structure. To allow for the formation of carbon nanotubes, we need to introduce defects in the hexagonal graphene structure. Pentagonal or heptagonal faces will alter the bond angles of some carbon atoms in the structure  $\Rightarrow$  the structure will bend into a 3D configuration.

In CVD, first we will introduce hydrogen into the vacuum chamber. The hydrogen will interact with the oxygen atoms in the alumina. When the alumina particles leave the wafer, they leave behind holes in the surface. Because of the rising temperature, the iron atoms are agitated and will start to move to occupy these holes effectively forming clusters where CNTs will be able to form. When we introduce methane into the vacuum chamber, the carbon atoms deposited on top of the iron particles will form curved structures.

Now, let's discuss the exact numerical parameters and methodology used in the experiment.

In order to introduce the gases into the chamber, we used *mass flow controllers* receiving an input voltage to control their output flow, measured in *sccm* (standard cubic centimeters per minute).

For example, the valve on the  $H_2$  controller was calibrated for a maximum flow of 100 sccm at an input of 10 volts. We applied 30% of this max flow rate, that is 30 sccm.

For example, the valve on the  $CH_4$  controller was calibrated for a maximum flow of 50 sccm at an input of 10 volts. We applied 20% of this max flow rate, that is 10 sccm.

We agreed to keep this proportion of 3  $H_2$  molecules for every methane molecule for all the CVD procedures we performed. All of the wafers had the same carbon deposition conditions.

We started the hydrogen value and simultaneously started heating the chamber. In approximately 2 minutes, the temperature measured in the chamber went from  $200^\circ$  to  $800^\circ$ . At this point, we kept tried our best to the temperature constant at  $800^\circ$  and started the methane flow into the chamber.

For temperatures above  $900^\circ$ , carbon nanotubes experience thermal decomposition. So there is no CNT growth which is to be avoided.

Once the methane flow into the chamber started, we set a timer to control the carbon

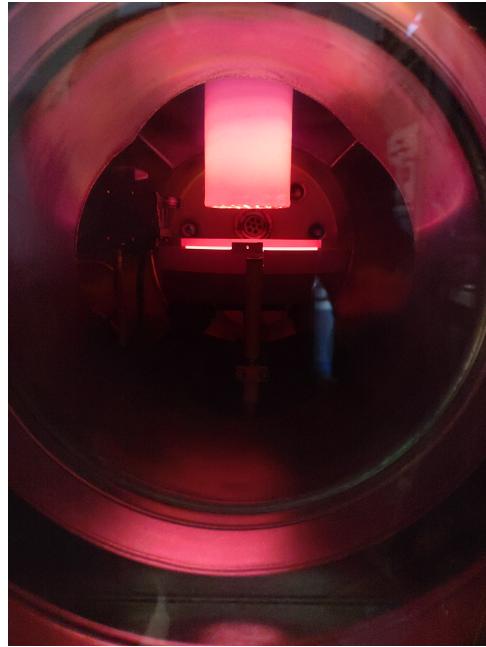


FIGURE 5 – Vacuum chamber during CVD procedure

deposition time. For the majority of the samples, we used a 30 minutes deposition time but we also experimented with 1 hour to check the impact on the resulting carbon nanotube density.

During the whole growth process, we maintained a pressure of 3 mbar.

## 2.2 RESULTS

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Two approaches were used to verify the growth of CNTs on the wafer :

- *Raman spectroscopy* ;
- *Scanning Electron Microscopy* (SEM)

### 2.2.1 • RAMAN SPECTROSCOPY

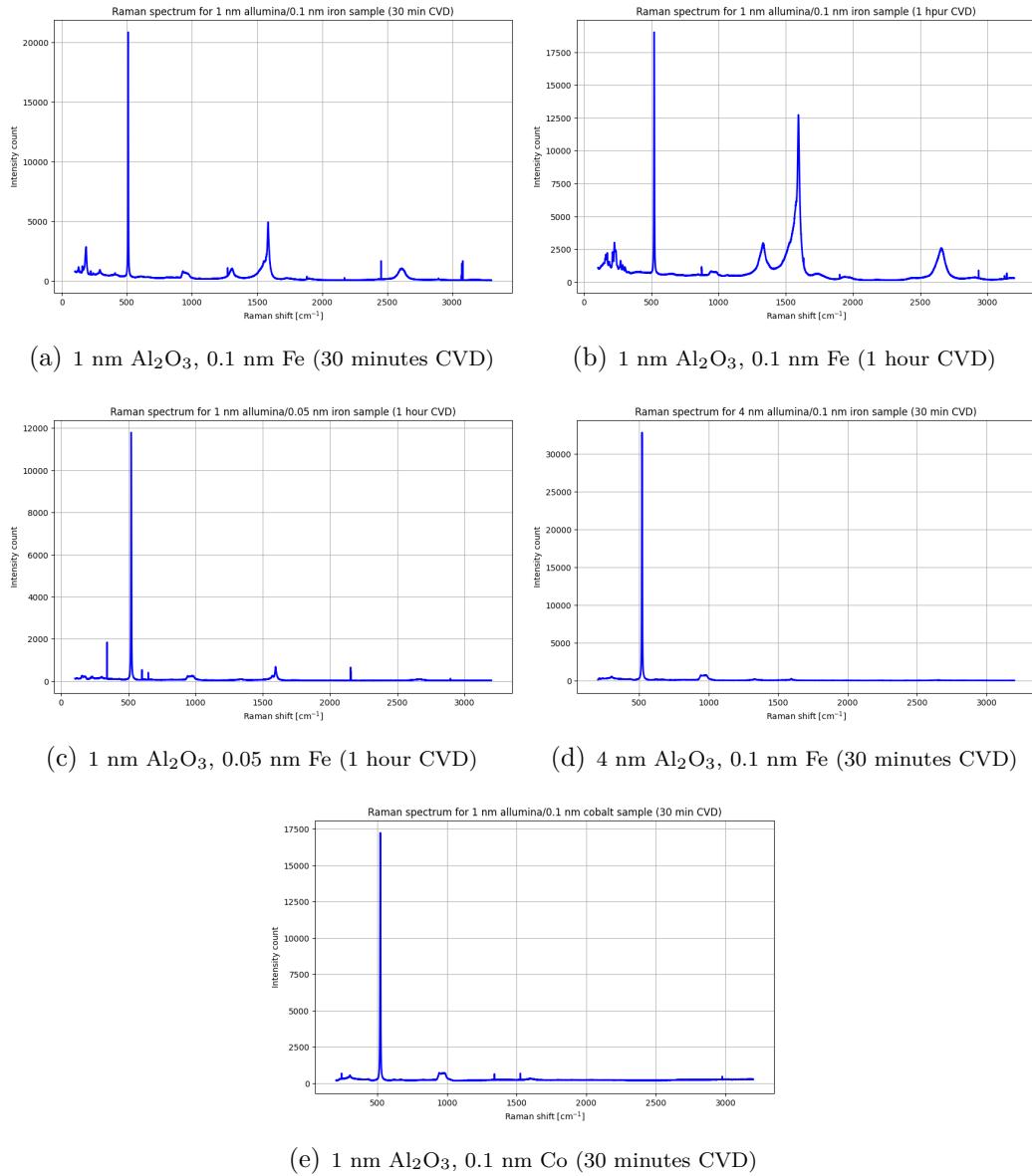


FIGURE 6 – Raman spectroscopy plots

Raman spectroscopy allows identifying chemical structures through a light scattering technique. The sample is hit with a high intensity laser source of wavelength  $\lambda_{\text{laser}}$ . Most of the scattered light also has wavelength  $\lambda_{\text{laser}}$   $\Rightarrow$  does not provide information about the sample, this is called *Rayleigh scattering*. But, a very small percentage of the light is scattered at different wavelengths depending on the chemical structure of the sample, this is called *Raman scattering*.

The new lines appearing in the spectrum of the scattered light are symmetrical with respect

to  $\lambda_{\text{laser}}$ [3], called the *Rayleigh line* in the spectrum. We can express the wavelength of two symmetrical lines in the Raman spectrum by  $\lambda = \lambda_{\text{laser}} \pm \Delta\lambda_{\text{Raman}}$ . The quantity  $\Delta\lambda_{\text{Raman}}$  is called the *Raman shift*.

So in Raman spectrum plots, we do not characterize the new scattered light lines by their frequency or wavelength but by their *Raman shift* with respect to the source laser.

Each peak we observe in a Raman spectrum corresponds to the vibration of a specific molecular bond hit by the source laser. In our spectrums, we are interested in four regions of the plot :

- one associated with the silica substrate at  $\Delta\lambda_{\text{Raman}} = 500\text{cm}^{-1}$ ;
- one associated with the radial vibration (expansion and contraction) of the nanotube diameter at  $\Delta\lambda_{\text{Raman}} = 100\text{cm}^{-1}$  (this is called the *radial breathing mode*);
- one associated with the  $\text{sp}^2$  bonds between carbon atoms. In graphene we see a single, sharp peak at  $\Delta\lambda_{\text{Raman}} = 1580\text{cm}^{-1}$ , and in carbon nanotubes we see two peaks at  $\Delta\lambda_{\text{Raman}} = 1560\text{cm}^{-1}$  and  $\Delta\lambda_{\text{Raman}} = 1590\text{cm}^{-1}$ . This is called the *graphitic band* or *G-band*.
- one small peak at  $\Delta\lambda_{\text{Raman}} = 1350\text{cm}^{-1}$  depending on the defects in the nanotubes. This is called the *defect band* or *D-band*.

In the sample 6(b), with 1 nm  $\text{Al}_2\text{O}_3$  and 1 nm Fe with 1 hour CVD ; we observe very clearly the *radial breathing modes* at  $100 - 350\text{cm}^{-1}$ , and a very clear *G-band*. We can conclude that in these control conditions, the growth of carbon nanotubes was sucessful.

Now in the sample 6(a), where we reduced the CVD time to 30 minutes ; we observe that the growth of carbon nanotubes was not as succesful. We can still see peaks associated with the *radial breathing modes* and the *G-band* but they are not as strong as in sample 6(b). We can conclude that the CVD time has a direct impact on the growth of carbon nanotubes. Of course, to determine which of the two samples has a good concentration for making CNFET devices, we need to move on to the next stage of our project.

In the remaining samples shown, the growth of CNTs was probably a failure. When we reduced the thickness of the iron layer by half to 0.05nm in sample 6(c), the *G-band* disappeared which is a clue that no CNTs were formed.

In sample 6(d), where we used a 4nm alumina layer, there was also no observable growth. However in this specific sample, we suspect an error was made during the deposition of the metallic catalyst layers. So the results do not allow us to make a conclusion about the ideal alumina layer thickness.

And finally, in sample 6(e), where we used a 1nm cobalt layer instead of iron ; there was also no observed growth. We observed the same results with Nickel. This may indicate that, when using a less active catalyst, it is necessary to use a longer CVD time. We observed that growth in iron had difficulties with 30 minutes, so it is logical that cobalt and nickel had problems since thise metals are known as less capable catalysts.

## 2.2.2 • SCANNING ELECTRON MICROSCOPY (SEM)

We got to analyse more samples in the SEM than in Raman, however here our results are not based on a numerical metric but on visual evidence.

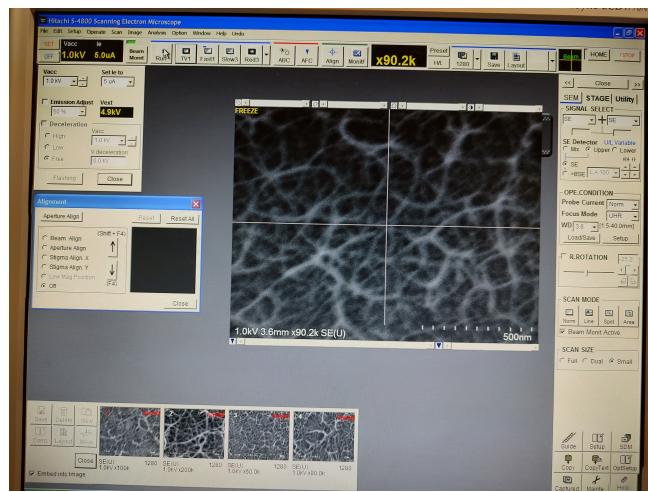


FIGURE 7 – Sample with 1 nm  $\text{Al}_2\text{O}_3$  and 0.15 nm Fe with 30 minutes CVD on the SEM

The conclusions are the same. Given that very high densities can short circuit CNFET device terminals and turn the surface conductive (higher probability to have conductive CNTs among semiconducting CNTs), the most promising samples we observed at this stage were the 0.075nm and 0.1nm iron samples with 1 hour of CVD. One of the 0.05 *Fe* sample, which was grown by the other group, looked also very promising.

Similar to Raman spectroscopy, we could not observe traces of CNTs in the cobalt and nickel samples. Further experimentation is required to verify conditions for growth with these catalysts.

## 3

# ELECTRODE DEPOSIT USING PHOTOLITHOGRAPHY

To make CNTFET devices, one may add metallic electrodes on top of the substrates covered by carbon nanotubes (Figure 1(b)). This can be done using *photolithography*.

To perform photolithography, we were able to use machines from the clean room of the Thales research center on the *Plateau de Saclay*. For this part, we followed a procedure with values and timing calibrated for our particular deposition with the specific machines present. Unable to take notes for security reasons, we were unable to write down the specific values and chemical components used in this part. We will thus refer them by their purpose.

Here are the main steps we followed :

### a) Substrate cleaning

The process begins with cleaning the silicon wafer substrate. The substrate is emerged in a bath of a chemical cleaner which is shaken by an ultrasonic cleaning device to remove all potential contaminants. After 10 to 20 seconds, the wafer is then rinsed with deionized water and dried on a 150°C plate. This is all done under a fume hood.

### b) Photoresist application

A thin layer of photoresist, a light-sensitive liquid, is applied to the substrate using spin coating. After having put a few droplets of liquid photoresist, the substrate is rotated at speed of around 3000RMP for 30 seconds allowing the liquid to spread evenly on the surface. The spin speed and time determine the thickness of the photoresist layer. The coated substrate is then baked on a hot plate (around 150°C) for a 5 minutes.

### c) Exposure and developing

The coated substrate is exposed to UV light through a photomask, which contains the desired pattern for the devices for the whole wafer. The UV light modifies the chemical structure of the photoresist in the exposed regions. Since we used a positive photoresist, the exposed areas became soluble in the developer. After exposure, the substrate is immersed in a developer solution to dissolve the soluble regions, revealing the pattern transferred from the photomask.

### d) Etching and material deposition

The exposed areas of the substrate, revealed after developing, are subjected to etching to remove material and create the desired pattern. The desired material (in our case, we deposit palladium electrodes) which will form electrodes is deposited onto the patterned areas of the substrate when immersed in a specific chemical solution. The remaining photoresist acts as a mask, ensuring that the material adheres only to the exposed regions, the unwanted material will then be removed alongside the photoresist.

### e) Photoresist removal and cleanup

The remaining photoresist is stripped away using a photoresist remover solvent. This

step ensures that only the desired pattern remains on the substrate. The substrates were immersed in a photoresist removal solution for a specific duration (27 seconds in our configuration). Timing in this step is critical as too much immersion would allow the solution to attack the deposited electrodes while an immersion too short would leave some unwanted metal.

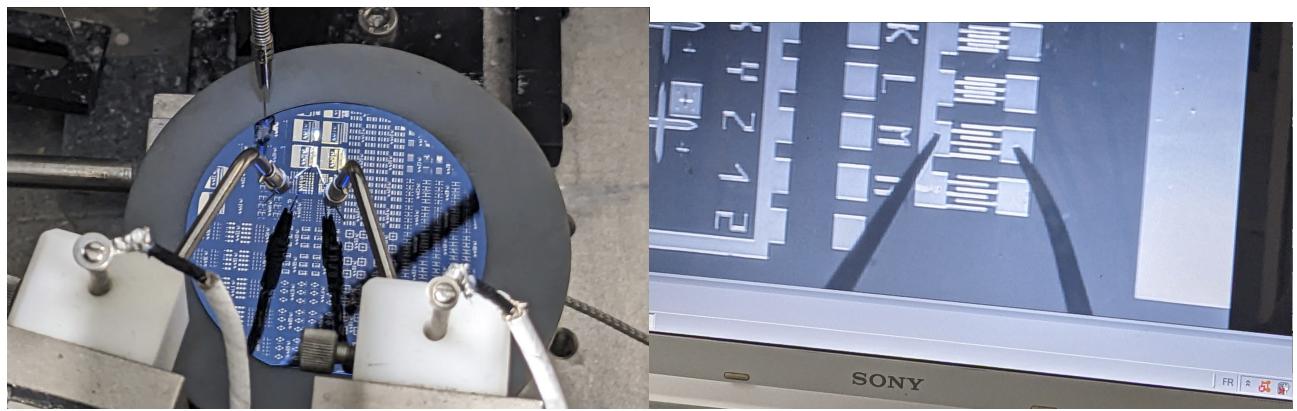
Finally, the substrate is cleaned again to remove any residues or particles left over from the etching and stripping processes to obtain the final sample.



FIGURE 8 – Sample with electrodes, ready to be tested

## 4 ELECTRONIC CHARACTERIZATION

As a last step, we tried to characterize the electronic properties of some transistor devices chosen from the most promising substrates.



(a) Sample in the electronic characterization tool

(b) Camera view, which lets us observe the connected electrodes on the micro scale devices

FIGURE 9 – A device ready to be tested

First of all, we scratched one point of the wafer to place a probe directly in contact with the silicon. In our setup, this will act as the gate. The silica on top is a dielectric layer, the carbon nanotube is the channel for passing current and the device fingers act as the source/drain terminals.

Therefore, the air surrounding our device acts as a substrate terminal. The energy difference between the Fermi level of the palladium terminals and the air is high. This means that our device is a type p-type transistor because the nanotubes will favor hole conduction.

In order to measure our transistor characteristics,  $V_S = 0V$  is kept constant and we apply a constant high voltage  $V_D$  to keep the transistor in the saturation region when the device is in ON state.

During the experiment, the gate node performed a DC sweep of voltage from  $V_G = -10V$  to  $V_G = +10V$  and then back in the opposite direction to check for *hysteresis*.

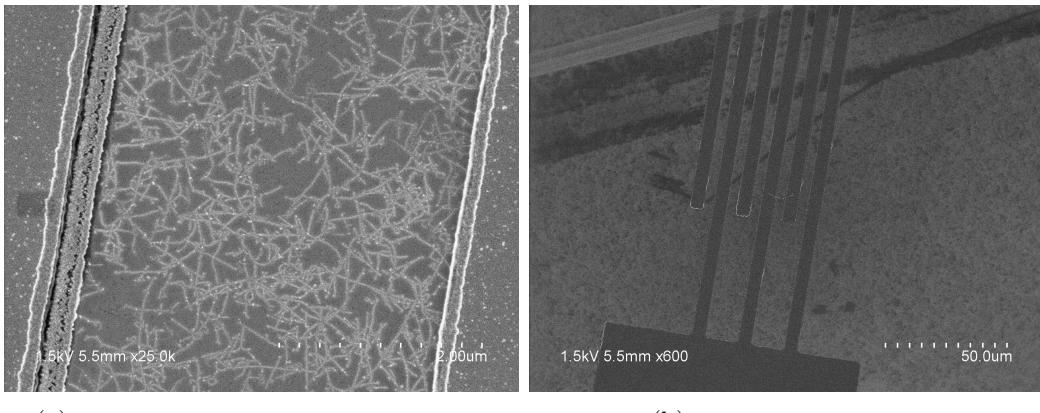
When  $V_G < V_{th} < 0$  (where  $V_{th}$  is the threshold voltage), the transistor is in ON state and we observe a decreasing drain current. As  $V_G$  becomes positive, the device switches to OFF state and the current drops to zero.

Hysteresis is the change of threshold voltage due to the finite switching speed between the transistor's ON and OFF states. In the plots below, the hysteresis curve is below the original curve.

We observed that when placing the probes on the device terminals, sometimes we scratched the surface of the device which resulted in a leakage current during the measurement of the de-

vice characteristics. Unfortunately we did not export the numerical data for these experiments, which is why they are not presented in the plots.

In the samples where nanotube growth did not happen, we observed a constant characteristic indicating no change in behavior as the gate voltage varied, namely the device acted as an insulator.



(a) Carbon nanotubes between device fingers

(b) Device fingers on SEM

Finally, to better visualize the threshold voltage in our device, we remade these plots with a log scale on the y axis. We picked the 0.05 nm Fe sample to display here because in spite of the noise it shows a behavior very close to a textbook curve. We observe a switch in behavior when the concavity of the log  $I_{DS}$  changes near 0.

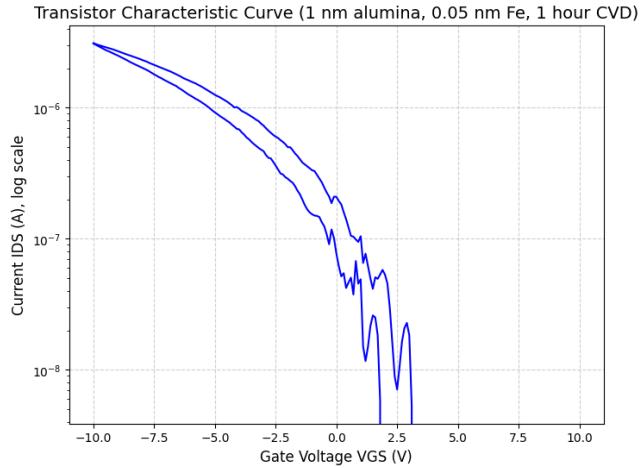


FIGURE 11 – 1 nm  $\text{Al}_2\text{O}_3$ , 0.05 nm Fe (1 hour CVD) with y log scale

The above figures show 3 characteristic curves looking close to the expected behavior of p-type transistors.

Figures c) and d) show that the tested transistors in this configuration have an OFF state which is not well defined (current not close to 0 when off), we can graphically estimate the threshold voltages to be  $V_{th_c} = 2.5V$  and  $V_{th_d} = 2.4V$ .

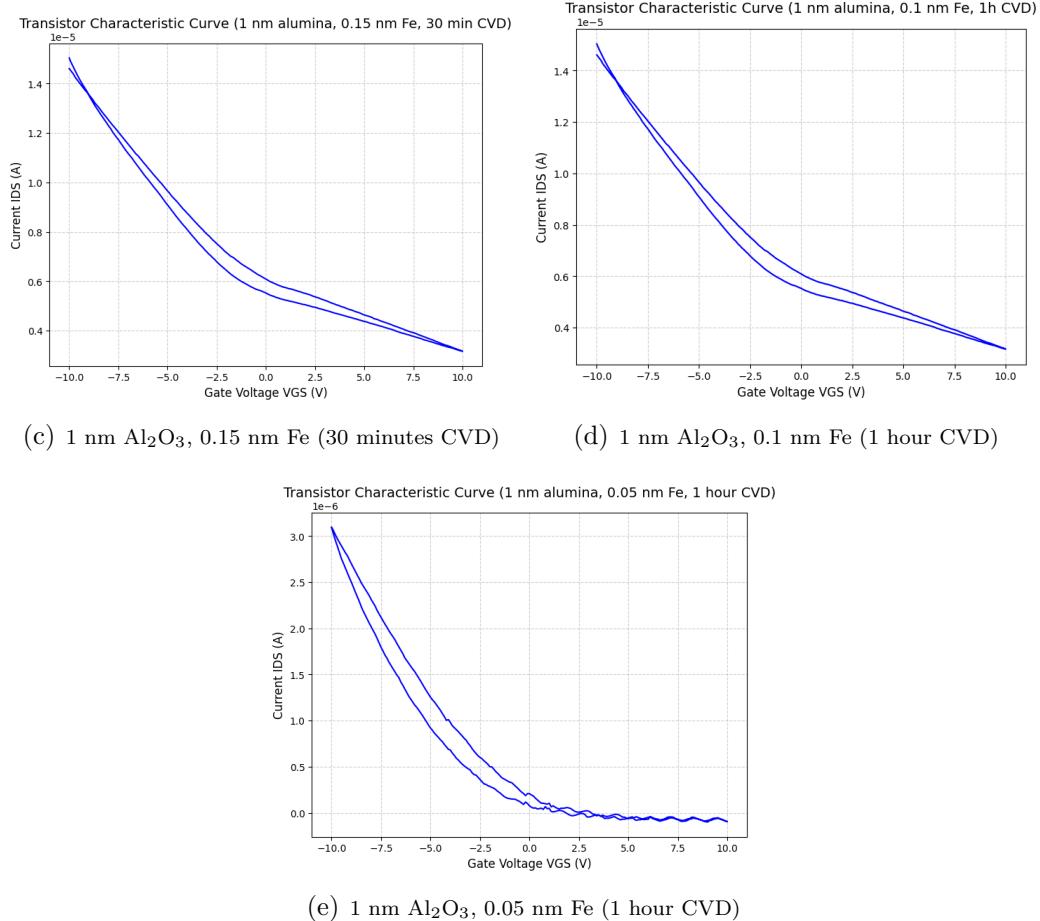


FIGURE 10 – P type transistor characteristics measured on our samples

On the other hand, the e) sample ( $1.00 \text{ Al}_2\text{O}_3$   $0.05 \text{ Fe}$ ) had a very satisfactory looking curve and a clear OFF state region (current close to 0 when off), with an estimated threshold voltage of  $V_{th_e} = -1.0V$ .

## FINAL COMMENTS

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The purpose of this project was to make us discover the science behind CNTFETs and a procedure on how to produce simple transistor devices. We were able to understand challenges related to the production of nanoscale components, and more broadly challenges related to laboratory experiments.

During the semester, we have made a few mistakes related to the operation of the machines (such as forgetting to close valves) which thankfully were not critical. We also made mistakes which rendered some samples irrelevant. For example, we wished to make a substrate using cobalt as catalyst instead of iron to see the impact of the catalyst choice. However, as no traces of CNTs could be found using SEM, neither using raman spectroscopy we think that no CNTs were able to grow on it. Reviewing our notes, we think we made a mistake calculating the deposition time which may have been too short. This example illustrates the fact that in such production process, a mistake at one step would likely ruin the whole processes for this sample. At last, we were delighted to see that we were successfully able to make a P-type transistor device with a satisfactory behavior and characteristic curve, although some of the samples had not good photolithography.

Finally, this project helped us gain insights on how scalable CNTFET production technology is for large and complex chips. Although we have built devices with the whole *Si* layer acting as the gate for all devices, building independent gates should be doable (still difficult) using current etching technologies (for example, one may deposit gates above each CNT channel with a dielectric layer to separate the channel and gate using photolithography). Another issue we did not discuss about yet is that using this process, the CNT layer is made of countless CNTs where most are connected, which makes it likely for the whole CNT layer to be seen as one big semiconducting layer, common for all devices. A method to make all devices have independent semiconducting layer should be found for a multiple transistor device.

What we think could be the most critical issue is that it is very hard to control the physical properties (diameter and chirality) of the grown CNTs, which means that the control over the electrical properties of the devices is very uncertain. For example, if the diameter of some CNTs is too large the gate simply becomes conductive. At last, the devices we tested were of micrometer or hundreds of nanometer scale which is obviously negating all effects that we could experience with nanometric devices, were we could experience for example the need to align the CNT to link the electrodes.

## RÉFÉRENCES

- [1] Vincent Huc Evgeny Norman Marc Chaigneau Jean-Luc Maurice Talal Mallah Fatima Z. Bouanis, Costel S. Cojocaru and Didier Pribat. Direct synthesis and integration of individual, diameter-controlled single-walled nanotubes (swcnts). *Chemistry of Materials*.
- [2] MANOHARAN GOWTHAM BERND MARQUARDT SUNG HUN LIM SHAIMA ENOUZ COSTEL SORIN COJOCARU KYUNG AH PARK YOUNG HEE LEE HEE JIN JEONG, LAURENT EUDE and DIDIER PRIBAT. Atomic hydrogen-driven size control of catalytic nanoparticles for single-walled carbon nanotube growth. *World Scientific*.
- [3] Gabor Kereszty. Raman spectroscopy : Theory. *Hungarian Academy of Sciences, Budapest, Hungary*.