Microelectronics Experimental ASIC Design

Project Defense

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March 18, 2025

Overview

1. Introduction
2. Modeling photodetector input signal
3. Preamplifier Block
4. Discriminator block

Project goals

- Design a SiPM(silicon photomultiplier) for single photon detection in the context of accelerator-based particle physics experiments.
- Application requires high sensitivity, high efficiency and fast rise/fall times.

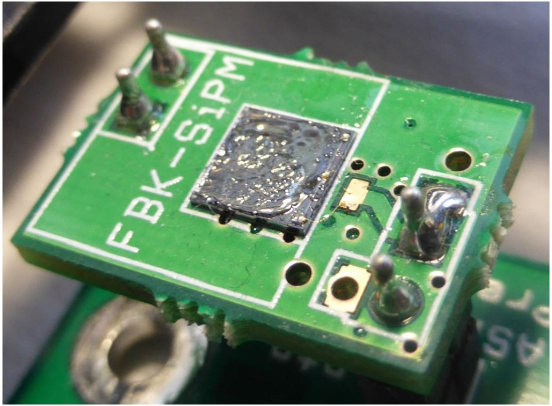


Figure: Casing for a commercial SiPM

Another use case: PET scan imaging

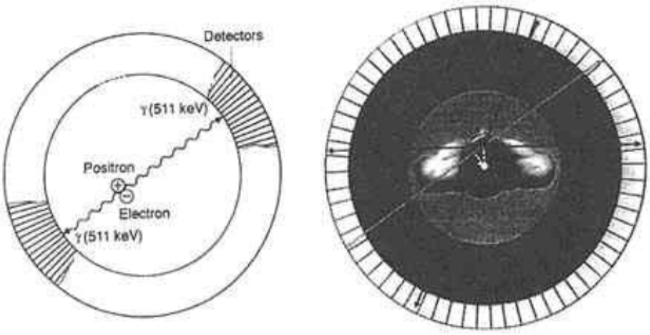


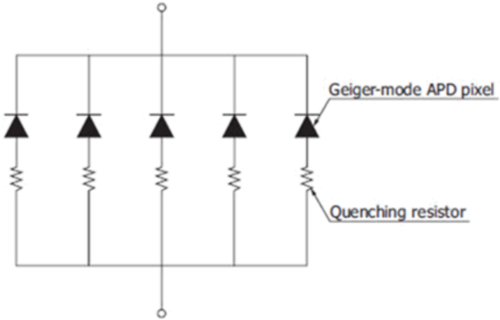
Figure: Photon detection in PET scan

The model we used for our photodetector input signal is not universal for all SiPM applications!

Parameters

We consider a 100x100 array of Single Photon Avalanche Diodes (SPADs).

- each cell has dimensions $50\mu m \times 50\mu m$, a capacitance of $100fF$ and a quenching resistor of $100k\Omega$;
- one photo electron corresponds to a charge of $100fC$ which is equivalent to a current pulse of $1mA$;
- the duration of the pulse is estimated as $100ps$, with a rise time of $1ps$ and a fall time of $1ps$.



Photodetector schematic

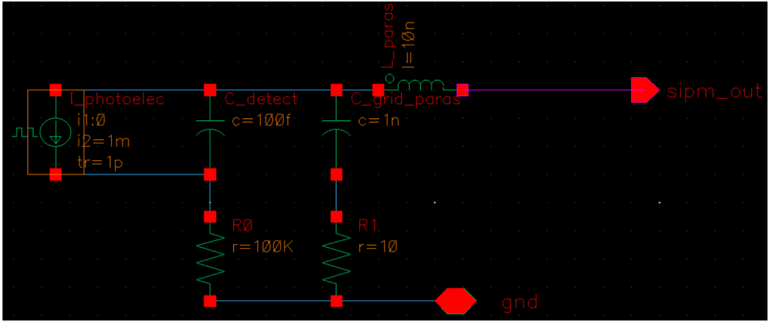


Figure: Photodetector block schematic

The parasitic inductance in the readout bus models the effect of current from previous detections, that induced a voltage in the conductor.

CMOS Current Source

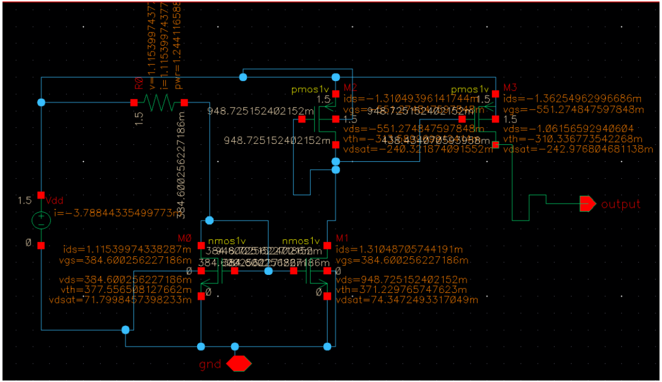


Figure: Current source design: NMOS current sink with PMOS current source

Two stage current source increases output resistance and helps stabilize output current!

Cascode amplifier configuration

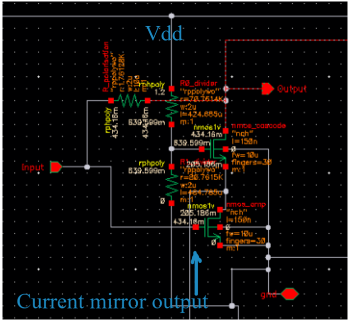


Figure: Final cascode configuration for preamplifier

Compared to single stage CS amplifier, cascode has:

- higher gain $A_v = \left(\frac{g_{m_1}}{g_{ds_1}}\right) \cdot \left(\frac{g_{m_2}}{g_{ds_2}}\right)$;
- larger bandwidth (consequence of the Miller Effect $f_{-3db} = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$)

Complete pre-amplifier schematic

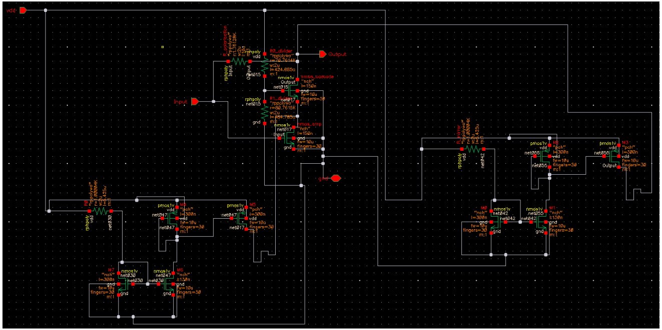
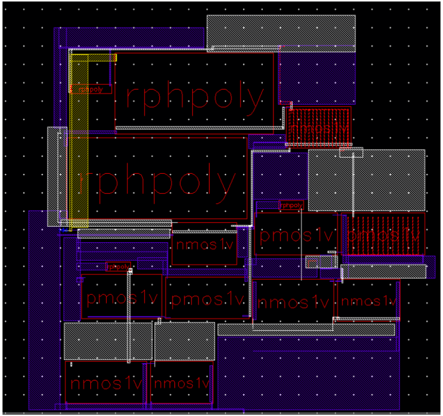


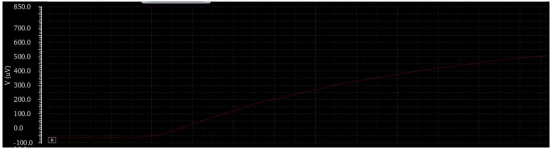
Figure: Complete schematic for the preamplifier module

Layout view for pre-amplifier

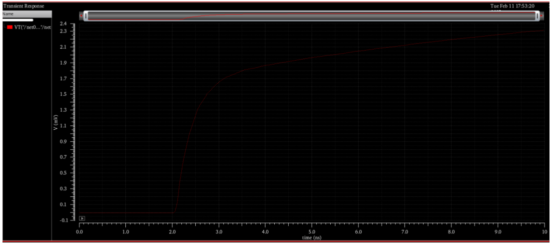


Represents real circuit on silicon! We ran DRC (to check circuit feasibility) and LVS (to compare nets and devices layout and schematic).

Importance of path widths on layout!



(a) In first layout, output peaks at $\approx 0.5mV$



(b) In first layout, output peaks at $\approx 2.3mV$

Figure: Transient response (minus DC) simulations on extracted views. In (b), gain is bigger by a factor of ≈ 4.6

Choosing a threshold voltage for the discriminator

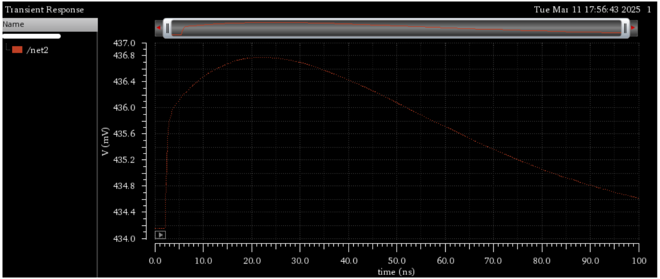


Figure: Transient response (with DC bias)

Considering RMS noise of $\approx 0.7mV$, we consider $435mV$ a good threshold!

Goals

After the pre-amplifier, our goal is to take the output signal and

1. determine if a photon was detected (the peak of the signal is above a certain threshold voltage);
2. and produce a digital signal if a photon was detected (so far, we are working only with analog signals, but if we want to use this signal in software, it must saturate to V_{SS} or V_{DD}).

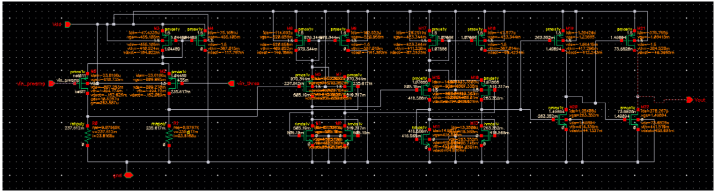


Figure: Complete schematic of discriminator circuit

Differential Pair principle

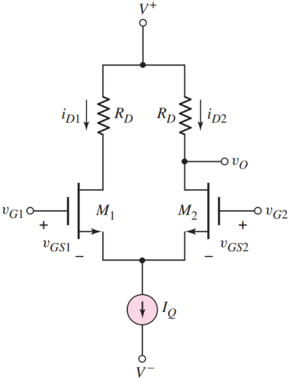


Figure: Schematic for a differential pair amplifier

DC operating point

$$\begin{cases} I_{D_1} + I_{D_2} & = I_Q \\ I_{D_1} & = I_{D2} \quad \text{by symmetry} \end{cases} \tag{1}$$

Now, we observe the differential behavior of the block

$V_{G_1} > V_{G_2}$

$\implies V_{GS_1} > V_{GS_2}$

$\implies I_{D_1} > I_{D_2}$

First discriminator stage

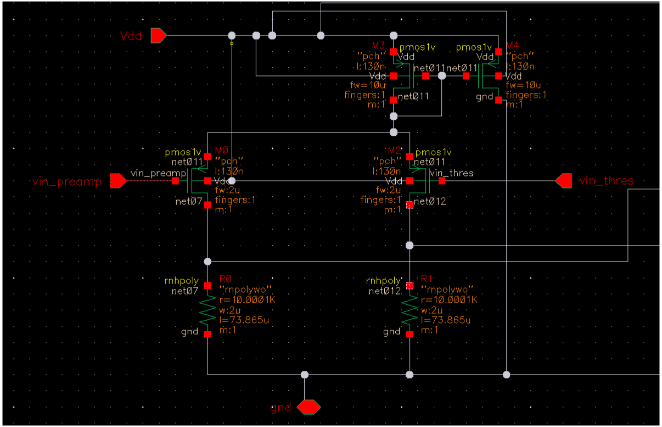


Figure: Schematic for first stage of our discriminator, a classic differential pair

Because the output of the preamplifier is small compared to the transistor's threshold

Second and third discriminator stage

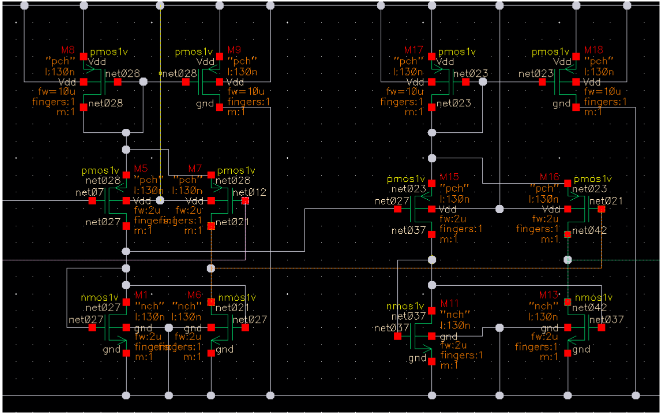


Figure: Schematic for next two stages of our discriminator, more differential pair amplifiers!

- In stages 2 and 3 of the discriminator, we reuse V_{G_1} from the previous stage and we use the output of the previous stage as V_{G_2} $\implies$ this difference gives us a factor of

Convert to digital signal

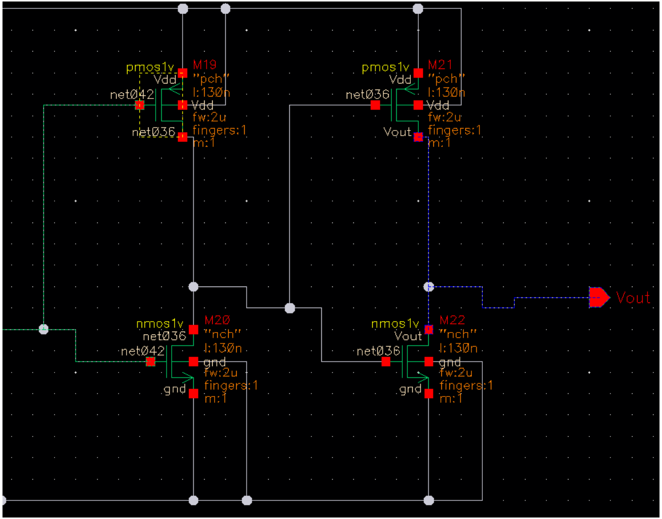


Figure: Schematic for the AC/DC converter of our discriminator (a logical buffer)

Layout for discriminator block

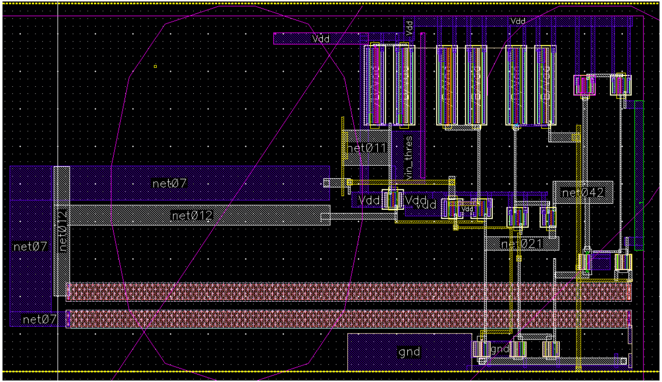


Figure: Layout for discriminator circuit

Transient reponse simulation for discriminator

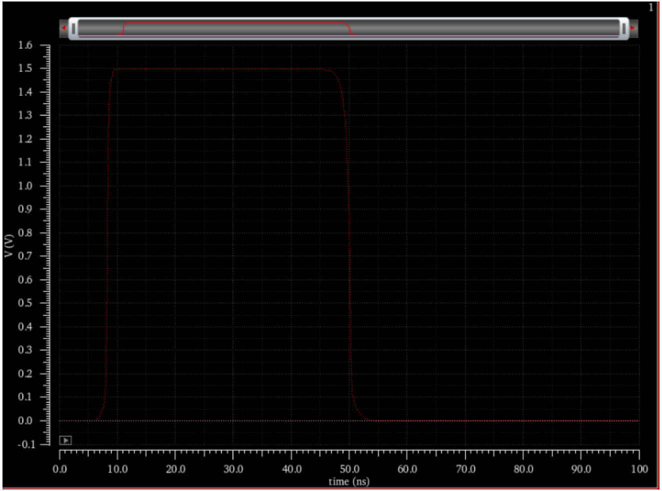


Figure: Transient response for the discriminator

Thank you for your attention!