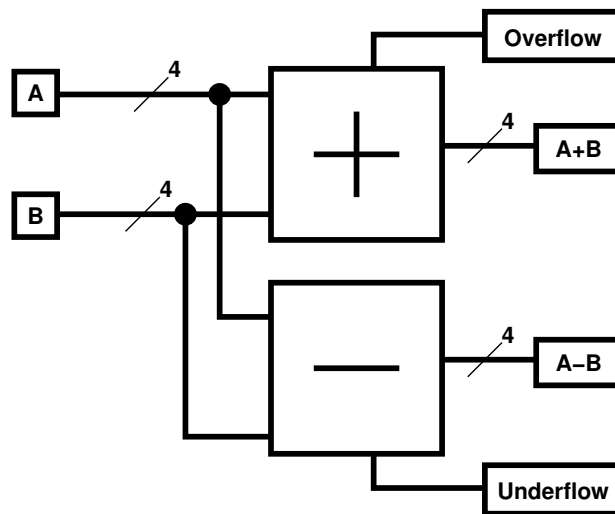


A 4-bit Adder/Subtractor and a Sequential Circuit



You are given an 8-input, 10-output circuit. A and B are numbers encoded in natural binary, using 4 bits: A_3, A_2, A_1, A_0 and B_3, B_2, B_1, B_0 .

The outputs are also encoded in natural binary and defined as follows:

$A+B = (P_3, P_2, P_1, P_0)$ and $A-B = (M_3, M_2, M_1, M_0)$.

Finally, the overflow **O** and the underflow **U** outputs indicate that the result can not be described in 4 bits (capacity of the adder/subtractor is exceeded).

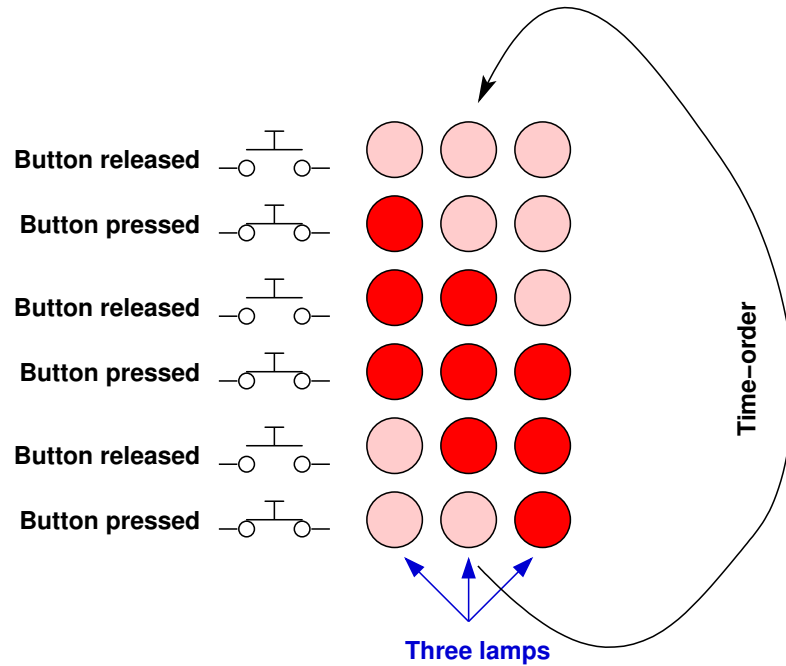
Your task is to design a gate-level schematic of the circuit.

Questions:

1. Draw a truth table of the adder.
2. Using Logisim, design and verify a gate-level schematic of the adder.
3. Draw a truth table of the subtractor.
4. Using Logisim, design and verify a gate-level schematic of the subtractor.

A 4-bit Adder/Subtractor and a Sequential Circuit

The purpose of this exercise is to design a controller circuit for a three-light-system,. The state of the three lights changes on each press or release of the button, according to the scheme below:



Tasks to complete:

5. Implement a system with the described functionality in Logisim. You are only allowed to use simple logic gates, SR-latches, LEDs, and buttons.
6. Download your design to the GECKO4Education board. What do you observe?