American International University-Bangladesh (AIUB)

Dept. of EEE, CSE & CoE, Faculty of Engineering

EEE 3101: Digital Logic and Circuits

ASSIGNMENT # 1 ***(30 Points)***

(Deadline: 28th June 2021, Monday, till 11:50 pm) (Format: Handwritten and Scanned by CAMSCANNER)

(Submission: *https://forms.office.com/r/qBbdEfNyqG*)

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Instructions:

- **No assignment will be accepted after the deadline. Don't wait for the last minute)**
- **Don't copy from your peers. If you do so, both the copies will be negatively marked.**
- **Use this page as cover page for the assignment**. Don't forget to write your **Name & ID** in **each page** (*top right corner*) of assignment.

Solve the following Problems

1. In a home security system, the main door (O) of home is controlled by a logic operation with the help of RFID card. the Owner, Mrs. Owner, Security Guard and Guest have a designated RFID card - Owner with card W, Mrs. Owner with card X, security guard with card Y and guest with card Z. Whenever, any of the card is NOT inserted, Door remains Closed; when, all the cards are inserted together, the Door is opened. C**onsider, card NOT inserted as Logic Low (0), card inserted as High Logic (1), door open as Low Logic (0) and door close means High Logic (1).**

(i) **Identify** the logic based on the problem statement
(ii) **Develop** the truth table (W, X, Y & Z – inputs, O – output)
(iii) **Find** the Standard SOP and Standard POS expression
(iv) **Find** the Simplified SOP expression using KMAP.
(v) **Design** the system using **basic logic gate**.

[Note: WXYZO = **1st 2nd 3rd 4th 5th letters of your name(s) as in AIUB ID**. For repeated letter, take next letter]

2. Draw the block diagram of both **half subtractor** and **full subtractor, develop** the truth table for both, **write** the logic POS expression and **design** both half subtractor and full subtractor using **basic logic** gates only.

3. For the given expression F (A, B, C, D) = Π (1,3,9,11) and d (A, B, C, D) = (0,2,8,10) where d (A, B, C, D) represents the don't care conditions.

(a) Without using the don't care conditions, **draw a k-map** and **obtain (i)** Simplified SOP expression **(ii)** Simplified POS expression

(b) Using the don't care conditions, **draw a k-map** and **obtain (iii)** Simplified SOP expression **(iv)** Simplified POS expression

(c) For the most simplified expression obtained in a(i), draw a logic diagram **(v)** Using universal NOR gate only **(vi)** Using universal NAND gate only **(vii)** Using universal gates only (NAND &/ NOR)

[Note: ABCD = **1st 2nd 3rd 4th letters of your name(s) as in AIUB ID**. For repeated letter, take next letter]

Ans to the ques: 1

i) As per the given data,

If any of the card is not inserted Door remains closed means output is '1'.

If all cards are inserted together the door is opened and output is '0'.

ii) Truth Table:

Input				output
K	A	B	I	R
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

function $F = \Sigma m(0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14)$

iii) Standard SOP

$$F = \bar{B}(W+\bar{W})(A+\bar{A})(I+\bar{I}) + \bar{W}(A+\bar{A})(B+\bar{B})(I+\bar{I})$$
$$+ B\bar{I}(W+\bar{W})(A+\bar{A})\bar{A}B(W+\bar{W})(I+\bar{I})$$

$$= \bar{B}WAI + \bar{B}\bar{W}A\bar{I} + \bar{W}ABI + \bar{W}\bar{A}\bar{B}\bar{I} + WB\bar{I}A$$
$$+ \bar{W}\bar{A}B\bar{I} + WB\bar{A}\bar{I} + \bar{W}B\bar{A}\bar{I}$$
$$= WA\bar{B}I + \bar{W}\bar{A}\bar{B}\bar{I} + \bar{W}\bar{A}BI + WB\bar{I}A + \bar{W}A\bar{B}\bar{I}$$
$$WB\bar{A}I$$

$$F(W, A, B, I) = \Sigma m(0, 2, 7, 11, 13, 14)$$

In the function the remaining terms are called maxterms (POS) that is

$$F(W, A, B, I) = \Pi M(1, 3, 4, 5, 6, 8, 9, 10, 12, 15)$$

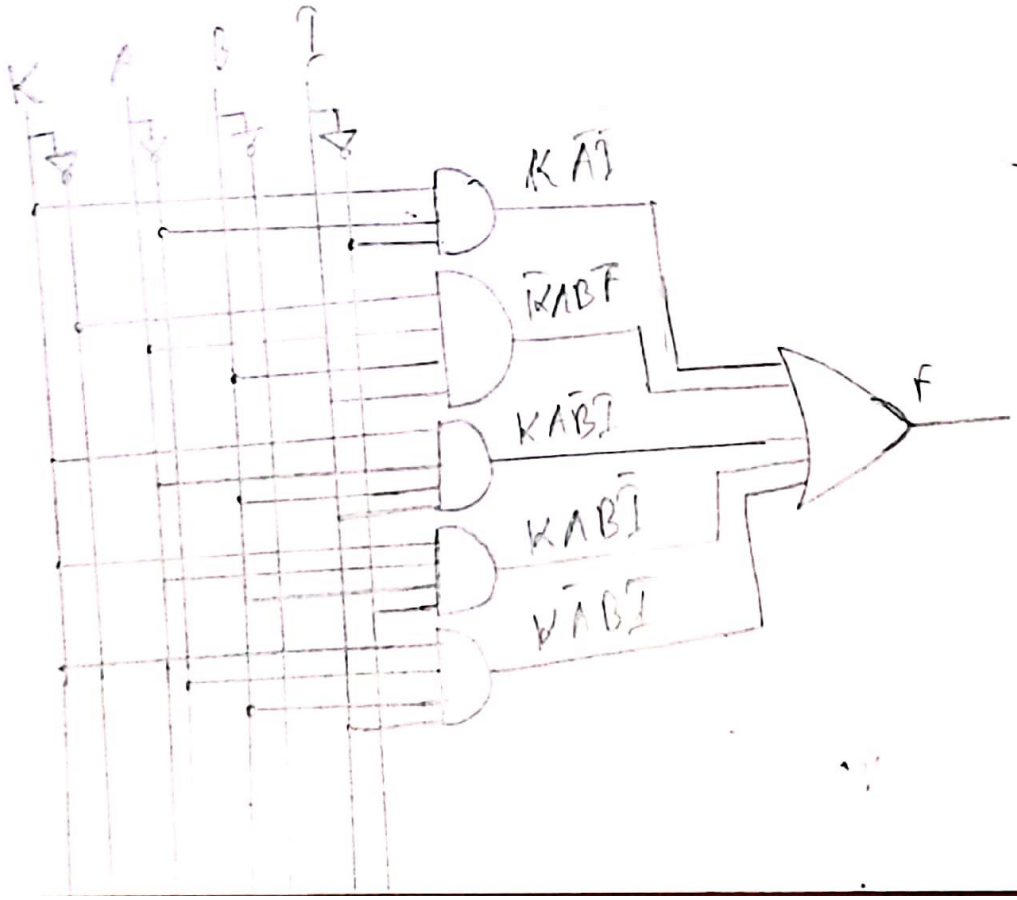
$$F = (W+A+B+\bar{I})(W+A+\bar{B}+I)(W+\bar{A}+B+I)(W+\bar{A}+B+\bar{I})$$
$$(W+\bar{A}+\bar{B}+I)(\bar{W}+A+B+I)(\bar{W}+A+B+\bar{I})(\bar{W}+A+\bar{B}+I)$$
$$(\bar{W}+\bar{A}+B+I)(\bar{W}+\bar{A}+\bar{B}+\bar{I})$$

iv) Kmap for SOP :-

KA \ BI	$\bar{B}\bar{I}$ 00	$\bar{B}I$ 01	BI 11	$B\bar{I}$ 10
$\bar{K}\bar{A}$ 00	0	1	3	2
$\bar{K}A$ 01	4	5	7	6
KA 11	12	13	15	14
$K\bar{A}$ 10	8	9	11	10

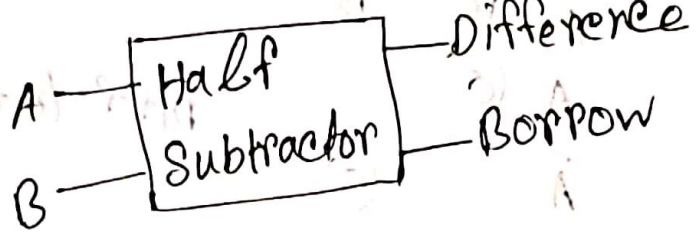
$$F = K\bar{A}\bar{I} + \bar{K}AB\bar{I} + KA\bar{B}\bar{I} + KAB\bar{I} + K\bar{A}B\bar{I}$$

v) The logic System.



Ans to the question-2

Block diagram of Half subtractor



truth table

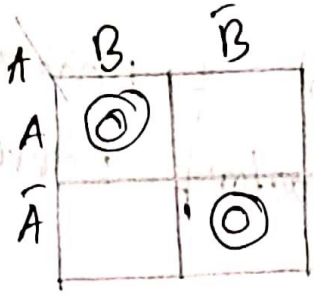
Inputs		outputs	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$\therefore$ Diff $= \Sigma m(1,2) \Rightarrow \pi M(0,3)$

Borrow $= \Sigma m(1) \Rightarrow \pi M(0,2,3)$

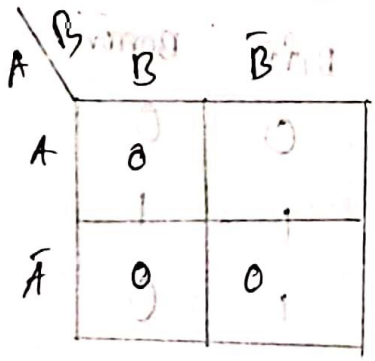
Logical POS expression for Half subtractor

Difference



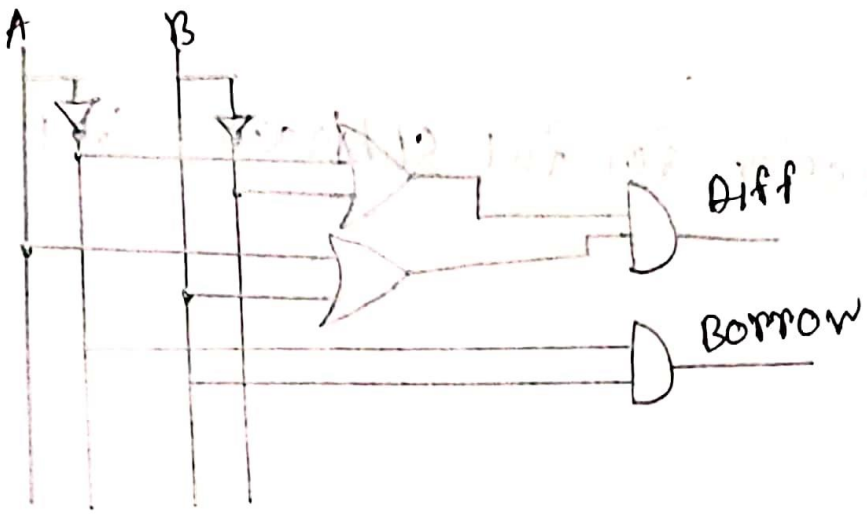
$Diff = (A+B).(\bar{A}+\bar{B})$

Borrow



$Borrow = (B).(\bar{A})$

logic circuit for Half Subtractor



Full Subtractor

It has 3- inputs A, B, B in

2 - outputs B Difference D

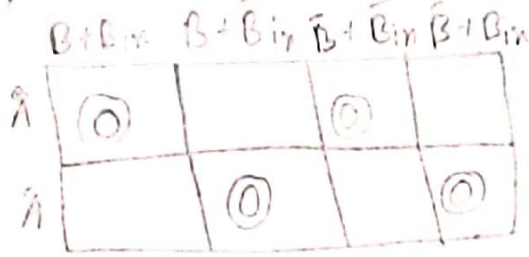
Truth table

Input			output	
A	B	Bin	Diff	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Diff $= \Sigma m(1,2,4,7) = \Pi M(0,3,5,6)$

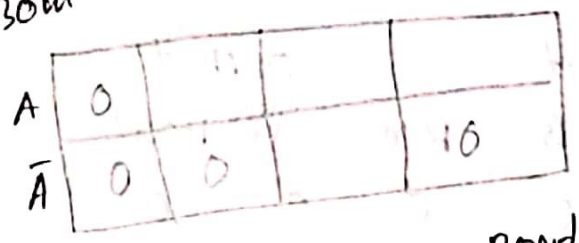
Boud $= \Sigma m(1,2,3,7) = \Pi M(0,4,5,6)$

expression for full subtractor in POS



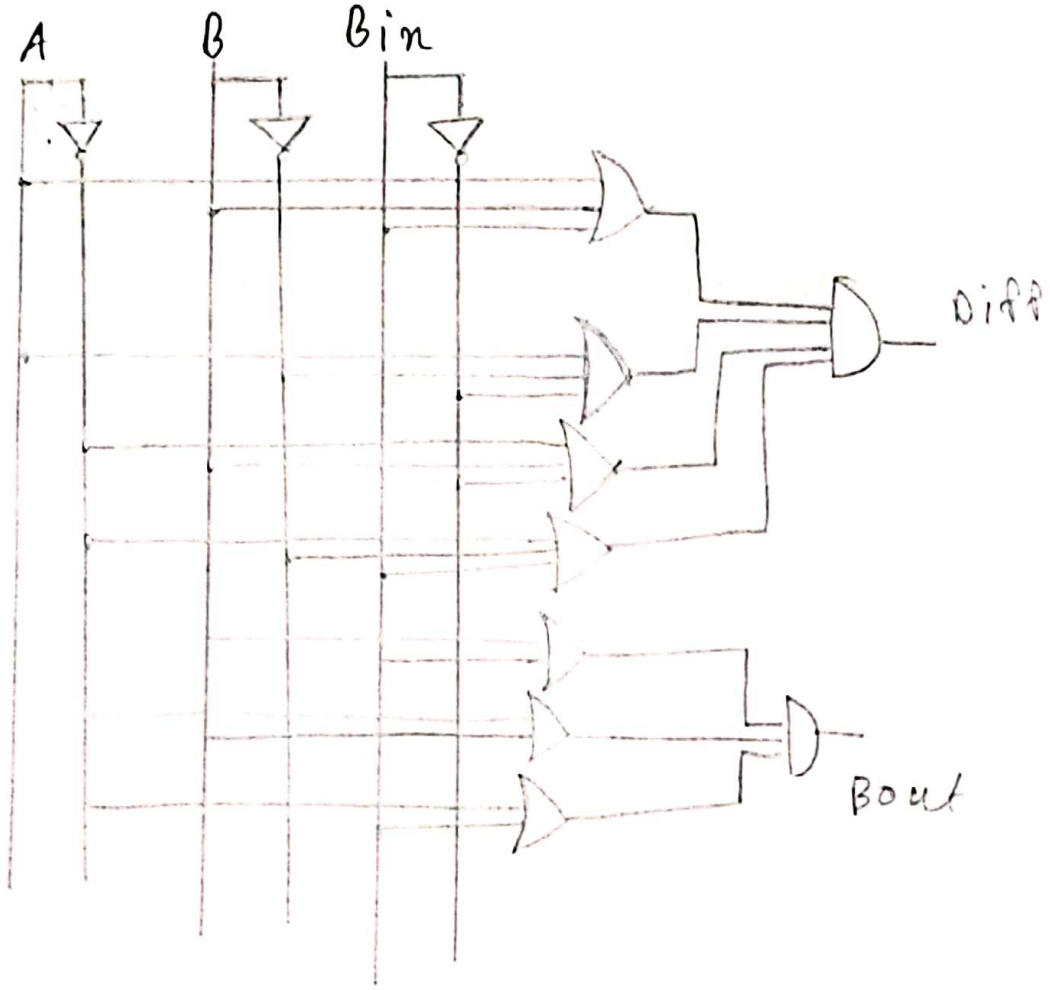
$$Diff = (A+B+B_{in})(A+\bar{B}+B_{in})(\bar{A}+B+\bar{B}_{in})(\bar{A}+\bar{B}+B_{in})$$

Boud



$$Boud = (B+B_{in})(\bar{A}+B)(\bar{A}+B_{in})$$

Logic circuit



3 NO Q/Ans:

$F(K, A, B, I) = \Pi(1, 3, 9, 11)$

$d[K, A, B, I) = (0, 2, 8, 10)$

a) without using don't care condition

KA \ BI	00	01	11	10
00	1	0	0	1
01	1			1
11	1	1	1	1
10	1	0	0	1

(i)

KA \ BI	00	01	11	10
00	1			1
01	1	1	1	1
11	1	1	1	1
10	1			1

$\therefore F(SOP) = A + \bar{I}$

(ii)

	00	01	11	10
00		0	0	
01				
11				
10		0	0	

$F(POS) = A + \bar{I}$

b) using dont care condition

KA \ BT	00	01	11	10
00	X	0	0	X
01				
11				
10	X	0	0	X

(iii)

KA \ BT	00	01	11	10
00	X			X
01	1	1	1	1
11	1	1	1	1
10	X			X

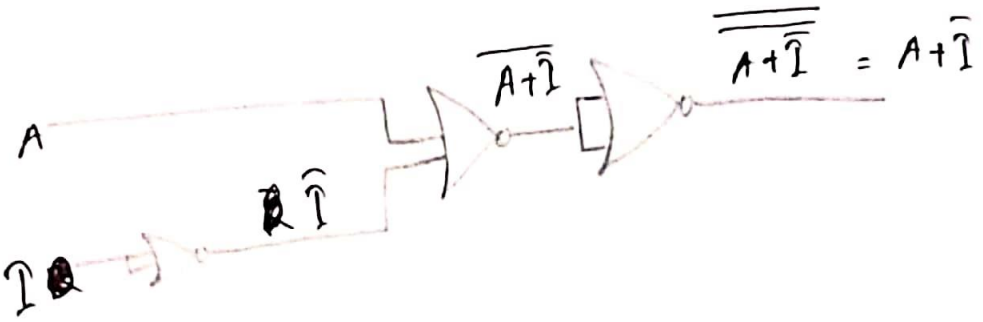
F(SOP) = A

KA \ BT	00	01	11	10
00	X	0	0	X
01				
11				
10	X	0	0	X

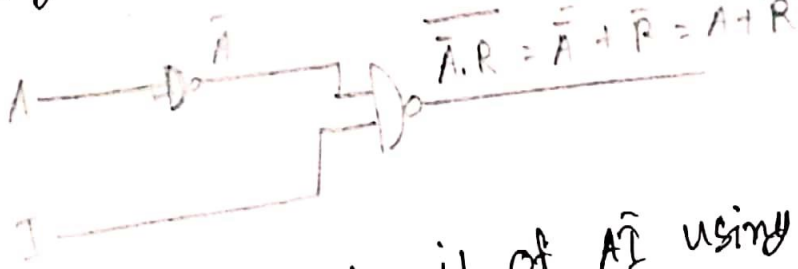
F(POS) = B

c) v) From a(i) we have found SOP = $A + \bar{I}$

Drawing $A + \bar{I}$ using universal NOR Gate



vi) Drawing a logic circuit of $A + \bar{I}$ using NAND gate only



vii) Drawing a logic circuit of $A\bar{I}$ using NAND and NOR gate: