ArmSoM-AIM7

ArmSoM-AIM7

Main Functions Introduction

1) PMIC: 1xRK806-1
2) RAM: 2xLPDDR4/4X_32bit
3) ROM: eMMC5.1
4) Support: 1 x TYPEC3.0+ 2 x USB2.0 HOST+ 1 x USB2.0 OTG
5) Support: 1 x 4Lane PCIe3.0 Connector + 1 x 1Lane PCIe2.0 Connector
6) Support: 1 x 4Lanes DP Port
7) Support: 1 x HDMI2.1 TX or 1 x eDP1.4 TX
8) Support: 4 x 2Lanes MIPI DPHY RX Camera
9) Support: 1 x 4Lanes MIPI D/CPHY RX Camera
10) Support: 1 x 2Lanes MIPI D/CHY-TX
11) Support: 1 x SDMMC3.0 Card
12) Support: 1 x 10/100/1000 RJ45 Port(RGMII)
13) Support: 15 x GPIO
14) Support: 2 x I2S
15) Support: 4 x I2C
16) Support: 2 x SPI
17) Support: 3 x UART

armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	Cover Page				
Date:	Tuesday, October 08, 2024			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	1 of 24

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Description

Note

Option

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Note

The power suffix S0 or S3 means:

S3: Keep power On during sleeping

S0:Power off during sleeping

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Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2023-11-27	Liu Xinglin	First Release;	
V1.1	2024-03-19	Liu Xinglin	1. Swap singals for CON2.115&CON2.117; 2. CON2.188 change to LED2, CON2.194 change to LED0; 3. U1000.U33 chane to GMAC0_RSTn, U1000.T32 change to SLEEP/WAKE; 4. Swap singals for U1000.R31 and U1000.T30; 5. RTC(U4) I2C6 change to I2C3;del R9000&R9001(VBUS_DET); 6. del R9002/R9003/R9004/R9005(ADC0 and SD_DET); 7. CON2.126 change to SD_DET, CON2.124 change to PCIE20X1_2_WAKE; 8. del Q9003&Q9004&R9016&R9017&R9018&R9019, voltage transformer circuit change to IC; 9.del:Q1901/Q1902/Q1903/Q1904/R1908/R1909/R1914/R1915/R1916/R1917/R1918/R1919; Voltrans circuits change to ic U9000/C9001/C9002;add voltrans circuit for HDMI_CEC&HDMI_I2C; 10. PCIE clk ic change to Au5426;	
V1.2	2024-07-02	Liu Xinglin	1. Swap CON2: MIPI_CSI0_D2/D3 and MIPI_CSI1_D0/D1; 2. add Q9000 circuits for HDMI_HPD_L;	
V1.2	2024-10-08	Park	1. U9001 pwr change to VCC_1V8_S3; RTC I2C change to I2C4; I2C3 add pull-up resisters; 2. Swap singals PMIC_PWR_CTRL2&CPU_BIG0_VSEL,and add U9002 circuit; add maskrom key;	

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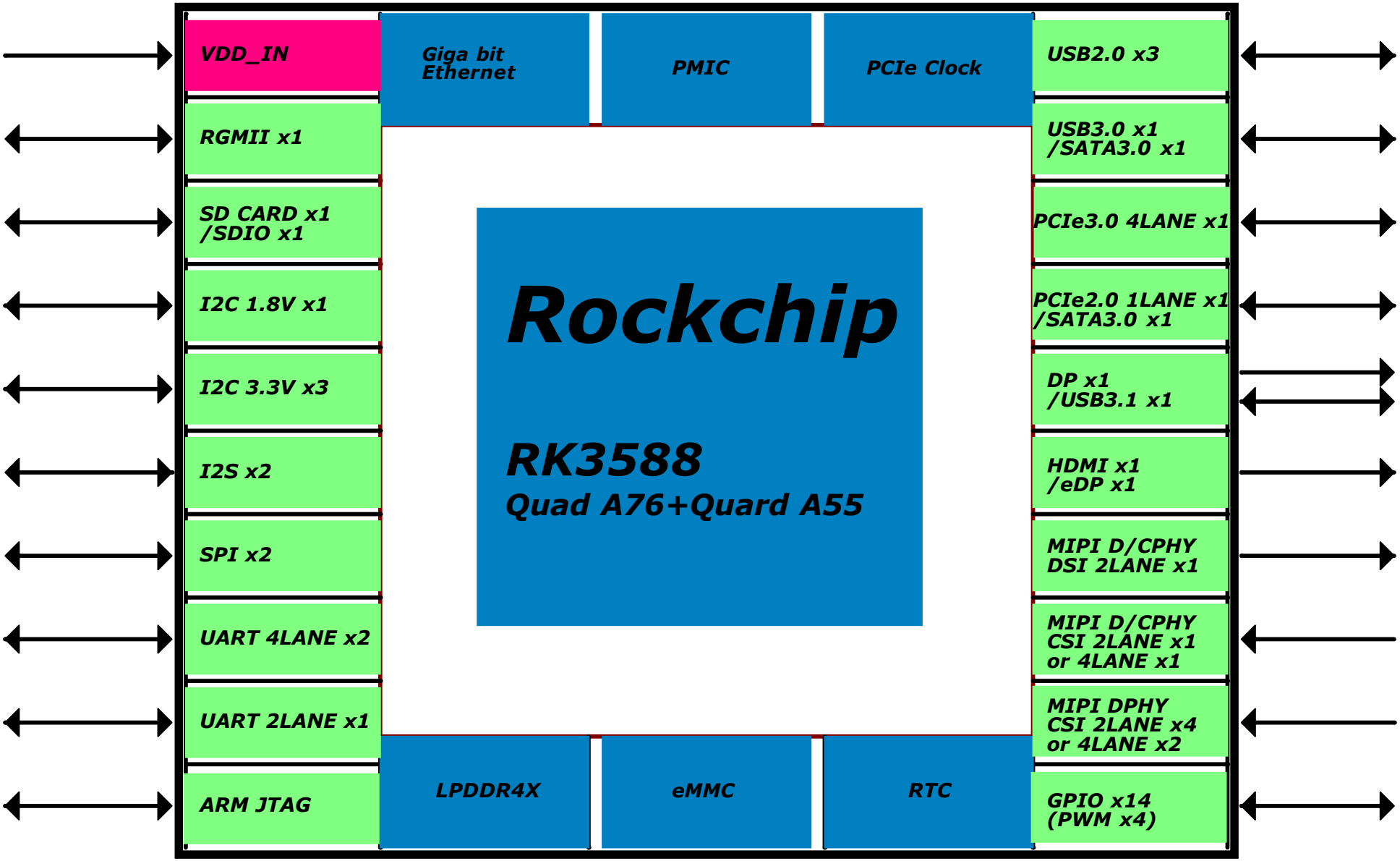
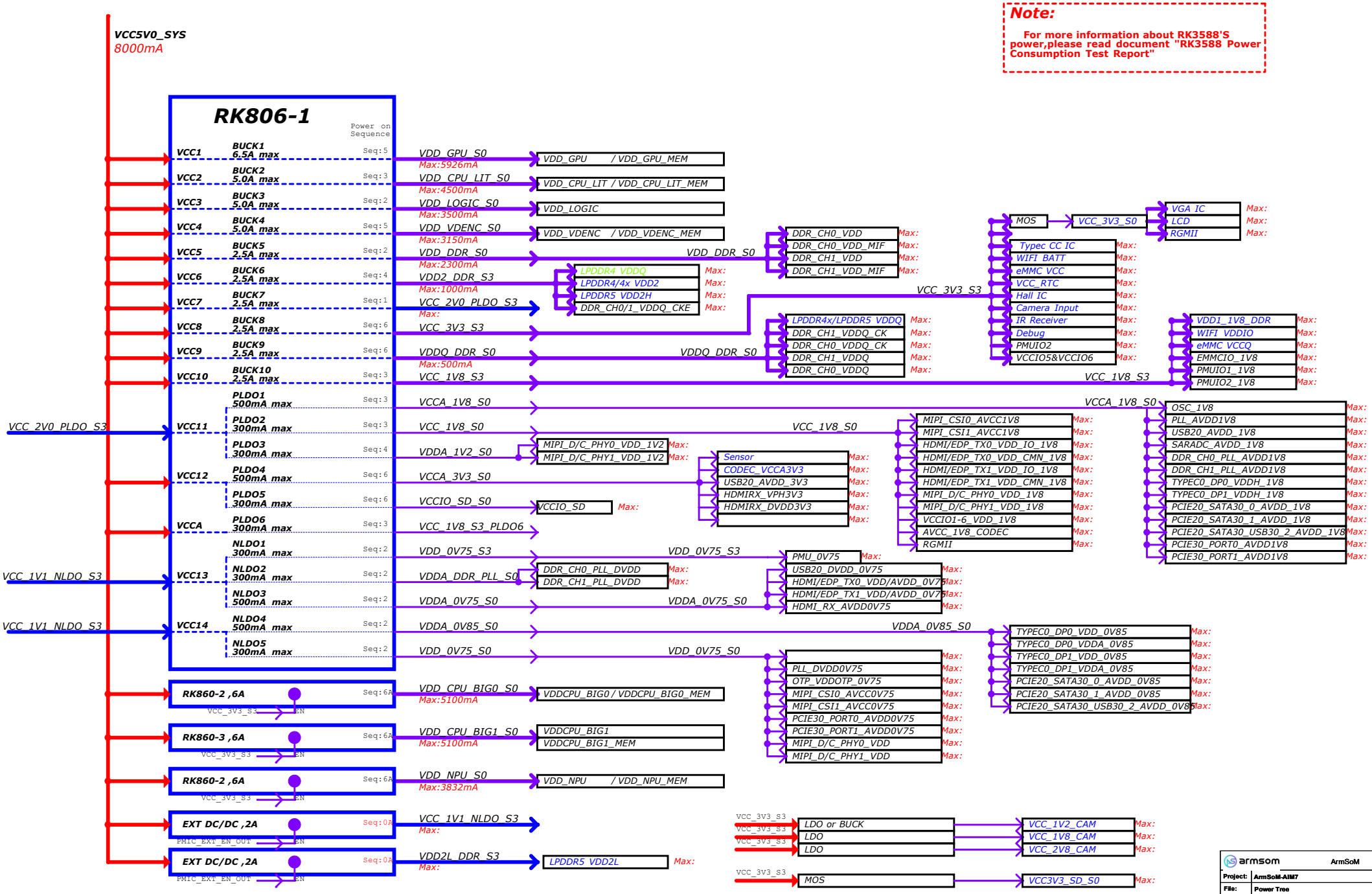
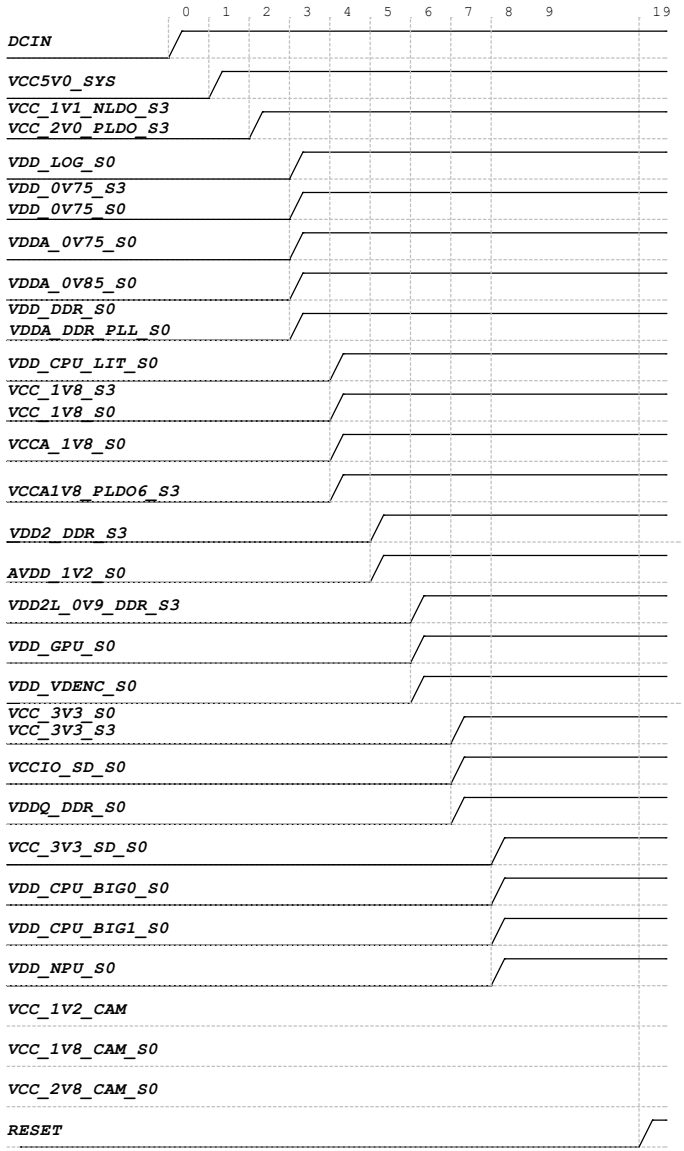


armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	Block Diagram				
Date:	Tuesday, October 08, 2024			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	4 of 24

Power Tree


VCC5V0_SYS
8000mA
RK806-1
Power on Sequence
VCC1 BUCK1 6.5A max Seq:5 VDD_GPU_S0 Max:5926mA
VCC2 BUCK2 5.0A max Seq:3 VDD_CPU_LIT_S0 Max:4500mA
VCC3 BUCK3 5.0A max Seq:2 VDD_LOGIC_S0 Max:3500mA
VCC4 BUCK4 5.0A max Seq:5 VDD_VDENC_S0 Max:3150mA
VCC5 BUCK5 2.5A max Seq:2 VDD_DDR_S0 Max:2300mA
VCC6 BUCK6 2.5A max Seq:4 VDD2_DDR_S3 Max:1000mA
VCC7 BUCK7 2.5A max Seq:1 VCC_2V0_PLDO_S3 Max:
VCC8 BUCK8 2.5A max Seq:6 VCC_3V3_S3
VCC9 BUCK9 2.5A max Seq:6 VDDQ_DDR_S0 Max:500mA
VCC10 BUCK10 2.5A max Seq:3 VCC_1V8_S3
PLDO1 500mA max Seq:3 VCCA_1V8_S0
VCC11 PLDO2 300mA max Seq:3 VCC_1V8_S0
PLDO3 300mA max Seq:4 VDDA_1V2_S0
VCC12 PLDO4 500mA max Seq:6 VCCA_3V3_S0
PLDO5 300mA max Seq:6 VCCIO_SD_S0
VCCA PLDO6 300mA max Seq:3 VCC_1V8_S3_PLDO6
NLDO1 300mA max Seq:2 VDD_0V75_S3
VCC13 NLDO2 300mA max Seq:2 VDDA_DDR_PLL_S0
NLDO3 500mA max Seq:2 VDDA_0V75_S0
VCC14 NLDO4 500mA max Seq:2 VDDA_0V85_S0
NLDO5 300mA max Seq:2 VDD_0V75_S0
RK860-2 ,6A Seq:6A VDD_CPU_BIG0_S0 Max:5100mA
RK860-3 ,6A Seq:6A VDD_CPU_BIG1_S0 Max:5100mA
RK860-2 ,6A Seq:6A VDD_NPU_S0 Max:3832mA
EXT DC/DC ,2A Seq:0A VCC_1V1_NLDO_S3 Max:
EXT DC/DC ,2A Seq:0A VDD2L_DDR_S3 Max:
VCC_3V3_S3
PMIC_EXT_EN_OUT
EN
VCC_2V0_PLDO_S3
VCC_1V1_NLDO_S3
VCC_1V1_NLDO_S3
VDD_GPU_S0 VDD_GPU / VDD_GPU_MEM
VDD_CPU_LIT_S0 VDD_CPU_LIT / VDD_CPU_LIT_MEM
VDD_LOGIC_S0 VDD_LOGIC
VDD_VDENC_S0 VDD_VDENC / VDD_VDENC_MEM
VDD_DDR_S0
LPDDR4 VDDQ Max:
LPDDR4/4x VDD2 Max:
LPDDR5 VDD2H Max:
DDR_CH0/1_VDDQ_CKE Max:
VCC_3V3_S3
VDDQ_DDR_S0
LPDDR4x/LPDDR5 VDDQ Max:
DDR_CH1_VDDQ_CK Max:
DDR_CH0_VDDQ_CK Max:
DDR_CH1_VDDQ Max:
DDR_CH0_VDDQ Max:
DDR_CH0_VDD Max:
DDR_CH0_VDD_MIF Max:
DDR_CH1_VDD Max:
DDR_CH1_VDD_MIF Max:
MOS
VCC_3V3_S0
VGA_IC Max:
LCD Max:
RGMII Max:
Typec CC IC Max:
WIFI_BATT Max:
eMMC VCC Max:
VCC_RTC Max:
Hall IC Max:
Camera Input Max:
IR_Receiver Max:
Debug Max:
PMUIO2 Max:
VCCIO5&VCCIO6 Max:
VCC_1V8_S3
VDD1_1V8_DDR Max:
WIFI_VDDIO Max:
eMMC VCCQ Max:
EMMCIO_1V8 Max:
PMUIO1_1V8 Max:
PMUIO2_1V8 Max:
VCCA_1V8_S0
OSC_1V8 Max:
PLL_AVDD1V8 Max:
USB20_AVDD_1V8 Max:
SARADC_AVDD_1V8 Max:
DDR_CH0_PLL_AVDD1V8 Max:
DDR_CH1_PLL_AVDD1V8 Max:
TYPEC0_DP0_VDDH_1V8 Max:
TYPEC0_DP1_VDDH_1V8 Max:
PCIE20_SATA30_0_AVDD_1V8 Max:
PCIE20_SATA30_1_AVDD_1V8 Max:
PCIE20_SATA30_USB30_2_AVDD_1V8 Max:
PCIE30_PORT0_AVDD1V8 Max:
PCIE30_PORT1_AVDD1V8 Max:
VCC_1V8_S0
MIPI_CSI0_AVCC1V8 Max:
MIPI_CSI1_AVCC1V8 Max:
HDMI/EDP_TX0_VDD_IO_1V8 Max:
HDMI/EDP_TX0_VDD_CMN_1V8 Max:
HDMI/EDP_TX1_VDD_IO_1V8 Max:
HDMI/EDP_TX1_VDD_CMN_1V8 Max:
MIPI_D/C_PHY0_VDD_1V8 Max:
MIPI_D/C_PHY1_VDD_1V8 Max:
VCCIO1-6_VDD_1V8 Max:
AVCC_1V8_CODEC Max:
RGMII Max:
MIPI_D/C_PHY0_VDD_1V2 Max:
MIPI_D/C_PHY1_VDD_1V2 Max:
Sensor Max:
CODEC_VCCA3V3 Max:
USB20_AVDD_3V3 Max:
HDMIRX_VPH3V3 Max:
HDMIRX_DVDD3V3 Max:
VCCIO_SD Max:
VDD_0V75_S3
PMU_0V75 Max:
USB20_DVDD_0V75 Max:
HDMI/EDP_TX0_VDD/AVDD_0V75 Max:
HDMI/EDP_TX1_VDD/AVDD_0V75 Max:
HDMI_RX_AVDD0V75 Max:
DDR_CH0_PLL_DVDD Max:
DDR_CH1_PLL_DVDD Max:
VDDA_0V75_S0
VDDA_0V85_S0
TYPEC0_DP0_VDD_0V85 Max:
TYPEC0_DP0_VDDA_0V85 Max:
TYPEC0_DP1_VDD_0V85 Max:
TYPEC0_DP1_VDDA_0V85 Max:
PCIE20_SATA30_0_AVDD_0V85 Max:
PCIE20_SATA30_1_AVDD_0V85 Max:
PCIE20_SATA30_USB30_2_AVDD_0V85 Max:
VDD_0V75_S0
PLL_DVDD0V75 Max:
OTP_VDDOTP_0V75 Max:
MIPI_CSI0_AVCC0V75 Max:
MIPI_CSI1_AVCC0V75 Max:
PCIE30_PORT0_AVDD0V75 Max:
PCIE30_PORT1_AVDD0V75 Max:
MIPI_D/C_PHY0_VDD Max:
MIPI_D/C_PHY1_VDD Max:
VDD_CPU_BIG0_S0 VDDCPU_BIG0 / VDDCPU_BIG0_MEM
VDD_CPU_BIG1_S0 VDDCPU_BIG1 / VDDCPU_BIG1_MEM
VDD_NPU_S0 VDD_NPU / VDD_NPU_MEM
VDD2L_DDR_S3 LPDDR5 VDD2L Max:
VCC_3V3_S3
LDO or BUCK
LDO
LDO
VCC_1V2_CAM Max:
VCC_1V8_CAM Max:
VCC_2V8_CAM Max:
MOS
VCC3V3_SD_S0 Max:
Note:
For more information about RK3588'S power,please read document "RK3588 Power Consumption Test Report"
armsom ArmSoM
Project: ArmSoM-AIM7
File: Power Tree
Date: Tuesday, October 08, 2024 Rev: V1.2
Designed by: Park Reviewed by: <Checker> Sheet: 5 of 24

Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC5V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC5V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC5V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC5V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC5V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC5V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC5V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC5V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC5V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_3V3_S3	EXT_BUCK	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	IO Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VCCIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_3V3_S0	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

armsom ArmSoM

Project:	ArmSoM-AIM7				
File:	System Power Sequence				
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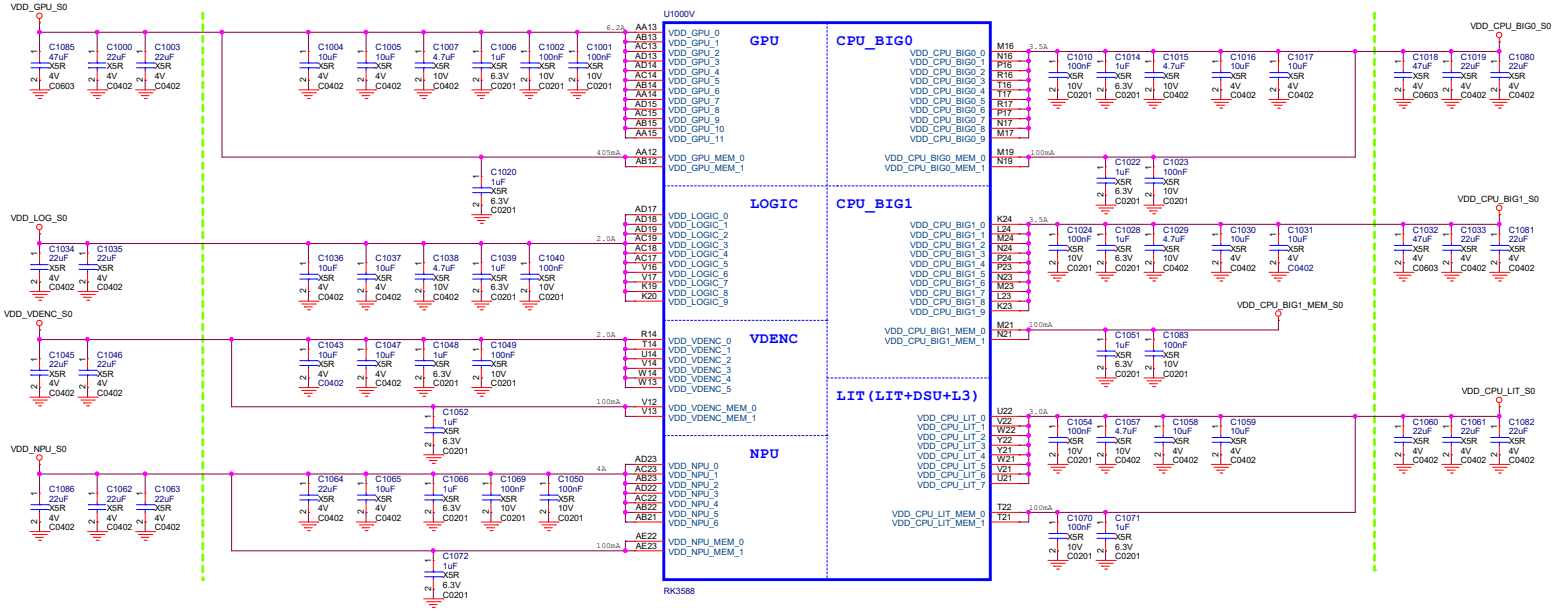
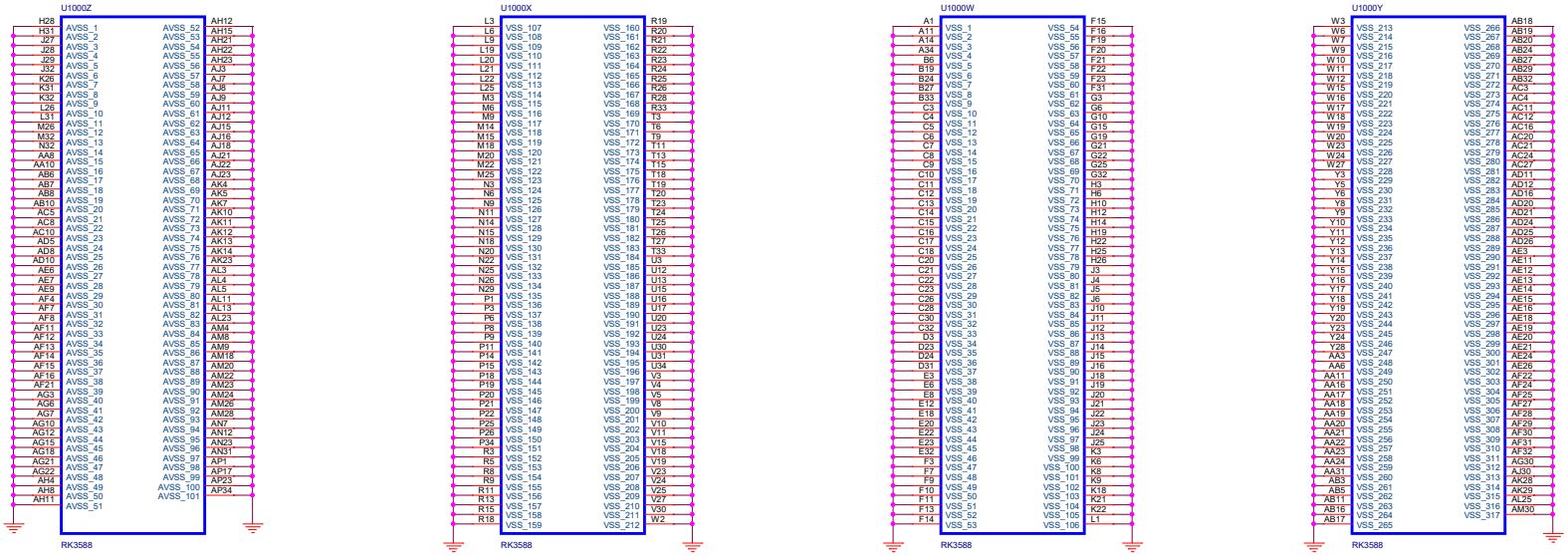
RK3588_V(POWER)



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



armsom	ArmSoM		
Project:	ArmSoM-AIM7		
File:	RK3588_Power/GND		
Date:	Tuesday, October 08, 2024	Rev:	V1.2
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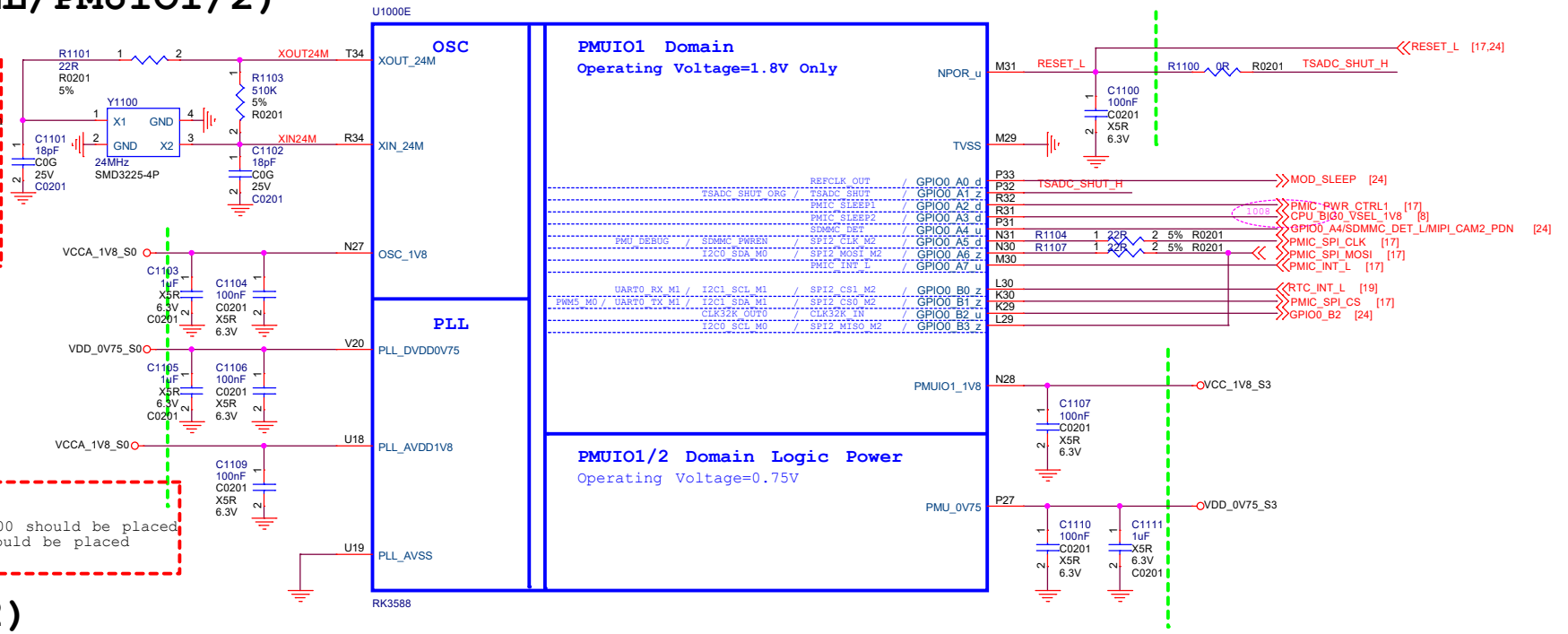
RK3588_E(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification

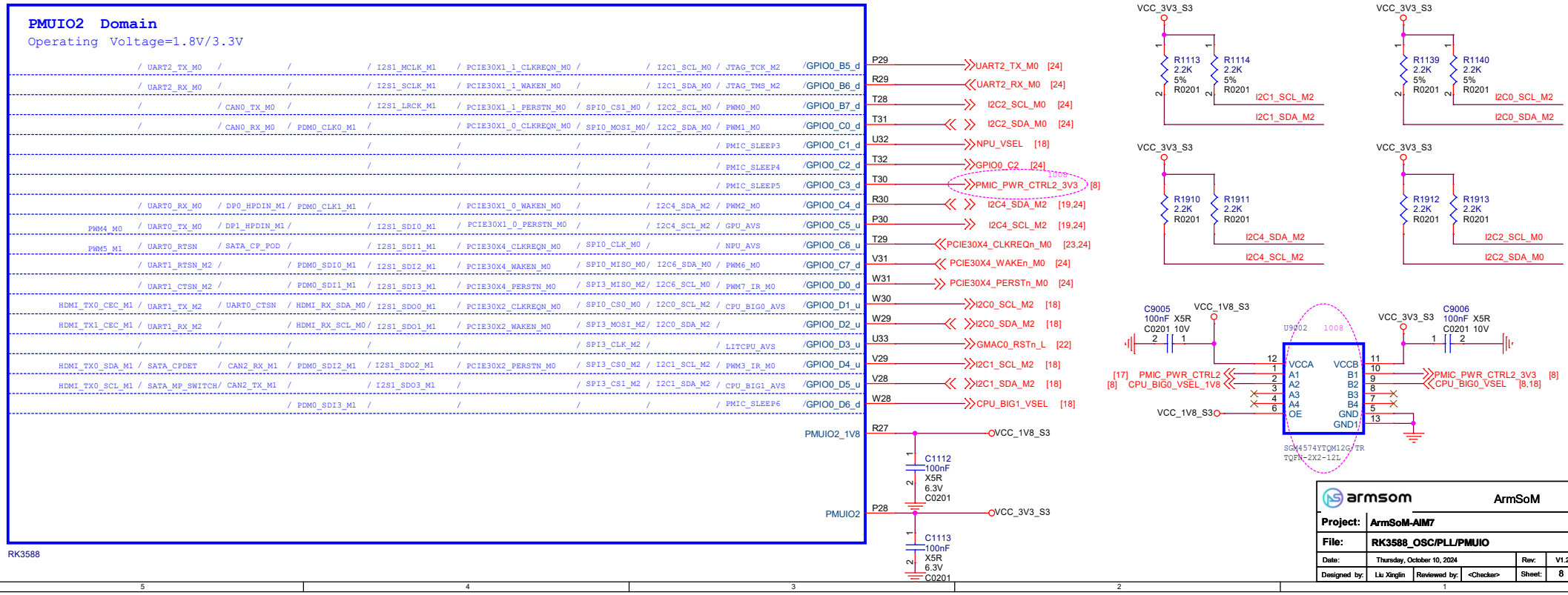
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF

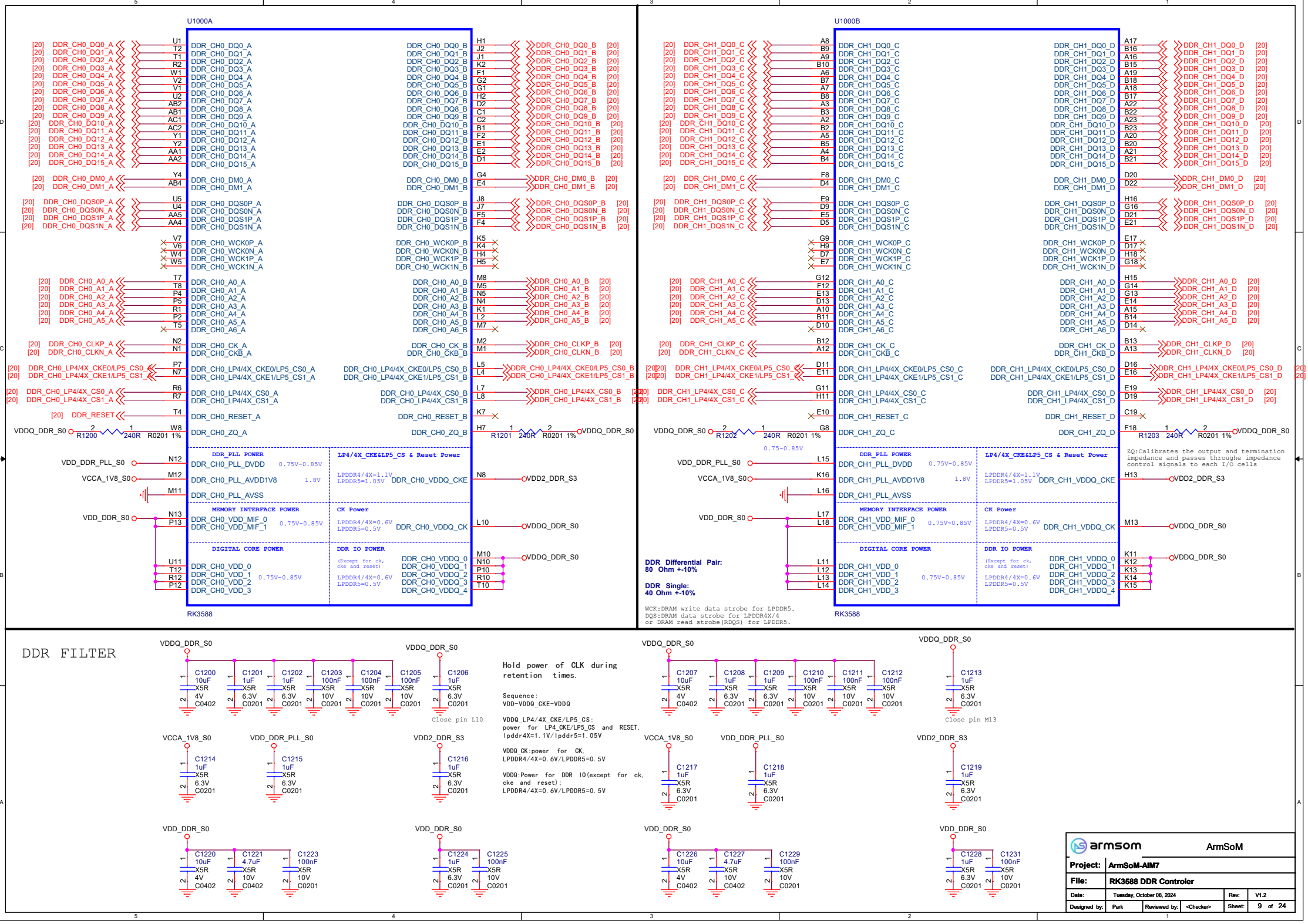


Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

RK3588_F(PMUIO2)



armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	RK3588_OSC/PLL/PMUIO				
Date:	Thursday, October 10, 2024		Rev:	V1.2	
Designed by:	Liu Xinglin	Reviewed by: <Checker>		Sheet:	8 of 24



armsom	ArmSoM		
Project:	ArmSoM-AIM7		
File:	RK3588 DDR Controler		
Date:	Tuesday, October 08, 2024	Rev:	V1.2
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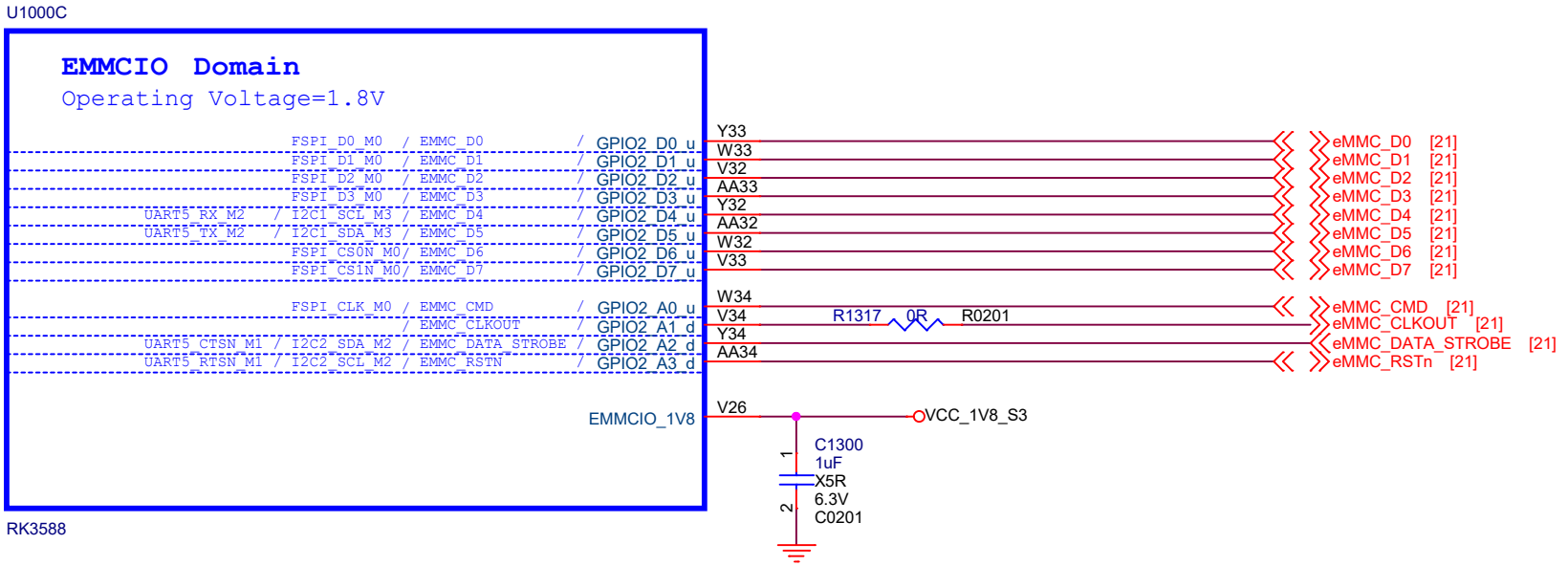
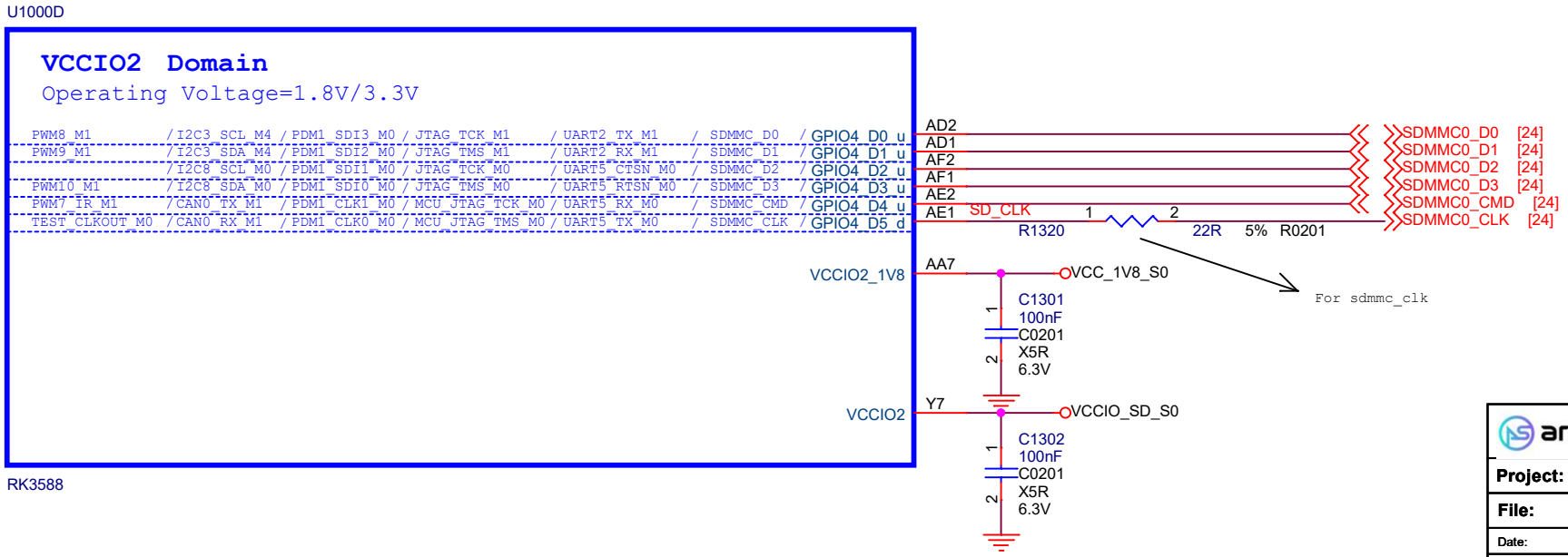
RK3588_C(EMMCIO Domain)

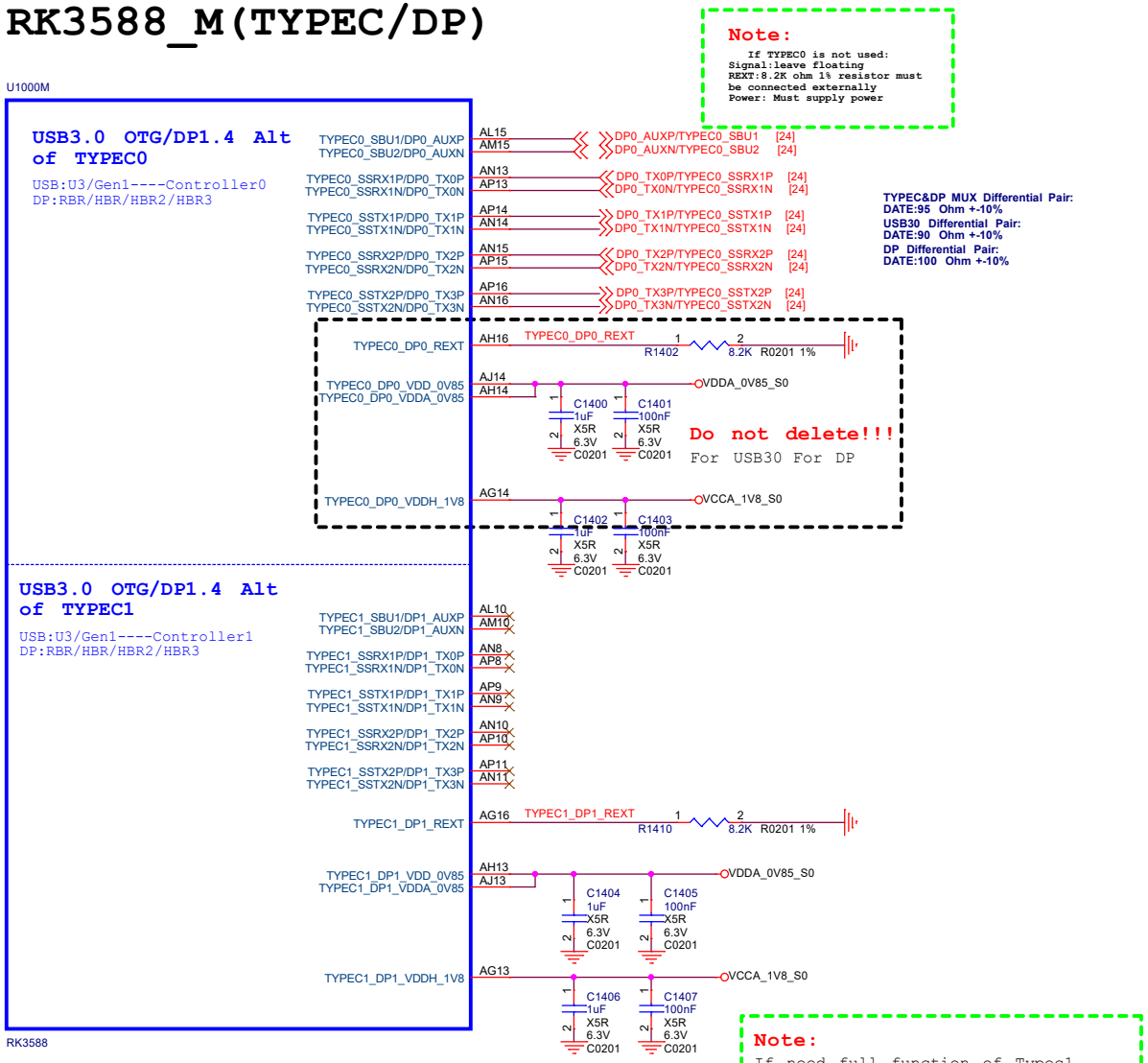


RK3588_D(VCCIO2 Domain)



armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	RK3588_Flash/SD Controller				
Date:	Tuesday, October 08, 2024			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	10 of 24

RK3588_M(TYPEC/DP)



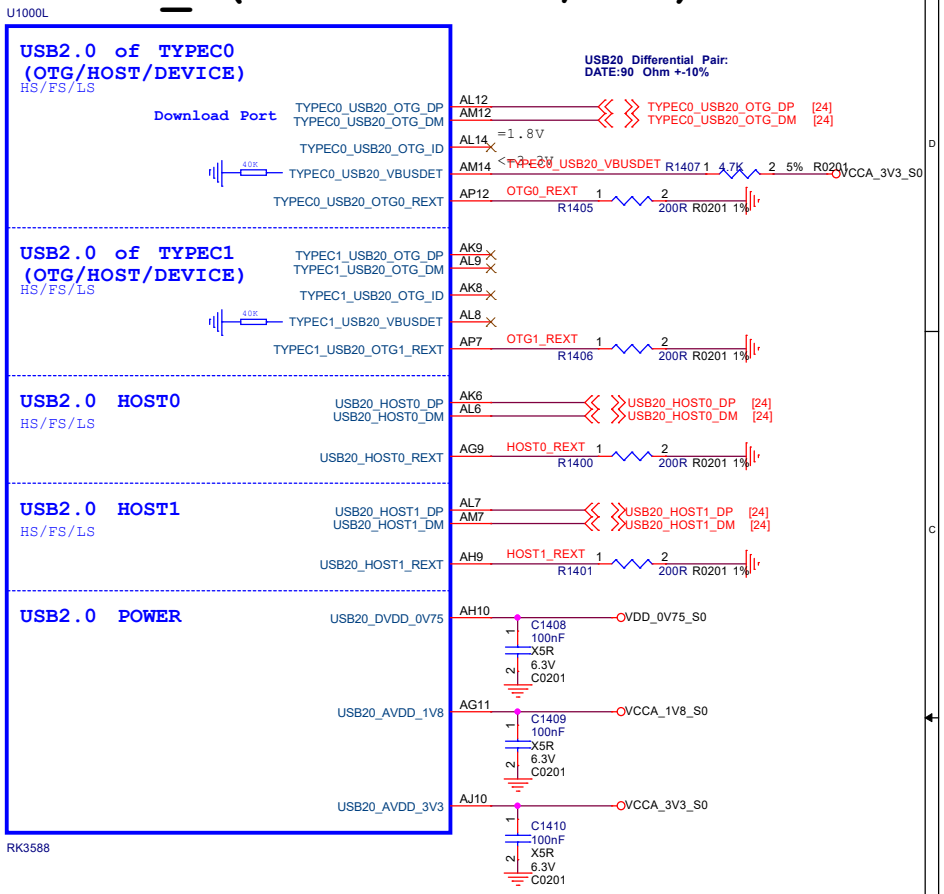
Note:
If need full function of Typec1 (With DP funtion) please Refer to the circuit of Typec0

If TYPEC1 is not used,
Signal: Leave floating
REXT: Leave floating
Power: Leave floating

USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*TYPEC_SSTX1P/1N&TYPEC_SSRX1P/1N or TYPEC_SSTX2P/2N&TYPEC_SSRX2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1 DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3 DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)



Note:
TYPEC0_USB20_OTG:
DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:
If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating
Power:Leave floating

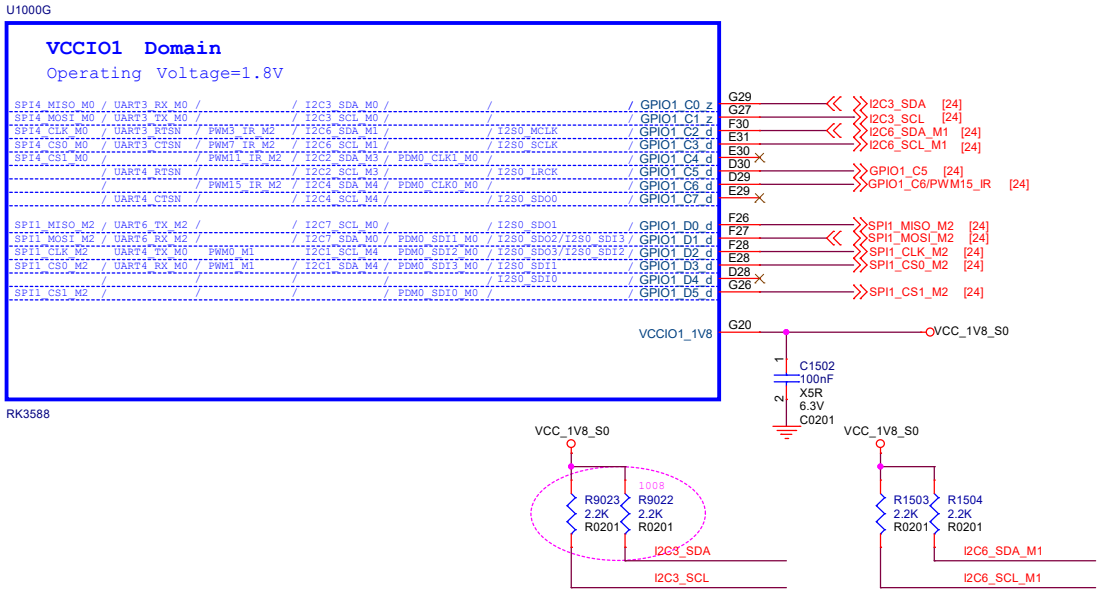
USB20_HOST0/USB20_HOST1:
If not used:
DP/DM:Leave floating
REXT:Leave floating
Power:Leave floating

Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

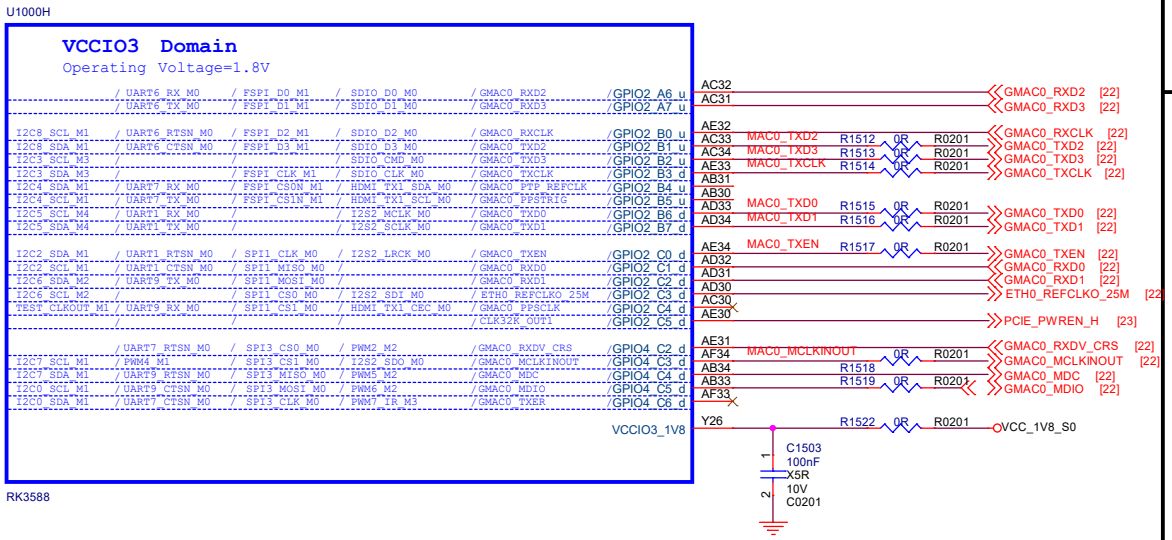
armsom ArmSoM

Project:	ArmSoM-AIM7				
File:	RK3588_USB30/USB20_Ctrl				
Date:	Tuesday, October 08, 2024			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	11 of 24

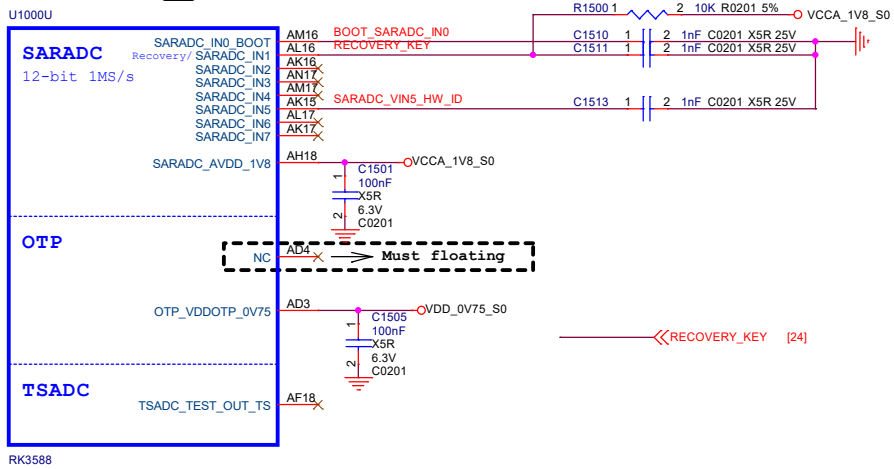
RK3588_G(VCCIO1 Domain)



RK3588_H(VCCIO3 Domain)



RK3588_U(SARADC/OTP)



BOOT MODE CONFIG

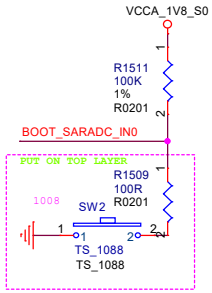


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	100K	0ohm	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG

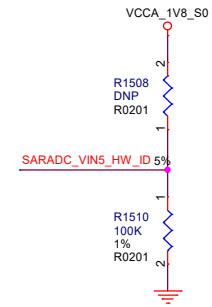


TABLE 2

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V2.0
LEVEL3	100K	51K	1365	0.6V	V3.0
LEVEL4	100K	100K	2047	0.9V	V4.0
LEVEL5	100K	200K	2730	1.2V	V5.0
LEVEL6	100K	499K	3412	1.5V	V6.0
LEVEL7	100K	DNP	4095	1.8V	V7.0

armsom ArmSoM

Project:	ArmSoM-AIM7				
File:	RK3588_SARADC/1.8V Only GPIO				
Date:	Tuesday, October 08, 2024			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	12 of 24

RK3588_Q/R(MIPI_D/C_PHY0/1)

U1000Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C — AN26
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B — AP26
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B — AN24
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A — AP24
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A — AN25
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C — AP25
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B — AN27
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A — AP27
MIPI_DPHY0_TX_D3P /NO_USE_AN28 — AN28
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C — AP28

MIPI DPHY Differential Pair:
100 Ohm +-10%

MIPI CPHY Single:
50 Ohm +-10%

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port0

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

Note:
此D-PHY不支持受限!!!
详细情况请参阅硬件设计指南。
This D-PHY is limited!!!
Please refer to the hardware design guide for details.

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C — AN32 — MIPI_DPHY0_RX_CLKP [24]
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B — AP31 — MIPI_DPHY0_RX_CLKN [24]
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B — AN29 — MIPI_DPHY0_RX_D0P [24]
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A — AP29 — MIPI_DPHY0_RX_D0N [24]
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A — AN30 — MIPI_DPHY0_RX_D1P [24]
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C — AP30 — MIPI_DPHY0_RX_D1N [24]
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B — AN33 — MIPI_DPHY0_RX_D2P [24]
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A — AP32 — MIPI_DPHY0_RX_D2N [24]
MIPI_DPHY0_RX_D3P /NO_USE_AN34 — AN34 — MIPI_DPHY0_RX_D3P [24]
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C — AP33 — MIPI_DPHY0_RX_D3N [24]

Note:
Suggest Using 1/2 lane mode
Using 4Lane is limited,
Please refer to the hardware design guide for details.

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG — AF20 — C16001 1uF — C0201 X5R 6.3V
MIPI_D/C_PHY0_VDD — AG20 — VDD_0V75_S0
C1602 100nF X5R 6.3V C0201
C1601 1uF X5R 6.3V C0201 C-PHY 5.7Gbps 0.85V D-PHY 2.5Gbps & C-PHY 5.7Gbps 0.75V
MIPI_D/C_PHY0_VDD_1V2 — AH20 — VDDA_1V2_S0
C1603 1uF X5R 6.3V C0201
MIPI_D/C_PHY0_VDD_1V8 — AJ20 — VCC_1V8_S0
C1605 1uF X5R 6.3V C0201

RK3588

U1000R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C — AN20 — MIPI_DPHY1_TX_CLKP [24]
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B — AP20 — MIPI_DPHY1_TX_CLKN [24]
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B — AN18 — MIPI_DPHY1_TX_D0P [24]
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A — AP18 — MIPI_DPHY1_TX_D0N [24]
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A — AN19 — MIPI_DPHY1_TX_D1P [24]
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C — AP19 — MIPI_DPHY1_TX_D1N [24]
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B — AN21 — AP21
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A
MIPI_DPHY1_TX_D3P /NO_USE_AN22 — AN22 — AP22
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port1

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

Note:
此D-PHY不支持受限!!!
详细情况请参阅硬件设计指南。
This D-PHY is limited!!!
Please refer to the hardware design guide for details.

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C — AK20
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B — AL20
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B — AK18
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A — AL18
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A — AK19
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C — AL19
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B — AK21
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A — AL21
MIPI_DPHY1_RX_D3P /NO_USE_AK22 — AK22
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C — AL22

Note:
Suggest Using 1/2 lane mode
Using 4Lane is limited,
Please refer to the hardware design guide for details.

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG — AF19 — C1608 1uF — C0201 X5R 6.3V
MIPI_D/C_PHY1_VDD — AG19 — VDD_0V75_S0
C1609 1uF X5R 6.3V C0201
MIPI_D/C_PHY1_VDD_1V2 — AH19 — VDDA_1V2_S0
C1611 100nF X5R 6.3V C0201
MIPI_D/C_PHY1_VDD_1V8 — AJ19 — VCC_1V8_S0
C1613 1uF X5R 6.3V C0201

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588

RK3588_P(MIPI_DPHY_CSI_RX_PHY)

U1000P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P/MIPI_CSI0_CLK0N — AJ33/AJ34 — MIPI_CSI0_RX_CLK0P/N [24]
MIPI_CSI0_D0P/MIPI_CSI0_D0N — AG33/AG34 — MIPI_CSI0_RX_D0P/N [24]
MIPI_CSI0_D1P/MIPI_CSI0_D1N — AH33/AH34 — MIPI_CSI0_RX_D1P/N [24]
MIPI_CSI0_CLK1P/MIPI_CSI0_CLK1N — AM33/AM34 — MIPI_CSI0_RX_CLK1P/N [24]
MIPI_CSI0_D2P/MIPI_CSI0_D2N — AK33/AK34 — MIPI_CSI0_RX_D2P/N [24]
MIPI_CSI0_D3P/MIPI_CSI0_D3N — AL33/AL34 — MIPI_CSI0_RX_D3P/N [24]

MIPI CSI Differential Pair:
100 Ohm +-10%

MIPI_CSI0_AVCC0V75 — AB25 — VDD_0V75_S0
C1616 100nF X5R 6.3V C0201
C1615 1uF X5R 6.3V C0201
MIPI_CSI0_AVCC1V8 — AB26 — VCC_1V8_S0
C1617 1uF X5R 6.3V C0201

Note:
建议先使用U1000P这个模块的DPHY CSI_RX。
First use the DPHY_CSI_RX controller of U1000P.

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P/MIPI_CSI1_CLK0N — AJ31/AJ32 — MIPI_CSI1_RX_CLK0P/N [24]
MIPI_CSI1_D0P/MIPI_CSI1_D0N — AG31/AG32 — MIPI_CSI1_RX_D0P/N [24]
MIPI_CSI1_D1P/MIPI_CSI1_D1N — AH31/AH32 — MIPI_CSI1_RX_D1P/N [24]
MIPI_CSI1_CLK1P/MIPI_CSI1_CLK1N — AM31/AM32 — MIPI_CSI1_RX_CLK1P/N [24]
MIPI_CSI1_D2P/MIPI_CSI1_D2N — AK31/AK32 — MIPI_CSI1_RX_D2P/N [24]
MIPI_CSI1_D3P/MIPI_CSI1_D3N — AL31/AL32 — MIPI_CSI1_RX_D3P/N [24]

MIPI_CSI1_AVCC0V75 — AA25 — VDD_0V75_S0
C1619 1uF X5R 6.3V C0201
MIPI_CSI1_AVCC1V8 — AA26 — VCC_1V8_S0
C1621 100nF X5R 6.3V C0201

RK3588

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

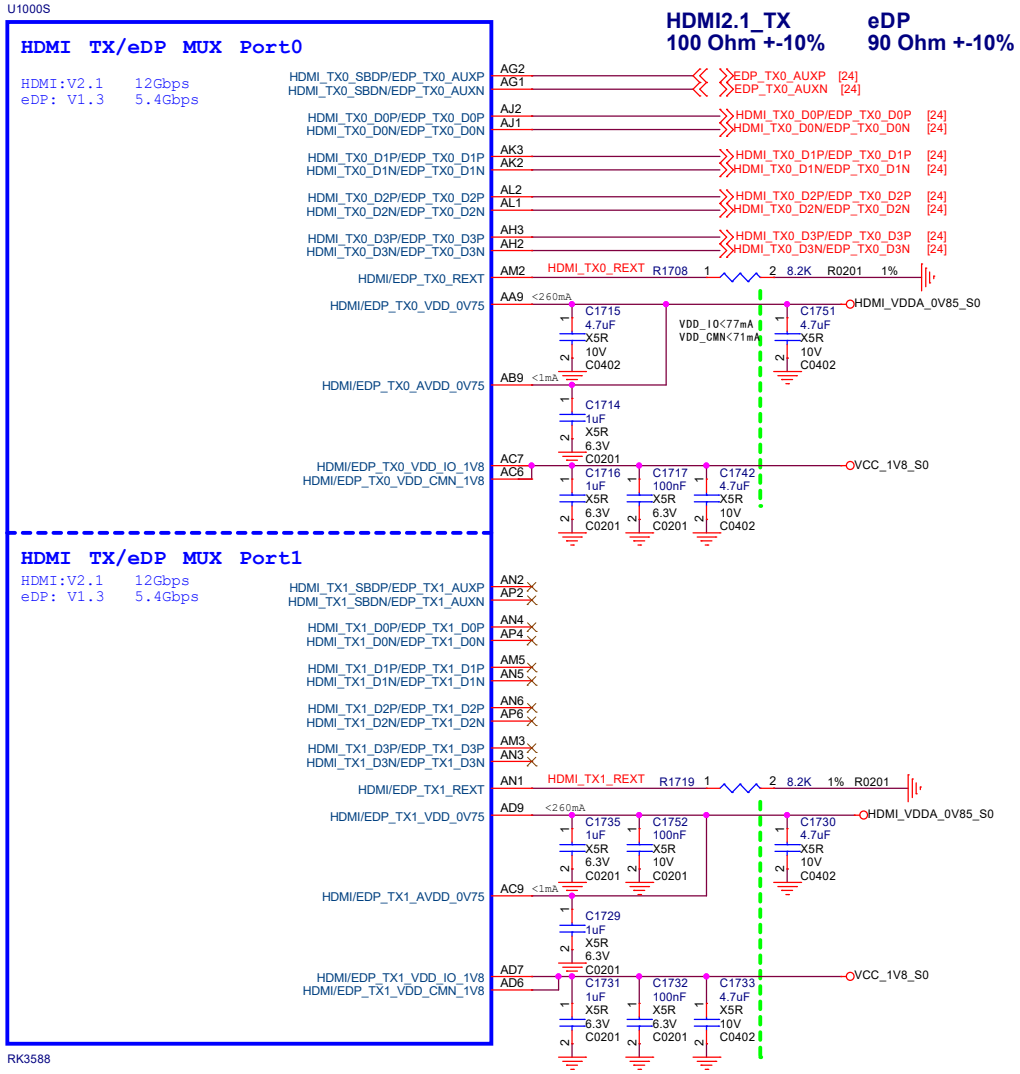
Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating

armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	RK3588_MIPI Interface				
Date:	Tuesday, October 08, 2024			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	13 of 24

RK3588_S(HDMI2.1 TX)

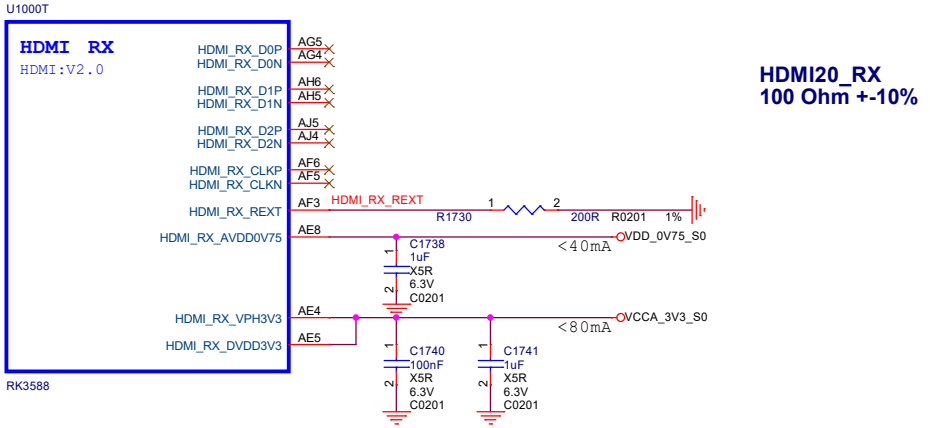
Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.



Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

RK3588_T(HDMI20 RX)



Note:
If not used:
Signal:leave floating
Power: Floating

armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	RK3588_HDMI/eDP Interface				
Date:	Tuesday, October 08, 2024			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	14 of 24

RK3588_N(PCIE20)

U1000N

Note:
If not used:
Signal:leave floating
Power: Floating

PCIE20/SATA30 Mux0

PCIe20x1_2
1Lane(RC)--4(1L2)

SATA30 HOST
Controller0

MUX

input or output

PCIE20_0_REFCLKP L32 / PCIE20_0_REFCLKN L33 — PCIE20_0_REFCLKP [24] / PCIE20_0_REFCLKN [24]
PCIE20_0_TXP/SATA30_0_TXP M34 / PCIE20_0_TXN/SATA30_0_TXN M33 — PCIE20_0_TXP/SATA30_0_TXP [24] / PCIE20_0_TXN/SATA30_0_TXN [24]
PCIE20_0_RXP/SATA30_0_RXP N33 / PCIE20_0_RXN/SATA30_0_RXN N34 — PCIE20_0_RXP/SATA30_0_RXP [24] / PCIE20_0_RXN/SATA30_0_RXN [24]

PCIE20_SATA30_0_AVDD_0V85 M28 — C1810 10uF X5R 4V C0402 — VDDA_0V85_S0
PCIE20_SATA30_0_AVDD_1V8 M27 — C1808 1uF X5R 6.3V C0201 — VCCA_1V8_S0

CLK Differential Pair:
100 Ohm± 10 %
DATA Differential Pair:
PCIE20: 85 Ohm ± 10 %
SATA30: 100 Ohm ± 10 %
USB30: 90ohm ± 10 %

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0
1Lane(RC)--2(1L0)

SATA30 HOST
Controller1

MUX

input or output

PCIE20_1_REFCLKP H32 / PCIE20_1_REFCLKN H33
PCIE20_1_TXP/SATA30_1_TXP K33 / PCIE20_1_TXN/SATA30_1_TXN K34
PCIE20_1_RXP/SATA30_1_RXP J33 / PCIE20_1_RXN/SATA30_1_RXN J34

PCIE20_SATA30_1_AVDD_0V85 L28 — C1818 100nF X5R 6.3V C0201 — VDDA_0V85_S0
PCIE20_SATA30_1_AVDD_1V8 L27 — C1816 100nF X5R 6.3V C0201 — VCCA_1V8_S0

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1
1Lane(RC)--3(1L1)

SATA30 HOST
Controller2

USB30 HOST
Controller2

MUX

input or output

PCIE20_2_REFCLKP G31 / PCIE20_2_REFCLKN G30
PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP H30 / PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN H29 — USB30_2_SSTXP/SATA30_2_TXP [24] / USB30_2_SSTXN/SATA30_2_TXN [24]
PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP J31 / PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN J30 — USB30_2_SSRXP/SATA30_2_RXP [24] / USB30_2_SSRXN/SATA30_2_RXN [24]

PCIE20_SATA30_USB30_2_AVDD_0V85 K28 — C1806 1uF X5R 6.3V C0201 — VDDA_0V85_S0
PCIE20_SATA30_USB30_2_AVDD_1V8 K27 — C1804 1uF X5R 6.3V C0201 — VCCA_1V8_S0

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588

Note:
The SATA differential trace impedance is 100 OHM
The SATA trace length is less than 5 inch

RK3588_O(PCIE30)

Note:
Only PCIE3.0 Controller 0 support RC and EP,Other controller only support RC Mode.

U1000O

PCIE30X4

PCIe30X4
4Lane(DM)--0(4L)

PCIe30x1_0
1Lane(RC)--2(1L0)

PCIE20/SATA30 MUX1

PCIe30x2
2Lane(RC)--1(2L)

PCIe30x1_1
1Lane(RC)--3(1L1)

PCIE20/SATA30/USB30 MUX2

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0

input PCIE30_PORT0_REF_CLKP / PCIE30_PORT0_REF_CLKN

Lane0
PCIE30_PORT0_TX0P / PCIE30_PORT0_TX0N
PCIE30_PORT0_RX0P / PCIE30_PORT0_RX0N

Lane1
PCIE30_PORT0_TX1P / PCIE30_PORT0_TX1N
PCIE30_PORT0_RX1P / PCIE30_PORT0_RX1N

PCIE30_PORT0_RESREF — PCIE30_0_REF B34 — R1801 R0201 200R 1%
PCIE30_PORT0_AVDD0V75 G24 — VDD_0V75_S0
C1802 1uF X5R 6.3V C0201 / C1803 4.7uF X5R 10V C0402
PCIE30_PORT0_AVDD1V8 G23 — VCCA_1V8_S0
C1800 1uF X5R 6.3V C0201 / C1801 4.7uF X5R 10V C0402

PCIE30 PORT1

input PCIE30_PORT1_REF_CLKP / PCIE30_PORT1_REF_CLKN

Lane0
PCIE30_PORT1_TX0P / PCIE30_PORT1_TX0N
PCIE30_PORT1_RX0P / PCIE30_PORT1_RX0N

Lane1
PCIE30_PORT1_TX1P / PCIE30_PORT1_TX1N
PCIE30_PORT1_RX1P / PCIE30_PORT1_RX1N

PCIE30_PORT1_RESREF — PCIE30_1_REF A33 — R1807 R0201 200R 1%
PCIE30_PORT1_AVDD0V75 H24 — VDD_0V75_S0
C1814 1uF X5R 6.3V C0201 / C1815 4.7uF X5R C0402 10V
PCIE30_PORT1_AVDD1V8 H23 — VCCA_1V8_S0
C1812 100nF X5R 6.3V C0201 / C1813 4.7uF X5R 10V C0402

CLK Differential Pair:
100 Ohm ± 10 %
DATA Differential Pair:
PCIE30: 85 Ohm ± 10 %

E33 PCIE30_PORT0_REFCLKP_IN [23] / E34 PCIE30_PORT0_REFCLKN_IN [23]
D32 PCIE30_PORT0_TX0P [24] / D33 PCIE30_PORT0_TX0N [24]
G33 PCIE30_PORT0_RX0P [24] / G34 PCIE30_PORT0_RX0N [24]
C33 PCIE30_PORT0_TX1P [24] / C34 PCIE30_PORT0_TX1N [24]
F32 PCIE30_PORT0_RX1P [24] / F33 PCIE30_PORT0_RX1N [24]

A28 PCIE30_PORT1_REFCLKP_IN [23] / B28 PCIE30_PORT1_REFCLKN_IN [23]
B30 PCIE30_PORT1_TX2P [24] / A30 PCIE30_PORT1_TX2N [24]
B32 PCIE30_PORT1_RX2P [24] / A32 PCIE30_PORT1_RX2N [24]
C29 PCIE30_PORT1_TX3P [24] / B29 PCIE30_PORT1_TX3N [24]
C31 PCIE30_PORT1_RX3P [24] / B31 PCIE30_PORT1_RX3N [24]

RK3588

Note:
If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

armsom ArmSoM

Project:	ArmSoM-AIM7				
File:	RK3588_PCIE30/PCIE20/SATA30				
Date:	Tuesday, October 08, 2024			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	15 of 24

RK3588_I(VCCIO4 Domain)

U1000I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

		/SPI4_MISO_M2	/PCIE30X1_1_CLKREQN_M2	/ DP0_HPDIN_M2	/ I2C2_SDA_M4	/ UART6_RX_M1	/GPIO1_A0_d
SATA1_ACT_LED_M1	/	/	/SPI4_MOSI_M2	/PCIE30X1_1_WAKEN_M2	/ DP1_HPDIN_M2	/ I2C2_SCL_M4	/ UART6_TX_M1	/GPIO1_A1_d
		/ PWM0_M2	/SPI4_CLK_M2	/	/ VOP_POST_EMPTY	/ I2C4_SDA_M3	/ UART6_RTSN_M1	/GPIO1_A2_d
		/ PWM1_M2	/SPI4_CS0_M2	/	/ HDMI_TX1_SDA_M2	/ I2C4_SCL_M3	/ UART6_CTSN_M1	/GPIO1_A3_d
		/	/SPI2_MISO_M0	/	/ HDMI_TX1_SCL_M2	/	/	/GPIO1_A4_d
		/	/SPI2_MOSI_M0	/	/ HDMI_TX0_HPD_M0	/	/	/GPIO1_A5_d
		/	/SPI2_CLK_M0	/	/ HDMI_TX1_HPD_M0	/	/	/GPIO1_A6_d
		/ PWM3_IR_M3	/SPI2_CS0_M0	/PCIE30X1_1_PERSTN_M2	/	/ PDM1_SDI0_M1	/	/GPIO1_A7_u
		/	/SPI2_CS1_M0	/PCIE30X4_CLKREQN_M3	/	/ PDM1_SDI1_M1	/	/GPIO1_B0_u
		/	/SPI0_MISO_M2	/PCIE30X4_WAKEN_M3	/	/ PDM1_SDI2_M1	/	/GPIO1_B1_d
		/	/SPI0_MOSI_M2	/PCIE30X4_PERSTN_M3	/	/ PDM1_SDI3_M1	/ UART4_RX_M2	/GPIO1_B2_d
SATA0_ACT_LED_M1	/	/	/SPI0_CLK_M2	/PCIE30X1_0_WAKEN_M2	/	/ PDM1_CLK1_M1	/ UART4_TX_M2	/GPIO1_B3_d
		/	/SPI0_CS0_M2	/PCIE30X1_0_PERSTN_M2	/	/ PDM1_CLK0_M1	/ UART7_RX_M2	/GPIO1_B4_u
		/	/SPI0_CS1_M2	/PCIE30X1_0_CLKREQN_M2/	/	/	/ UART7_TX_M2	/GPIO1_B5_u
	HDMI_RX_HPDOUT_M2 /		/SPDIF0_TX_M0	/PCIE30X2_WAKEN_M3	/ MIPI_CAMERA1_CLK_M0	/ I2C5_SCL_M3	/ UART1_TX_M1	/GPIO1_B6_u
SATA2_ACT_LED_M1 /	HDMI_RX_CEC_M2	/ PWM3_M2	/SPDIF1_TX_M0	/PCIE30X2_PERSTN_M3	/ MIPI_CAMERA2_CLK_M0	/ I2C5_SDA_M3	/ UART1_RX_M1	/GPIO1_B7_u
	HDMI_RX_SCL_M2	/ PWM14_M2	/	/	/ MIPI_CAMERA3_CLK_M0	/ I2C8_SCL_M2	/ UART1_RTSN_M1	/GPIO1_D6_u
	HDMI_RX_SDA_M2	/ PWM15_IR_M3	/	/PCIE30X2_CLKREQN_M3	/ MIPI_CAMERA4_CLK_M0	/ I2C8_SDA_M2	/ UART1_CTSN_M1	/GPIO1_D7_u

A24	GPIO1_A0_d	OP0_HPDIN_M2 [24]
A25	GPIO1_A1_d	
A26	GPIO1_A2_d	
A27	GPIO1_A3_d	
B25	GPIO1_A4_d	
B26	GPIO1_A5_d	HDMI_TX0_HPD_M0 [24]
C24	GPIO1_A6_d	
C25	GPIO1_A7_u	
C27	GPIO1_B0_u	
D25	GPIO1_B1_d	SPI0_MISO_M2 [24]
D26	GPIO1_B2_d	SPI0_MOSI_M2 [24]
D27	GPIO1_B3_d	SPI0_CLK_M2 [24]
E24	GPIO1_B4_u	SPI0_CS0_M2 [24]
E25	GPIO1_B5_u	SPI0_CS1_M2 [24]
E26	GPIO1_B6_u	UART1_TX_M1 [24]
E27	GPIO1_B7_u	UART1_RX_M1 [24]
F24	GPIO1_D6_u	UART1_RTSn_M1 [24]
F25	GPIO1_D7_u	UART1_CTSn_M1 [24]

VCCIO4_1V8 — H20 — OVCC_1V8_S0

C1907 100nF X5R 6.3V C0201

VCCIO4 — H21 — OVCC_1V8_S0

C1906 100nF X5R 6.3V C0201

RK3588

RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	/ SPI4_MISO_M1	/	/ I2C6_SDA_M4	/FSPI_D0_M2	/I2S3_MCLK	/ SDIO_D0_M1	/GMAC1_TXD2	/ GPIO3_A0_u
AUDDSM_LN	/ SPI4_MOSI_M1	/ PWM11_IR_M0	/I2C6_SCL_M4	/FSPI_D1_M2	/I2S3_SCLK	/ SDIO_D1_M1	/GMAC1_TXD3	/ GPIO3_A1_u
AUDDSM_LP	/ SPI4_CLK_M1	/ UART8_TX_M1	/	/FSPI_D2_M2	/I2S3_LRCK	/ SDIO_D2_M1	/GMAC1_RXD2	/ GPIO3_A2_u
AUDDSM_RN	/ SPI4_CS0_M1	/ UART8_RX_M1	/	/FSPI_D3_M2	/I2S3_SDO	/ SDIO_D3_M1	/GMAC1_RXD3	/ GPIO3_A3_u
AUDDSM_RP	/ SPI4_CS1_M1	/ UART8_RTSN_M1	/	/	/I2S3_SDI	/ SDIO_CMD_M1	/GMAC1_TXCLK	/ GPIO3_A4_d
	/ MIPI_CAMERA0_CLK_M1	/ UART8_CTSN_M1	/I2C4_SDA_M0	/FSPI_CLK_M2	/	/ SDIO_CLK_M1	/GMAC1_RXCLK	/ GPIO3_A5_d
	/ MIPI_CAMERA1_CLK_M1	/	/I2C4_SCL_M0	/	/	/	/ ETH1_REFCLKO_25M	/ GPIO3_A6_d
PWM8_M0	/ MIPI_CAMERA2_CLK_M1	/	/	/	/	/	/GMAC1_RXD0	/ GPIO3_A7_u
PWM9_M0	/ MIPI_CAMERA3_CLK_M1	/	/	/	/	/	/GMAC1_RXD1	/ GPIO3_B0_u
PWM2_M1	/ MIPI_CAMERA4_CLK_M1	/ UART2_TX_M2	/	/	/	/	/GMAC1_RXDV_CRS	/ GPIO3_B1_d
PWM3_IR_M1	/	/ UART2_RX_M2	/	/	/I2S2_SDI_M1	/	/GMAC1_TXER	/ GPIO3_B2_d
	/	/ UART2_RTSN	/	/	/I2S2_SDO_M1	/	/GMAC1_TXD0	/ GPIO3_B3_u
	/	/ UART2_CTSN	/	/	/I2S2_MCLK_M1	/	/GMAC1_TXD1	/ GPIO3_B4_u
PWM12_M0	/ CAN1_RX_M0	/ UART3_TX_M1	/	/	/I2S2_SCLK_M1	/	/GMAC1_TXEN	/ GPIO3_B5_u
PWM13_M0	/ CAN1_TX_M0	/ UART3_RX_M1	/	/	/I2S2_LRCK_M1	/	/GMAC1_MCLKINOUT	/ GPIO3_B6_d
	/	/	/ I2C3_SCL_M1	/ SPI1_MOSI_M1	/HDMI_TX1_HPD_M1	/	/GMAC1_PTP_REF_CLK	/ GPIO3_B7_d
	/	/ UART7_TX_M1	/ I2C3_SDA_M1	/ SPI1_MISO_M1	/	/	/GMAC1_PPSTRIG	/ GPIO3_C0_d
	/ PCIE30X2_BUTTON_RSTN	/ UART7_RX_M1	/	/ SPI1_CLK_M1	/	/	/GMAC1_PPSCLK	/ GPIO3_C1_d
PWM14_M0	/	/ UART7_RTSN_M1	/ I2C8_SCL_M4	/ SPI1_CS0_M1	/	/ MIPI_TE0	/ GMAC1_MDC	/ GPIO3_C2_d
PWM15_IR_M0	/	/ UART7_CTSN_M1	/ I2C8_SDA_M4	/ SPI1_CS1_M1	/	/ MIPI_TE1	/ GMAC1_MDIO	/ GPIO3_C3_d
CAN2_RX_M0	/ PCIE30X4_CLKREQN_M2	/ UART5_TX_M1	/	/FSPI_CS0N_M2	/ SPI3_CS0_M3	/ HDMI_TX1_CEC_M2	/	/ GPIO3_C4_u
CAN2_TX_M0	/ PCIE30X4_WAKEN_M2	/ UART5_RX_M1	/	/FSPI_CS1N_M2	/ SPI3_CS1_M3	/ HDMI_TX1_SDA_M1	/	/ GPIO3_C5_u
	/ PCIE30X4_PERSTN_M2	/	/	/	/ SPI3_MISO_M3	/ HDMI_TX1_SCL_M1	/	/ GPIO3_C6_u
	/ PCIE20X1_2_CLKREQN_M0	/	/ I2C5_SCL_M0	/ SPI3_MOSI_M3	/ HDMI_TX0_SCL_M2	/	/ CIF_D11	/ GPIO3_C7_u
PWM8_M2	/ PCIE20X1_2_WAKEN_M0	/ UART4_RX_M1	/ I2C5_SDA_M0	/ SPI3_CLK_M3	/ HDMI_TX0_SDA_M2	/	/ CIF_D12	/ GPIO3_D0_u
PWM9_M2	/ PCIE20X1_2_PERSTN_M0	/ UART4_TX_M1	/	/ SPI3_MISO_M3	/ HDMI_RX_CEC_M1	/	/ CIF_D13	/ GPIO3_D1_d
	/ PCIE30X2_CLKREQN_M2	/ UART9_RTSN_M2	/ I2C7_SCL_M2	/ SPI3_MOSI_M3	/HDMI_RX_SCL_M1	/	/ CIF_D14	/ GPIO3_D2_d
PWM10_M2	/ PCIE30X2_WAKEN_M2	/ UART9_CTSN_M2	/ I2C7_SDA_M2	/ SPI3_CLK_M3	/ HDMI_RX_SDA_M1	/	/ CIF_D15	/ GPIO3_D3_d
	/ PCIE30X2_PERSTN_M2	/ UART9_RX_M2	/	/ SPI3_CS0_M3	/HDMI_RX_HPDOUT_M1/	HDMI_TX0_HPD_M1/	MCU_JTAG_TCK_M1	/ GPIO3_D4_d
PWM11_IR_M3	/ PCIE30X4_BUTTON_RSTN	/ UART9_TX_M2	/	/ SPI3_CS1_M3	/DP1_HPDIN_M0	/	/ MCU_JTAG_TMS_M1	/ GPIO3_D5_d

AA29	GPIO3_A0_u	GPIO3_A0/PWM10 [24]
AA30	GPIO3_A1_u	GPIO3_A1/PWM11_IR/MIPI_CAM4_PDN [24]
AD27	GPIO3_A2_u	MIPI_CAM0_PDN_L [24]
AE27	GPIO3_A3_u	
AD28	GPIO3_A4_d	
AH30	GPIO3_A5_d	MIPI_CAM0_CLKOUT [24]
AH27	GPIO3_A6_d	MIPI_CAM1_CLKOUT [24]
AG29	GPIO3_A7_u	GPIO3_A7/MIPI_CAM2_CLKOUT [24]
AG28	GPIO3_B0_u	GPIO3_B0/MIPI_CAM3_CLKOUT [24]
AH29	GPIO3_B1_d	GPIO3_B1/PWM2/MIPI_CAM4_CLKOUT [24]
AE28	GPIO3_B2_d	I2S2_SDI_M1 [24]
AC28	GPIO3_B3_u	I2S2_SDO_M1 [24]
AC29	GPIO3_B4_u	GPIO3_B4/I2S2_MCLK_M1/MIPI_CAM3_PDN [24]
AD29	GPIO3_B5_u	I2S2_SCLK_M1 [24]
AE29	GPIO3_B6_d	I2S2_LRCK_M1 [24]
AA28	GPIO3_B7_d	
Y29	GPIO3_C0_d	UART7_TX_M1 [24]
Y27	GPIO3_C1_d	UART7_RX_M1 [24]
Y31	GPIO3_C2_d	UART7_RTSN_M1 [24]
Y30	GPIO3_C3_d	UART7_CTSN_M1 [24]
AH26	GPIO3_C4_u	CAN2_RX [24]
AH25	GPIO3_C5_u	CAN2_TX [24]
AG26	GPIO3_C6_u	
AJ24	GPIO3_C7_u	PCIE20X1_2_CLKREQN [24]
AH24	GPIO3_D0_u	PCIE20X1_2_WAKEN [24]
AG23	GPIO3_D1_d	PCIE20X1_2_PERSTN [24]
AG25	GPIO3_D2_d	
AG24	GPIO3_D3_d	
AA27	GPIO3_D4_d	
AB28	GPIO3_D5_d	

VCCIO5_1V8 — W25 — OVCC_1V8_S0

C1903 100nF X5R 6.3V C0201

VCCIO5 — W26 — OVCC_1V8_S0

C1902 100nF X5R 6.3V C0201

RK3588

RK3588_K(VCCIO6 Domain)

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

	/ SPI0_MISO_M1	/ UART9_RTSN_M1 /	/ I2S1_MCLK_M0	/ PCIE30X1_1_CLKREQN_M1	/ BT1120_D0	/ CIF_D0	/ GPIO4_A0_d
	/ SPI0_MOSI_M1	/ UART9_CTSN_M1 /	/ I2S1_SCLK_M0	/ PCIE30X1_1_WAKEN_M1	/ BT1120_D1	/ CIF_D1	/ GPIO4_A1_d
	/ SPI0_CLK_M1	/	/ I2S1_LRCK_M0	/ PCIE30X1_1_PERSTN_M1	/ BT1120_D2	/ CIF_D2	/ GPIO4_A2_d
	/	UART0_TX_M2 /	/	/ PCIE30X1_0_CLKREQN_M1	/ BT1120_D3	/ CIF_D3	/ GPIO4_A3_d
	/ SPI2_MISO_M1	/ UART0_RX_M2	/ I2C3_SCL_M2	/ PCIE30X1_0_WAKEN_M1	/ BT1120_D4	/ CIF_D4	/ GPIO4_A4_d
	/ SPI2_MOSI_M1	/ UART3_TX_M2	/ I2C3_SDA_M2	/ I2S1_SDI0_M0	/ PCIE30X1_0_PERSTN_M1	/ BT1120_D5	/ CIF_D5	/ GPIO4_A5_d
	/ SPI2_CLK_M1	/ UART3_RX_M2	/ I2C5_SCL_M2	/ I2S1_SDI1_M0	/ PCIE30X2_CLKREQN_M1	/ BT1120_D6	/ CIF_D6	/ GPIO4_A6_d
	/ SPI2_CS0_M1	/	/ I2C5_SDA_M2	/ I2S1_SDI2_M0	/ PCIE30X2_WAKEN_M1	/ BT1120_D7	/ CIF_D7	/ GPIO4_A7_d
	/ SPI2_CS1_M1	/ UART8_TX_M0	/ I2C6_SDA_M3	/ I2S1_SDI3_M0	/ PCIE30X2_PERSTN_M1	/ BT1120_CLKOUT	/ CIF_CLKIN	GPIO4_B0_d
SATA2_ACT_LED_M0	/ SPDIF1_TX_M1	/ SPI0_CS1_M1	/ UART8_RX_M0	/ I2C6_SCL_M3	/ I2S1_SDO0_M0	/ PCIE30X1_0_BUTTON_RSTN	/	/ MIPI_CAMERA0_CLK_M0	/ GPIO4_B1_u
CAN1_RX_M1	/ PWM14_M1	/ SPI0_CS0_M1	/ UART8_RTSN_M0	/ I2C7_SCL_M3	/ I2S1_SDO1_M0	/ PCIE30X1_1_BUTTON_RSTN	/ BT1120_D8	/ CIF_HREF	/ GPIO4_B2_u
CAN1_TX_M1	/ PWM15_IR_M1	/	/ UART8_CTSN_M0	/ I2C7_SDA_M3	/ I2S1_SDO2_M0	/ PCIE20X1_2_BUTTON_RSTN	/ BT1120_D9	/ CIF_VSYNC	/ GPIO4_B3_u
SPDIF0_TX_M1	/ PWM11_IR_M1	/ DP0_HPDIN_M0	/ UART9_TX_M1	/	/ I2S1_SDO3_M0	/ PCIE30X4_CLKREQN_M1	/ BT1120_D10	/ CIF_CLKOUT	/ GPIO4_B4_u
SATA1_ACT_LED_M0	/ PWM12_M1	/ SPI3_MISO_M1	/ UART9_RX_M1	/	/HDMI_RX_CEC_M0	/ PCIE30X4_WAKEN_M1	/ BT1120_D11	/	/ GPIO4_B5_d
SATA0_ACT_LED_M0	/ PWM13_M1	/ SPI3_MOSI_M1	/	/ I2C5_SCL_M1	/HDMI_RX_HPDOUT_M0	/ PCIE30X4_PERSTN_M1	/ BT1120_D12	/	/ GPIO4_B6_d
	/	/ SPI3_CLK_M1	/	/ I2C5_SDA_M1	/HDMI_TX0_SCL_M0	/ PCIE20X1_2_CLKREQN_M1	/ BT1120_D13	/	/ GPIO4_B7_u
		/ SPI3_CS0_M1	/	/ I2C8_SCL_M3	/HDMI_TX0_SDA_M0	/ PCIE20X1_2_WAKEN_M1	/ BT1120_D14	/	/ GPIO4_C0_u
SPDIF1_TX_M2	/ PWM6_M1	/ SPI3_CS1_M1	/	/ I2C8_SDA_M3	/HDMI_TX0_CEC_M0	/ PCIE20X1_2_PERSTN_M1	/ BT1120_D15	/	/ GPIO4_C1_d

AK30	GPIO4_A0_d	GPIO4_A0/I2S1_MCLK_M0/PCIE30X1_1_CLKREQN_M1 [24]
AL30	GPIO4_A1_d	I2S1_SCLK_M0/PCIE30X1_1_WAKEN_M1 [24]
AM29	GPIO4_A2_d	I2S1_LRCK_M0/PCIE30X1_1_PERSTN_M1 [24]
AL29	GPIO4_A3_d	GPIO4_A3/PCIE30X1_0_CLKREQN_M1 [24]
AL28	GPIO4_A4_d	GPIO4_A4/PCIE30X1_0_WAKEN_M1 [24]
AK27	GPIO4_A5_d	I2S1_SDI0_M0/PCIE30X1_0_PERSTN_M1 [24]
AL27	GPIO4_A6_d	MIPI_CAM1_PDN/PCIE30X2_CLKREQN_M1 [24]
AM27	GPIO4_A7_d	GPIO4_A7/PCIE30X2_WAKEN_M1 [24]
AK26	GPIO4_B0_d	GPIO4_B0/PCIE30X2_PERSTN_M1 [24]
AL24	GPIO4_B1_u	I2S1_SDO0_M0 [24]
AK25	GPIO4_B2_u	
AM25	GPIO4_B3_u	
AL26	GPIO4_B4_u	
AJ26	GPIO4_B5_d	
AJ27	GPIO4_B6_d	
AJ28	GPIO4_B7_u	HDMI_TX0_SCL [24]
AJ25	GPIO4_C0_u	HDMI_TX0_SDA [24]
AK24	GPIO4_C1_d	HDMI_TX0_CEC [24]

VCCIO6_1V8 — AC25 — OVCC_1V8_S0

C1909 100nF X5R 6.3V C0201

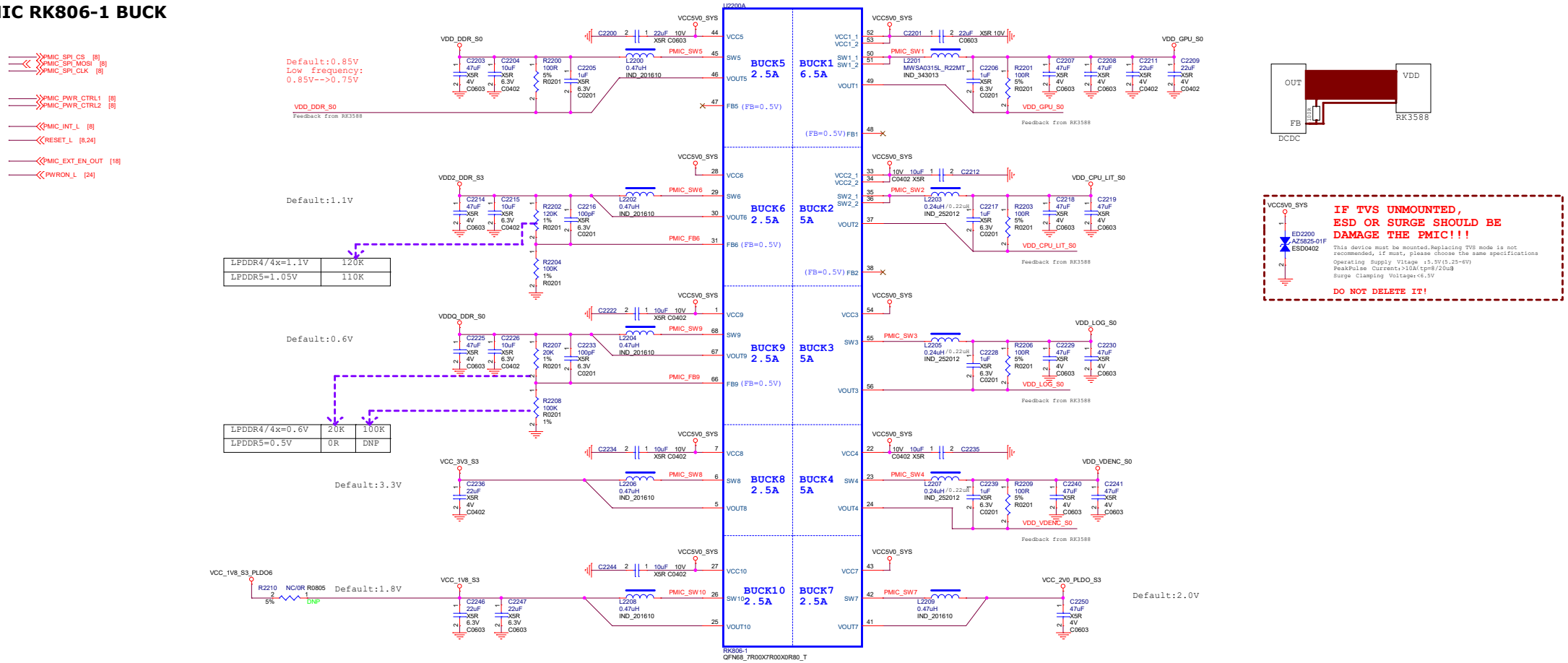
VCCIO6 — AC26 — OVCC_1V8_S0

C1908 100nF X5R 6.3V C0201

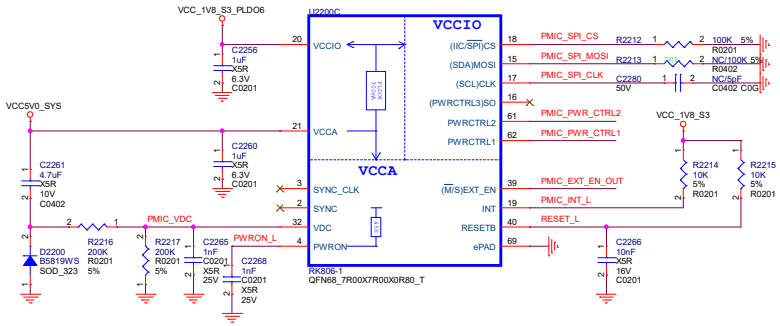
RK3588

armsom	ArmSoM		
Project:	ArmSoM-AIM7		
File:	RK3588_1.8V/ 3.3V GPIO		
Date:	Tuesday, October 08, 2024	Rev:	V1.2
Designed by:	Park	Reviewed by: <Checker>	Sheet: 16 of 24

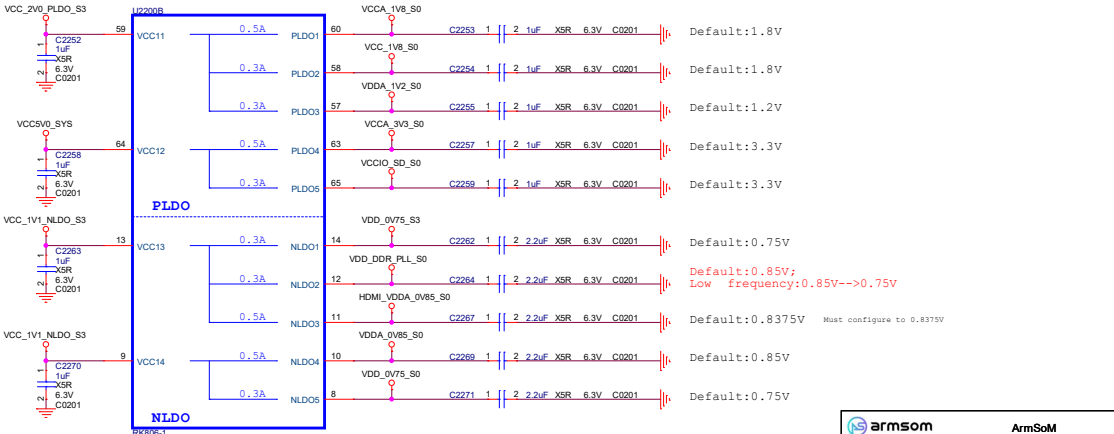
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment

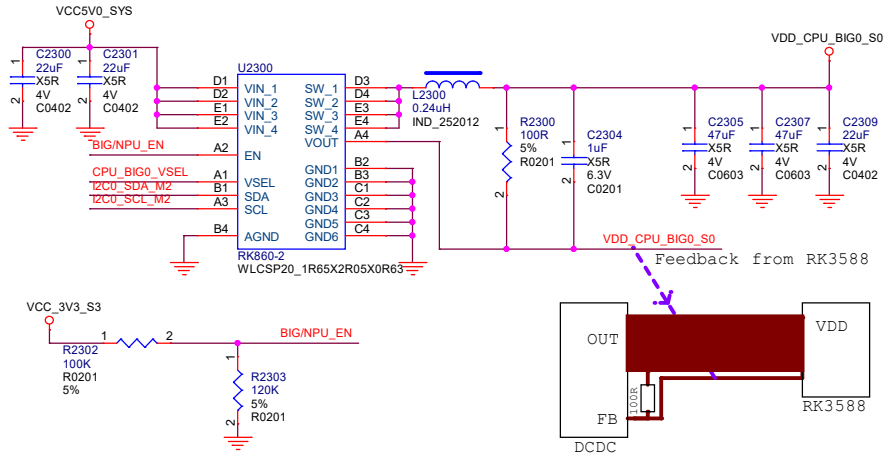


PMIC RK806-1 LDO

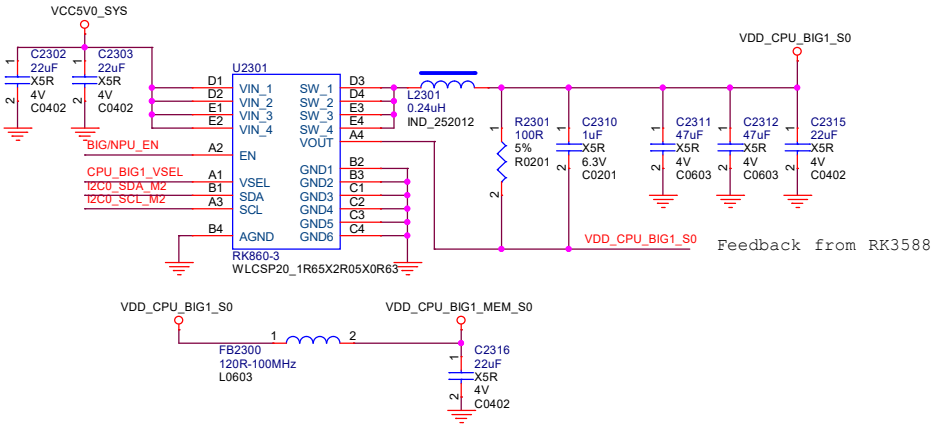


armsom	ArmSoM			
Project:	ArmSoM-AIM7			
File:	Power-PMIC_RK806-1			
Date:	Tuesday, October 08, 2024	Rev:	V1.2	
Designed by:	Park	Reviewed by:	<Checker>	Sheet: 17 of 24

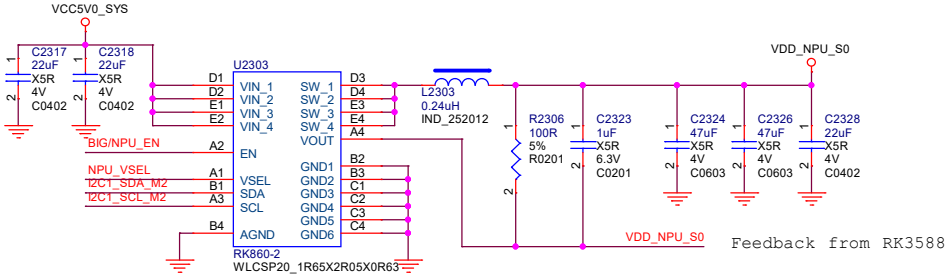
VDD_CPU_BIG0



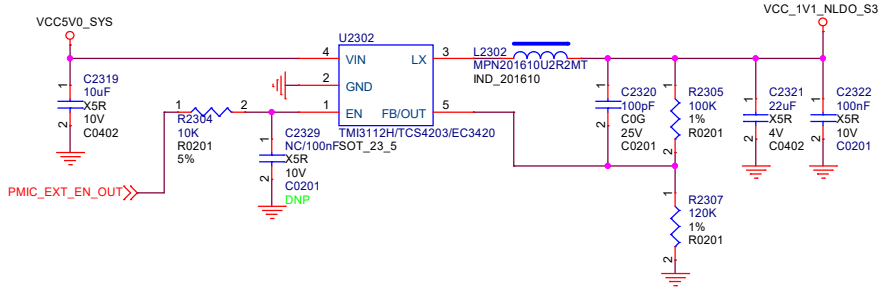
VDD_CPU_BIG1

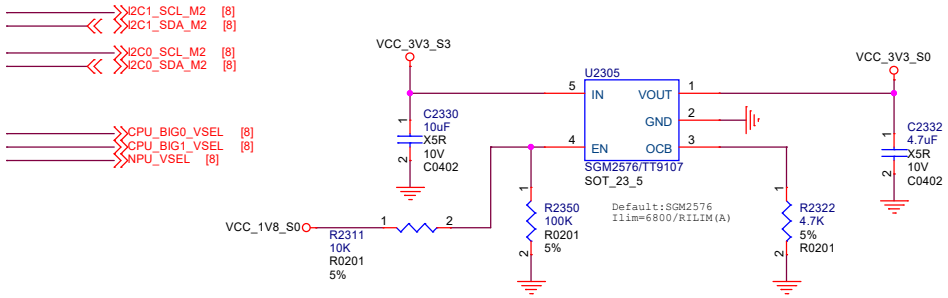


VDD_NPU

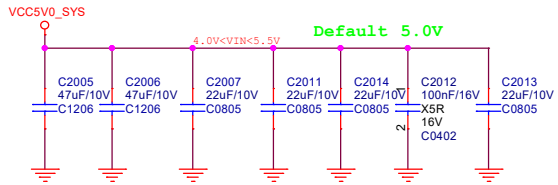


VCC_1V1_NLDO_S3





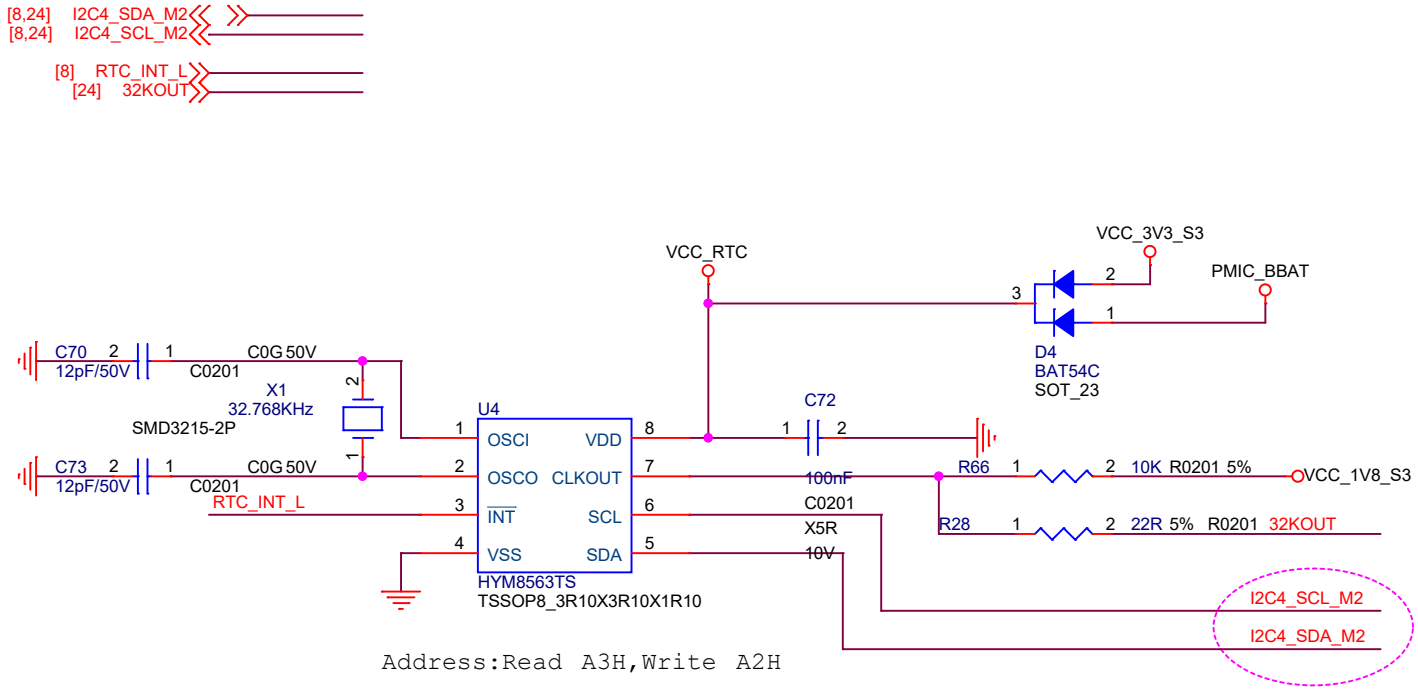
VCC5V0_SYS



armsom ArmSoM

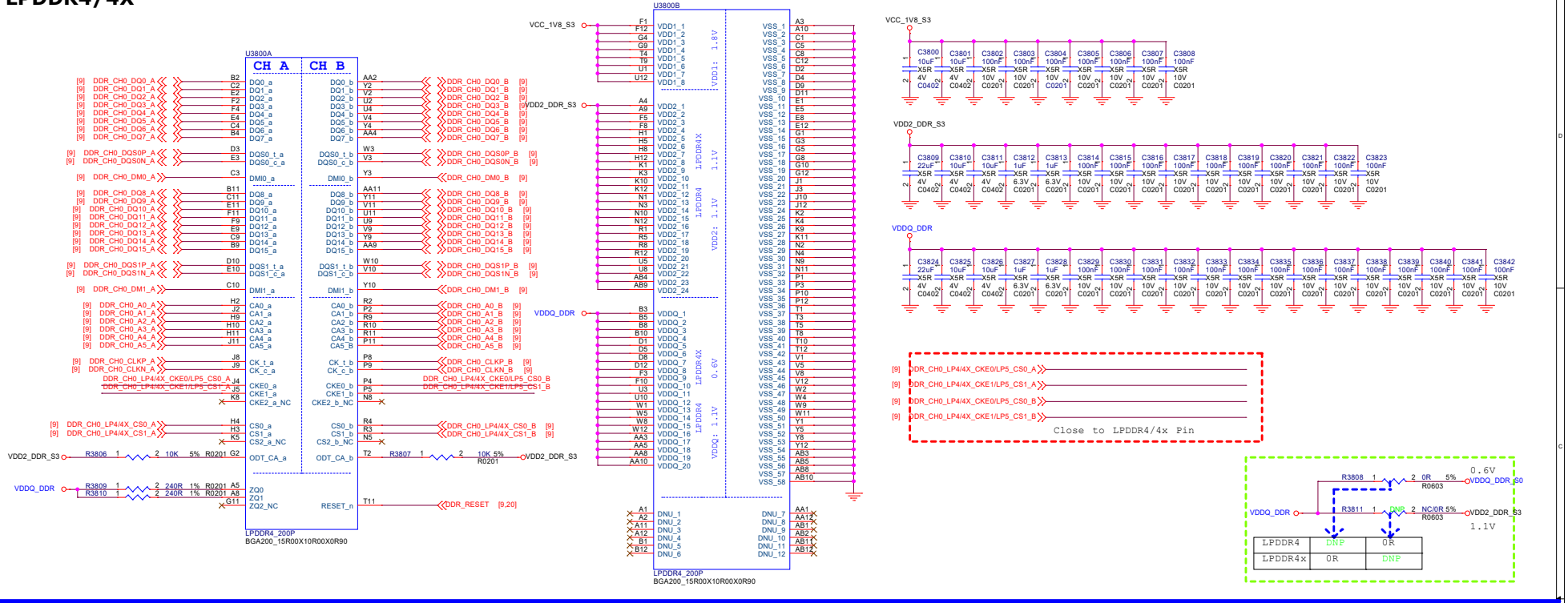
Project:	ArmSoM-AIM7				
File:	Power_Ext Discrete				
Date:	Tuesday, October 08, 2024			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	18 of 24

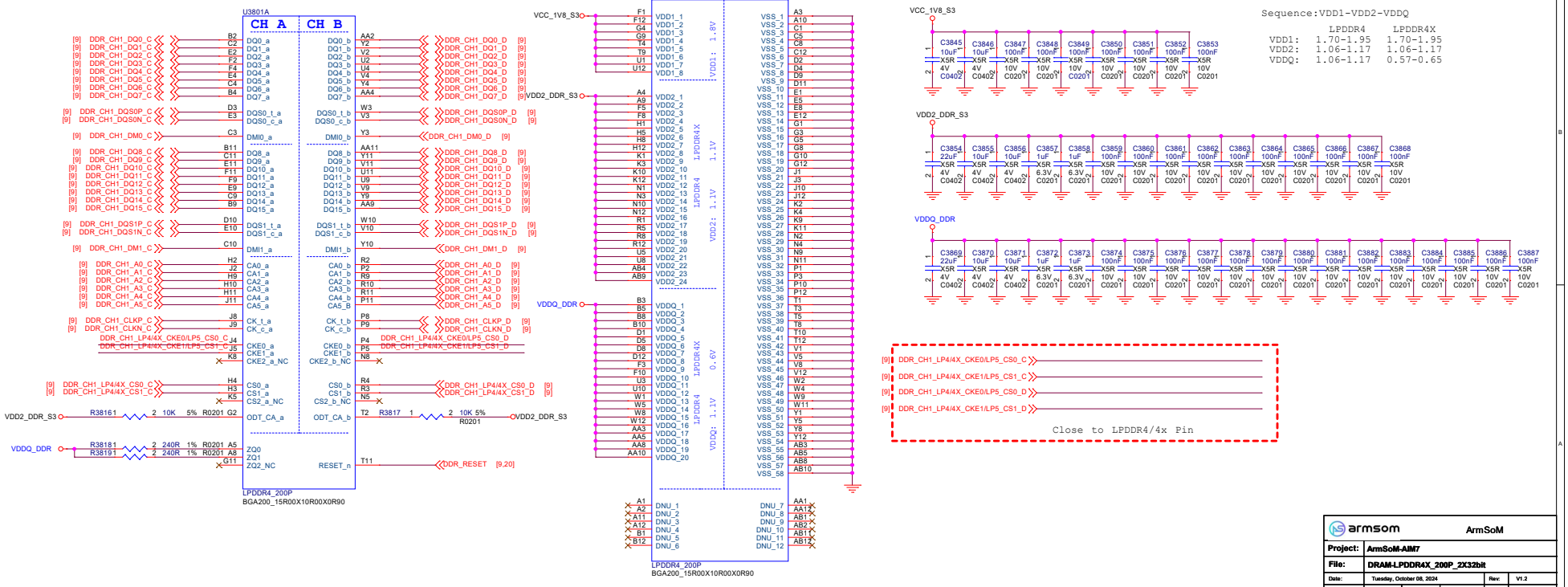
RTC IC



armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	RTC				
Date:	Tuesday, October 08, 2024			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	19 of 24

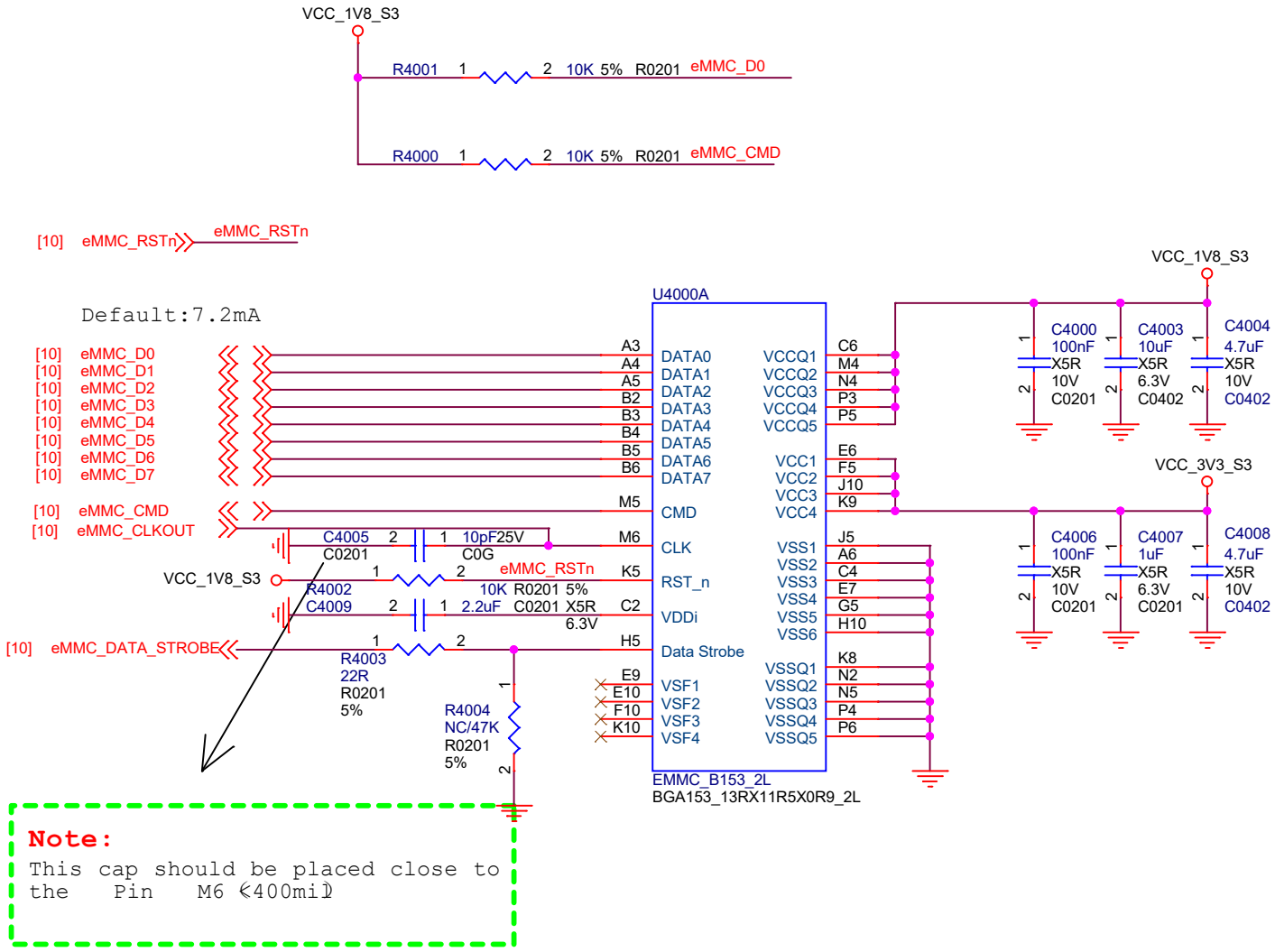
LPDDR4/4X

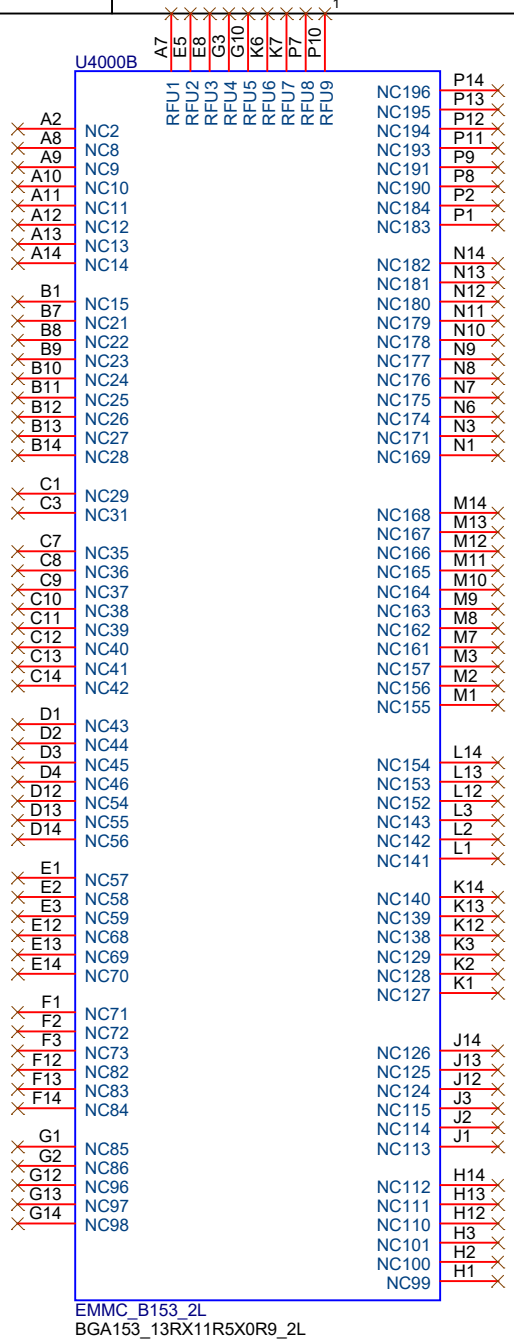




armsom	ArmSoM		
Project:	ArmSoM-AIM7		
File:	DRAM-LPDDR4X_200P_2X32bit		
Date:	Tuesday, October 08, 2024	Rev:	V1.2
Designed by: Park	Reviewed by: <Checker>	Sheet:	20 of 24

eMMC FLASH





armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	Flash-eMMC Flash				
Date:	Tuesday, October 08, 2024			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	21 of 24

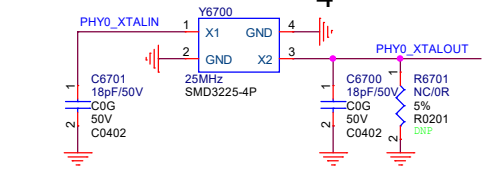
RGMII TO RJ45

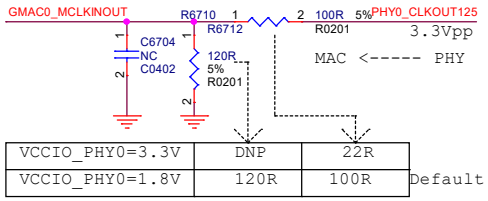
GMAC0_TXD0 [12]
GMAC0_TXD1 [12]
GMAC0_TXD2 [12]
GMAC0_TXD3 [12]
GMAC0_TXEN [12]
GMAC0_TXCLK [12]

GMAC0_RXD0 [12]
GMAC0_RXD1 [12]
GMAC0_RXD2 [12]
GMAC0_RXD3 [12]
GMAC0_RXDV_CRS [12]

GMAC0_RXCLK [12]
ETH0_REFCLKO_25M [12]
GMAC0_MCLKINOUT [12]
GMAC0_MDC [12]
GMAC0_MDIO [12]

GMAC0_RSTn_L [8]

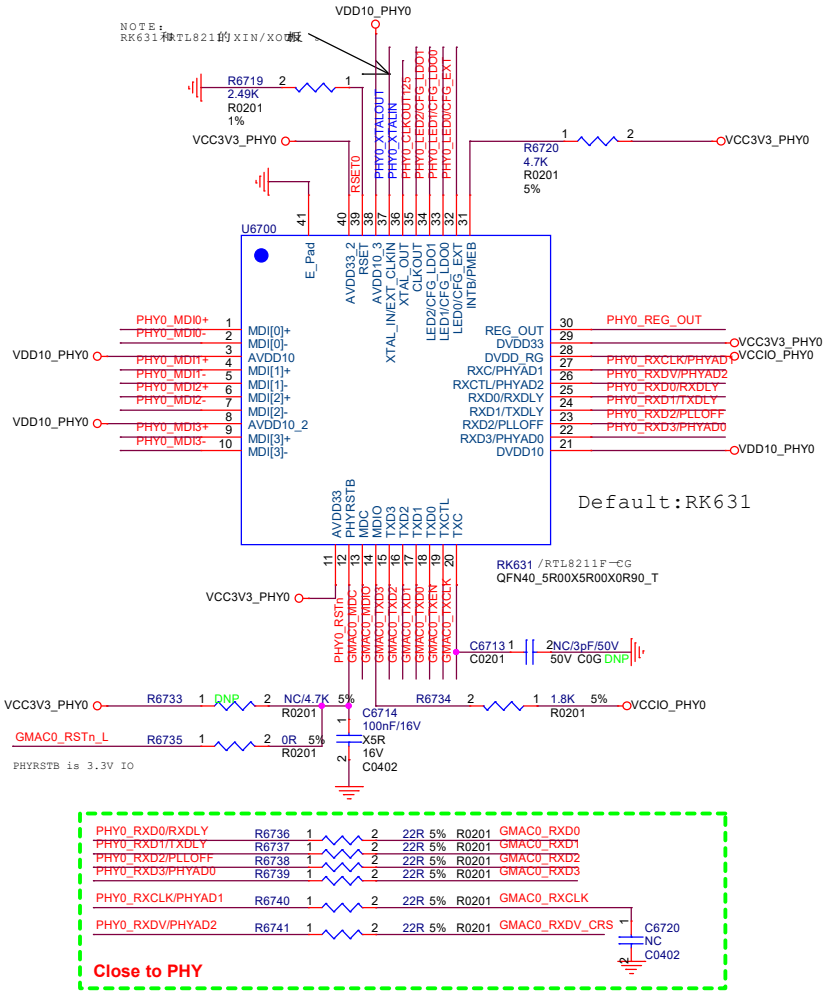




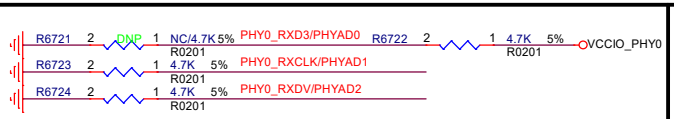
VCCIO_PHY0=3.3V	DNP	22R
VCCIO_PHY0=1.8V	120R	100R

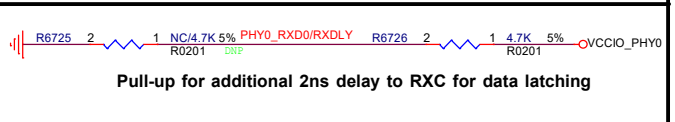
Default

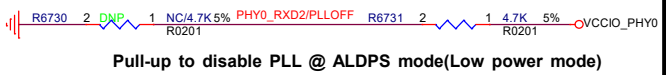
PHY0_MDI0- [24]
PHY0_MDI0+ [24]
PHY0_LED0/CFG_EXT [24]
PHY0_MDI1- [24]
PHY0_MDI1+ [24]
PHY0_LED2/CFG_LDO1 [24]
PHY0_MDI2- [24]
PHY0_MDI2+ [24]
PHY0_MDI3- [24]
PHY0_MDI3+ [24]

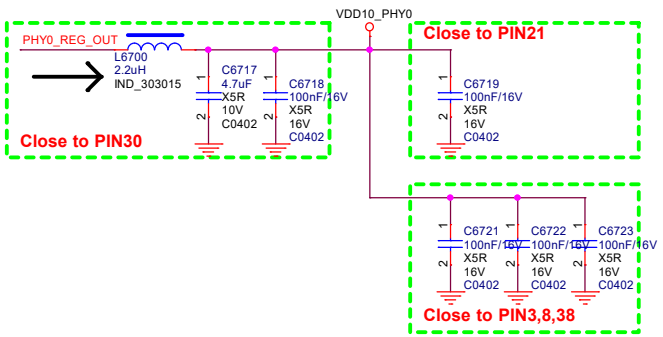


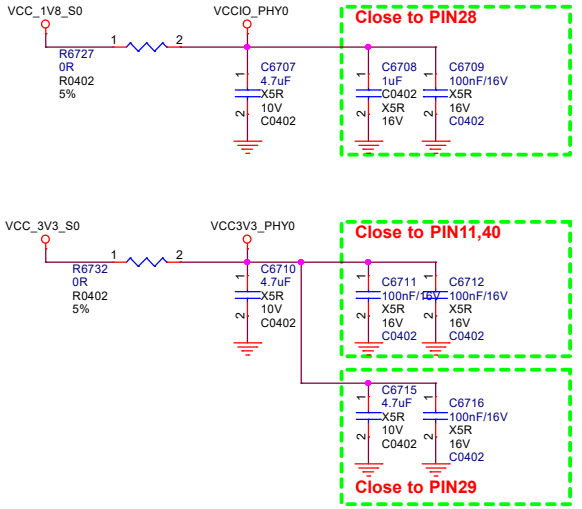
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V(default)	1'b1	2'b00	CFG_EXT: 1:External Power Source for IO pad. 0:Integrated LDO for IO pad CFG_LDO(1:0) 10:1.8V 00:3.3V
External 1.8V	1'b1	2'b10	
Internal 1.8V	1'b0	2'b10	











armsom	ArmSoM
Project:	ArmSoM-AIM7
File:	Ethernet-GPHY_RGMII1
Date:	Tuesday, October 08, 2024
Rev:	V1.2
Designed by:	Park
Reviewed by:	<Checker>
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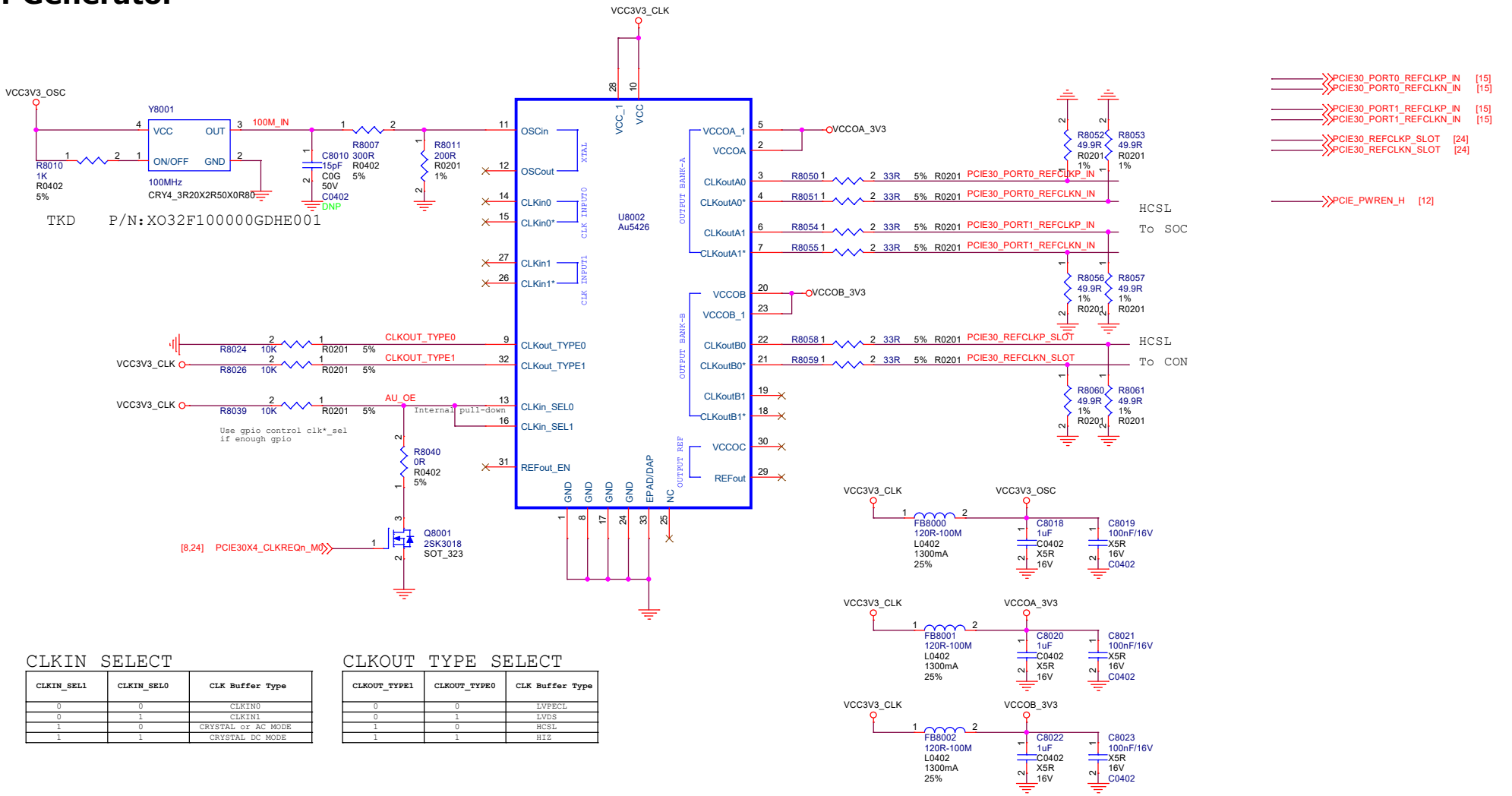
Crystal Generator



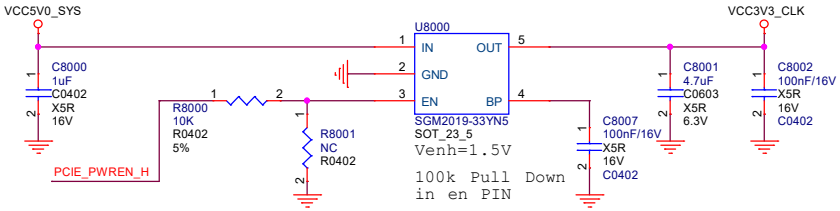
CLKIN SELECT

CLKIN_SEL1	CLKIN_SEL0	CLK Buffer Type
0	0	CLKIN0
0	1	CLKIN1
1	0	CRYSTAL or AC MODE
1	1	CRYSTAL DC MODE

CLKOUT TYPE SELECT

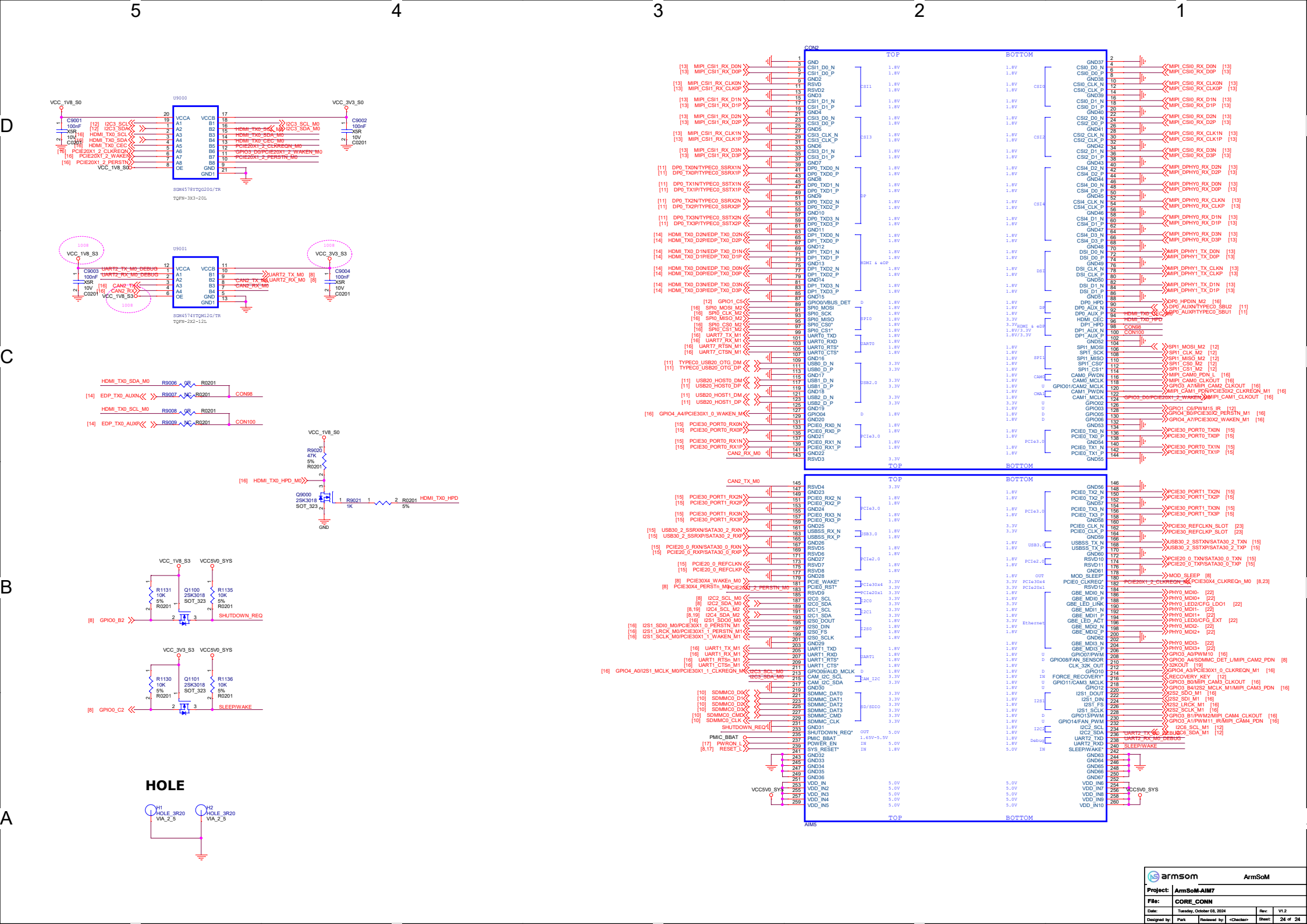
CLKOUT_TYPE1	CLKOUT_TYPE0	CLK Buffer Type
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	HIZ

PCIe3.0 POWER



Note:
Please select one option

armsom	ArmSoM			
Project:	ArmSoM-AIM7			
File:	PCIE-PCIE3.0 CLK GENERATOR			
Date:	Tuesday, October 08, 2024		Rev:	V1.2
Designed by:	Park	Reviewed by: <Checker>	Sheet:	23 of 24


5
4
3
2
1
D
C
B
A
U9000
SGM4578YTQG20G/TR
TQFN-3X3-20L
U9001
SGM4574YTQM12G/TR
TQFN-2X2-12L
VCC_1V8_S0
VCC_3V3_S0
VCC_1V8_S3
VCC_3V3_S3
VCC5V0_SYS
CON2
AIM5
TOP
BOTTOM
HOLE
H1
H2
HOLE_3R20
VIA_2_5
armsom
ArmSoM
Project: ArmSoM-AIM7
File: CORE_CONN
Date: Tuesday, October 08, 2024
Rev: V1.2
Designed by: Park
Reviewed by: <Checker>
Sheet: 24 of 24