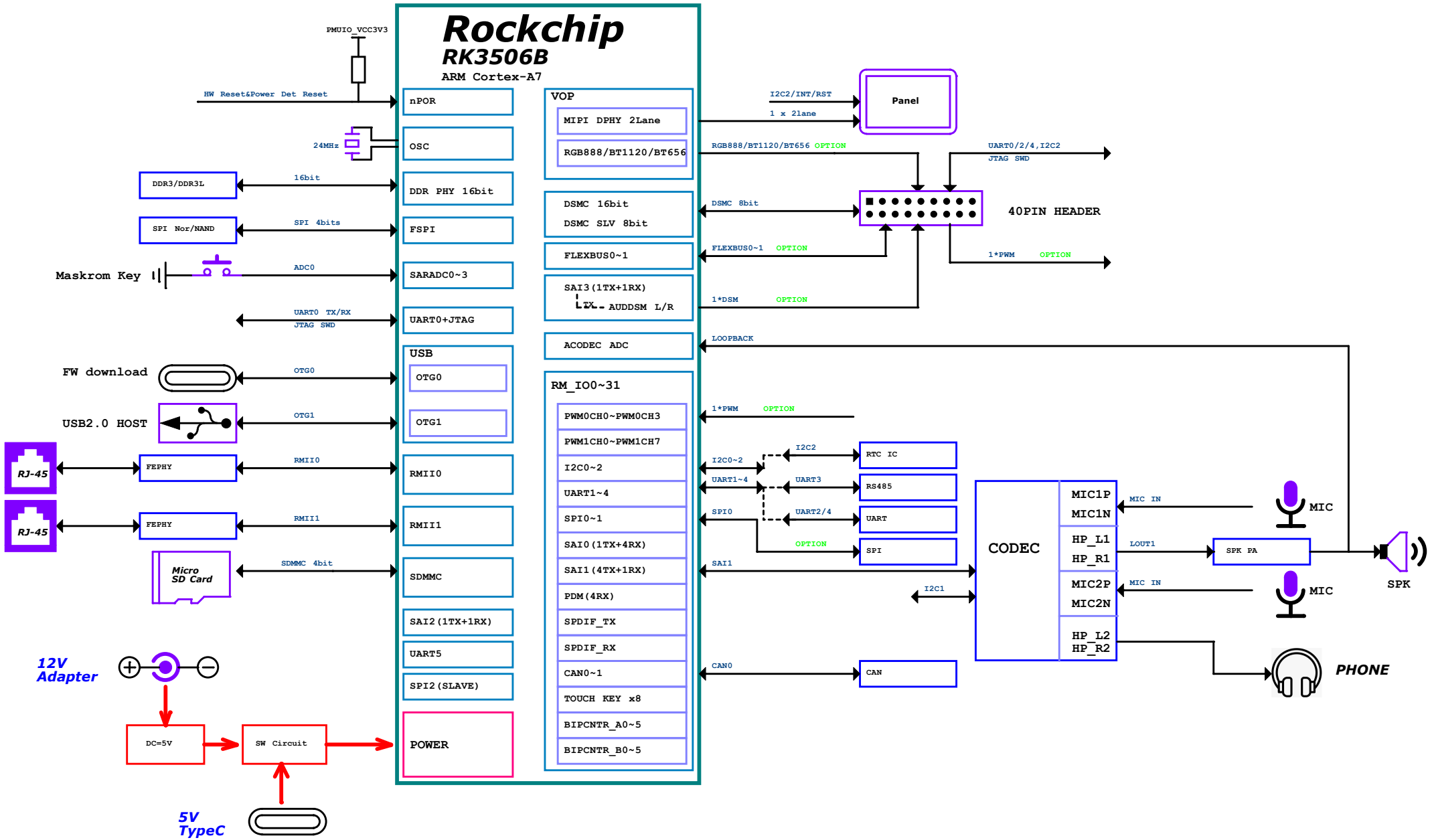
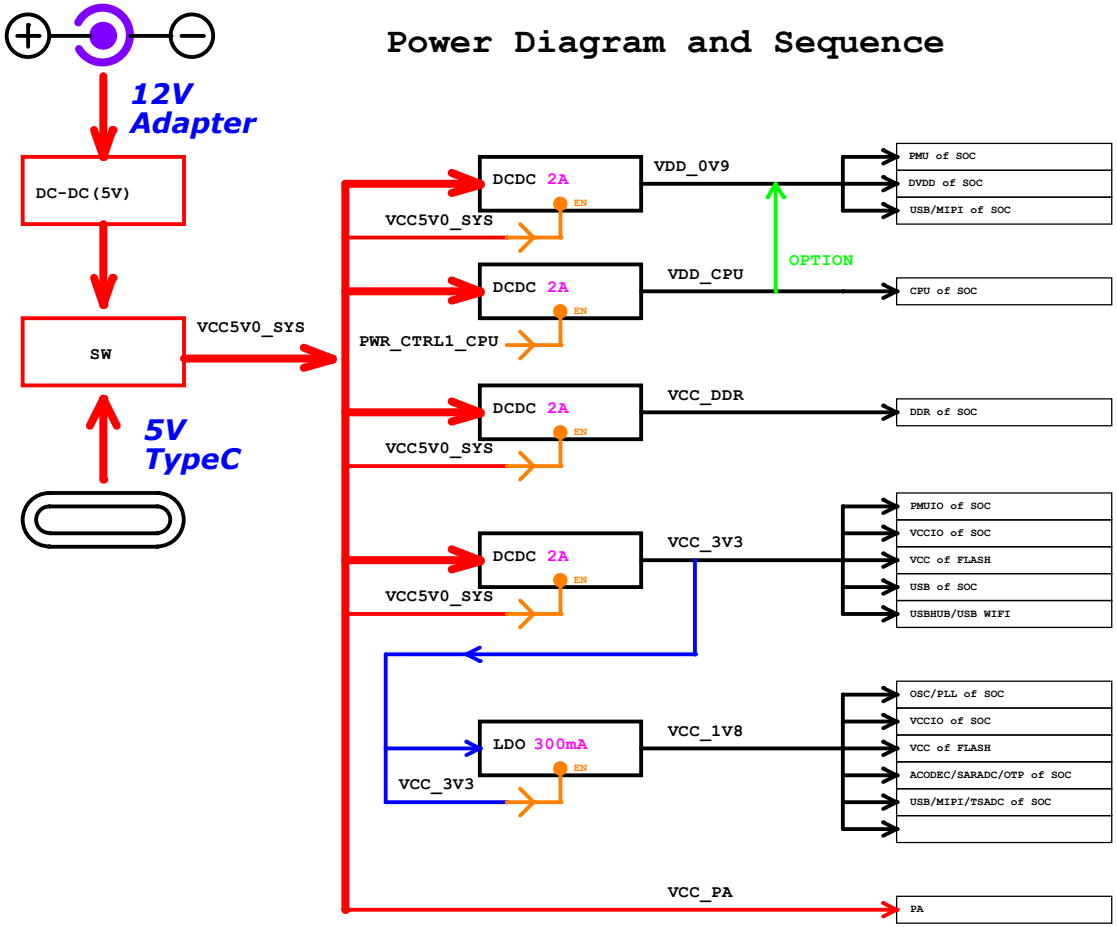
ArmSoM-FORGE1 Block Diagram

Rockchip IC | Other IC



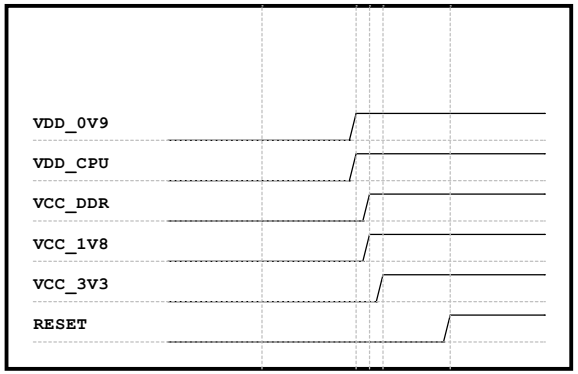
armsom	https://armsom.org/
Project:	ArmSoM-FORGE1
File:	Block Diagram
Date:	Tuesday, March 25, 2025
Rev:	V1.0
Designed by:	Park
Reviewed by:	<Checker>
Sheet:	1 of 21

Power Diagram and Sequence



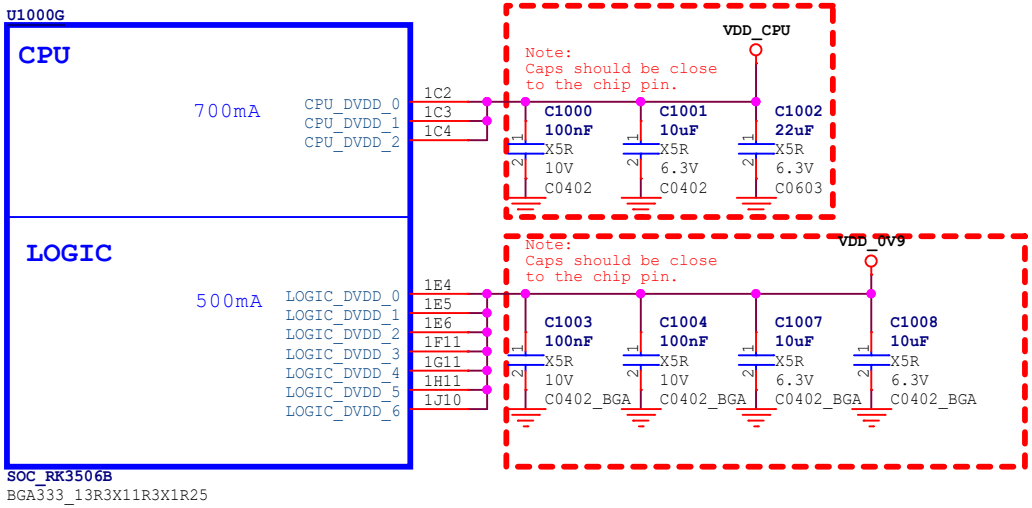
Power-on Sequence

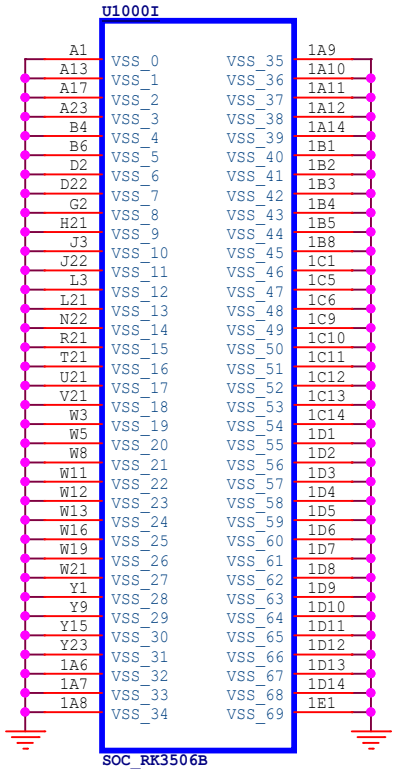
Power Name	PMIC Channel	Time Slot	Default voltage	Peak Current
VDD_0V9	DC-DC BUCK	Slot: 1	0.9V	
VDD_CPU	DC-DC BUCK	Slot: 1	0.95V	
VCC_DDR	DC-DC BUCK	Slot: 2	1.35V	
VCC_1V8	LDO	Slot: 2a	1.8V	
VCC_3V3	DC-DC BUCK	Slot: 3	3.3V	
RESET				
	Finally , nPOR RESET 10ms after PMUIO VCC3V3 is ready			

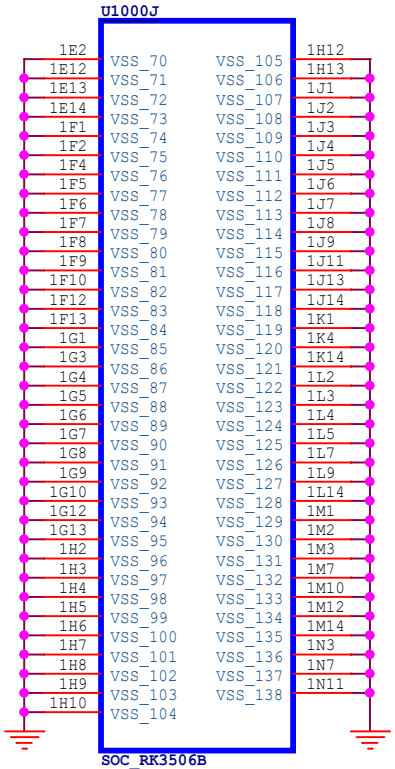


armsom https://armsom.org/

Project:	ArmSoM-FORGE1				
File:	Power Diagram				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	2 of 21







armsom https://armsom.org/					
Project:	ArmSoM-FORGE1				
File:	SOC-POWER/GND				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	3 of 21

U1000A

OSC/PLL

Operating Voltage=1.8V Only

OSC_XOUT
OSC_XIN
REF_CLK0_OUT/OSC_CLK_OUT/GPIO0_D0_d
RFU
20mA SYS_PLL_AVDD1V8

H2 OSC_XOUT
H3 OSC_XIN
R1101 22R R0201
R1100 1M R0201
Y1100 24MHz CRY4_3R20X2R50X0R80
C1100 18pF C0G 50V C0201
C1101 18pF C0G 50V C0201
G1 WIFI_WAKE_HOST_H PHONE_DET_L_1V8 [17]
1G2 VCC_1V8
1H1
C1102 100nF X5R 10V C0402

PMUIO Domain

Operating Voltage=3.3V Only

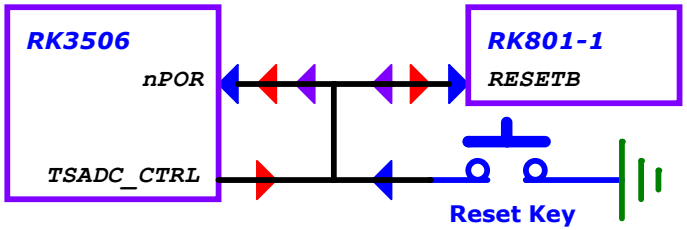
NPOR
RM_IO0/SAI0_LRCK/GPIO0_A0_u
RM_IO1/SAI0_SCLK/GPIO0_A1_d
RM_IO2/SAI0_MCLK/GPIO0_A2_u
RM_IO3/SAI0_SDO/GPIO0_A3_d
RM_IO4/SAI0_SDI0/GPIO0_A4_d
RM_IO5/SAI0_SDI1/GPIO0_A5_d
RM_IO6/SAI0_SDI2/GPIO0_A6_d
RM_IO7/SPI1_CSN1/SAI0_SDI3/GPIO0_A7_d
RM_IO8/SPI1_CLK/SAI1_MCLK/GPIO0_B0_d
RM_IO9/SPI1_MOSI/SAI1_SCLK/GPIO0_B1_d
RM_IO10/SPI1_MISO/SAI1_LRCK/GPIO0_B2_d
RM_IO11/SAI1_SDI/GPIO0_B3_d
RM_IO12/SAI1_SDO0/GPIO0_B4_d
RM_IO13/SAI1_SDO1/GPIO0_B5_d
RM_IO14/SPI1_CSN0/SAI1_SDO2/GPIO0_B6_d
RM_IO15/SPI0_CSN1/SAI1_SDO3/GPIO0_B7_d
RM_IO16/SPI0_CLK/GPIO0_C0_d
RM_IO17/SPI0_MOS/GPIO0_C1_d
RM_IO18/SPI0_MISO/REF_CLK1_OUT/GPIO0_C2_d
RM_IO19/SPI0_CSN0/ETH_CLK1_25M_OUT/GPIO0_C3_d
RM_IO20/AUPLL_CLK_IN/ETH_CLK0_25M_OUT/GPIO0_C4_d
RM_IO21/CPU_AVS/GPIO0_C5_z
RM_IO22/JTAG_TCK_M1/UART0_TX/GPIO0_C6_u
RM_IO23/JTAG_TMS_M1/UART0_RX/GPIO0_C7_u
200mA PMU_LOGIC_DVDD0V9
PMUIO_VCC3V3

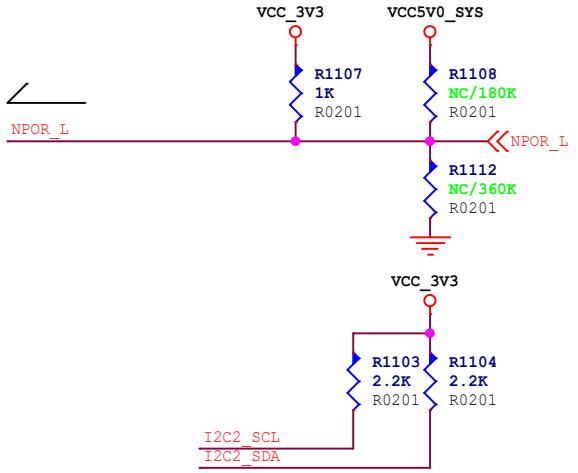
T3 NPOR_L C1103 C0402 10nF C0G 25V
V3 UART2_RX/PWM0_CH3_IR_RX [20]
W1 LCD_PWREN_H [13]
W2 UART2_TX [20]
V2 PWM0_CH2_LCD_BL SDMMC_DET_L [12]
U2 I2C2_SCL [13,14,20]
U1 I2C2_SDA [13,14,20]
U3 TP_INT_L [13]
T2 TP_RST_L [13]
R2 SAI1_MCLK [17]
R1 SAI1_SCLK [17]
R3 SAI1_LRCK [17]
P2 SAI1_SDI [17]
P3 SAI1_SDO0 [17]
N1 RTC_INT [14]
N3 UART3_TX [20]
N2 UART3_RX [20]
M2 I2C1_SCL [17]
M3 I2C1_SDA [17]
L1 RMII0_RSTn [15]
L2 CAN0_TX [20]
K2 CAN0_RX [20]
K3 PWM0_CH0_CPU [18]
J2 UART0_TX/JTAG_TCK_M1 [20]
J1 UART0_RX/JTAG_TMS_M1 [20]
VDD_0V9
VCC_3V3
1K2
1L1
C1104 100nF X5R 10V C0402
C1105 100nF X5R 10V C0402

SOC_RK3506B
BGA333_13R3X11R3X1R25

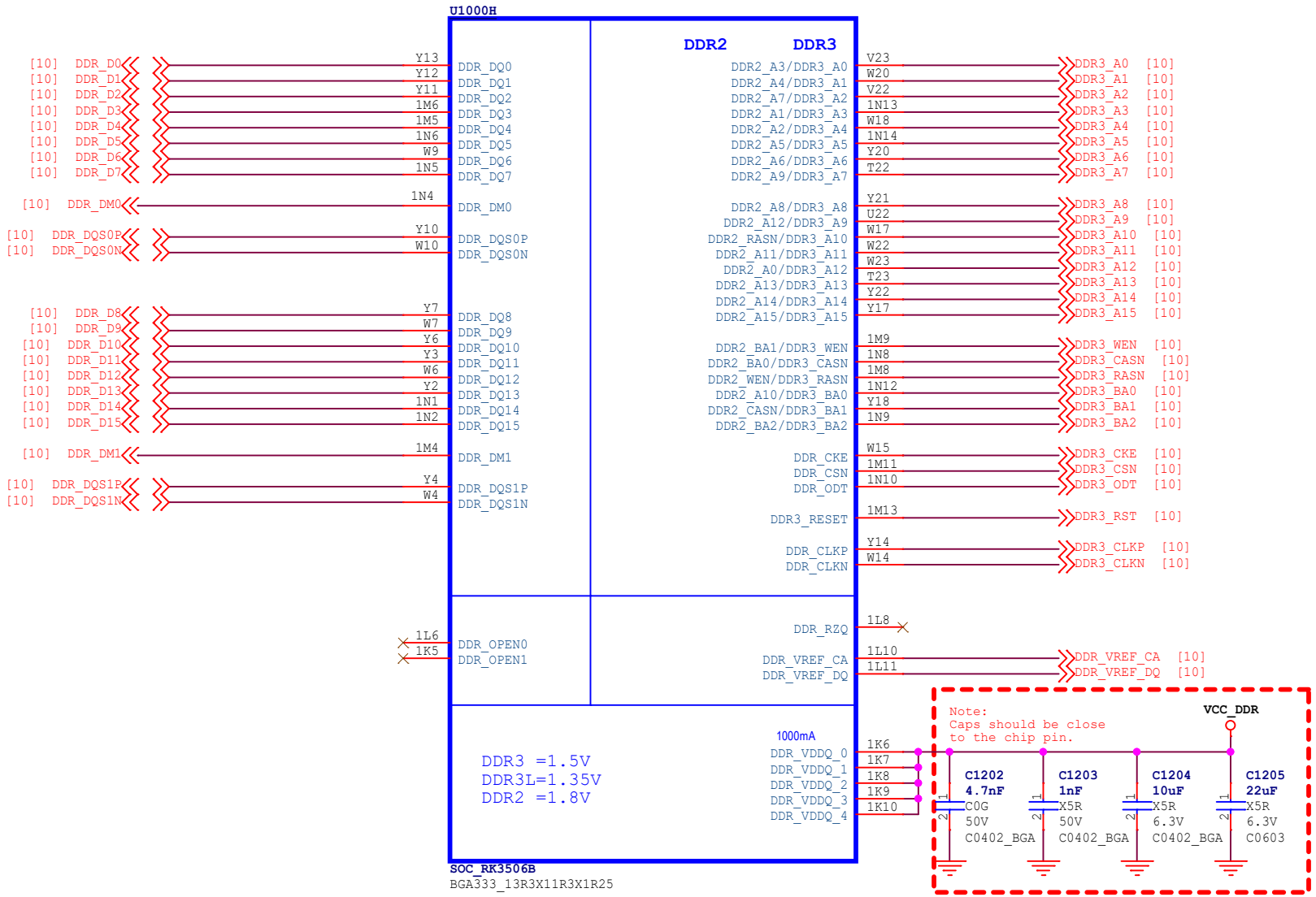
Note:

- Reset Key Control Path
- TSADC_SHUT Control Path
- PMIC Control Path



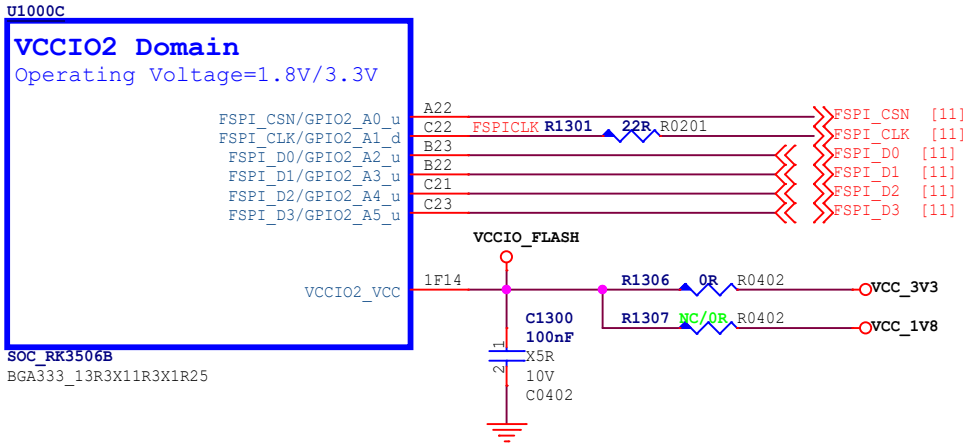


armsom	https://armsom.org/				
Project:	ArmSoM-FORGE1				
File:	SOC-OSC/PLL/PMUIO				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	4 of 21



armsom https://armsom.org/

Project:	ArmSoM-FORGE1				
File:	SOC-DRAM Controller				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	5 of 21



armsom https://armsom.org/					
Project:	ArmSoM-FORGE1				
File:	SOC-Flash Controller				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	6 of 21

U1000F

MIPI
Operating Voltage=1.8V
GPO is output only

MIPI_DPHY_DSI_TX_D0N/GPO4_A0_z
MIPI_DPHY_DSI_TX_D0P/GPO4_A1_z
MIPI_DPHY_DSI_TX_D1N/GPO4_A2_z
MIPI_DPHY_DSI_TX_D1P/GPO4_A3_z
MIPI_DPHY_DSI_TX_CLKN/GPO4_A4_z
MIPI_DPHY_DSI_TX_CLKP/GPO4_A5_z

20mA MIPI_DPHY_AVDD0V9
50mA MIPI_DPHY_AVDD1V8

USB2.0 OTG0
HS/FS/LS
(Download Port)

USB20_OTG0_DP
USB20_OTG0_DM
USB20_OTG0_ID
USB20_OTG0_VBUSDET

USB2.0 OTG1
HS/FS/LS

USB20_OTG1_DP
USB20_OTG1_DM

USB2.0 PHY Power
for OTG0/1

5mA USB20_OTG_AVDD0V9
30mA USB20_OTG_AVDD1V8
10mA USB20_OTG_AVDD3V3

SARADC
Operating Voltage=1.8V

SARADC_IN0/GPIO4_B0_z
SARADC_IN1/GPIO4_B1_z
SARADC_IN2/GPIO4_B2_z
SARADC_IN3/GPIO4_B3_z

60mA OTP_AVDD1V8/SARADC_AVDD1V8

TSADC

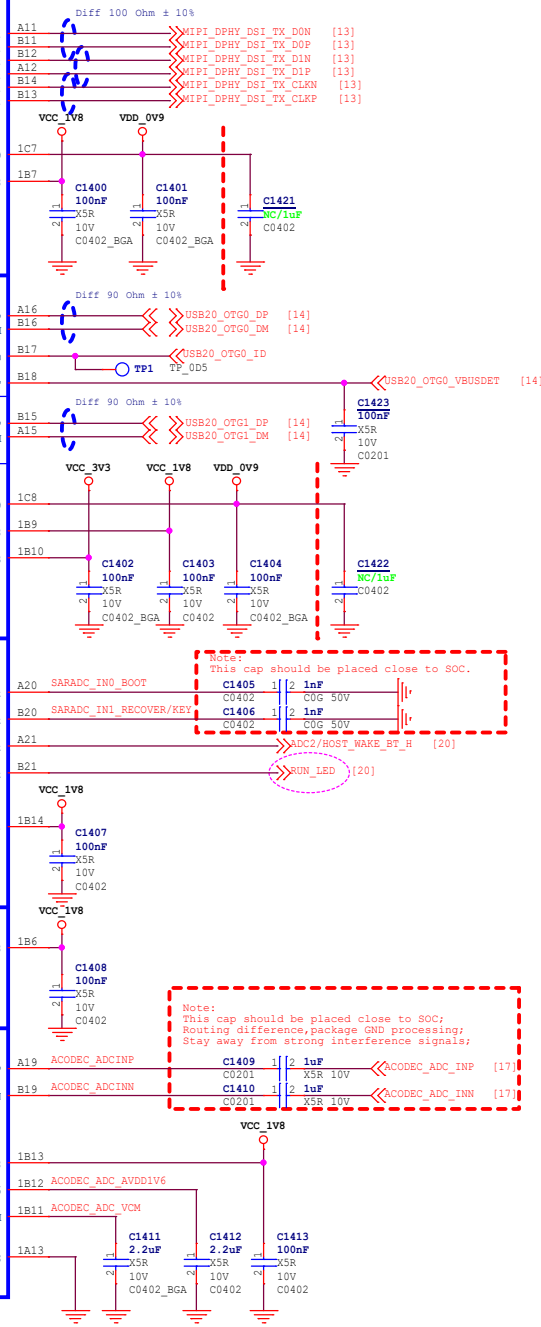
1.5mA TSADC_VCC1V8

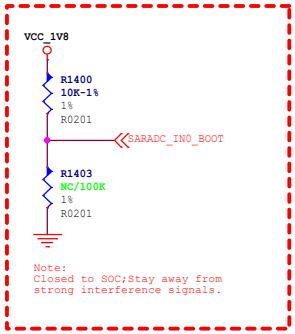
ACODEC

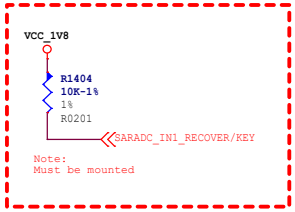
ACODEC_ADC_INP
ACODEC_ADC_INN

10mA ACODEC_ADC_AVDD1V8
ACODEC_ADC_AVDD1V6
ACODEC_ADC_VCM
ACODEC_ADC_AVSS

SOC_RK3506B
BGA333_13R3X11R3X1R25

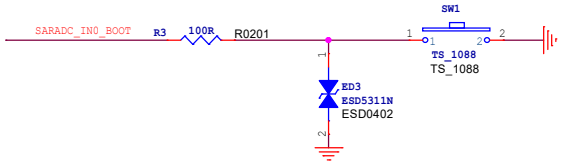






SARADC_IN0_BOOT TABLE

Item	Rup	Rdown	ADC	BOOT MODE
LEVEL1	DNP	100K	0	USB (Maskrom mode)/SPI2APB
LEVEL2	100K	12K	110	SPI2APB
LEVEL3	100K	27K	217	FSPI--USB/SPI2APB
LEVEL4	100K	51K	345	
LEVEL5	100K	82K	461	
LEVEL6	100K	120K	558	SDMMC(eMMC/SD Card)--USB/SPI2APB
LEVEL7	100K	200K	682	
LEVEL8	100K	330K	785	
LEVEL9	100K	820K	912	
LEVEL10	10K	DNP	1023	FSPI--SDMMC(eMMC/SD Card)--USB/SPI2APB



armsom https://armsom.org/

Project:	ArmSoM-FORGE1				
File:	SOC-USB/ACODEC/SARADC/MIPI				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	7 of 21

Mode	RGB					BT1120	BT656	MCU				
	24bit	18bit	16bit	8bit	6bit	16bit	8bit	24bit	18bit	16bit	8bit	6bit
LCDC_DEN	DEN	DEN	DEN	DEN	DEN	--	--	RDN	RDN	RDN	RDN	RDN
LCDC_VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	--	--	CSN	CSN	CSN	CSN	CSN
LCDC_HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	--	--	WRN	WRN	WRN	WRN	WRN
LCDC_CLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK	RS	RS	RS	RS	RS
LCDC_D23	D23	D17	D15	D7_m1	D5_m1	D15	D7_m1	D23	D17	D15	D7_m1	D5_m1
LCDC_D22	D22	D16	D14	D6_m1	D4_m1	D14	D6_m1	D22	D16	D14	D6_m1	D4_m1
LCDC_D21	D21	D15	D13	D5_m1	D3_m1	D13	D5_m1	D21	D15	D13	D5_m1	D3_m1
LCDC_D20	D20	D14	D12	D4_m1	D2_m1	D12	D4_m1	D20	D14	D12	D4_m1	D2_m1
LCDC_D19	D19	D13	D11	D3_m1	D1_m1	D11	D3_m1	D19	D13	D11	D3_m1	D1_m1
LCDC_D18	D18	D12	--	--	--	--	--	D18	D12	--	--	--
LCDC_D17	D17	--	--	--	--	--	--	D17	--	--	--	--
LCDC_D16	D16	--	--	--	--	--	--	D16	--	--	--	--
LCDC_D15	D15	D11	D10	D2_m1	D0_m1	D10	D2_m1	D15	D11	D10	D2_m1	D0_m1
LCDC_D14	D14	D10	D9	D1_m1	--	D9	D1_m1	D14	D10	D9	D1_m1	--
LCDC_D13	D13	D9	D8	D0_m1	--	D8	D0_m1	D13	D9	D8	D0_m1	--
LCDC_D12	D12	D8	D7	D7_m0	D5_m0	D7	D7_m0	D12	D8	D7	D7_m0	D5_m0
LCDC_D11	D11	D7	D6	D6_m0	D4_m0	D6	D6_m0	D11	D7	D6	D6_m0	D4_m0
LCDC_D10	D10	D6	D5	D5_m0	D3_m0	D5	D5_m0	D10	D6	D5	D5_m0	D3_m0
LCDC_D9	D9	--	--	--	--	--	--	D9	--	--	--	--
LCDC_D8	D8	--	--	--	--	--	--	D8	--	--	--	--
LCDC_D7	D7	D5	D4	D4_m0	D2_m0	D4	D4_m0	D7	D5	D4	D4_m0	D2_m0
LCDC_D6	D6	D4	D3	D3_m0	D1_m0	D3	D3_m0	D6	D4	D3	D3_m0	D1_m0
LCDC_D5	D5	D3	D2	D2_m0	D0_m0	D2	D2_m0	D5	D3	D2	D2_m0	D0_m0
LCDC_D4	D4	D2	D1	D1_m0	--	D1	D1_m0	D4	D2	D1	D1_m0	--
LCDC_D3	D3	D1	D0	D0_m0	--	D0	D0_m0	D3	D1	D0	D0_m0	--
LCDC_D2	D2	D0	--	--	--	--	--	D2	D0	--	--	--
LCDC_D1	D1	--	--	--	--	--	--	D1	--	--	--	--
LCDC_D0	D0	--	--	--	--	--	--	D0	--	--	--	--

armsom https://armsom.org/

Project:	ArmSoM-FORGE1				
File:	SOC-VO Interface/GPIO				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	8 of 21

U1000D

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

SPI2 only support slave

SPI2_CLK/ETH_RMII0_RXD0/GPIO2_B0_d	D21				RMII0_RXD0 [15]
SPI2_CSN/ETH_RMII0_RXD1/GPIO2_B1_d	D23				RMII0_RXD1 [15]
SPI2_MOSI/ETH_RMII0_CLK/GPIO2_B2_d	E21	RMII0CLK	R1602	22R R0201	RMII0_CLK [15]
SPI2_MISO/ETH_RMII0_TXD0/GPIO2_B3_d	E22	RMII0TXD0	R1603	22R R0201	RMII0_TXD0 [15]
SAI3_SCLK/DSM_AUD_RN_M1/ETH_RMII0_TXD1/GPIO2_B4_d	F21	RMII0TXD1	R1604	22R R0201	RMII0_TXD1 [15]
SAI3_LRCK/DSM_AUD_RP_M1/ETH_RMII0_TXEN/GPIO2_B5_d	F23	RMII0TXEN	R1605	0R R0201	RMII0_TXEN [15]
SAI3_SDI/DSM_AUD_LN_M1/ETH_RMII0_MDC/GPIO2_B6_d	F22				RMII0_MDC [15]
SAI3_SDO/DSM_AUD_LP_M1/ETH_RMII0_MDIO/GPIO2_B7_d	G21				RMII0_MDIO [15]
SAI3_MCLK/ETH_RMII0_RXDVCRS/GPIO2_C0_d	G22				RMII0_RXDV_CRS [15]

VCC_3V3

VCCIO3_VCC — 1G14

C1600 100nF X5R 10V C0402

SOC_RK3506B

BGA333_13R3X11R3X1R25

U1000E

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

SDMMC_CLK/GPIO3_A0_d	K21				SDMMC_CLK [12]
SDMMC_CMD/GPIO3_A1_d	J21				SDMMC_CMD [12]
SDMMC_D0/GPIO3_A2_d	K23				SDMMC_D0 [12]
TEST_CLK_OUT/SDMMC_D1/GPIO3_A3_d	K22				SDMMC_D1 [12]
JTAG_TCK_M0/SDMMC_D2/GPIO3_A4_d	H23				SDMMC_D2 [12]
JTAG_TMS_M0/SDMMC_D3/GPIO3_A5_d	H22				SDMMC_D3 [12]
ETH_RMII1_RXD0/SAI2_SDI_M0/GPIO3_A6_d	L22				RMII1_RXD0 [16]
ETH_RMII1_RXD1/SAI2_SCLK_M0/GPIO3_A7_d	M22				RMII1_RXD1 [16]
ETH_RMII1_CLK/SAI2_SDO_M0/GPIO3_B0_d	M23	RMII1CLK	R1622	22R R0201	RMII1_CLK [16]
ETH_RMII1_TXD0/SAI2_LRCK_M0/GPIO3_B1_d	M21	RMII1TXD0	R1624	22R R0201	RMII1_TXD0 [16]
ETH_RMII1_TXD1/UART5_CTSN_M0/GPIO3_B2_d	N21	RMII1TXD1	R1626	22R R0201	RMII1_TXD1 [16]
ETH_RMII1_TXEN/UART5_RX_M0/GPIO3_B3_d	P22	RMII1TXEN	R1628	0R R0201	RMII1_TXEN [16]
ETH_RMII1_MDC/UART5_TX_M0/GPIO3_B4_d	P23				RMII1_MDC [16]
ETH_RMII1_MDIO/UART5_RTSN_M0/GPIO3_B5_d	P21				RMII1_MDIO [16]
ETH_RMII1_RXDVCRS/SAI2_MCLK_M0/GPIO3_B6_d	R22				RMII1_RXDV_CRS [16]

VCC_3V3

VCCIO4_VCC — 1H14

C1602 100nF X5R 10V C0402

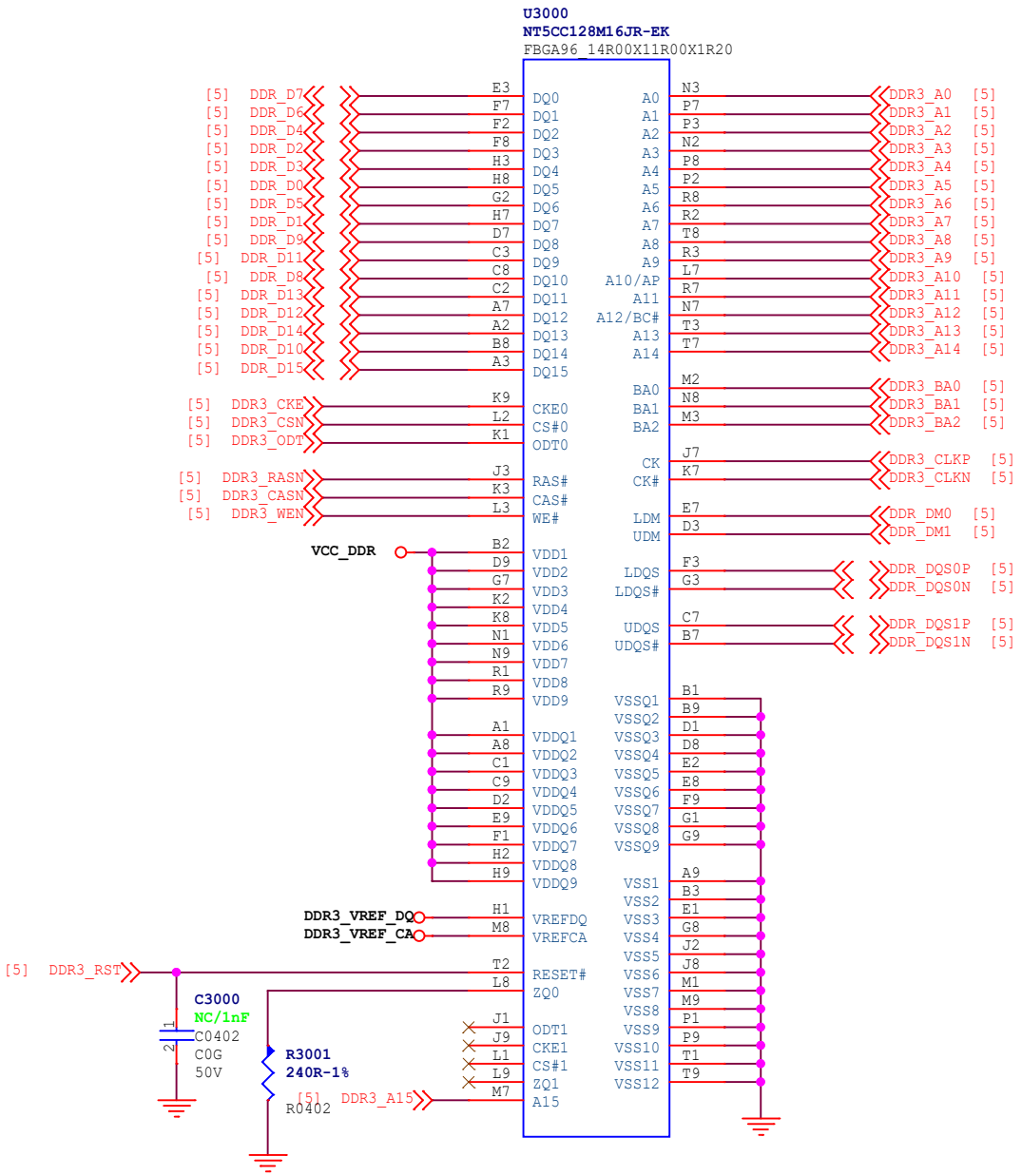
SOC_RK3506B

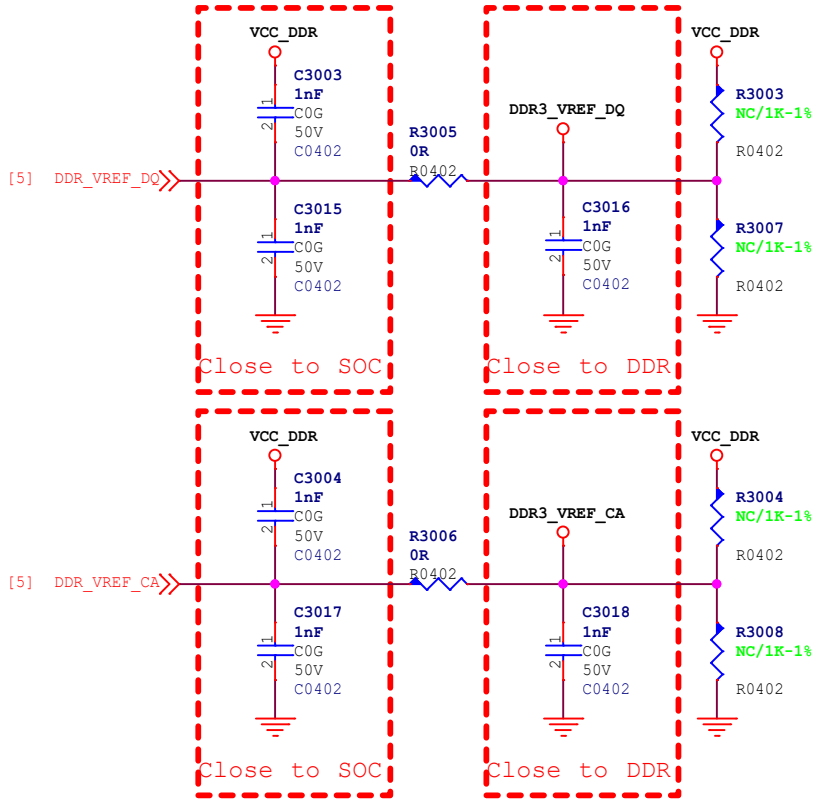
BGA333_13R3X11R3X1R25

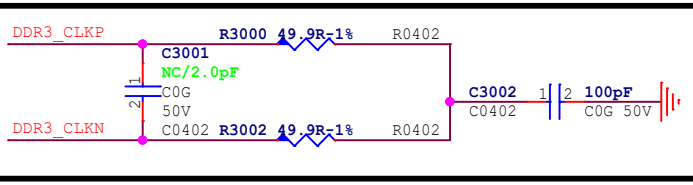
armsom https://armsom.org/

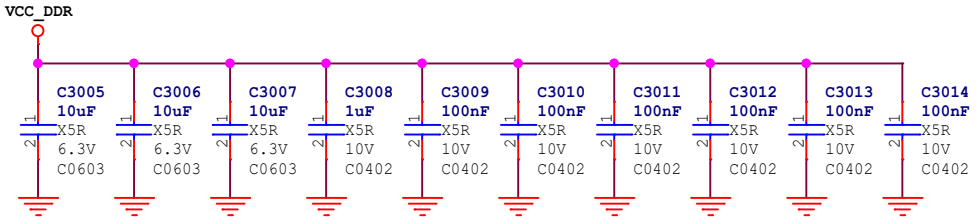
Project:	ArmSoM-FORGE1				
File:	SOC-RMII/SDMMC/GPIO				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	9 of 21

DDR3/DDR3L 1x16bit







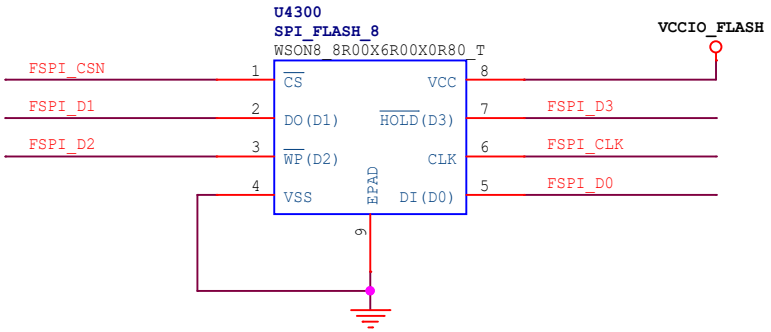


Note:All the Power filter capacitors should be placed close to the power pins of DDR

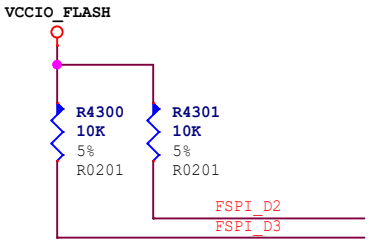
armsom	https://armsom.org/			
Project:	ArmSoM-FORGE1			
File:	DRAM_DDR3/DDR3L_96P_1X16bit			
Date:	Tuesday, March 25, 2025		Rev:	V1.0
Designed by:	Park	Reviewed by: <Checker>	Sheet:	10 of 21

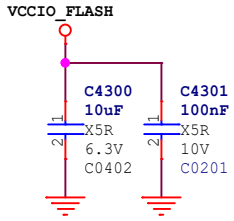
SPI Flash

NOTE:
Refer to the latest AVL for parts selection.



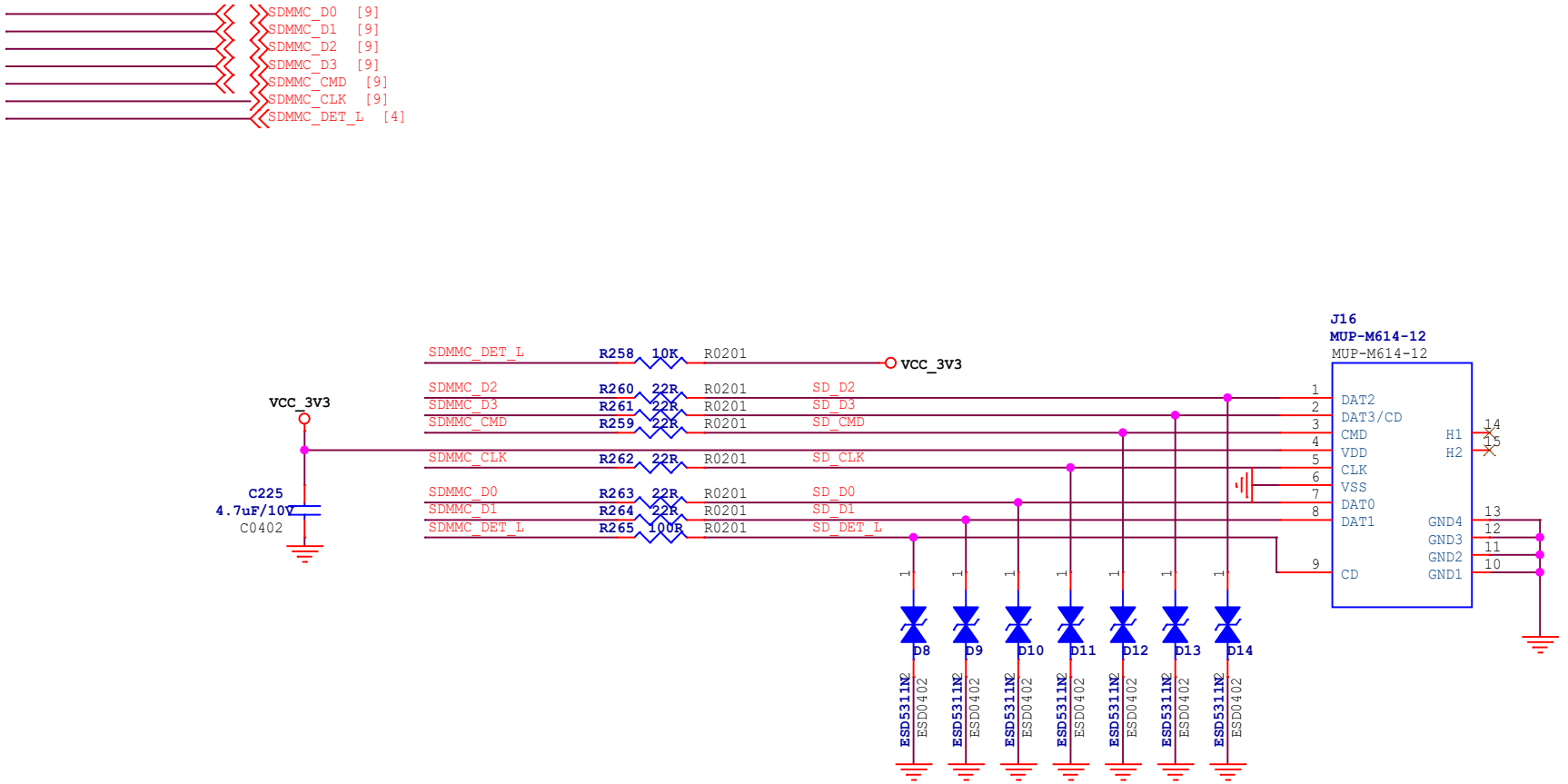
Default:3.3V





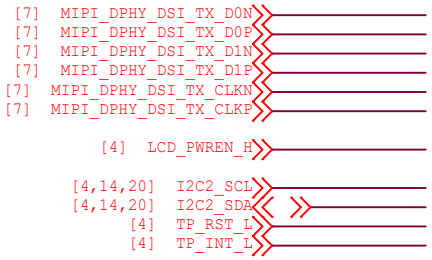
armsom https://armsom.org/					
Project:	ArmSoM-FORGE1				
File:	Flash-SPI Flash				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	11 of 21

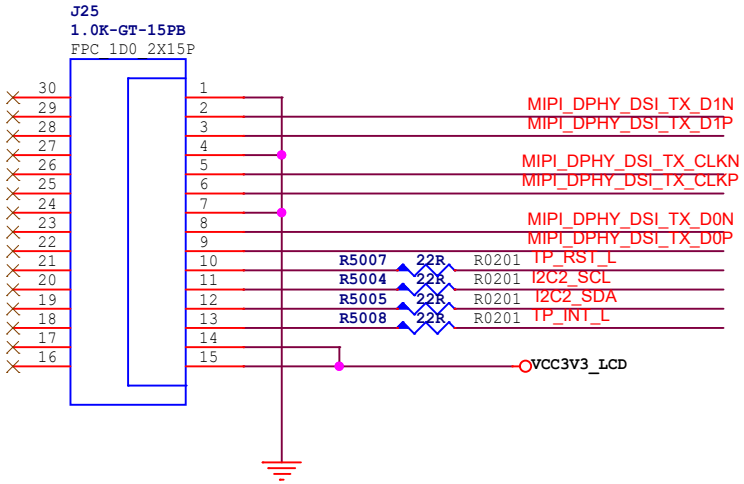
TF Card

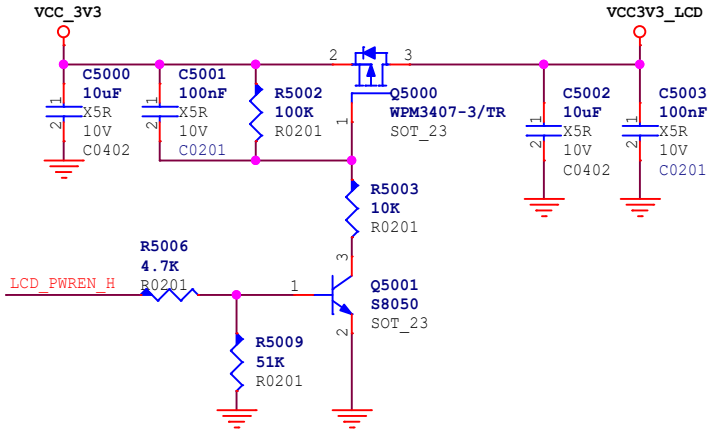


armsom https://armsom.org/					
Project:	ArmSoM-FORGE1				
File:	TF Card				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	12 of 21

MIPI Panel Interface

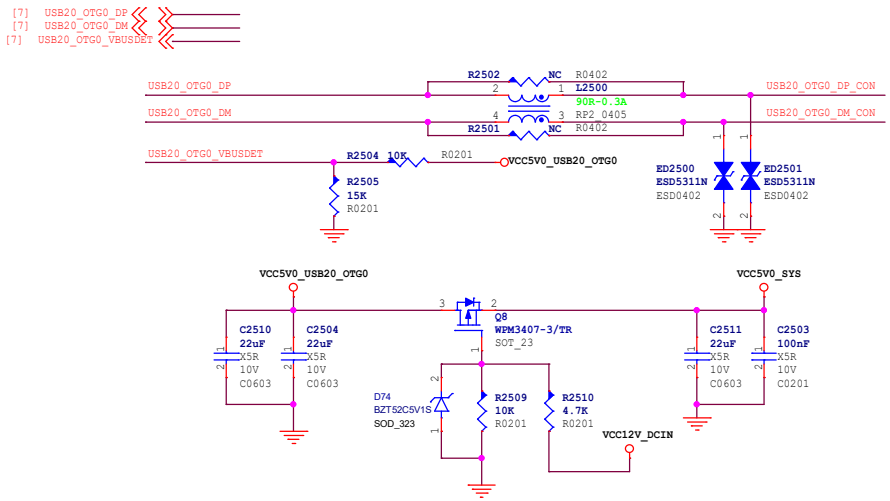


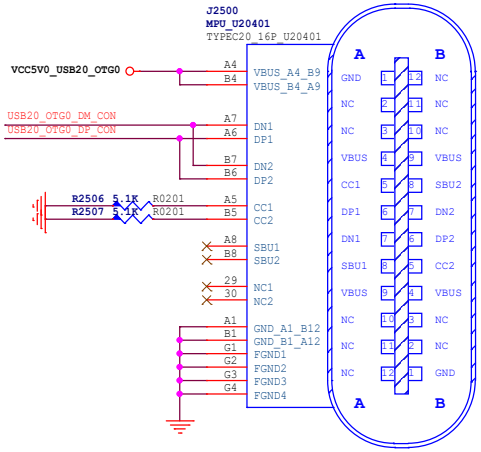




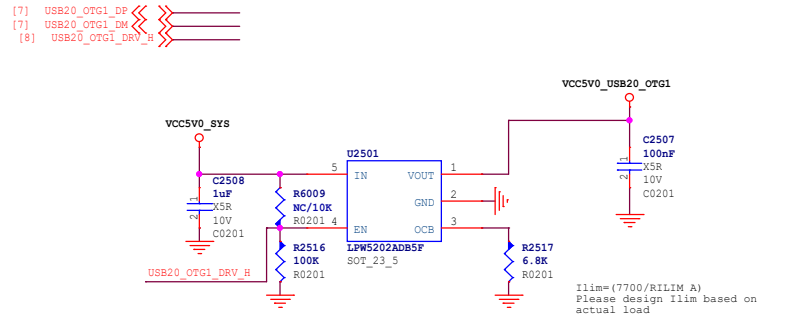
armsom https://armsom.org/					
Project:	ArmSoM-FORGE1				
File:	VO-MIPI-DSI				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	13 of 21

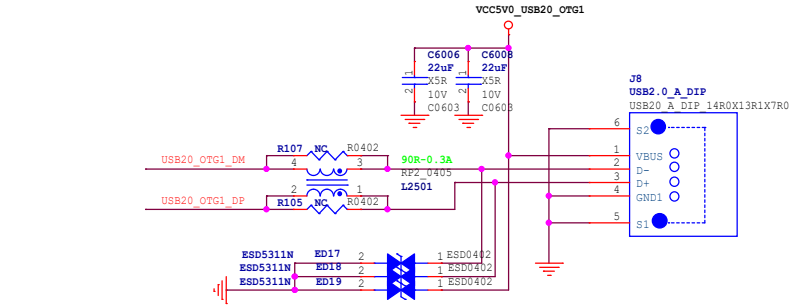
USB2.0 OTG0



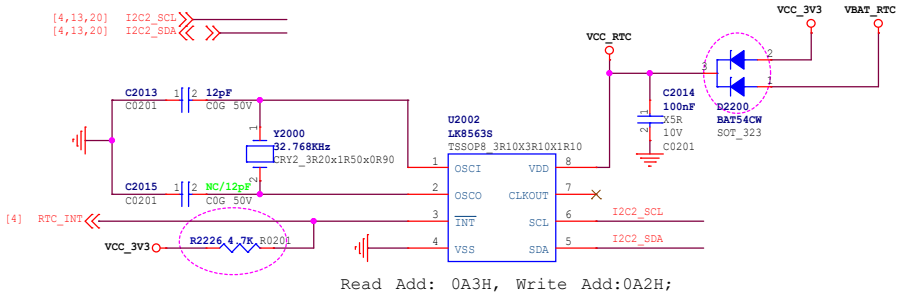


USB2.0 OTG1





RTC



Read Add: 0A3H, Write Add:0A2H;

armsom	https://armsom.org/				
Project:	ArmSoM-FORGE1				
File:	USB-Port-RTC				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	14 of 21

FEPHY0

[9] RMII0_TXD0
[9] RMII0_TXD1
[9] RMII0_TXEN
[9] RMII0_RXD0
[9] RMII0_RXD1
[9] RMII0_RXDV_CRS
[9] RMII0_CLK
[9] RMII0_MDIO
[9] RMII0_MDC
[4] RMII0_RSTn

OPTION1

Y6600
25MHz
CRY4_3R20X2R50X0R80

PHY0_XTALOUT — X1 — GND — PHY0_XTALIN
GND — X2

C6600 18pF C0G 50V C0201
C6601 18pF C0G 50V C0201

OPTION2

RMII0_CLK — R6604 0R R0201 — PHY0_TXC

MAC -----> PHY

J6600
LPJG0926HENL
RJ45_LPJG0926HENL

PHY0_RX0-
PHY0_RX0+
PHY0_TX0-
PHY0_TX0+

MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
TCT0
TCT1
G+
G-
Y+
Y-
NC0
NC1
GND0
GND1
VC1
VC2
VC3
VC4

C6602 100nF X5R 10V C0201
C6603 100nF X5R 10V C0201

PHY0_LED1/PHYAD1
PHY0_LED1-
PHY0_LED0+
PHY0_LED0/PHYAD0

RJ45_GND

R6610 1M R1206
C6605 1nF/2KV 2KV C1206

Note:
VCCIO_RMII=3.3V

VCC_3V3
R6611 510R R0201 PHY0_LED1-
R6612 510R R0201 PHY0_LED0+

VCC_3V3 — R6615 0R R0402 — VCCIO_RMII0

U6601
YT8522H
QFN32_5R00X5R00X1R00_T

VCCIO_RMII0

C6608 4.7uF C0402 X5R 10V
C6609 100nF C0201 X5R 10V

DVDDIO

RMII0_RXD0 — R6621 22R R0201 — PHY0_RXD0
RMII0_RXD1 — R6622 22R R0201 — PHY0_RXD1
PHY0_INT
PHY0_CLK_CTL
PHY0_RXDV
RMII0_RXDV_CRS — R6623 22R R0201 — PHY0_RXDV_CRS
PHY0_RXER

RXC
RXD0
RXD1
RXD2/INTB
RXD3/CLK_CTL
RXDV
CRS/CRS_DV/XTAL_SEL
RXER

PHY0_TXC
RMII0_TXD0
RMII0_TXD1
RMII0_TXEN
RMII0_RSTn
RMII0_MDC
RMII0_MDIO
PHY0_LED0/PHYAD0
PHY0_LED1/PHYAD1
PHY0_COL

TXC
TXD0
TXD1
TXD2
TXD3
TXEN
PHYRSTB
MDC
MDIO
LED0/PHYAD0/PMEB
LED1/PHYAD1
COL/BP_I2C

VCCIO_RMII0
R6625 NC/4.7K R0201
R6626 4.7K R0201
R6627 1.8K R0201

C6617 100nF X5R 10V C0201

DVDDL_O
AVDDL_O
PHY0_DVDDL
PHY0_AVDDL

C6610 100nF X5R 10V C0201
C6611 1uF X5R 10V C0201
C6612 100nF X5R 10V C0201
C6613 1uF X5R 10V C0201

AVDD33_0
AVDD33_1
VCC_3V3

C6614 100nF C0201 X5R 10V
C6615 100nF C0201 X5R 10V
C6616 4.7uF C0402 X5R 10V

MDI0+
MDI0-
MDI1+
MDI1-
PHY0_TX0+
PHY0_TX0-
PHY0_RX0+
PHY0_RX0-

RBIAS
R6630 2.49K-1% R0201
PHY0_RBIAS

XTAL_OUT
XTAL_IN
PHY0_XTALOUT
PHY0_XTALIN

E_PAD

R6613 4.7K R0201 PHY0_LED1/PHYAD1
C6606 NC/100pF C0G 50V C0201

VCCIO_RMII0 — R6614 4.7K R0201 PHY0_LED0/PHYAD0
C6607 NC/100pF C0G 50V C0201

PHY Address Config

PHY Address	PHYAD[1:0]
1 (default)	2'b01

R6616 NC/4.7K R0201 PHY0_CLK_CTL R6617 4.7K R0201 VCCIO_RMII0

RMII REF_CLK direction:
(0 = RMII REF_CLK PHY Output mode; 1 = RMII REF_CLK PHY Intput mode)

R6618 4.7K R0201 PHY0_RXDV_CRS R6619 NC/4.7K R0201 VCCIO_RMII0

Reference Clock input selection:
(0 = Reference Clock from XTAC; 1 = Reference Clock from TXC)

PHY0_INT R6620 4.7K R0201 VCCIO_RMII0

This pin is pulled high by an external 4.7Kohm.
This pin is used for the interrupt function only when in the RMII mode.

PHY0_RXDV R6624 4.7K R0201 VCCIO_RMII0

MII/RMII Selection: (Pull High for RMII mode(default))

R6628 4.7K R0201 PHY0_RXD1 R6629 NC/4.7K R0201 VCCIO_RMII0

WOL/LED0 Selection: (0 = LED0 Mode(default); 1 = WOL(Wake-on-LAN) Mode)

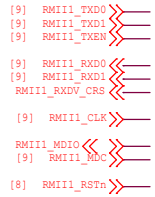
R6631 4.7K R0201 PHY0_RXER R6632 NC/4.7K R0201 VCCIO_RMII0

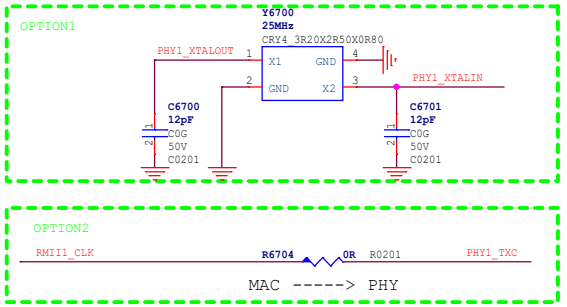
UTP / Fiber Selection: (0 = UTP Mode(default); 1 = Fiber Mode)

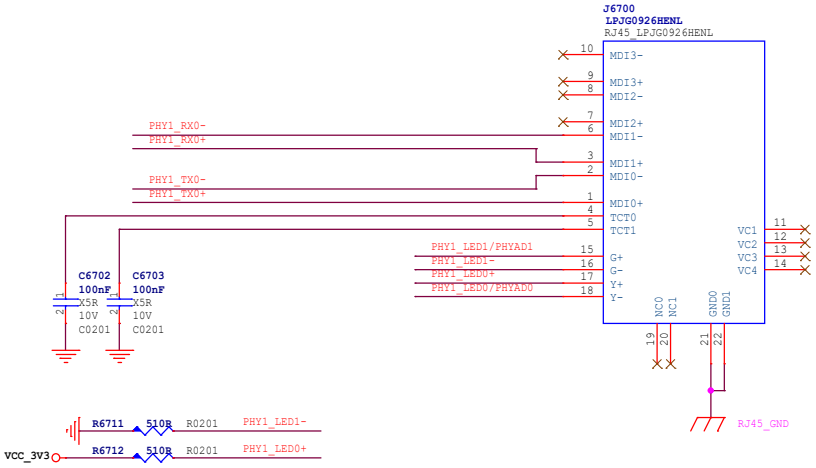
armsom https://armsom.org/

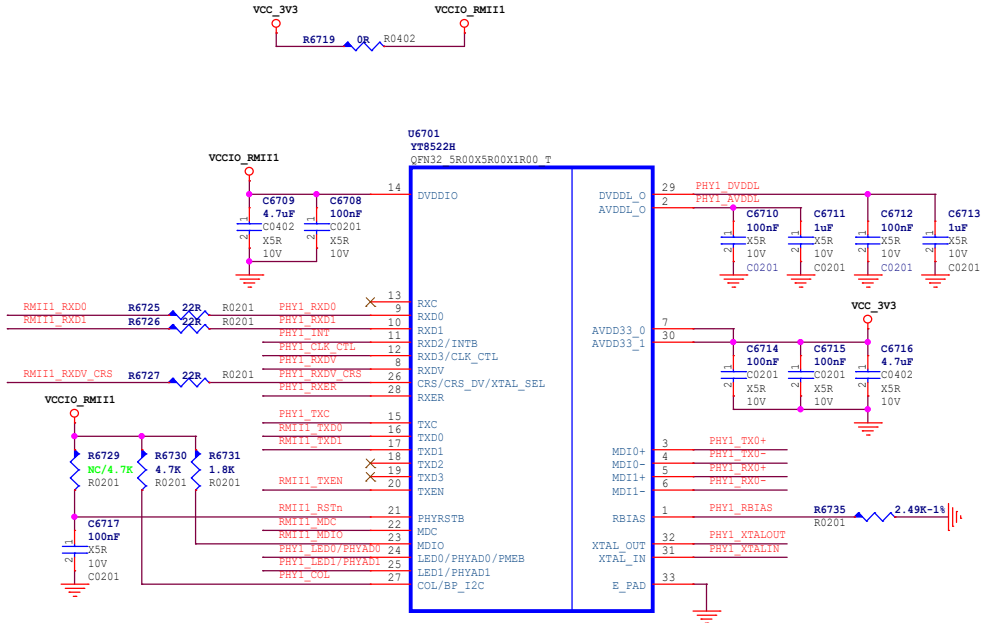
Project:	ArmSoM-FORGE1				
File:	Ethernet-FEPHY_RMII0				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	15 of 21

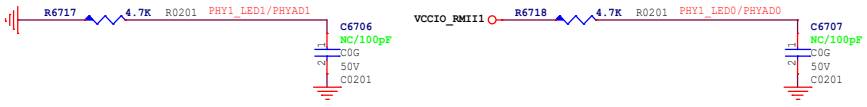
FEPHY1







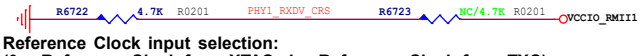




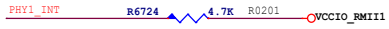
PHY Address Config

PHY Address	PHYAD[1:0]
1 (default)	2'b01

RMII REF_CLK direction:
(0 = RMII REF_CLK PHY Output mode; 1 = RMII REF_CLK PHY Intput mode)



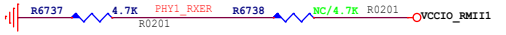
Reference Clock input selection:
(0 = Reference Clock from XTAC; 1 = Reference Clock from TXC)



This pin is pulled high by an external 4.7Kohm.
This pin is used for the interrupt function only when in the RMII mode.

MII/RMII Selection:Pull High for RMII mode (default)

WOL/LED0 Selection: (0 = LED0 Mode(default); 1 = WOL(Wake-on-LAN) Mode)

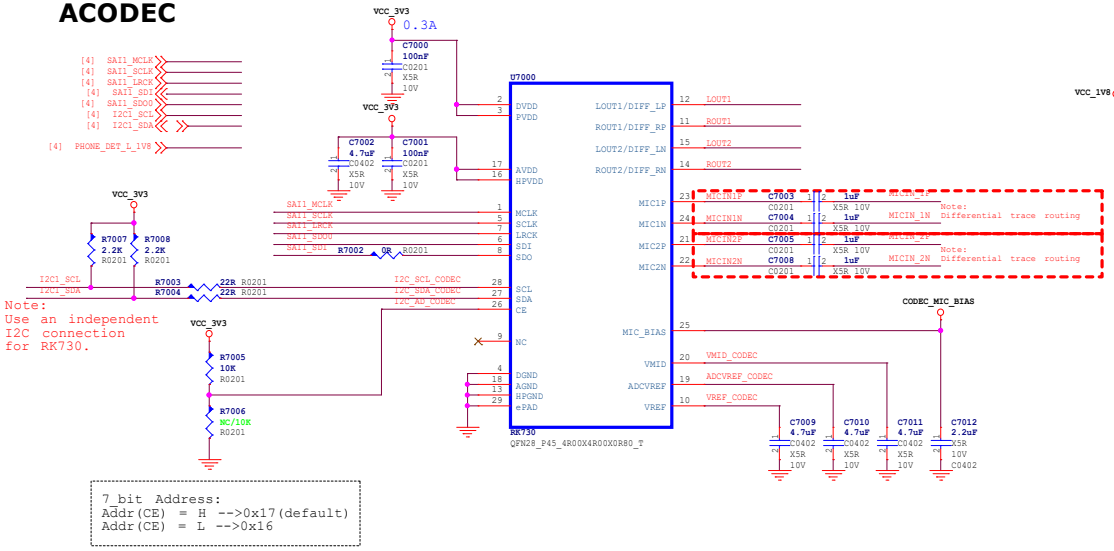


UTP / Fiber Selection: (0 = UTP Mode(default); 1 = Fiber Mode)

armsom https://armsom.org/

Project:	ArmSoM-FORGE1				
File:	Ethernet-FEPHY_RMII1				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	16 of 21

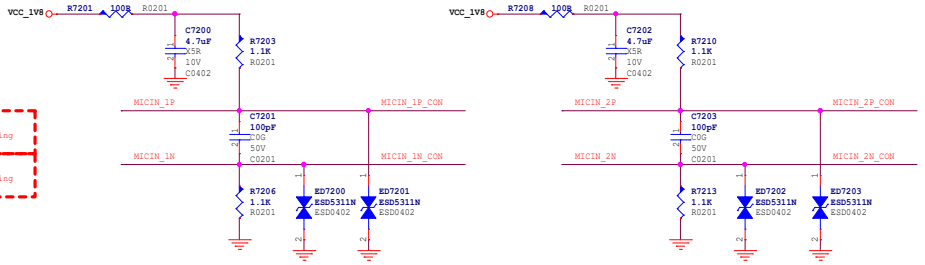
ACODEC



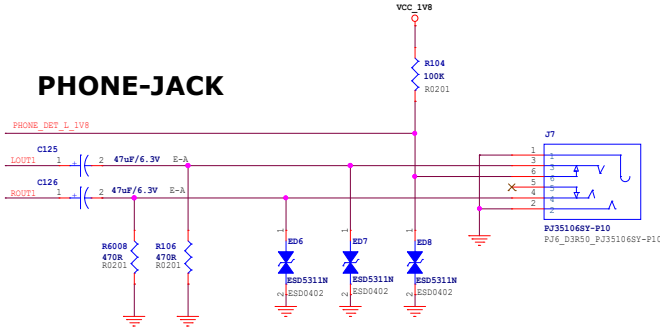
Note:
Use an independent
I2C connection
for RK730.

7_bit Address:
Addr(CE) = H -->0x17(default)
Addr(CE) = L -->0x16

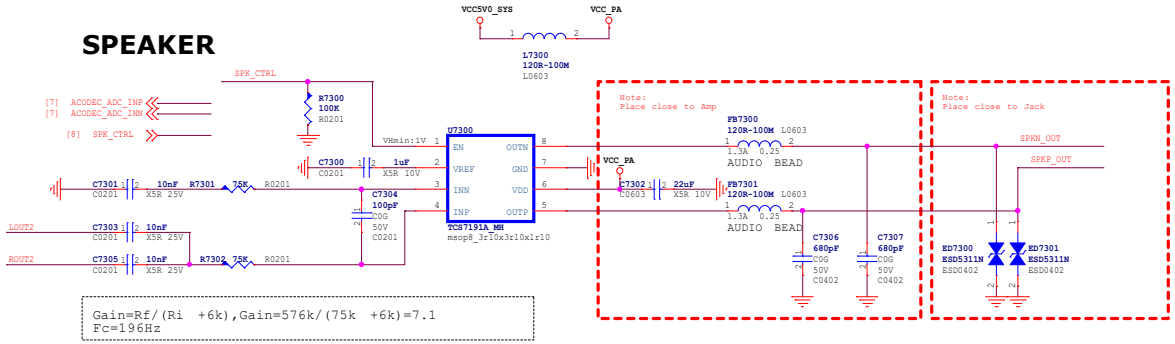
MIC



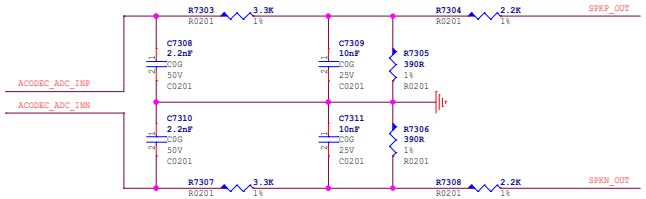
PHONE-JACK



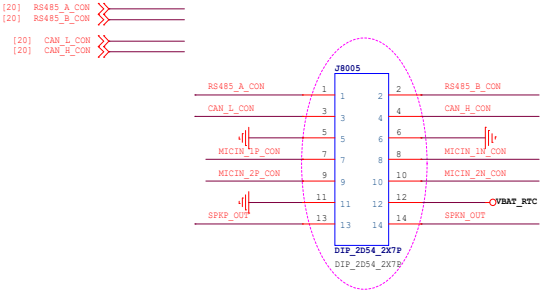
SPEAKER



Gain=Rf/(Ri +6k),Gain=576k/(75k +6k)=7.1
Fc=196Hz



AUDIO-CONN

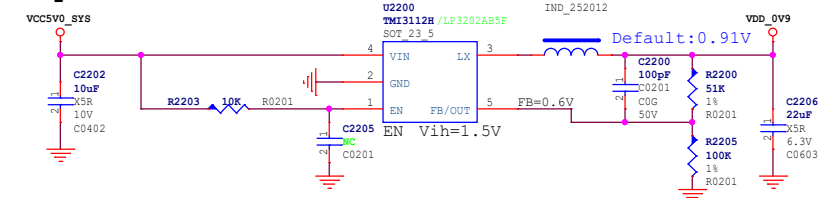


armsom https://armsom.org/

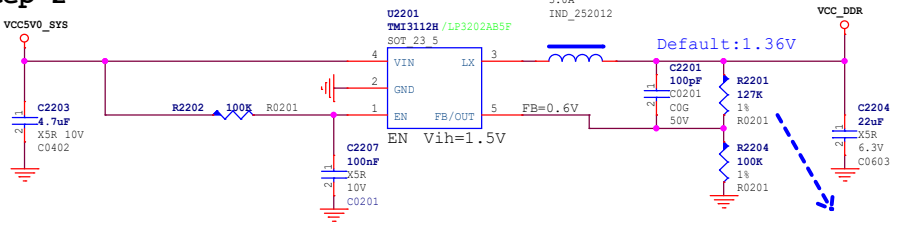
Project:	ArmSoM-FORGE1		
File:	Audio-Codec		
Date:	Tuesday, March 25, 2025	Rev:	V1.0
Designed by:	Park	Reviewed by: <Checker>	Sheet: 17 of 21

[4] PWM0_CH0_CPU

VDD_0V9 Step 1



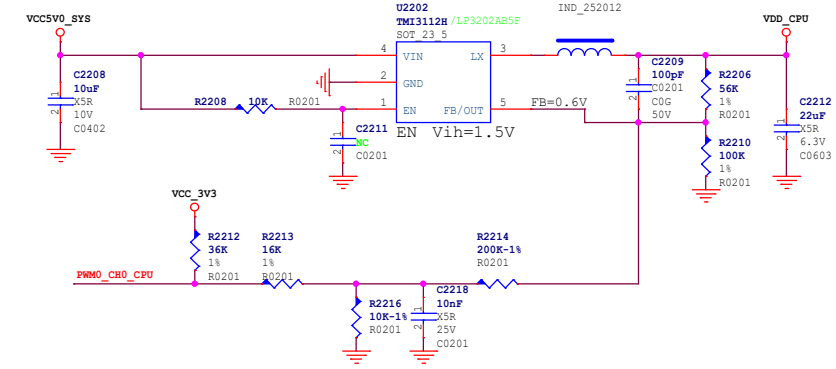
VCC_DDR Step 2



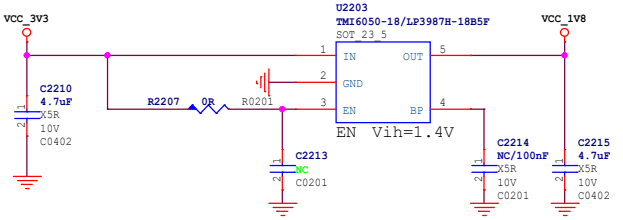
DDR2	1.81V	200K
DDR3	1.50V	150K
DDR3L	1.36V	127K

VDD_CPU Step 1

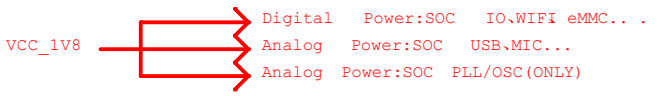
Range:0.754~1.099V
Default:0.954V
Vout=1.099-(1.099-0.754)*Duty



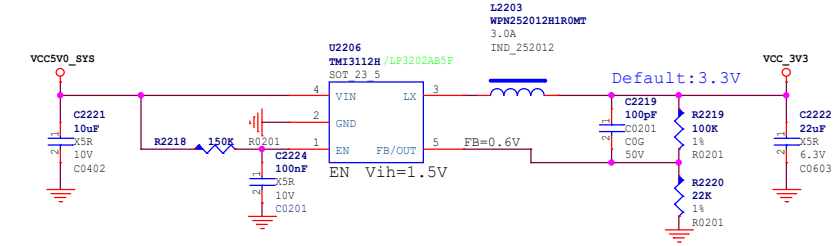
VCC_1V8 Step 2a



Note:
1.Do not have a soft opening inside the LDO.
2.Star line, distinguish between analog and digital power supply



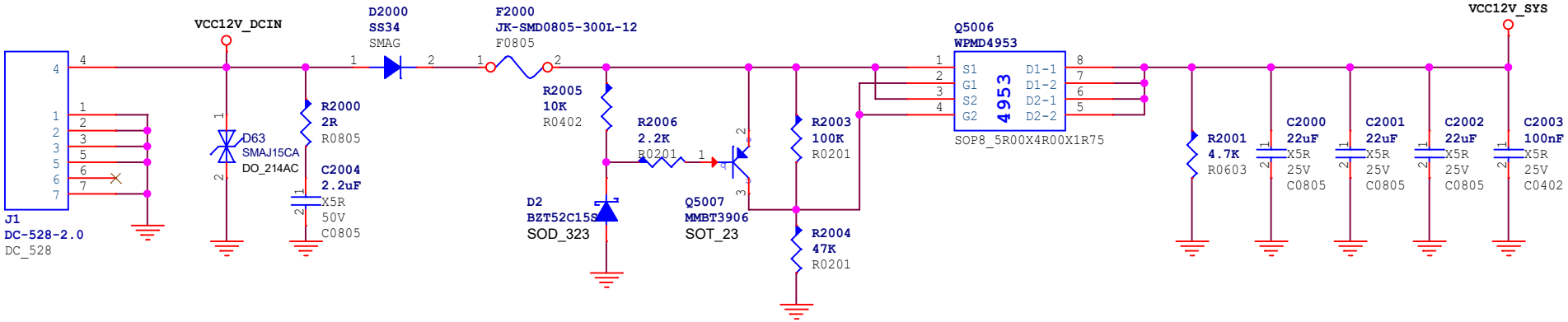
VCC_3V3 Step 3



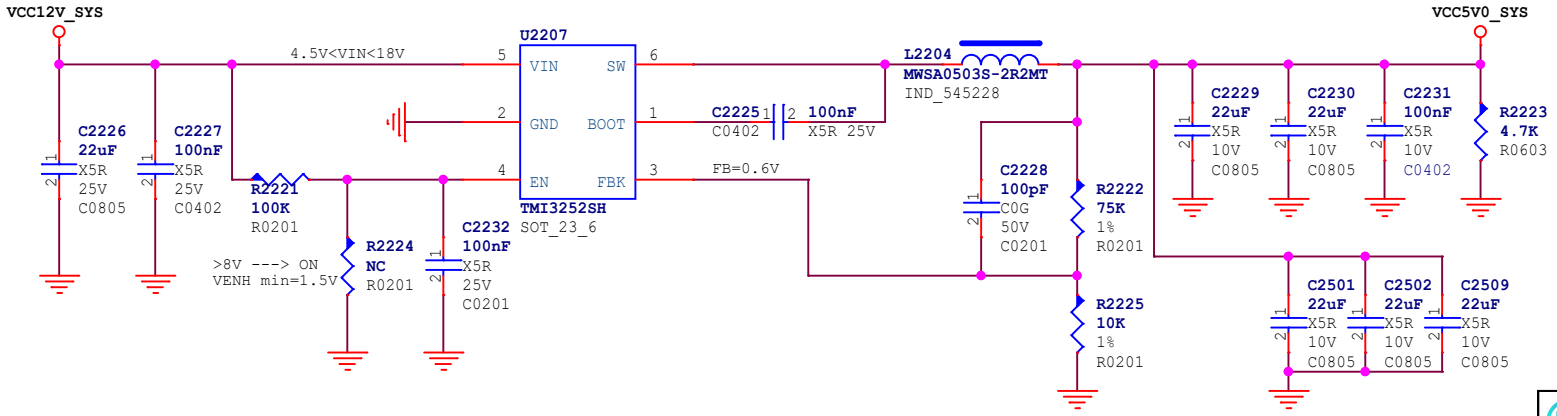
armsom https://armsom.org/

Project:	ArmSoM-FORGE1				
File:	Power-Discrete				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	18 of 21

12V DCIN



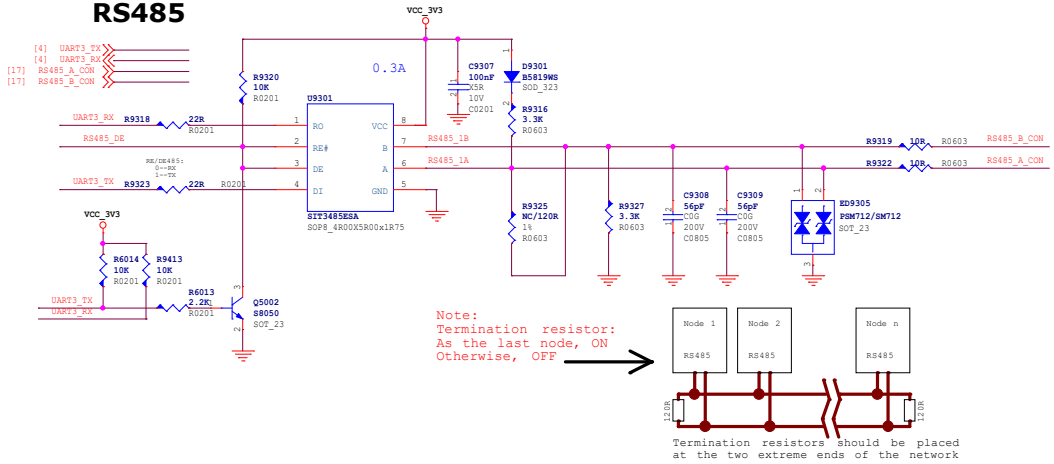
VCC5V0_SYS



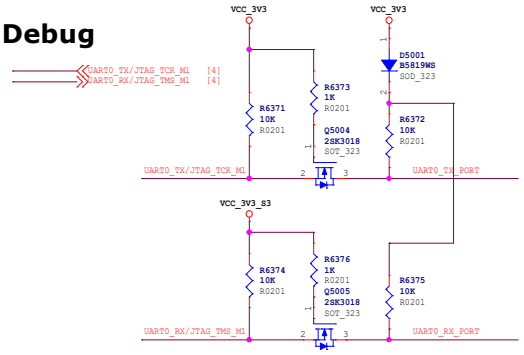
armsom https://armsom.org/

Project:	ArmSoM-FORGE1				
File:	Power-DC IN				
Date:	Monday, March 31, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	19 of 21

RS485



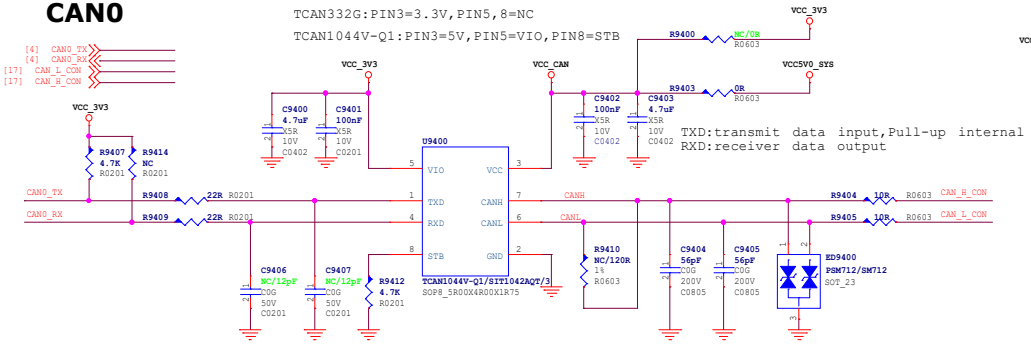
Debug



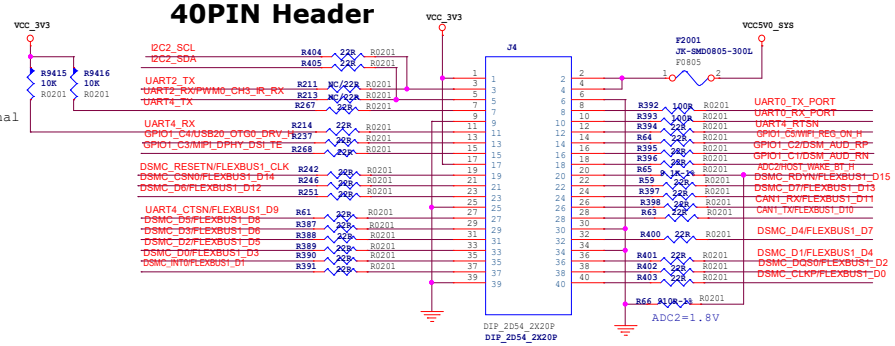
CAN0

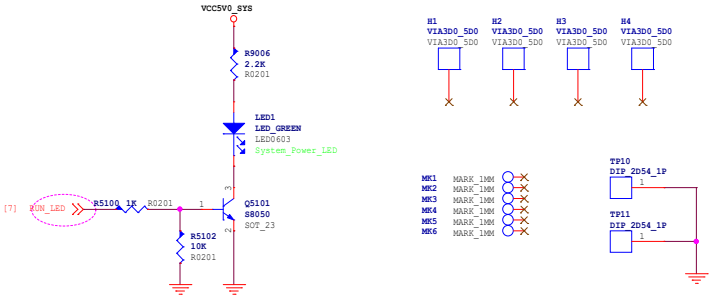
TCAN332G:PIN3=3.3V,PIN5,8=NC

TCAN1044V-Q1:PIN3=5V,PIN5=VIO,PIN8=STB



40PIN Header





armsom	https://armsom.org/		
Project:	ArmSoM-FORGE1		
File:	25.GPIO-40PIN Header		
Date:	Tuesday, March 25, 2025	Rev:	V1.0
Designed by: Park	Reviewed by: <Checker>	Sheet:	20 of 21

Revision History

Version	Date	Change Note	Approved
V1.0	2025-01-08	First release;	
V1.1	2025-03-25	RTC: add R2226/D2200,J8005=12PIN change to 14PIN;(add RTC_INT and VBAT);	

armsom	https://armsom.org/				
Project:	ArmSoM-FORGE1				
File:	Revision History				
Date:	Tuesday, March 25, 2025			Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	21 of 21