Arman Khondker
Aak2464

Part 2

Constraint File

```
## Switches
set_property PACKAGE_PIN V17 [get_ports {c}]
        set_property IOSTANDARD LVCMOS33 [get_ports {c}]
set_property PACKAGE_PIN V16 [get_ports {b}]
        set_property IOSTANDARD LVCMOS33 [get_ports {b}]
set_property PACKAGE_PIN W16 [get_ports {a}]
        set_property IOSTANDARD LVCMOS33 [get_ports {a}]
set_property PACKAGE_PIN W17 [get_ports {e}]
        set_property IOSTANDARD LVCMOS33 [get_ports {e}]

## LEDs
set_property PACKAGE_PIN U16 [get_ports {d7}]
   set_property IOSTANDARD LVCMOS33 [get_ports {d7}]
set_property PACKAGE_PIN E19 [get_ports {d6}]
   set_property IOSTANDARD LVCMOS33 [get_ports {d6}]
set_property PACKAGE_PIN U19 [get_ports {d5}]
   set_property IOSTANDARD LVCMOS33 [get_ports {d5}]
set_property PACKAGE_PIN V19 [get_ports {d4}]
   set_property IOSTANDARD LVCMOS33 [get_ports {d4}]
set_property PACKAGE_PIN W18 [get_ports {d3}]
   set_property IOSTANDARD LVCMOS33 [get_ports {d3}]
set_property PACKAGE_PIN U15 [get_ports {d2}]
   set_property IOSTANDARD LVCMOS33 [get_ports {d2}]
set_property PACKAGE_PIN U14 [get_ports {d1}]
   set_property IOSTANDARD LVCMOS33 [get_ports {d1}]
set_property PACKAGE_PIN V14 [get_ports {d0}]
   set_property IOSTANDARD LVCMOS33 [get_ports {d0}]
```

Part 3

Code of Module for Structural Modeling

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
```

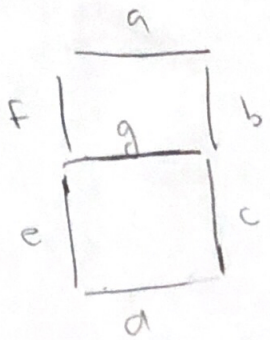
EE 316 Lab 3

Arman Khandker
aak2464

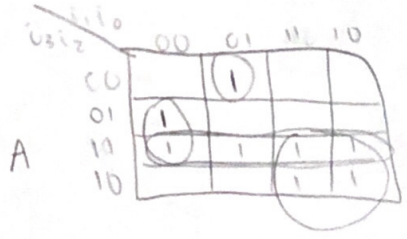
Part 3: BCD to 7 segment LED display

Truth Table

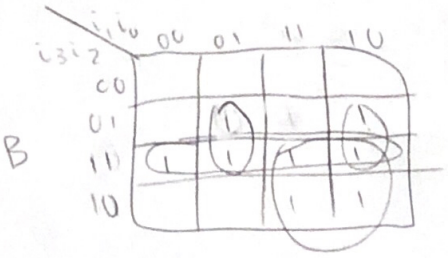
i_3 i_2 i_1 i_0	a	b	c	d	e	f	g
0 0 0 0	0	0	0	0	0	0	1
0 0 0 1	1	0	0	1	1	1	1
0 0 1 0	0	0	1	0	0	1	0
0 0 1 1	0	0	0	0	1	1	0
0 1 0 0	1	0	0	1	1	0	0
0 1 0 1	0	1	0	0	1	0	0
0 1 1 0	0	1	0	0	0	0	0
0 1 1 1	0	0	0	1	1	1	1
1 0 0 0	0	0	0	0	0	0	0
1 0 0 1	0	0	0	1	1	0	0
1 0 1 0	1	1	1	1	1	1	1
1 0 1 1	1	1	1	1	1	1	1
1 1 0 0	1	1	1	1	1	1	1
1 1 0 1	1	1	1	1	1	1	1
1 1 1 0	1	1	1	1	1	1	1
1 1 1 1	1	1	1	1	1	1	1



K MAPS

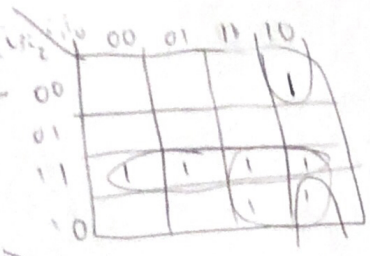


$$A = i_3 i_2 + i_3 i_1 + i_2 i_1' i_0' + i_3' i_2' i_1' i_0$$



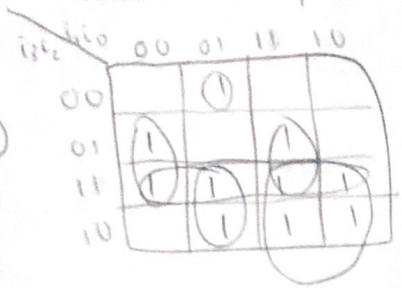
$$B = i_3 i_2 + i_3 i_1 + i_2 i_1' i_0 + i_2 i_1' i_0$$

C



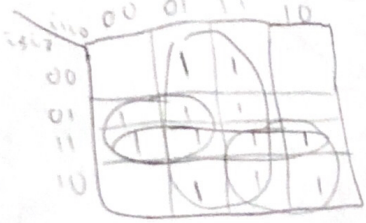
$$C = i_3 i_2 + i_3 i_1 + i_2' i_1 i_0'$$

D



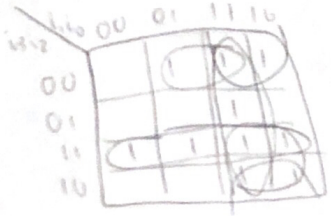
$$D = i_3 i_2 + i_3 i_1 + i_2 i_1' i_0' + i_2 i_1 i_0 + i_3' i_2' i_1' i_0 + i_3 i_2' i_0$$

E



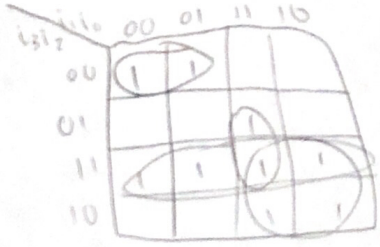
$$E = i_3 i_1 + i_2 i_1' + i_0'$$

F



$$F = i_3 i_2 + i_3 i_1 + i_1 i_0 + i_3' i_2' i_0 + i_2' i_1$$

G



$$G = i_3 i_2 + i_3 i_1 + i_3' i_2' i_1' + i_2 i_1 i_0$$

Arman Khondker
Aak2464

```
// Create Date: 02/27/2019 06:38:59 PM
// Design Name:
// Module Name: BCD_Structural
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// i3dditional Comments:
//
//////////////////////////////////////////////////////////////////////////////////

//Arman
//aak2464

module BCD_Seg_Display(
   input i0,
   input i1,
   input i2,
   input i3,
   output an0,
   output an1,
   output an2,
   output an3,
   output a,
   output b,
   output c,
   output d,
   output e,
   output f,
   output g,
   output dp
   );


   //wires for outputs
   wire and_m0, and_m1, and_m2, and_m3, and_m4, and_m5, and_m6,
   and_m7, and_m8, and_m9, and_m10, and_m11, and_m12, and_m13, and_m14, and_m15,
not_i3, not_i2, not_i1, not_i0;;
```

```
  assign an0=1'b0;
  assign an1=1'b1;
  assign an2=1'b1;
  assign an3=1'b1;
  assign dp = 1'b1;

 //Instantiating Not gates
 not n0 (not_i3, i3);
 not n1 (not_i2, i2);
 not n2 (not_i1, i1);
 not n3 (not_i0, i0);

 //make AND gates
 and m0 (and_m0, i3, i2);
 and m1 (and_m1, i3, i1);
 and m2 (and_m2, i2, not_i1 ,not_i0);
 and m3 (and_m3, not_i3, not_i2, not_i1, i0);
 and m4 (and_m4, i2, not_i1, i0);
 and m5 (and_m5, i2, i1, not_i0);
 and m6 (and_m6, not_i2, i1, not_i0);
 and m7 (and_m7, not_i3, not_i2, not_i1, i0);
 and m8 (and_m8, i2, i1, i0);
 and m9 (and_m9, not_i3, i2, not_i1);
 and m10 (and_m10, not_i3, i0);
 and m11 (and_m11, i1, i0);
 and m12 (and_m12, not_i3, not_i2, i0);
 and m13 (and_m13,not_i3, not_i2, not_i1);
 and m14 (and_m14, not_i2, i1);
 and m15 (and_m15, i3, not_i1, i0);

 //set up the OR gates
 or agate (a, and_m0, and_m1, and_m2, and_m3);
 or bgate (b, and_m0, and_m1, and_m4, and_m5);
 or cgate (c, and_m0, and_m1, and_m6);
 or dgate (d, and_m0, and_m1, and_m2, and_m7, and_m8, and_m15);
 or egate (e, and_m0, and_m1, and_m9, and_m10, i0);
 or fgate (f, and_m0, and_m1, and_m11, and_m12, and_m14);
 or ggate (g, and_m0, and_m1, and_m13, and_m8);


endmodule
```

Code of Testbench for Structural Modeling

Arman Khondker
Aak2464

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 02/27/2019 06:39:54 PM
// Design Name:
// Module Name: tb_BCD_Structural
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////

//Arman Khondker
//aak2464

module tb_BCD_structural;


   reg i3;
   reg i2;
   reg i1;
   reg i0;


   wire a,b,c,d,e,f,g, an0, an1, an2, an3, dp;


   BCD_Seg_Display uut(
      .i3(i3),
      .i2(i2),
      .i1(i1),
      .i0(i0),
      .a(a),
      .b(b),
      .c(c),
```

```
    .d(d),
    .e(e),
    .f(f),
    .g(g),
    .an0 (an0),
    .an1 (an1),
    .an2 (an2),
    .an3 (an3),
    .dp (dp)
);

initial begin


    i3 = 0;
    i2 = 0;
    i1 = 0;
    i0 = 0;

    #50

    i3 = 0;
    i2 = 0;
    i1 = 0;
    i0 = 0;
    $display ("TC01");
    if ({a,b,c,d,e,f,g}!= 7'b0000001)$display ("Result is Wrong");

    i3 = 0;
    i2 = 0;
    i1 = 0;
    i0 = 1;
    #50
    $display ("TC02");
    if({a,b,c,d,e,f,g}!= 7'b1001111) $display ("Result is Wrong");

    i3 = 0;
    i2 = 0;
    i1 = 1;
    i0 = 0;
    #50
    $display ("TC03");
    if( {a,b,c,d,e,f,g}!= 7'b0010010) $display ("Result is Wrong");
```

```
i3 = 0;
i2 = 0;
i1 = 1;
i0 = 1;
#50
$display ("TC04");
if( {a,b,c,d,e,f,g}!= 7'b0000110) $display ("Result is Wrong");

i3 = 0;
i2 = 1;
i1 = 0;
i0 = 0;
#50
$display ("TC05");
if({a,b,c,d,e,f,g}!= 7'b1001100) $display ("Result is Wrong");

i3 = 0;
i2 = 1;
i1 = 0;
i0 = 1;
#50
$display ("TC06");
if({a,b,c,d,e,f,g}!= 7'b0100100) $display ("Result is Wrong");

i3 = 0;
i2 = 1;
i1 = 1;
i0 = 0;
#50
$display ("TC07");
if({a,b,c,d,e,f,g}!= 7'b0100000) $display ("Result is Wrong");

i3 = 0;
i2 = 1;
i1 = 1;
i0 = 1;
#50
$display ("TC08");
if({a,b,c,d,e,f,g}!= 7'b0001111) $display ("Result is Wrong");

i3 = 1;
i2 = 0;
i1 = 0;
i0 = 0;
```

```
#50
$display ("TC09");
if({a,b,c,d,e,f,g}!= 7'b0000000) $display ("Result is Wrong");

i3 = 1;
i2 = 0;
i1 = 0;
i0 = 1;
#50
$display ("TC10");
if({a,b,c,d,e,f,g}!= 7'b0001100) $display ("Result is Wrong");

i3 = 1;
i2 = 0;
i1 = 1;
i0 = 0;
#50
$display ("TC11");
if({a,b,c,d,e,f,g}!= 7'b1111111) $display ("Result is Wrong");

i3 = 1;
i2 = 0;
i1 = 1;
i0 = 1;
#50
$display ("TC12");
if({a,b,c,d,e,f,g}!= 7'b1111111) $display ("Result is Wrong");

i3 = 1;
i2 = 1;
i1 = 0;
i0 = 0;
#50
$display ("TC13");
if({a,b,c,d,e,f,g}!= 7'b1111111) $display ("Result is Wrong");

i3 = 1;
i2 = 1;
i1 = 0;
i0 = 1;
#50
$display ("TC14");
if({a,b,c,d,e,f,g}!= 7'b1111111) $display ("Result is Wrong");
```

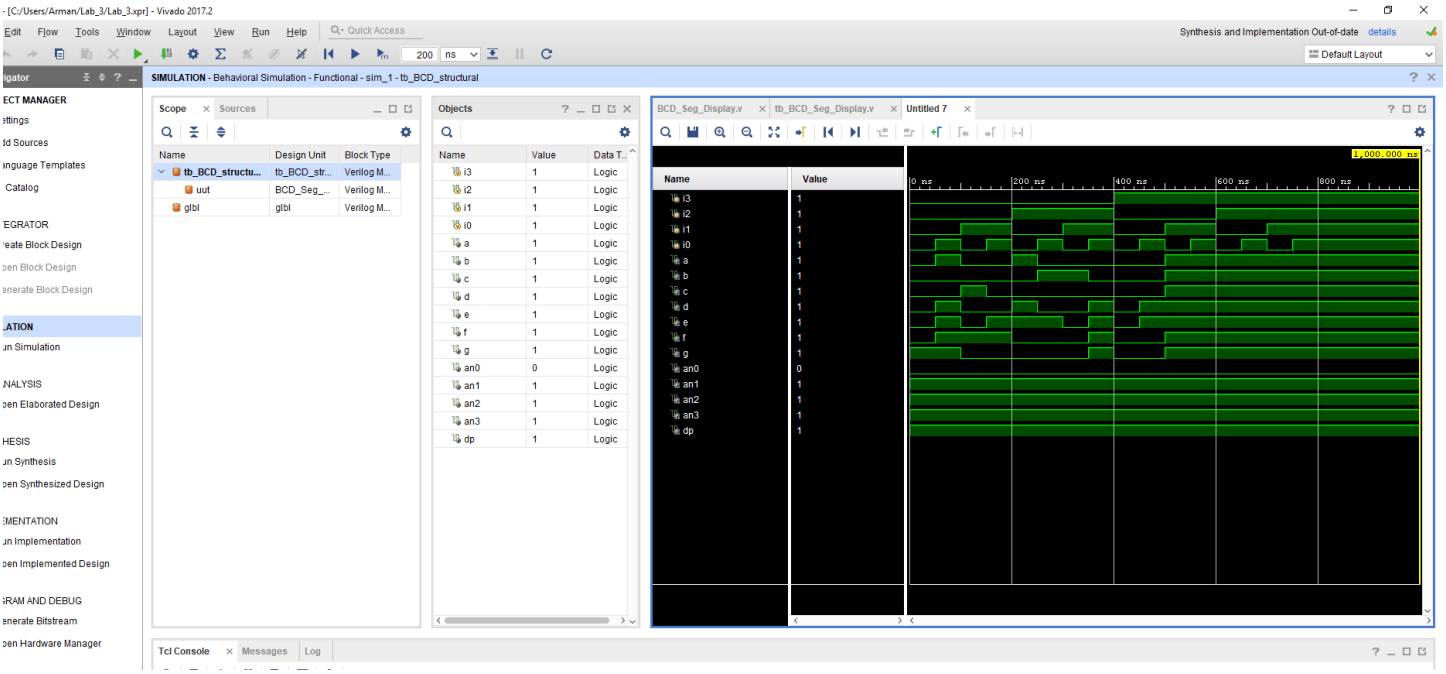
```
        i3 = 1;
        i2 = 1;
        i1 = 1;
        i0 = 0;
        #50
        $display ("TC15");
        if({a,b,c,d,e,f,g}!= 7'b1111111) $display ("Result is Wrong");

        i3 = 1;
        i2= 1;
        i1 = 1;
        i0 = 1;
        #50
        $display ("TC16");
        if({a,b,c,d,e,f,g}!= 7'b1111111) $display ("Result is Wrong");

        end

endmodule
```

Constraint File

```
## Switches
set_property PACKAGE_PIN V17 [get_ports {i0}]
   set_property IOSTANDARD LVCMOS33 [get_ports {i0}]
set_property PACKAGE_PIN V16 [get_ports {i1}]
   set_property IOSTANDARD LVCMOS33 [get_ports {i1}]
set_property PACKAGE_PIN W16 [get_ports {i2}]
   set_property IOSTANDARD LVCMOS33 [get_ports {i2}]
set_property PACKAGE_PIN W17 [get_ports {i3}]
   set_property IOSTANDARD LVCMOS33 [get_ports {i3}]

##7 segment display
set_property PACKAGE_PIN W7 [get_ports {a}]
   set_property IOSTANDARD LVCMOS33 [get_ports {a}]
set_property PACKAGE_PIN W6 [get_ports {b}]
   set_property IOSTANDARD LVCMOS33 [get_ports {b}]
set_property PACKAGE_PIN U8 [get_ports {c}]
   set_property IOSTANDARD LVCMOS33 [get_ports {c}]
set_property PACKAGE_PIN V8 [get_ports {d}]
   set_property IOSTANDARD LVCMOS33 [get_ports {d}]
```

Arman Khondker
Aak2464

```
set_property PACKAGE_PIN U5 [get_ports {e}]
   set_property IOSTANDARD LVCMOS33 [get_ports {e}]
set_property PACKAGE_PIN V5 [get_ports {f}]
   set_property IOSTANDARD LVCMOS33 [get_ports {f}]
set_property PACKAGE_PIN U7 [get_ports {g}]
   set_property IOSTANDARD LVCMOS33 [get_ports {g}]

set_property PACKAGE_PIN V7 [get_ports dp]
   set_property IOSTANDARD LVCMOS33 [get_ports dp]


set_property PACKAGE_PIN U2 [get_ports {an0}]
   set_property IOSTANDARD LVCMOS33 [get_ports {an0}]
set_property PACKAGE_PIN U4 [get_ports {an1}]
   set_property IOSTANDARD LVCMOS33 [get_ports {an1}]
set_property PACKAGE_PIN V4 [get_ports {an2}]
   set_property IOSTANDARD LVCMOS33 [get_ports {an2}]
set_property PACKAGE_PIN W4 [get_ports {an3}]
   set_property IOSTANDARD LVCMOS33 [get_ports {an3}]
```


- [C:/Users/Arman/Lab_3/Lab_3.xpr] - Vivado 2017.2
Edit Flow Tools Window Layout View Run Help
Quick Access
Synthesis and Implementation Out-of-date details
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_BCD_structural
Scope
Sources
Name Design Unit Block Type
tb_BCD_structu... tb_BCD_str... Verilog M...
uut BCD_Seg_... Verilog M...
glbl glbl Verilog M...
Objects
Name Value Data T...
i3 1 Logic
i2 1 Logic
i1 1 Logic
i0 1 Logic
a 1 Logic
b 1 Logic
c 1 Logic
d 1 Logic
e 1 Logic
f 1 Logic
g 1 Logic
an0 0 Logic
an1 1 Logic
an2 1 Logic
an3 1 Logic
dp 1 Logic
BCD_Seg_Display.v
tb_BCD_Seg_Display.v
Untitled 7
1,000.000 ns
0 ns
200 ns
400 ns
600 ns
800 ns
Tcl Console
Messages
Log