RK3399 USB 相关
DTS 配置

前言

概述

RK3399 支持两个 Type-C USB3&DP，两个 USB2.0 HOST。

Type-C0 USB3 支持 OTG（USB Peripheral 和 USB HOST）；

Type-C1 USB3 仅支持 USB3 HOST；

Type-C USB3 可以根据实际的应用需求，将物理接口设计为 Type-A USB3 HOST，Micro USB2.0 OTG，Micro USB3.0 OTG 等类型。

DTS 参考文档：

Documentation/devicetree/bindings/usb/generic.txt

Documentation/devicetree/bindings/usb/dwc3.txt

Documentation/devicetree/bindings/usb/rockchip,dwc3.txt

Documentation/devicetree/bindings/phy/phy-rockchip-typec.txt

Documentation/devicetree/bindings/phy/phy-rockchip-inno-usb2.txt

。

产品版本

芯片名称	内核版本
RK3399	Linux4.4

读者对象

本文档（本指南）主要适用于以下工程师：

技术支持工程师

软件开发工程师

修订记录

日期	版本	作者	修改说明
2017.3.28	1.0	吴良峰	
2017.5.22	1.1	吴良峰	修改格式，修正 micro usb2.0 dts 配置

1 Type-C USB3 (default) (方案 1)

图 1 Type-C 接口类型示意图

DTS 相关配置：

RK3399 DTS 的默认配置支持 Type-C0 USB3 OTG，Type-C1 USB3 HOST。DTS 的配置主要包括 USB3 控制器、USB3 PHY、USB2 PHY、fusb302 等。

1.1 Type-C0 /C1 USB3 控制器 DTS 配置

以 RK3399 EVB3 board 为例：

```
usbdrd3_0: usb@fe800000 {
        compatible = "rockchip,rk3399-dwc3";
        clocks = <&cru SCLK_USB3OTG0_REF>,
                 <&cru SCLK_USB3OTG0_SUSPEND>,
                 <&cru ACLK_USB3OTG0>, <&cru ACLK_USB3_GRF>;
        clock-names = "ref_clk", "suspend_clk",
                      "bus_clk", "grf_clk";
        power-domains = <&power RK3399_PD_USB3>;
        resets = <&cru SRST_A_USB3_OTG0>;
        reset-names = "usb3-otg";
        #address-cells = <2>;
        #size-cells = <2>;
        ranges;
        status = "disabled";
        usbdrd_dwc3_0: dwc3@fe800000 {
                compatible = "snps,dwc3";
                reg = <0x0 0xfe800000 0x0 0x100000>;
                interrupts = <GIC_SPI 105 IRQ_TYPE_LEVEL_HIGH 0>;
                dr_mode = "otg";
                phys = <&u2phy0_otg>, <&tcphy0_usb3>;
                phy-names = "usb2-phy", "usb3-phy";
                phy_type = "utmi_wide";
                snps,dis_enblslpm_quirk;
                snps,dis-u2-freeclk-exists-quirk;
                snps,dis_u2_susphy_quirk;
                snps,dis-del-phy-power-chg-quirk;
```

```
                        snps,xhci-slow-suspend-quirk;
                        status = "disabled";
                };
        };

usbdrd3_1: usb@fe900000 {
                compatible = "rockchip,rk3399-dwc3";
                clocks = <&cru SCLK_USB3OTG1_REF>,
                         <&cru SCLK_USB3OTG1_SUSPEND>,
                         <&cru ACLK_USB3OTG1>, <&cru ACLK_USB3_GRF>;
                clock-names = "ref_clk", "suspend_clk",
                              "bus_clk", "grf_clk";
                power-domains = <&power RK3399_PD_USB3>;
                resets = <&cru SRST_A_USB3_OTG1>;
                reset-names = "usb3-otg";
                #address-cells = <2>;
                #size-cells = <2>;
                ranges;
                status = "disabled";
                usbdrd_dwc3_1: dwc3@fe900000 {
                        compatible = "snps,dwc3";
                        reg = <0x0 0xfe900000 0x0 0x100000>;
                        interrupts = <GIC_SPI 110 IRQ_TYPE_LEVEL_HIGH 0>;
                        dr_mode = "host";
                        phys = <&u2phy1_otg>, <&tcphy1_usb3>;
                        phy-names = "usb2-phy", "usb3-phy";
                        phy_type = "utmi_wide";
                        snps,dis_enblslpm_quirk;
                        snps,dis-u2-freeclk-exists-quirk;
                        snps,dis_u2_susphy_quirk;
                        snps,dis-del-phy-power-chg-quirk;
                        snps,xhci-slow-suspend-quirk;
                        status = "disabled";
                };
        };


&usbdrd3_0 {
        extcon = <&fusb0>;
        status = "okay";
};

&usbdrd_dwc3_0 {
        status = "okay";
};

&usbdrd3_1 {
        extcon = <&fusb1>;
        status = "okay";
```

```
};

&usbdrd_dwc3_1 {
        status = "okay";
};
```

1.2 Type-C0 /C1 USB3 PHY DTS 配置

以 RK3399 EVB3 board 为例：

1.2.1 USB3 PHY

```
tcphy0: phy@ff7c0000 {
                compatible = "rockchip,rk3399-typec-phy";
                reg = <0x0 0xff7c0000 0x0 0x40000>;
                rockchip,grf = <&grf>;
                #phy-cells = <1>;
                clocks = <&cru SCLK_UPHY0_TCPDCORE>,
                         <&cru SCLK_UPHY0_TCPDPHY_REF>;
                clock-names = "tcpdcore", "tcpdphy-ref";
                assigned-clocks = <&cru SCLK_UPHY0_TCPDCORE>;
                assigned-clock-rates = <50000000>;
                power-domains = <&power RK3399_PD_TCPD0>;
                resets = <&cru SRST_UPHY0>,
                         <&cru SRST_UPHY0_PIPE_L00>,
                         <&cru SRST_P_UPHY0_TCPHY>;
                reset-names = "uphy", "uphy-pipe", "uphy-tcphy";
                rockchip,typec-conn-dir = <0xe580 0 16>;
                rockchip,usb3tousb2-en = <0xe580 3 19>;
                rockchip,usb3-host-disable = <0x2434 0 16>;
                rockchip,usb3-host-port = <0x2434 12 28>;
                rockchip,external-psm = <0xe588 14 30>;
                rockchip,pipe-status = <0xe5c0 0 0>;
                rockchip,uphy-dp-sel = <0x6268 19 19>;
                status = "disabled";

                tcphy0_dp: dp-port {
                        #phy-cells = <0>;
                };

                tcphy0_usb3: usb3-port {
                        #phy-cells = <0>;
                };
        };

tcphy1: phy@ff800000 {
                compatible = "rockchip,rk3399-typec-phy";
                reg = <0x0 0xff800000 0x0 0x40000>;
                rockchip,grf = <&grf>;
                #phy-cells = <1>;
                clocks = <&cru SCLK_UPHY1_TCPDCORE>,
```

```
                        <&cru SCLK_UPHY1_TCPDPHY_REF>;
                clock-names = "tcpdcore", "tcpdphy-ref";
                assigned-clocks = <&cru SCLK_UPHY1_TCPDCORE>;
                assigned-clock-rates = <50000000>;
                power-domains = <&power RK3399_PD_TCPD1>;
                resets = <&cru SRST_UPHY1>,
                         <&cru SRST_UPHY1_PIPE_L00>,
                         <&cru SRST_P_UPHY1_TCPHY>;
                reset-names = "uphy", "uphy-pipe", "uphy-tcphy";
                rockchip,typec-conn-dir = <0xe58c 0 16>;
                rockchip,usb3tousb2-en = <0xe58c 3 19>;
                rockchip,usb3-host-disable = <0x2444 0 16>;
                rockchip,usb3-host-port = <0x2444 12 28>;
                rockchip,external-psm = <0xe594 14 30>;
                rockchip,pipe-status = <0xe5c0 16 16>;
                rockchip,uphy-dp-sel = <0x6268 3 19>;
                status = "disabled";

                tcphy1_dp: dp-port {
                        #phy-cells = <0>;
                };

                tcphy1_usb3: usb3-port {
                        #phy-cells = <0>;
                };
        };

&tcphy0 {
        extcon = <&fusb0>;
        status = "okay";
};

&tcphy1 {
        extcon = <&fusb1>;
        status = "okay";
};

&pinctrl {
        ......
        fusb30x {
                fusb0_int: fusb0-int {
                        rockchip,pins = <1 2 RK_FUNC_GPIO &pcfg_pull_up>;
                };

                fusb1_int: fusb1-int {
                        rockchip,pins = <1 24 RK_FUNC_GPIO &pcfg_pull_up>;
                };
        };
}
```

```
&i2c0 {
        fusb1: fusb30x@22 {
                compatible = "fairchild,fusb302";
                reg = <0x22>;
                pinctrl-names = "default";
                pinctrl-0 = <&fusb1_int>;
                //USB VBUS 5V 的 GPIO 配置
                vbus-5v-gpios = <&gpio1 4 GPIO_ACTIVE_LOW>;
                int-n-gpios = <&gpio1 24 GPIO_ACTIVE_HIGH>;
                status = "okay";
        };
        ……
 };

 &i2c6 {
        status = "okay";
        fusb0: fusb30x@22 {
                compatible = "fairchild,fusb302";
                reg = <0x22>;
                pinctrl-names = "default";
                pinctrl-0 = <&fusb0_int>;
                //USB VBUS 5V 的 GPIO 配置
                vbus-5v-gpios = <&gpio1 3 GPIO_ACTIVE_LOW>;
                int-n-gpios = <&gpio1 2 GPIO_ACTIVE_HIGH>;
                status = "okay";
        };
};
```

1.2.2 USB2 PHY

```
grf: syscon@ff770000 {
        ……
u2phy0: usb2-phy@e450 {
                        compatible = "rockchip,rk3399-usb2phy";
                        reg = <0xe450 0x10>;
                        clocks = <&cru SCLK_USB2PHY0_REF>;
                        clock-names = "phyclk";
                        #clock-cells = <0>;
                        clock-output-names = "clk_usbphy0_480m";
                        status = "disabled";

                        u2phy0_otg: otg-port {
                                #phy-cells = <0>;
                                interrupts = <GIC_SPI 103 IRQ_TYPE_LEVEL_HIGH 0>,
                                             <GIC_SPI 104 IRQ_TYPE_LEVEL_HIGH 0>,
                                             <GIC_SPI 106 IRQ_TYPE_LEVEL_HIGH 0>;
                                interrupt-names = "otg-bvalid", "otg-id",
                                                  "linestate";
                                status = "disabled";
```

```
                        };
……
                };

u2phy1: usb2-phy@e460 {
                        compatible = "rockchip,rk3399-usb2phy";
                        reg = <0xe460 0x10>;
                        clocks = <&cru SCLK_USB2PHY1_REF>;
                        clock-names = "phyclk";
                        #clock-cells = <0>;
                        clock-output-names = "clk_usbphy1_480m";
                        status = "disabled";

                        u2phy1_otg: otg-port {
                                #phy-cells = <0>;
                                interrupts = <GIC_SPI 108 IRQ_TYPE_LEVEL_HIGH 0>,
                                             <GIC_SPI 109 IRQ_TYPE_LEVEL_HIGH 0>,
                                             <GIC_SPI 111 IRQ_TYPE_LEVEL_HIGH 0>;
                                interrupt-names = "otg-bvalid", "otg-id",
                                                  "linestate";
                                status = "disabled";
                        };
                        ……
            };
};

&u2phy0 {
        status = "okay";
        extcon = <&fusb0>;

        u2phy0_otg: otg-port {
                status = "okay";
        };
              ……
};

&u2phy1 {
        status = "okay";
        extcon = <&fusb1>;
        u2phy1_otg: otg-port {
                status = "okay";
        };
        ……
};
```

2 Type-A USB3 HOST (方案 2)

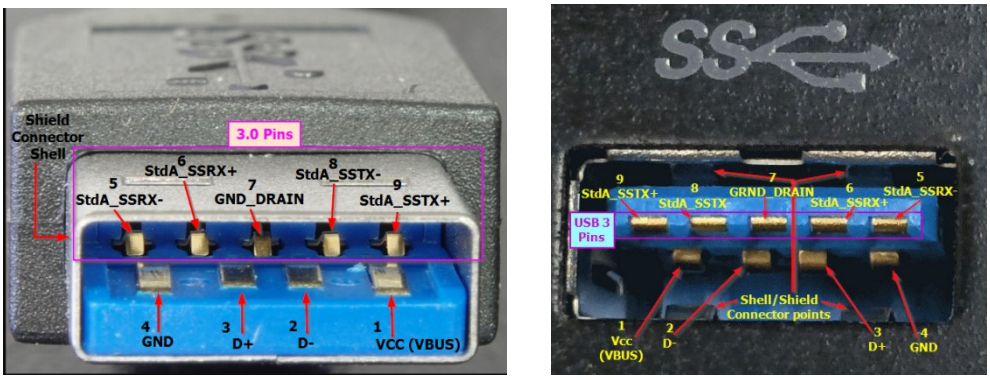

图 2 Type-A 接口类型示意图

RK3399 BOX SDK 的 Type-C1 USB3 经常会设计为 Type-A USB3 HOST 形式

此种设计，USB VBUS 5V 一般为常供电，不需要单独 GPIO 控制，Type-C 的供电需要正常开启，如下图所示：

图 3 Type-C 供电电路

DTS 的配置相比第一种方案，即 Type-C USB3 (default)，基本一样，不同点是，对应的 fusb 节点需要删除，比如 Type-C1 USB3 修改为 Type-A 接口，Type-C0 不变，DTS 参考如下（以 rk3399-box.dtsi 为例）：

```
&tcphy0 {
        extcon = <&fusb0>;
        status = "okay";
};

&tcphy1 {//这里删除了 fusb1 节点的引用
        status = "okay";
};

&u2phy0 {
        status = "okay";
        extcon = <&fusb0>;
```

```
        u2phy0_otg: otg-port {
                status = "okay";
        };
        ……
};

&u2phy1 {
        status = "okay";

        u2phy1_otg: otg-port {
                status = "okay";
        };
        ……
};


&usbdrd3_0 {
        extcon = <&fusb0>;
        status = "okay";
};

&usbdrd_dwc3_0 {
        dr_mode = "otg";
        status = "okay";
};

&usbdrd3_1 {
        status = "okay";
};

&usbdrd_dwc3_1 {
        dr_mode = "host";
        status = "okay";
};
```

此外，Type-C 的供电需要正常开启（参考方案 2）

3 Micro USB3.0 OTG (方案3)

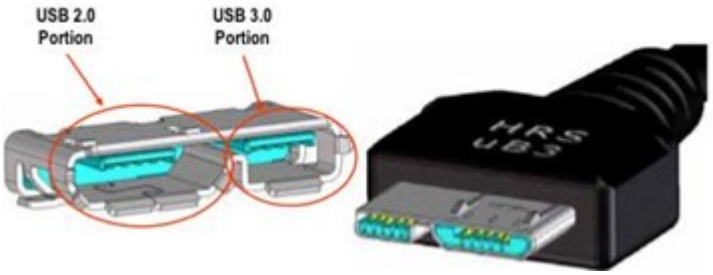

图 4 Micro USB 3.0 OTG 接口类型示意图

此种配置下，由于硬件上没有 fusb302 芯片，所以 DTS 需要做如下的修改：

1. 删除对应的 tcphy 节点和 u2phy 节点中的 extcon 属性；
2. 修改对应的 usbdrd3 节点 extcon 属性引用为 u2phy；
3. 在对应的 u2phy 节点中，配置 OTG 的 VBUS GPIO；
4. dr_mode 配置为 otg；

比如，将 Type-C0 USB3 修改为 Micro USB3.0 OTG，对应 DTS 配置如下：

```
&tcphy0 {
        status = "okay";
};
&u2phy0 {
           //VUBS GPIO 配置参考
           otg-vbus-gpios = <&gpio1 4 GPIO_ACTIVE_HIGH>;
           status = "okay";

           u2phy0_otg: otg-port {
                  status = "okay";
        };
        ……
};
&usbdrd3_0 {
        extcon = <& u2phy0>;
        status = "okay";
};
&usbdrd_dwc3_0 {
        dr_mode = "otg";
        status = "okay";
};
```

4 Micro USB2.0 OTG (方案4)

图 5 Micro USB 2.0 OTG 接口类型示意图

此种配置下，只支持 USB2.0 OTG，所以对应的 Type-C 如下供电可以关闭。

图 6 Type-C 供电电路

DTS 需要做如下修改：

1. Disable 对应的 tcphy 节点；
2. 修改对应的 usbdrd3 节点 extcon 属性引用为 u2phy；
3. 在对应的 u2phy 节点中，配置 OTG 的 VBUS GPIO，并且删除 extcon 属性；
4. usbdrd_dwc3_0 的 dr_mode 配置为 otg， 设置 maximum-speed 为 high-speed，phy 只引用 usb2-phy；

比如，将 Type-C0 USB3 修改为 Micro USB2.0 OTG，对应 DTS 配置如下：

```
&tcphy0 {
        status = "disabled";
};

&u2phy0 {
            //VBUS GPIO 配置参考
            otg-vbus-gpios = <&gpio1 4 GPIO_ACTIVE_HIGH>;
            status = "okay";

            u2phy0_otg: otg-port {
                    status = "okay";
           };
           ……
```

```
};

&usbdrd3_0 {
        extcon = <&u2phy0>;
        status = "okay";
};

&usbdrd_dwc3_0 {
        maximum-speed = “high-speed”;
        dr_mode = "otg";
        phys = <&u2phy0_otg>;
        phy-names = "usb2-phy";
        status = "okay";
};
```

5 USB2.0 HOST 相关 DTS 配置

相比 Type-C 的多种硬件设计方案，USB2.0 HOST 简单很多，一般只涉及 VBUS GPIO 的修改。

DTS 参考文档：

Documentation/devicetree/bindings/usb/usb-ehci.txt

Documentation/devicetree/bindings/usb/usb-ohci.txt

Documentation/devicetree/bindings/phy/phy-rockchip-inno-usb2.txt

5.1 USB2.0 HOST 控制器相关 DTS

```
usb_host0_ehci: usb@fe380000 {
        compatible = "generic-ehci";
        reg = <0x0 0xfe380000 0x0 0x20000>;
        interrupts = <GIC_SPI 26 IRQ_TYPE_LEVEL_HIGH 0>;
        clocks = <&cru HCLK_HOST0>,
                 <&cru HCLK_HOST0_ARB>,
                 <&cru SCLK_USBPHY0_480M_SRC>;
        clock-names = "hclk_host0", "hclk_host0_arb",
                      "usbphy0_480m";
        phys = <&u2phy0_host>;
        phy-names = "usb";
        power-domains = <&power RK3399_PD_PERIHP>;
            status = "disabled";
};

usb_host0_ohci: usb@fe3a0000 {
        compatible = "generic-ohci";
        reg = <0x0 0xfe3a0000 0x0 0x20000>;
        interrupts = <GIC_SPI 28 IRQ_TYPE_LEVEL_HIGH 0>;
        clocks = <&cru HCLK_HOST0>,
                 <&cru HCLK_HOST0_ARB>,
                 <&cru SCLK_USBPHY0_480M_SRC>;
        clock-names = "hclk_host0", "hclk_host0_arb",
                      "usbphy0_480m";
        phys = <&u2phy0_host>;
        phy-names = "usb";
        power-domains = <&power RK3399_PD_PERIHP>;
```

```
                status = "disabled";
};

usb_host1_ehci: usb@fe3c0000 {
                compatible = "generic-ehci";
                reg = <0x0 0xfe3c0000 0x0 0x20000>;
                interrupts = <GIC_SPI 30 IRQ_TYPE_LEVEL_HIGH 0>;
                clocks = <&cru HCLK_HOST1>,
                         <&cru HCLK_HOST1_ARB>,
                         <&cru SCLK_USBPHY1_480M_SRC>;
                clock-names = "hclk_host1", "hclk_host1_arb",
                              "usbphy1_480m";
                phys = <&u2phy1_host>;
                phy-names = "usb";
                power-domains = <&power RK3399_PD_PERIHP>;
                status = "disabled";
};

usb_host1_ohci: usb@fe3e0000 {
                compatible = "generic-ohci";
                reg = <0x0 0xfe3e0000 0x0 0x20000>;
                interrupts = <GIC_SPI 32 IRQ_TYPE_LEVEL_HIGH 0>;
                clocks = <&cru HCLK_HOST1>,
                         <&cru HCLK_HOST1_ARB>,
                         <&cru SCLK_USBPHY1_480M_SRC>;
                clock-names = "hclk_host1", "hclk_host1_arb",
                              "usbphy1_480m";
                phys = <&u2phy1_host>;
                phy-names = "usb";
                 power-domains = <&power RK3399_PD_PERIHP>;
                 status = "disabled";
};

&usb_host0_ehci {
        status = "okay";
};

&usb_host0_ohci {
        status = "okay";
};

&usb_host1_ehci {
        status = "okay";
};
```

```
&usb_host1_ohci {
        status = "okay";
};
```

5.2 USB2.0 HOST PHY 相关 DTS

```
grf: syscon@ff770000 {
        ……
        u2phy0: usb2-phy@e450 {
            ……
            u2phy0_host: host-port {
                #phy-cells = <0>;
                interrupts = <GIC_SPI 27 IRQ_TYPE_LEVEL_HIGH 0>;
                interrupt-names = "linestate";
                status = "disabled";
            };
        };

        u2phy1: usb2-phy@e460 {
            ……
            u2phy1_host: host-port {
                #phy-cells = <0>;
                interrupts = <GIC_SPI 31 IRQ_TYPE_LEVEL_HIGH 0>;
                interrupt-names = "linestate";
                status = "disabled";
            };
        };
};

&u2phy0 {
        ……
        u2phy0_host: host-port {
                phy-supply = <&vcc5v0_host>;
                status = "okay";
        };
};

&u2phy1 {
        ……
        u2phy1_host: host-port {
                phy-supply = <&vcc5v0_host>;
                status = "okay";
```

```
        };
};

vcc5v0_host: vcc5v0-host-regulator {
                compatible = "regulator-fixed";
                enable-active-high;
                // USB2 HOST VBUS 5V 的 GPIO 配置
                gpio = <&gpio4 25 GPIO_ACTIVE_HIGH>;
                pinctrl-names = "default";
                pinctrl-0 = <&host_vbus_drv>;
                regulator-name = "vcc5v0_host";
                regulator-always-on;
 };

&pinctrl {
        usb2 {
                host_vbus_drv: host-vbus-drv {
                //USB2 HOST VBUS 5V 的 GPIO pinctrl 配置
                rockchip,pins =
                      <4 25 RK_FUNC_GPIO &pcfg_pull_none>;
                };
        };
};
```