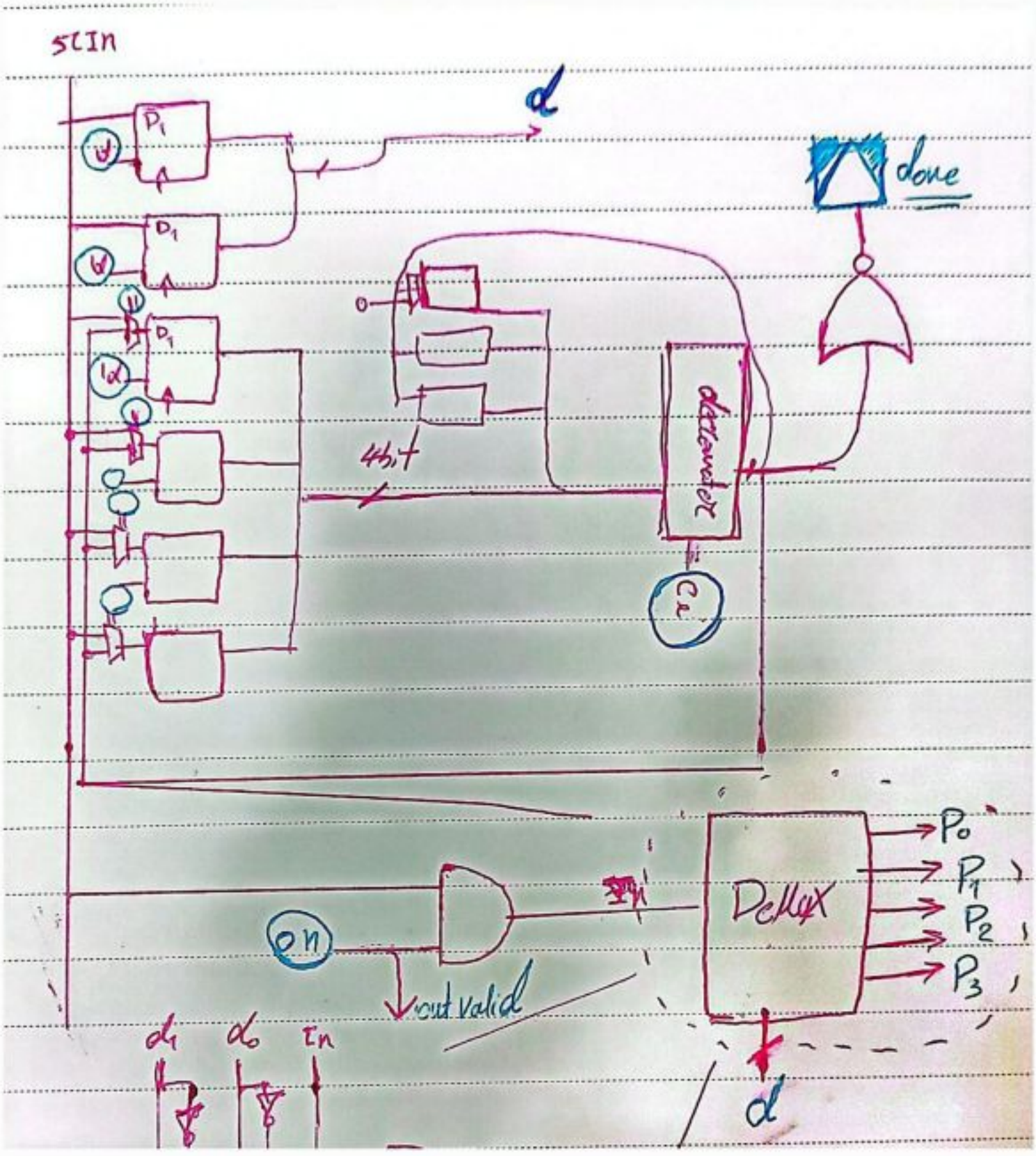
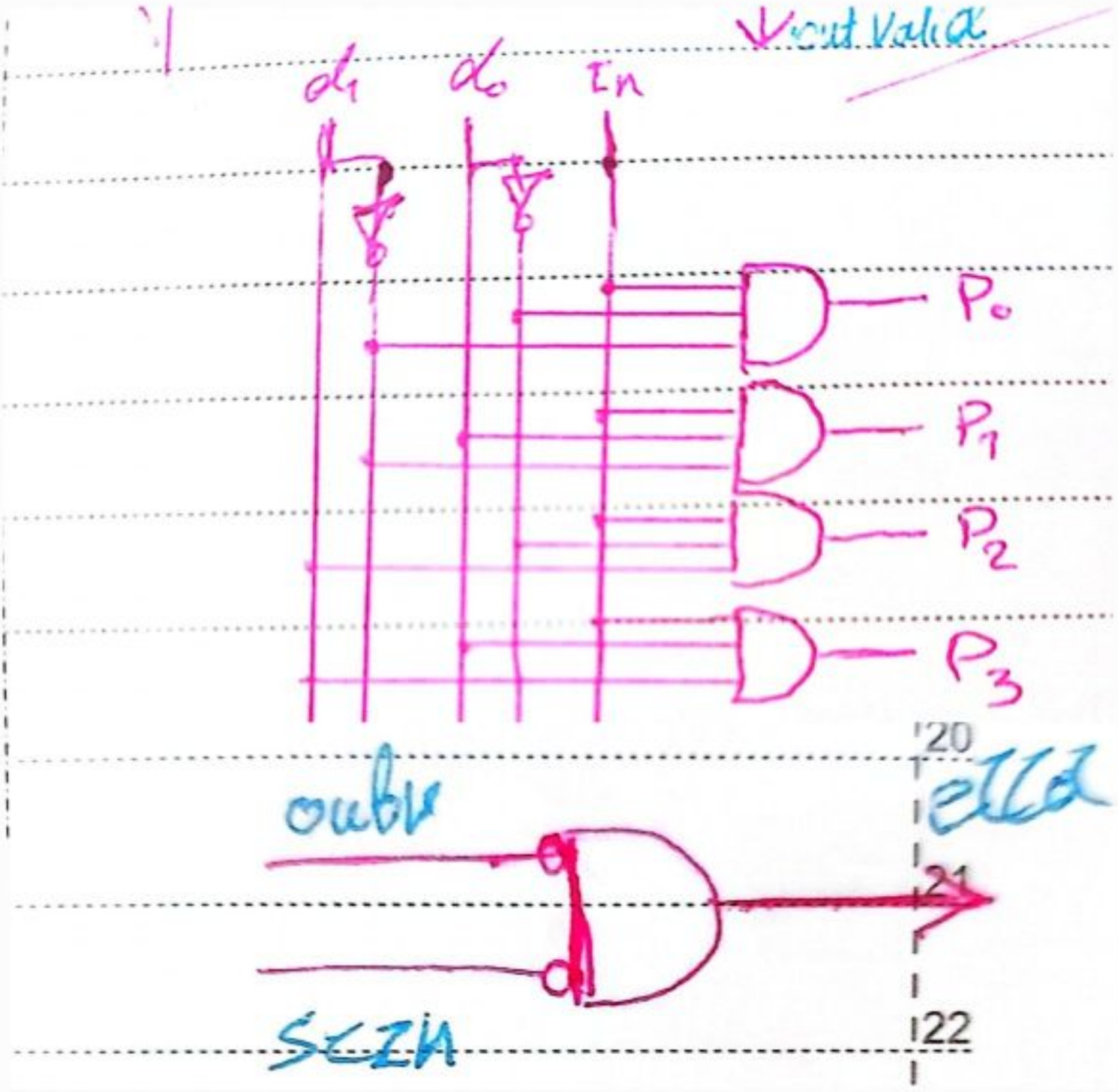
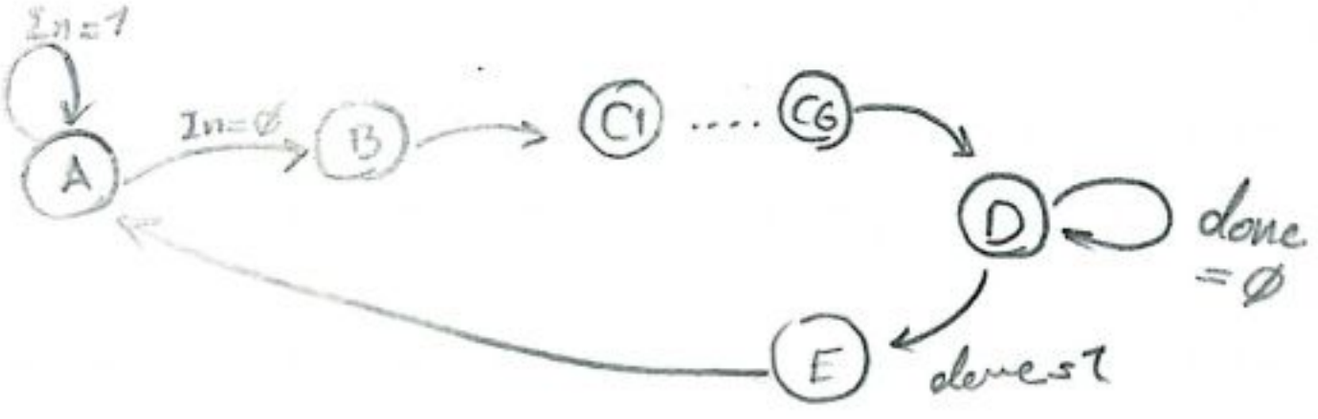
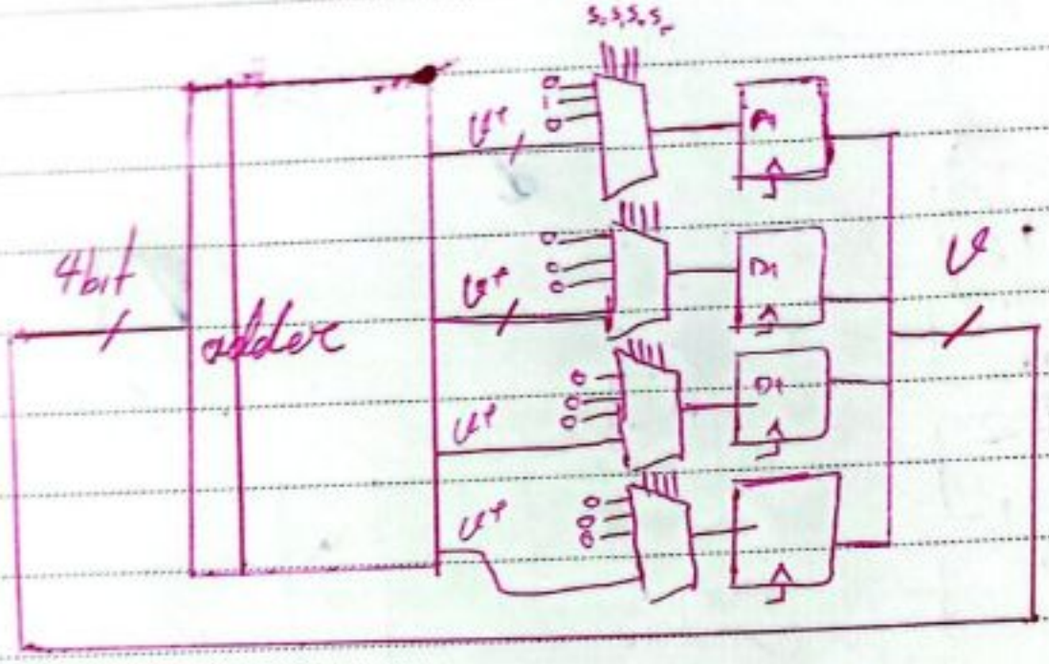
Simulation

A:




d_1
d_0
In
P_0
P_1
P_2
P_3
output
SCIN
120
121
122


In=1
In=0
A
B
C1
C6
D
E
done
=0
reset



S_0 e sain

S_1 e done

S_2 e

S_3 $S_1 S_2 S_0$

output ld_1 e=cool

ld_2 e=1

output ld_3 i $ld_5 = 1$

output

ON:

output

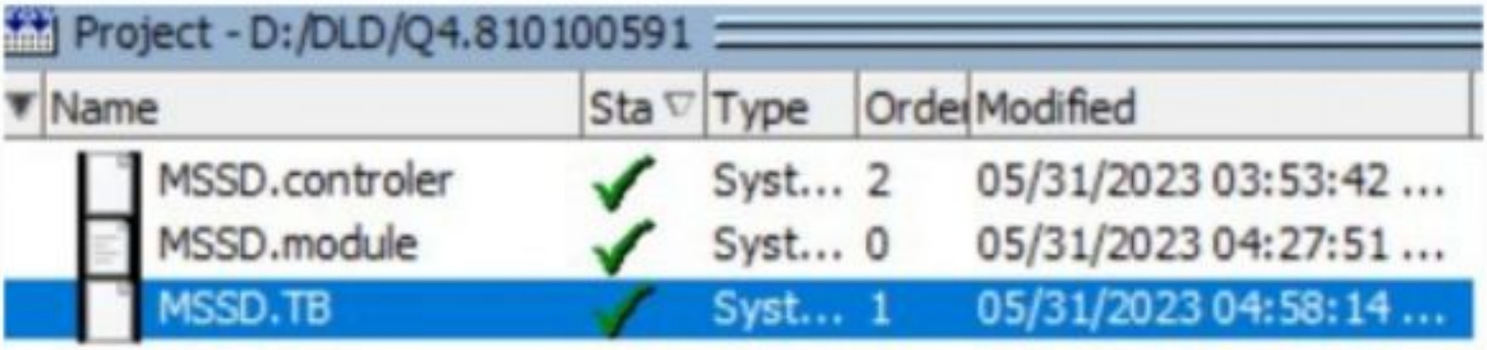
S_{03} e S_{13} → ON

$S_{IN} \equiv ON$

S_{04} e S_{05} e S_{06} e

در تصویر اول کلیت بخش **combinational** را میبینیم و تصویر دوم مولد خروجی **error** است.
مثلث های آبی سیگنال هایی هستند که ما به کنترلر مدار میفرستیم.
دایره های آبی سیگنال هایی هستند که کنترلر میفرستد.
تصویر سوم باز شده **Demultiplexer** است.
تصویر زیر مربوط به کنترلر **MSSD** است.
در کل ۹ **state** برای کنترلر داریم.

B:

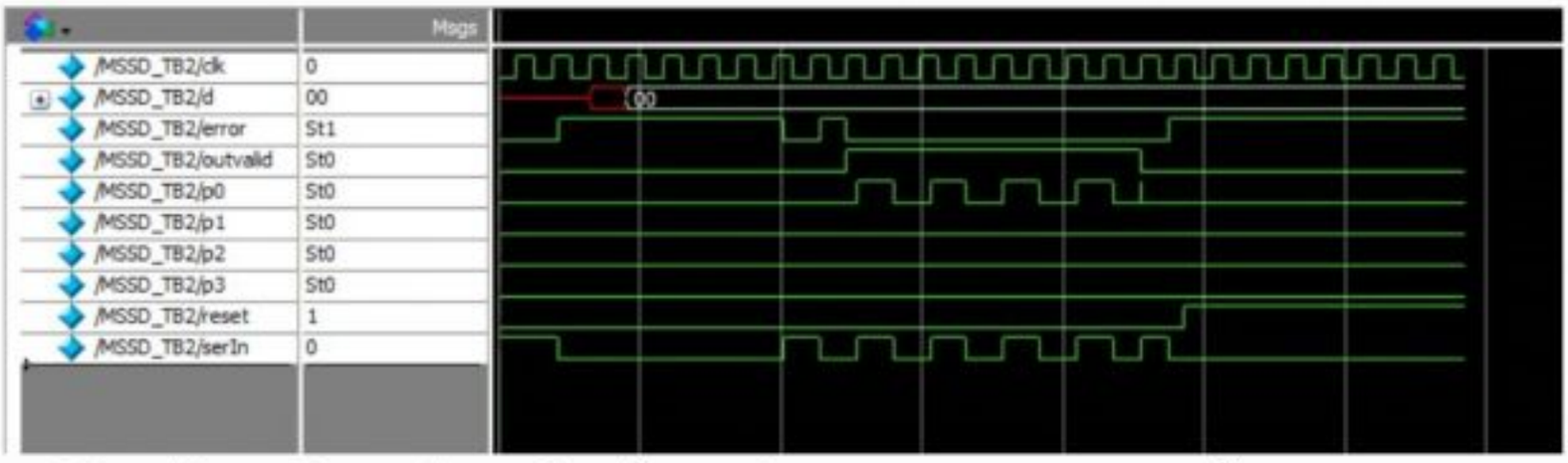


files:
MSSD.v
MSSD.CONTROL
MSSD.module

C:

```
`timescale 1ns/1ns

module MSSD_TB();
    logic CLK= 0;
    logic SERIN = 1;
    logic reset = 0;
    logic DONE, ON, CI, ERROR, OUTVAL, P0, P1, P2, P3;
    logic [3:0] PS;
    logic [1:6] LD;
    logic [3:6] S0, S1;
    logic [1:0] D;
    MSSD_combinational UUT(SERIN, CLK, CI, ON, LD, S0, S1, DONE, P0, P1, P2, P3, ERROR,OUTVAL, D);
    MSSD_controler UTT(reset, CLK, SERIN, DONE, LD, S0, S1, CI, ON, PS);
    initial repeat(1000) # 13 CLK = ~CLK;
    initial begin
            #43 SERIN = 1'b0;
            #159 SERIN = 1'b1;
            #26 SERIN = 1'b0;
            #26 SERIN = 1'b1;
            #26 SERIN = 1'b0;
            #26 SERIN = 1'b1;
            #26 SERIN = 1'b0;
            #26 SERIN = 1'b1;
            #26 SERIN = 1'b0;
            #26 SERIN = 1'b1;
            #26 SERIN = 1'b0;
            #19 SERIN = 1'b1;
            #20 SERIN = 1'b0;
            #10 reset = 1'b1;
            #200 $stop;
    end
endmodule
```



Netlist Synthesis (basic gates target)

A:

C:\Users\Digi Max\Desktop\New folder\yosys.exe

```
found and reported 0 problems.

yosys> dfflibmap -liberty mycells.lib

3. Executing DFFLIBMAP pass (mapping DFF cells to sequential cells from liberty file).
  cell DFF (noninv, pins=3, area=18.00) is a direct match for cell type $_DFF_P_.
  create mapping for $_DFF_N_ from mapping for $_DFF_P_.
  final dff cell mappings:
    DFF _DFF_N_ (.C(~C), .D( D), .Q( Q));
    DFF _DFF_P_ (.C( C), .D( D), .Q( Q));
    unmapped dff cell: $_DFF_NN0_
    unmapped dff cell: $_DFF_NN1_
    unmapped dff cell: $_DFF_NP0_
    unmapped dff cell: $_DFF_NP1_
    unmapped dff cell: $_DFF_PN0_
    unmapped dff cell: $_DFF_PN1_
    unmapped dff cell: $_DFF_PP0_
    unmapped dff cell: $_DFF_PP1_
    unmapped dff cell: $_DFFSR_NNN_
    unmapped dff cell: $_DFFSR_NNP_
    unmapped dff cell: $_DFFSR_NPN_
    unmapped dff cell: $_DFFSR_NPP_
    unmapped dff cell: $_DFFSR_PNN_
    unmapped dff cell: $_DFFSR_PNP_
    unmapped dff cell: $_DFFSR_PPN_
    unmapped dff cell: $_DFFSR_PPP_
Mapping DFF cells in module `\MSSD':
```

C:\Users\Digi Max\Desktop\New folder\yosys.exe

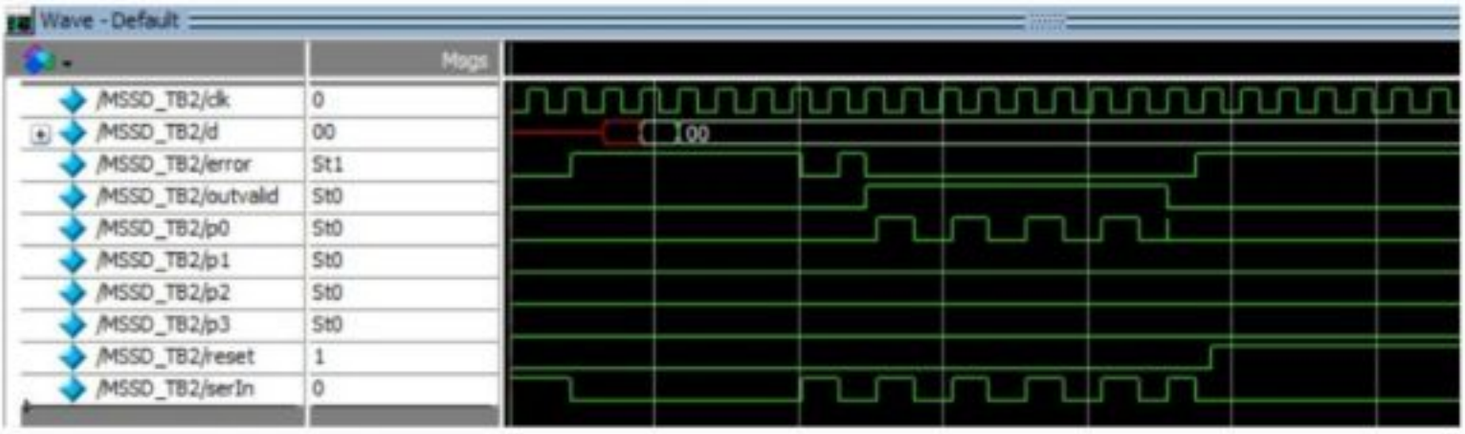
```
=== MSSD ===

   Number of wires:                113
   Number of wire bits:            137
   Number of public wires:          19
   Number of public wire bits:      43
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                126
     $_AND_                         9
     $_AOI3_                        4
     $_DFF_PP0_                     4
     $_DFF_P_                       9
     $_MUX_                        16
     $_NAND_                       17
     $_NOR_                        23
     $_NOT_                        16
     $_OAI3_                        4
     $_OAI4_                        1
     $_OR_                         13
     $_XNOR_                        9
     $_XOR_                         1

2.24. Executing CHECK pass (checking for obvious problems).
checking module MSSD..
found and reported 0 problems.
```

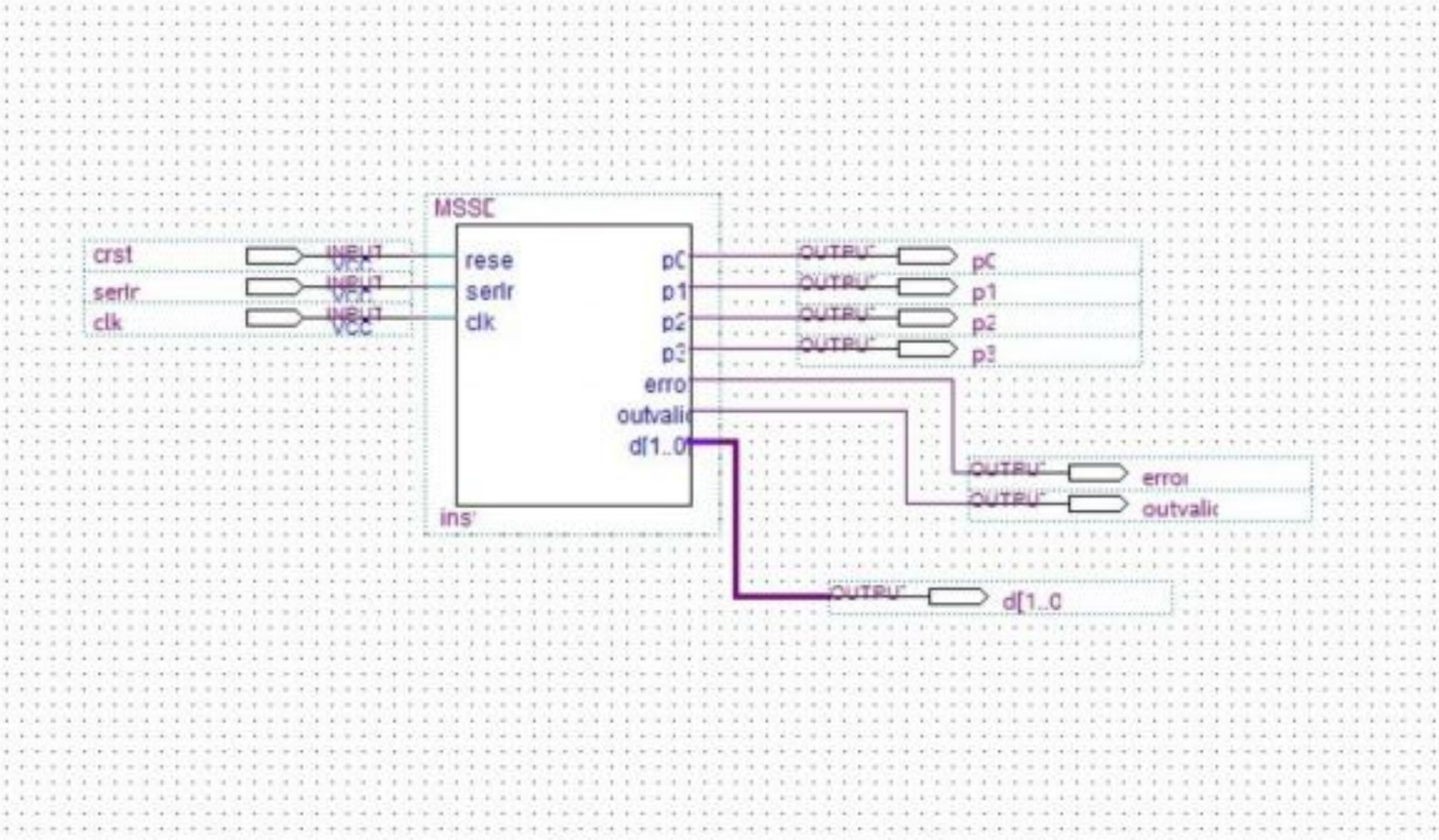
```
4.1.2. Re-integrating ABC results.
ABC RESULTS:                NAND cells:       35
ABC RESULTS:                 NOR cells:       57
ABC RESULTS:                 NOT cells:       28
ABC RESULTS:          internal signals:       94
ABC RESULTS:            input signals:       14
ABC RESULTS:           output signals:       19
Removing temp directory.
```

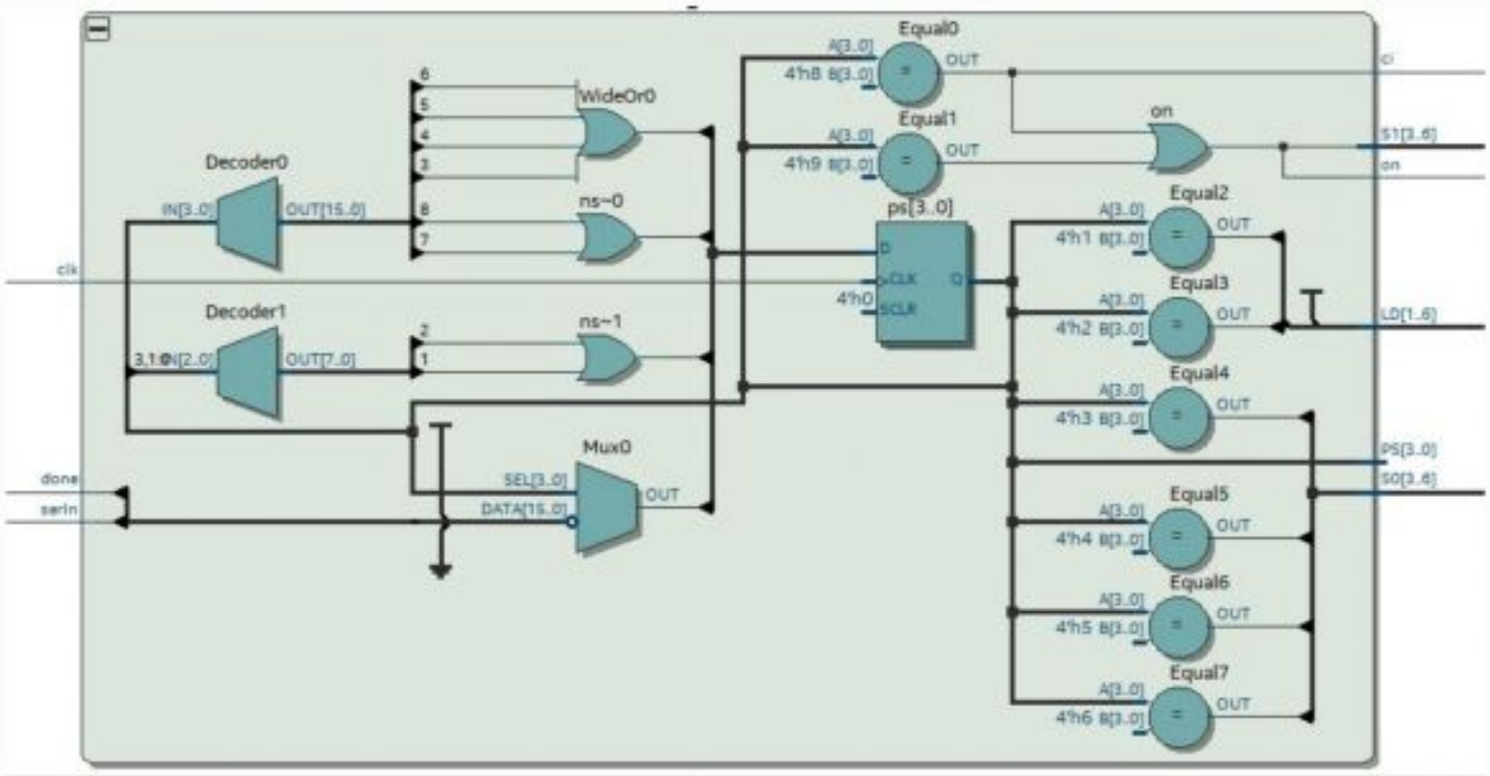
B:

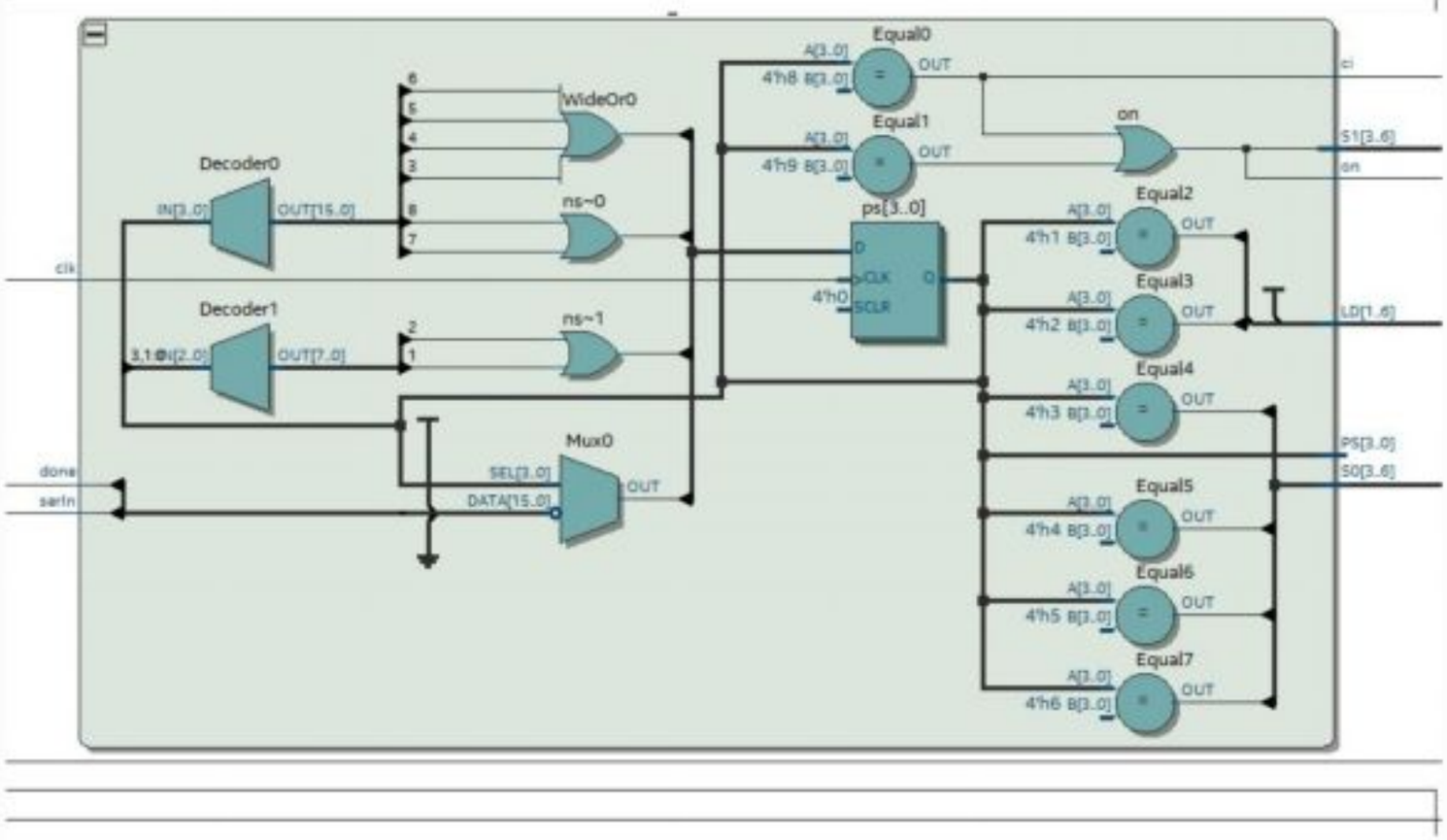


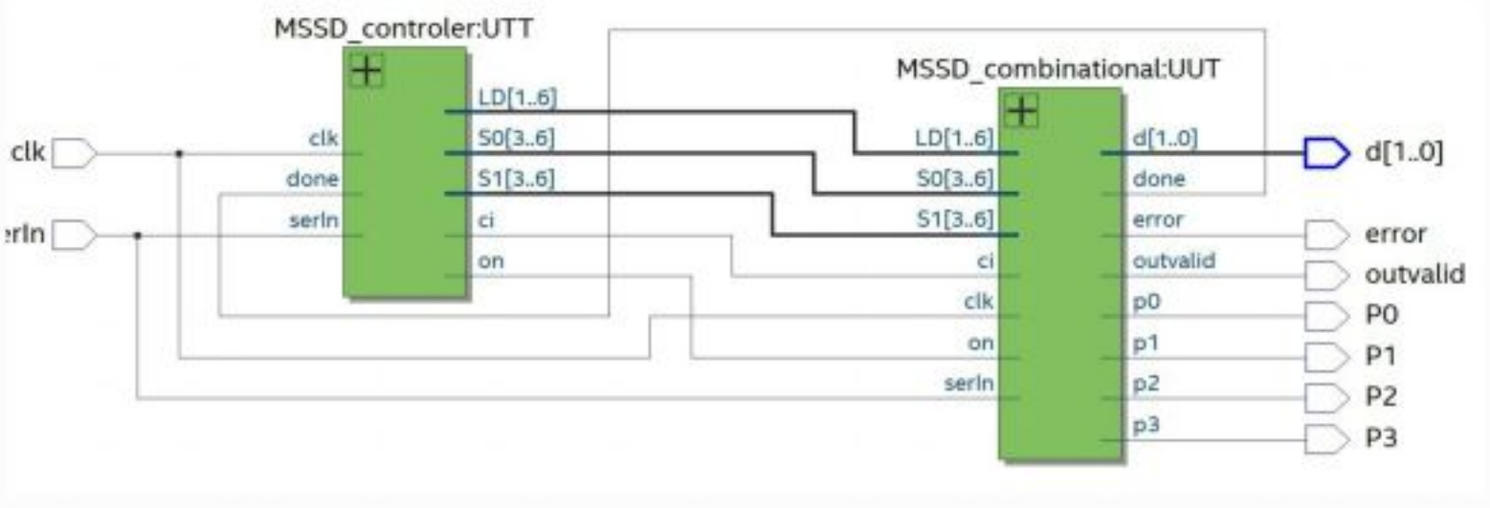
Synthesis and post–synthesis simulation (FPGA target)

C&D:

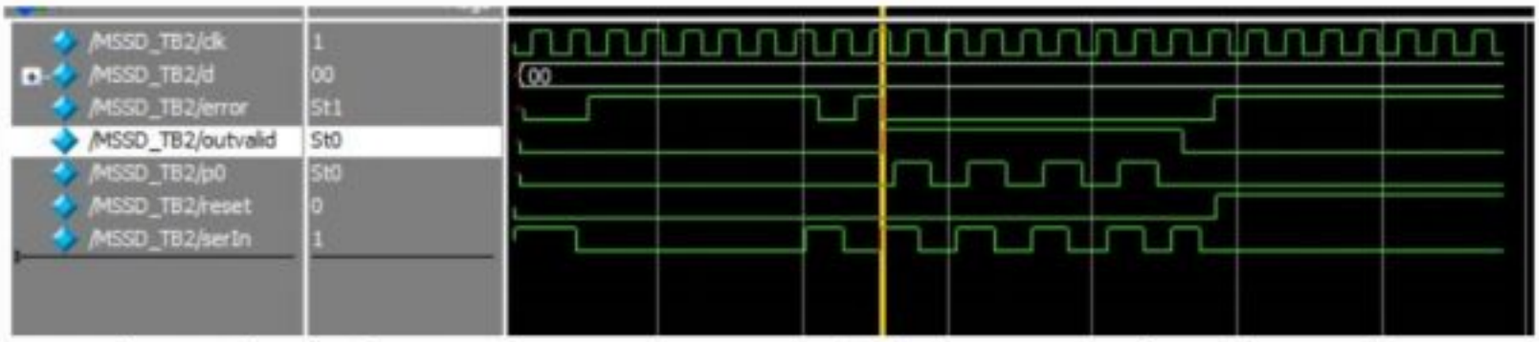



Equal0
Equal1
WideOr0
Decoder0
Decoder1
ns~0
ns~1
ps[3..0]
on
Equal2
Equal3
Equal4
Equal5
Equal6
Equal7
Mux0
clk
done
serIn
ci
S1[3..6]
LD[1..6]
PS[3..0]
S0[3..6]


Equal0
Equal1
WideOr0
Decoder0
Decoder1
ns~0
ns~1
ps[3..0]
on
Equal2
Equal3
Equal4
Equal5
Equal6
Equal7
Mux0
clk
done
serIn
ci
S1[3..6]
LD[1..6]
PS[3..0]
S0[3..6]


MSSD_controler:UTT
MSSD_combinational:UUT
clk
serIn
LD[1..6]
S0[3..6]
S1[3..6]
ci
on
done
d[1..0]
error
outvalid
P0
P1
P2
P3

E&F&G:



*مقادیر ناخواسته بسیار کمتری نسبت به مدل اولیه دارد.

*فلیپ فلاپ ها تاخیر دارند بیشتری دارند.

*مقادیر خروجی نیی با تاخیر از سر کلاک ظاهر میشوند.

که البته به مدل طبیعی یک مدار نزدیک تر است.