Optimizing PCB Thermal Performance for Cree® XLamp® LEDs

TABLE OF CONTENTS

INTRODUCTION

This Cree application note outlines a technique to assist with the development of cost-effective thermal management for the XT, XP, XB, MX and ML families of XLamp® LEDs.

One of the most critical design parameters for an LED illumination system is the system's ability to draw heat away from the LED junction. High operating temperatures at the LED junction adversely affect the performance of LEDs, resulting in decreased light output and lifetime.[1] To properly manage this heat, specific practices should be followed in the design, assembly and operation of LEDs in lighting applications.

This application note outlines a technique for designing a low-cost printed circuit board (PCB) layout that optimizes the transfer of heat from the LED. The technique involves the use of FR-4-based PCBs, which cost less than metal core printed circuit boards (MCPCB), but have greater thermal resistance. The use of metal-lined holes or vias underneath LED thermal pads is a method to dissipate heat through an FR-4 PCB and into an appropriate heat sink.

Cree XLamp LEDs are designed with an electrically isolated thermal path. Cree pioneered this LED feature almost ten years ago to enable the use of metalized vias in FR-4 PCBs. For certain illumination systems design, thermal vias enable the use of FR-4 circuit boards instead of metal core circuit boards. This can deliver system cost savings in circuit board and heat sink selection.

This application note serves as a practical guideline based on heat transfer fundamentals and includes suggestive, but not definitive, simulation and measurement data. Cree advocates this technique as appropriate design for certain lighting applications and encourages Cree's customers to evaluate this option when considering the many thermal management techniques available. For additional guidelines on LED thermal management, refer to the Thermal Management application note.

1 See the Long-Term Lumen Maintenance application note.

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THERMAL MANAGEMENT PRINCIPLES

The technique in this application note is not recommended for Cree LEDs that consume more than 5 W of power, including MC-E, MP-L and MT-G. For low power applications, this technique can be used for XM-L and XM-L EZW LEDs.

XLamp LED Thermal Characteristics

All XLamp LED packages have an electrically isolated thermal pad. The pad provides an effective channel for heat transfer and optimizes thermal resistance from the LED chip junction to the thermal pad. The pad is electrically isolated from the anode and cathode of the LED and can be soldered or attached directly to grounded elements on the board or heat sink system.

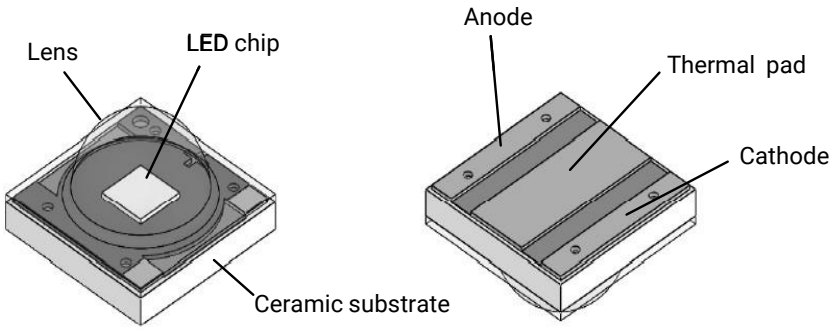

Figure 1: Cree XLamp XP LED package

Heat is conducted from the LED package through the thermal pad and into a PCB that should be mounted to a heat sink to transfer the conducted heat into the operating environment.[2]

Tables 1 and 2 list typical thermal resistance values (junction to solder point) for various XLamp series LEDs.

Table 1: Typical thermal resistance values for Cree XLamp white LEDs

Color	Thermal Resistance (°C/W)													
	ML-B	ML-C	ML-E	MX-3	MX-6	XB-D	XM-L	XM-L EZW	XM-L HVW	XP-C	XP-E	XP-G	XT-E	XT-E HVW
White (cool, neutral, warm)	25	13	11	11	5	6.5	2.5	2.5	3.5	12	9	4	5	6.5

Table 2: Typical thermal resistance values for Cree XLamp color LEDs
n/a indicates an LED that Cree does not offer

Color	Thermal Resistance (°C/W)		
	ML-E	XP-C	XP-E
Royal blue	n/a	12	9
Blue	11	12	9
Green	15	20	15
Amber	n/a	15	10
Red	15	10	10
Red-orange	n/a	10	10

2 For subsequent discussion and simulation in this document, we assume the PCB is mounted to an infinite heat sink that maintains the back side of the board at 25 °C.

PCB Thermal Characteristics

FR-4

FR-4 is one of the most commonly used PCB materials and is the National Electrical Manufacturers Association (NEMA) designation for a flame retardant, fiberglass-reinforced epoxy laminate. A by-product of this construction is that FR-4 has very low thermal conductivity. Figure 2 below shows a typical cross-sectional geometry for a two-layer FR-4 board.

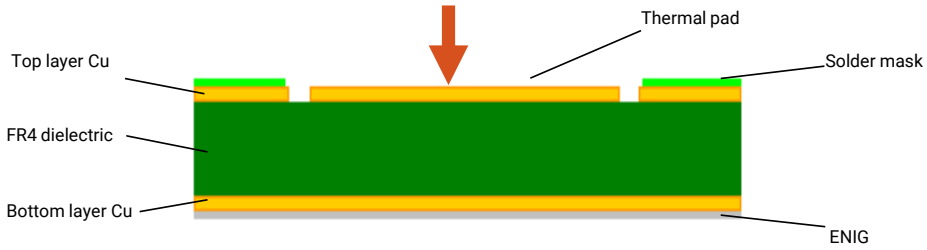

Figure 2: FR-4 cross-sectional geometry (not to scale)

Using the thermal conductivity values in Table 3 below, the total thermal resistance for an FR-4 board can be calculated by adding the thermal resistances of the layers.

$$\theta_{PCB} = \theta_{layer1} + \theta_{layer2} + \theta_{layer3} \ldots + \theta_{layerN} \quad (1)$$

For a given layer the thermal resistance is given by the formula:

$$\theta = l / (k \times A) \quad (2)$$

where l is the layer thickness, k is the thermal conductivity, and A is the area normal to the heat source.

For a 1.6-mm thick star board approximately 270 mm^2, the calculated through-plane thermal resistance is approximately 30 °C/W. Bear in mind that this calculation is one-dimensional and does not account for the size of the heat source, spreading, convection thermal resistances or boundary conditions. If a smaller heat source size is considered, for example 3.3 mm x 3.3 mm, the resulting one-dimensional thermal resistance increases to over 700 °C/W.

Table 3: Typical thermal conductivities of FR-4 board layers

Layer/Material	Thickness (µm)	Thermal conductivity (W/mK)
SnAgCu solder	75	58
Top layer copper	70	398
FR-4 dielectric	1588	0.2
Bottom layer copper	70	398
Electroless Nickel/Immersion Gold (ENIG)	5	4.2

Metal-Core Printed Circuit Board

A simple one-layer MCPCB is comprised of a solder mask, copper circuit layer, thermally conductive dielectric layer, and metal core base layer, as shown below in Figure 3. These three layers are laminated and bonded together, providing a path for the heat to dissipate. Often the metal substrate is aluminum, though steel and copper can also be used.

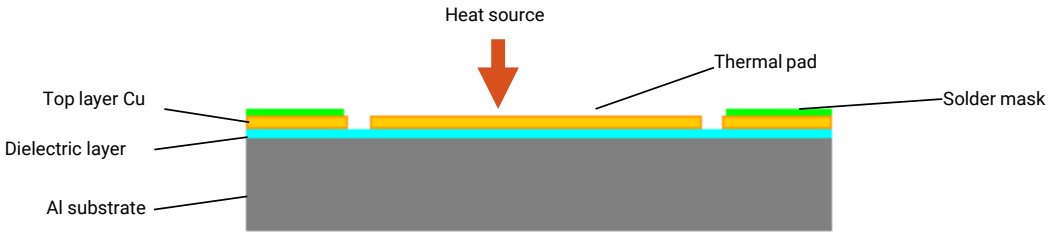

Figure 3: MCPCB cross-sectional geometry (not to scale)

Using the thermal conductivity values in Table 4 below, the one-dimensional through-plane thermal resistance for a 1.6-mm-thick star board of approximately 270 mm^2 is roughly 0.2 °C/W. If a smaller heat source size is considered, the resulting thermal resistance is 5.3 °C/W. In this case, the limiting factor is the PCB dielectric.

Table 4: Typical thermal conductivities of MCPCB layers

Layer/Material	Thickness (µm)	Thermal conductivity (W/mK)
SnAgCu solder	75	58
Top layer copper	70	398
PCB dielectric	100	2.2
Al plate	1588	150

Designing Thermal Vias

An inexpensive way to improve thermal transfer for FR-4 PCBs is to add thermal vias - plated through-holes (PTH) between conductive layers. Vias are created by drilling holes and copper plating them, in the same way that a PTH or via is used for electrical interconnections between layers.

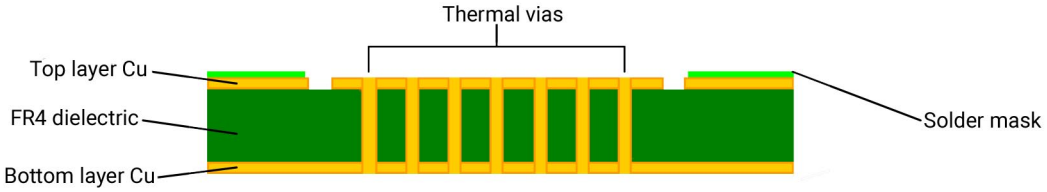

Figure 4: FR-4 cross-sectional geometry with thermal vias (not to scale)

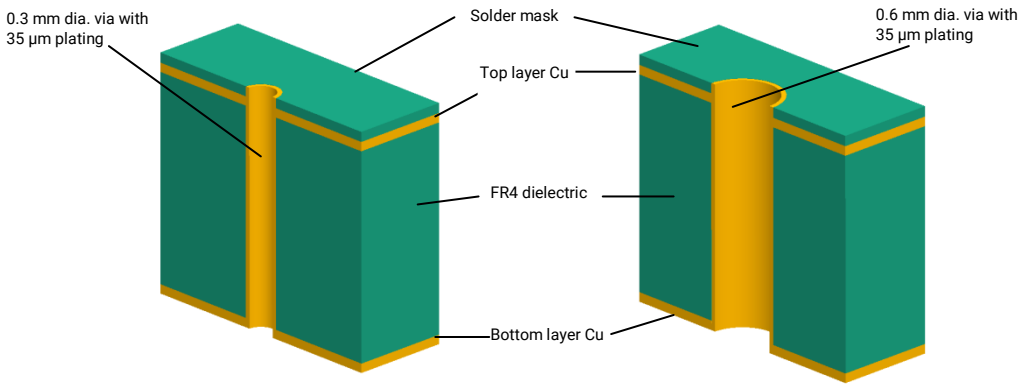

Figure 5: Cross-sectional geometry of small and large thermal vias in FR-4 substrate

Adding vias in an appropriate way will improve the thermal resistance of an FR-4 board. The thermal resistance of a single via can be calculated by the same formula, $\theta = l / (k \times A)$. Using the values in Table 5, a single solder-filled via with a diameter of 0.6 mm results in $(1.588 \times 10^{-3}) / (58 \times (\pi \times (0.5 \times 0.6 \times 10^{-3})^2)) = 96.8$ °C/W. However, when N vias are used, the area increases by a factor of N_{vias}, resulting in:

$$\theta_{vias} = l / (N_{vias} \times k \times A) \quad (3)$$

Note that this is applicable only if the heat source is directly normal to the thermal via; otherwise, the resistance increases due to thermal spreading effects. To calculate the total thermal resistance for the region underneath (or normal to) the LED thermal pad, the equivalent thermal resistance for the dielectric layer and vias must be determined. For simplicity, the two resistances are treated as parallel applying this formula.

$$\theta_{vias \,||\, FR\text{-}4} = [\,(1/\theta_{vias}) + (1/\theta_{FR\text{-}4})\,]^{-1} \quad (4)$$

Using the values in Table 5, for a 270 mm² board with five 0.6-mm-diameter solder-filled vias results in an approximate thermal resistance of 12 °C/W, a 60% improvement over the initial 30 °C/W derived from the data in Table 3.

Table 5: Typical thermal conductivities of FR-4 board layers including thermal vias

Layer/Material	Thickness (µm)	Thermal conductivity (W/mK)
SnAgCu solder	75	58
Top-layer copper	70	398
FR-4	1588	0.2
Filled vias (SnAgCu)	1588	58
Bottom-layer copper	70	398
Solder mask (optional)	25	0.2

Open Vias vs. Filled Vias

Open vias result in a higher thermal resistance than filled vias because the area normal to the heat source is reduced per the formula:

$$A = \pi \times (D \times t - t^2) \quad (5)$$

where D is the via diameter and t is the plating thickness.

For a 0.6-mm diameter via with 35 µm (1 oz.) copper plating, the area normal to the thermal pad is only 0.06 mm^2 compared to 0.28 mm^2 for a solder-filled via, resulting in a thermal resistance of 64 °C/W per via compared to 42 °C/W if filled with solder or 14 °C/W if filled completely with copper.

In general, increasing plating thickness during PCB production improves the thermal resistance of vias. In the example above, increasing the plating thickness to 70 µm (2 oz.) lowers the thermal resistance to 34 °C/W per via. Consult your PCB manufacturer to determine if thicker plating is feasible.

Non-filled vias may become filled with solder during reflow. However, depending on a number of factors, this may not occur reliably and as a result, the vias will conduct heat less effectively.

An option to creating a solid via during the plating process in PCB production is to fill the vias with a thermally conductive material such as epoxy as part of the PCB fabrication process. This adds an additional step to fabrication and may increase the cost of the board.

Solder voiding in open PTH vias

Figure 6 shows an example of unfilled vias after reflow. Figure 7 shows an example of solder voids underneath the device (shown in red). The voids increase the thermal resistance of the thermal interface. Also, the solder may overfill the hole leading to bumps on the bottom of the board that can reduce the contact area between the board and the heat sink.

Steps can be taken to limit the amount of solder wicking. One way is to maintain a via diameter smaller than 0.3 mm. With smaller vias, the surface tension of the liquid solder inside the via is better able to counter the force of gravity on the solder. If the via structure is constructed following the guideline above, holding the inside via diameter to around 0.25 mm – 0.3 mm, minimal solder wicking is achieved. The drawback to this approach is that smaller open vias result in a higher overall thermal resistance.

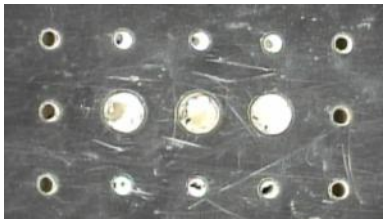

Figure 6: Unfilled vias

Figure 7: Solder voiding (not to scale)

Another technique for limiting solder wicking involves using solder mask to restrict the flow of solder from the top side of the PCB to the bottom side. One process, called tenting, uses solder mask to prevent solder from either entering or exiting the thermal vias, depending on the side of the board on which the solder mask is placed. Tenting the bottom side with solder mask to cover and plug the thermal vias can prevent solder from flowing down into the vias and onto the bottom of the board. In top-side via tenting, small areas of solder mask are placed over the thermal vias on the top side of the PCB to prevent solder from flowing into the vias from the top side of the board.

Figure 8: Tented vias with bottom-side solder mask (not to scale)

THERMAL PERFORMANCE SIMULATIONS

This section presents results obtained from computational thermal analysis for a series of PCB configurations.[3]

Surface Thermal Dissipation

The first configuration, shown in Figure 9, consists of a star FR-4 PCB with varying widths of the thermal pad and two board thicknesses (0.8 mm and 1.6 mm); the bottom copper layer is solid and there are no thermal vias.

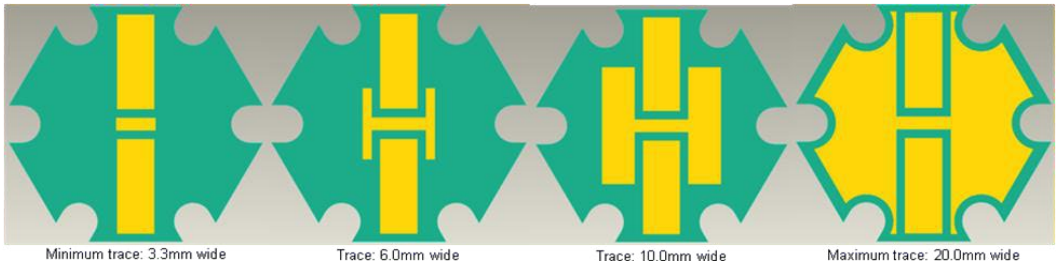

Figure 9: Variation in thermal pad width on top side of PCB

The analysis results in Chart 1 show that, for the 1.6-mm thick board, increasing the thermal pad width beyond 12 mm provides little improvement and, for the 0.8-mm thick board, improvement diminishes beyond a 16-mm width.

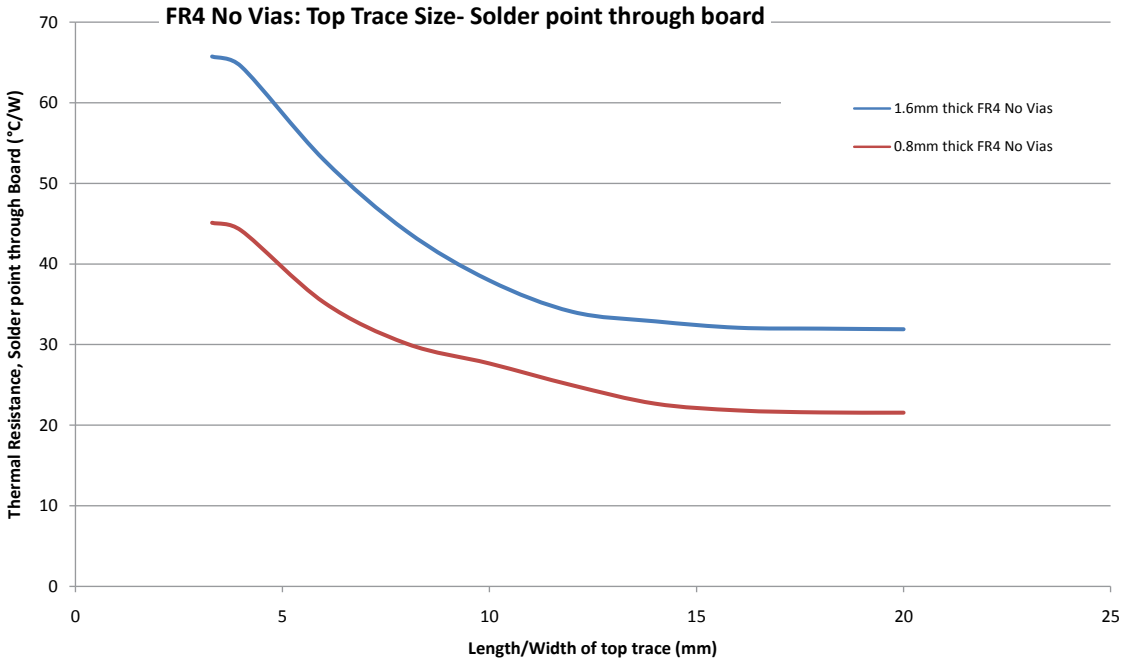

Chart 1: Thermal resistance for FR-4 PCB with no vias with varying thermal pad size

The next configuration is the same as the first except the board is an MCPCB. Chart 2 shows there is little benefit to extending the thermal pad width beyond 6 mm for either board thickness.

3 Cree used Ansys Design Space, www.ansys.com/products/structural-mechanics/products.asp

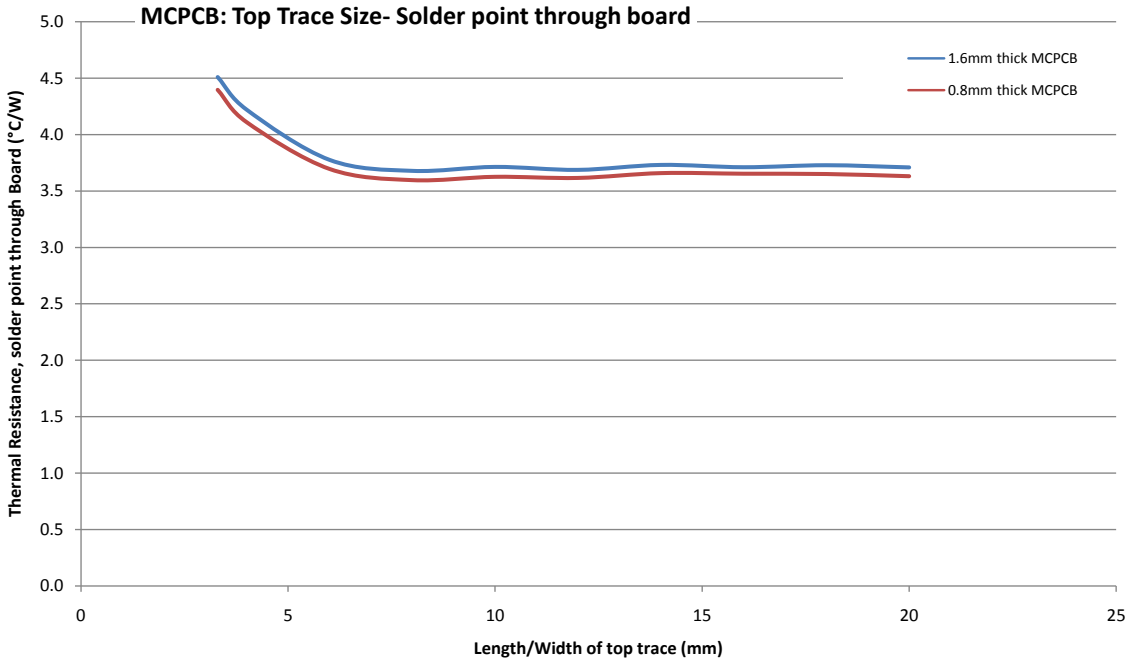

Chart 2: Thermal resistance for MCPCB with varying thermal pad size

Thermal Dissipation with Vias

Chart 3 shows the effects of various filling materials for 0.7-mm diameter vias with 1-mm center-to-center spacing for both 1.6-mm and 0.8-mm board thicknesses, shown in Figure 10. The analysis data indicate solid copper filled vias result in lower thermal resistance and unfilled vias deliver higher thermal resistance. A via filled with conductive epoxy performs only slightly better than an unfilled via.

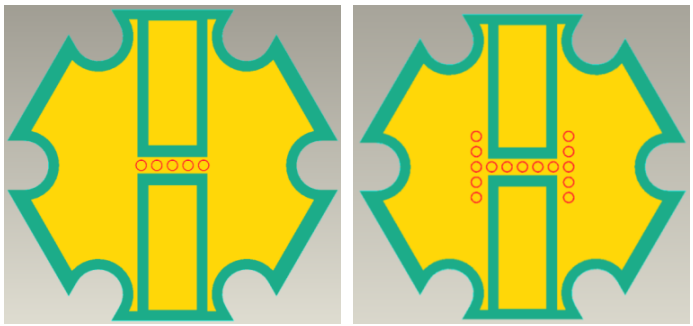

Figure 10: FR-4 board with five and fifteen 0.7-mm-diameter vias and 1-mm pitch

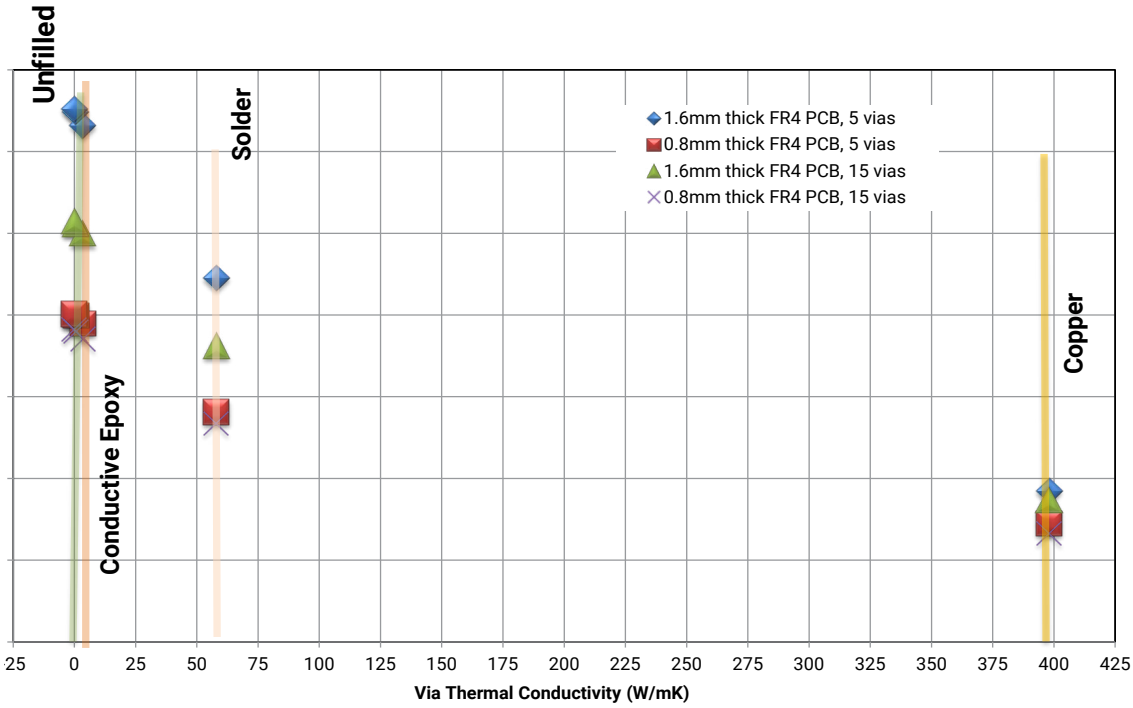

Chart 3: Thermal resistance for FR-4 vias filled with materials of differing conductivity

Chart 4 shows the effect of changing the diameter and number of vias. This chart assumes the vias are filled with SnAgCu solder. As expected, the larger the diameter of the via, the lower the thermal resistance becomes. Increasing the number of vias shows considerable improvement for smaller via diameters.

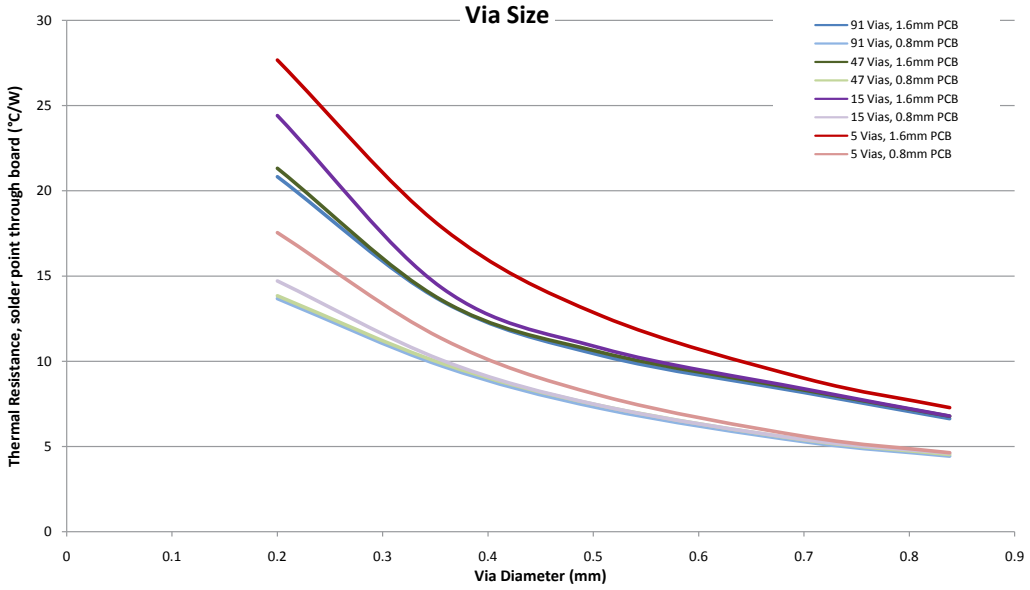

Chart 4: FR-4 PCB with various via diameters and numbers of vias

The next case considers the effect of varying the number of thermal vias as shown in Figure 11. These vias are solid-plated copper with a diameter of 0.254 mm (0.010 in.) and center-to-center spacing of 0.635 mm (0.025 in.). The results in Chart 5 indicate that increasing the number of vias beyond fourteen shows little improvement. (This is the maximum achievable density of the area normal to the LED thermal pad.)

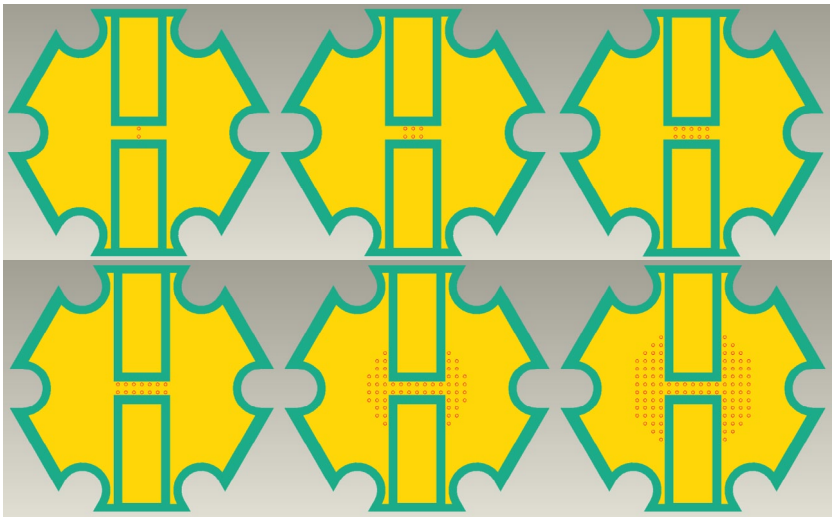

Figure 11: FR-4 board with varying numbers of thermal vias (2, 6, 8, 14, 58, and 102)

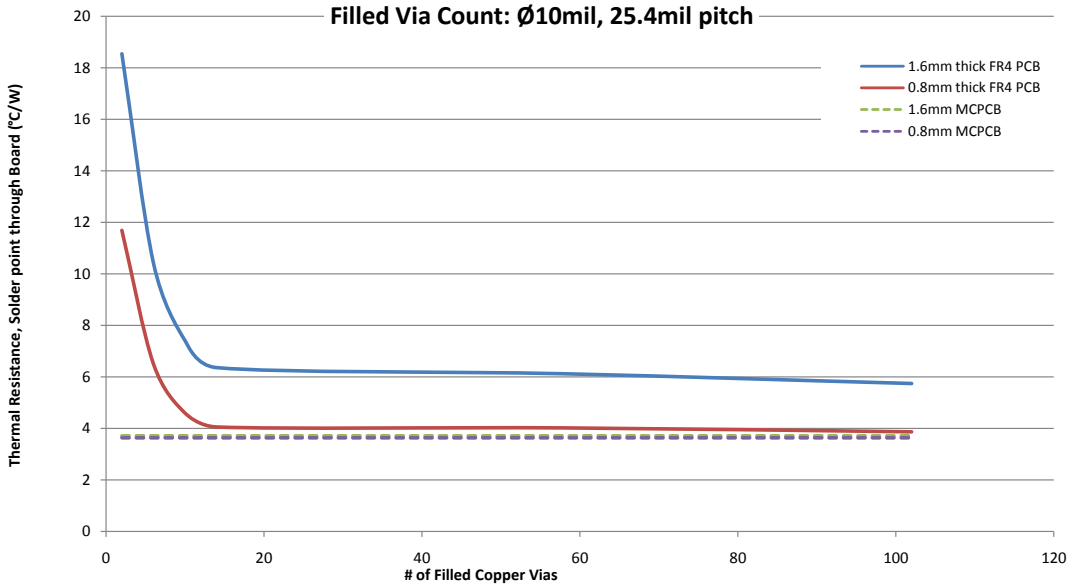

Chart 5: Thermal resistance values FR-4 board for varying numbers of copper-filled thermal vias

Combined Surface and Via Studies

The next configuration is an FR-4 PCB with fourteen 0.254-mm diameter copper plated vias with the thermal pad widths shown in Figure 12. The bottom copper layer is solid. The data in Chart 6 show that, beyond a 6-mm width, there is little improvement in thermal resistance.

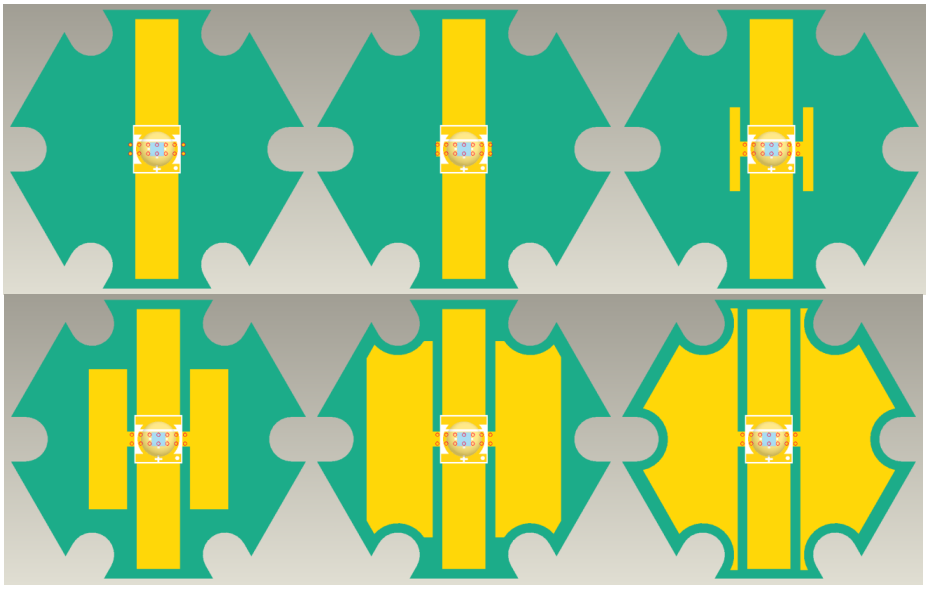

Figure 12: FR-4 PCB with 14 thermal vias and varying top thermal pad widths (3.3, 4.0, 6.0, 10.0, 14.0, 20.0 mm)

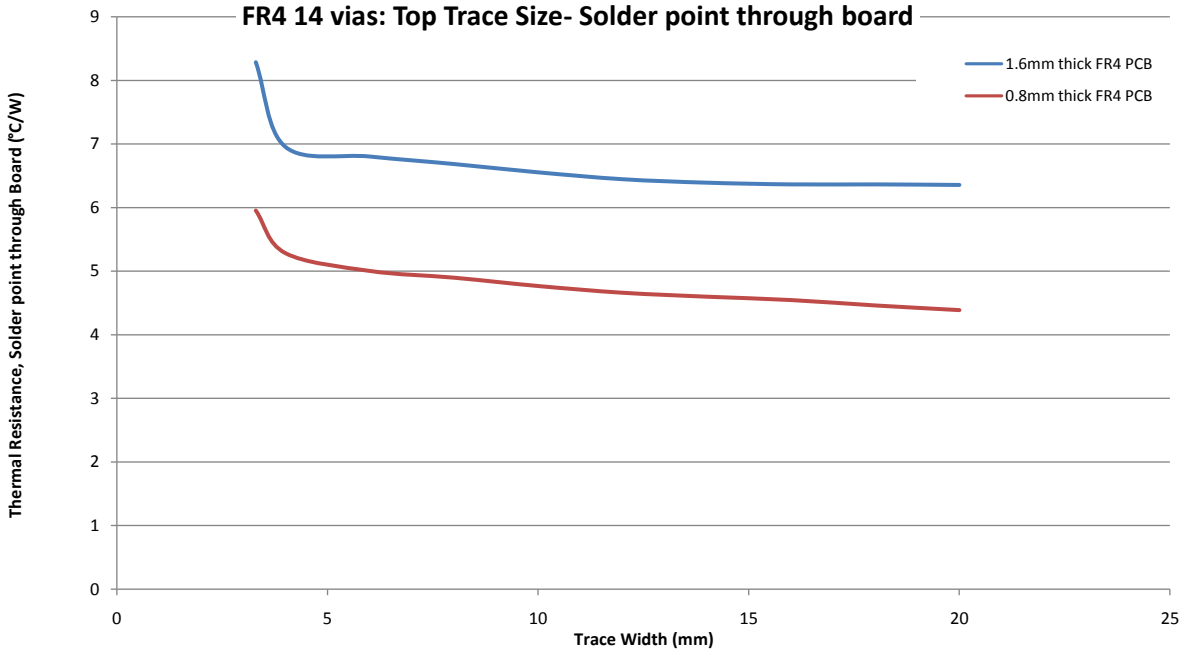

Chart 6: Thermal resistance of FR-4 PCB with 14 vias and varying thermal pad widths

Finally, the previous scenario is repeated with the bottom thermal pad widths shown in Figure 13. The results, shown in Chart 7, indicate that there is a small difference in thermal resistance that decreases as the width of the bottom pad increases.

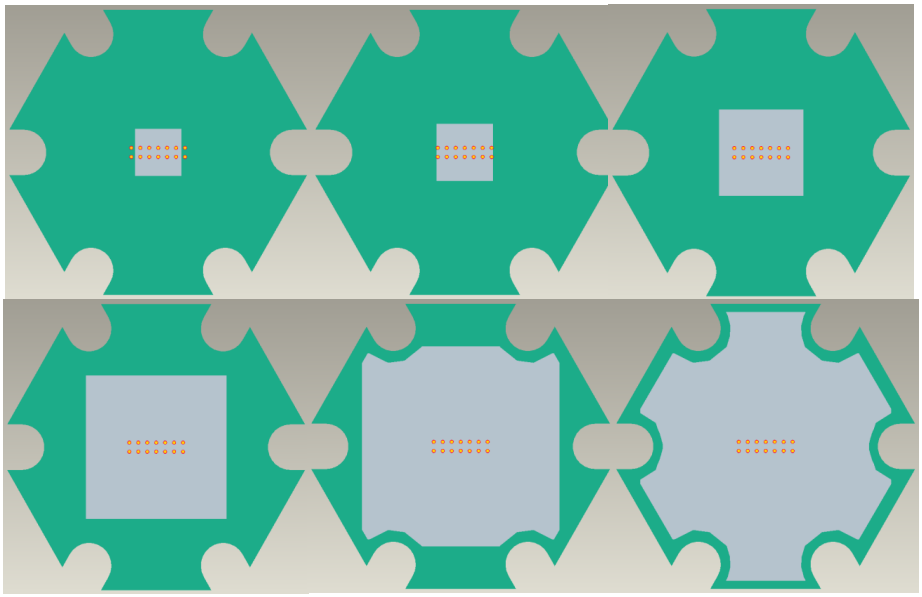

Figure 13: FR-4 PCB with 14 thermal vias and varying bottom thermal pad widths (3.3, 4.0, 6.0, 10.0, 14.0, 20.0 mm)

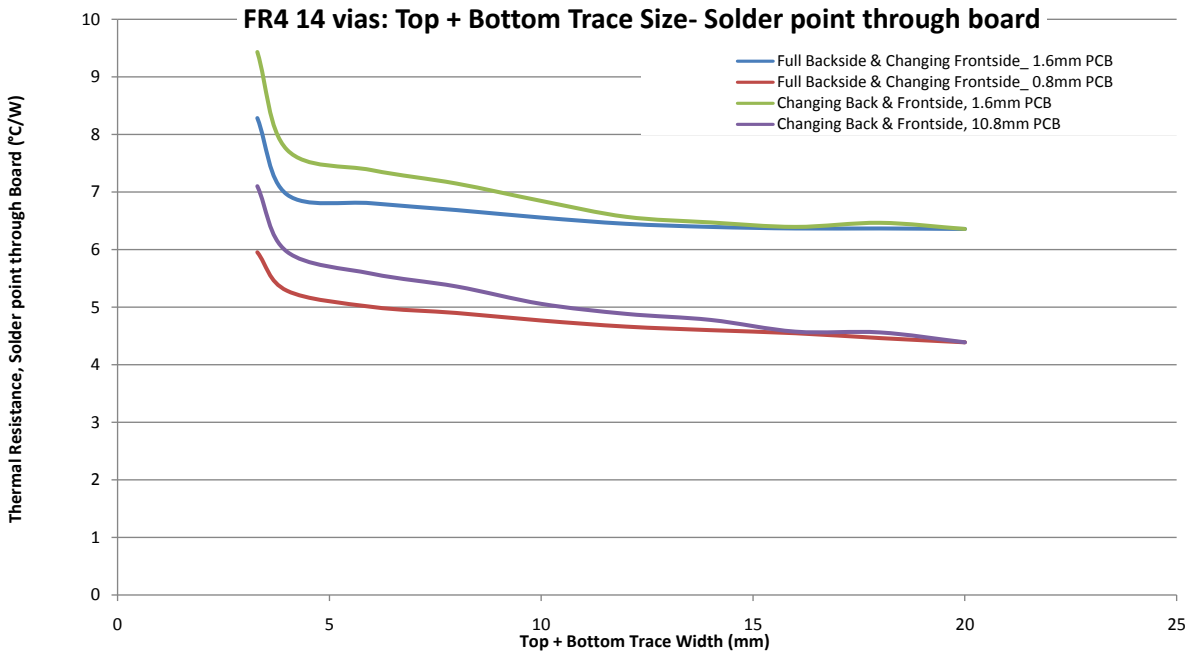

Chart 7: Thermal resistance of FR-4 PCB with 14 vias and varying top and bottom thermal pad widths

Summary Results of Thermal Simulations

1. The results from the various simulations show that the dielectric thickness should be 0.8 mm to achieve the lowest possible thermal resistance for an FR-4 board.

2. Although making the vias as large as possible reduces thermal resistance, the cost of manufacturing the board must also be considered. Larger unfilled vias introduce the possibility of the vias becoming partially filled during the soldering process. Smaller, closely spaced vias are a better solution.

3. Finally, adding additional vias and increasing the width of the thermal pad beyond a certain point have diminishing returns because of thermal spreading resistance.

Based on these conclusions, on page 15 Cree recommends an optimal thermal pad size, via size and spacing that is both thermally effective and manufacturable.

TEMPERATURE VERIFICATION MEASUREMENTS

Because LED junction temperature affects LED lifetime, Cree recommends performing a thermal verification test on the LED-board assembly under real-life conditions.[4]

This section illustrates practical LED board thermal measurement using thermocouples, which offers some corroboration for the simulations on which we base our recommendations.

Figure 14 shows a type-K thermocouple attached to the top copper layer close to the thermal pad. The solder mask (if present) should be removed to solder the thermocouple to the board. Alternately the thermocouple can be attached using a thermal epoxy or aluminum tape. If more than one LED is on the board, the lamp with the highest expected temperature should be selected. Another thermocouple is attached to the back of the heat sink using thermal epoxy. A third thermocouple is used to measure the ambient (air) temperature.[5] The thermocouple wires are held in place with Kapton® tape. To calculate the actual heat sink to ambient thermal resistance, divide the difference between Ths and Ta by the power of the heat source.

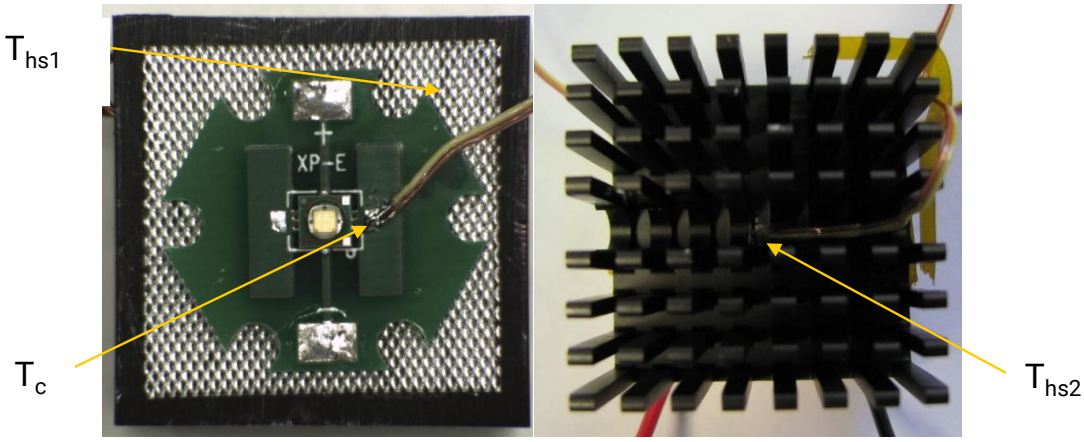

Figure 14: Thermocouple placement

Table 6 below contains data from five sets of five XLamp XP-E LEDs mounted on star boards. The first four sets are 1.6-mm thick FR-4 boards with via layouts similar to Figure 12 and Figure 13 with 10-mm wide bottom thermal pads; the last set is 1.6-mm thick aluminum clad boards. The PCBs were mounted to a heat sink with thermal adhesive.[6] Measurements of the forward voltage (V_f) and

4 Normally the junction temperature cannot be measured directly and must be derived from the temperature measured at a reference point on the top copper layer.
5 At least 2 mm away from the heat sink and/or illumination source and not in the path of illuminance.
6 Aavid Thermalloy part number 374424B00035G, with Chomerics THERMATTACH® T411 thermal tape for FR-4; CTS Electronics part number BDN10-5CB/A01for MCPCB

case temperature (T_c) were taken at 700 mA (I_f) at an ambient temperature of 20 °C (T_a). With these measurements, the power (P), PCB thermal resistance (θ_{pcb}), case to ambient thermal resistance (θ_{ca}), and heat sink to ambient thermal resistance (θ_{hs-a}) can all be calculated per the following equations.

$$P = I_f * V_f \quad (6)$$

$$\theta_{pcb} = (T_c - T_{hs}) / P \quad (7)$$

$$\theta_{ca} = (T_c - T_a) / P \quad (8)$$

$$\theta_{pcb} = (T_{hs} - T_a) / P \quad (9)$$

Table 6: PCB temperature measurements

Board	If (A)	Vf (V)	Power (W)	Tc (°C)	Ths (°C)	Ta (°C)	θpcb (°C/W)	θca (°C/W)	θhs-a (°C/W)	Avg. θpcb (°C/W)	Avg. θca (°C/W)	Avg. θhs-a (°C/W)
1 oz. #1	0.700	3.31	2.32	69.64	45.73	22.0	10.32	20.57	10.25			
1 oz. #2	0.700	3.26	2.28	70.29	48.03	22.0	9.75	21.16	11.40			
1 oz. #3	0.700	3.21	2.24	65.37	44.02	22.0	9.51	19.33	9.81	9.39	19.99	10.60
1 oz. #4	0.700	3.22	2.25	66.34	47.65	22.0	8.30	19.69	11.39			
1 oz. #5	0.700	3.25	2.28	65.77	45.15	22.0	9.06	19.23	10.17			
2 oz. #1	0.700	3.32	2.32	71.69	48.19	22.0	10.12	21.41	11.28			
2 oz. #2	0.700	3.34	2.34	68.60	45.34	22.0	9.96	19.95	9.99			
2 oz. #3	0.700	3.26	2.28	66.95	46.33	22.0	9.04	19.71	10.67	9.61	19.89	10.28
2 oz. #4	0.700	3.34	2.34	66.36	44.37	22.0	9.39	18.95	9.56			
2 oz. #5	0.700	3.35	2.35	67.57	45.19	22.0	9.54	19.43	9.89			
2 oz. filled #1	0.700	3.36	2.35	67.19	44.39	22.0	9.69	19.20	9.51			
2 oz. filled #2	0.700	3.33	2.33	67.48	45.11	22.0	9.59	19.51	9.92			
2 oz. filled #3	0.700	3.28	2.30	68.06	44.92	22.0	10.08	20.07	9.99	9.65	19.71	10.06
2 oz. filled #4	0.700	3.29	2.30	66.70	44.86	22.0	9.50	19.44	9.94			
2 oz. filled #5	0.700	3.37	2.36	70.03	47.87	22.0	9.39	20.35	10.96			
4 oz. #1	0.700	3.31	2.32	64.35	45.80	22.0	7.99	18.25	10.26			
4 oz. #2	0.700	3.34	2.33	68.31	48.75	22.0	8.38	19.83	11.46			
4 oz. #3	0.700	3.39	2.38	71.87	50.41	22.0	9.03	20.99	11.96	8.40	19.68	11.28
4 oz. #4	0.700	3.26	2.28	66.63	47.87	22.0	8.22	19.54	11.32			
4 oz. #5	0.700	3.33	2.33	68.12	48.55	22.0	8.40	19.80	11.40			
MCPCB #1	0.700	3.36	2.35	63.20	53.20	20.0	4.25	18.37	14.12			
MCPCB #2	0.700	3.04	2.13	57.60	50.90	20.0	3.15	17.67	14.52			
MCPCB #3	0.700	3.36	2.35	57.90	50.10	20.0	3.32	16.11	12.80	3.81	17.41	13.60
MCPCB #4	0.700	3.35	2.35	62.00	51.20	20.0	4.61	17.91	13.30			
MCPCB #5	0.700	3.37	2.36	60.10	51.30	20.0	3.73	17.00	13.27			

The results are close to the predicted performance in Chart 2 (which indicates a thermal resistance asymptote of about 3.5 °C/W for an MCPCB) and Chart 7 (which shows a fourteen-via 1.6-mm FR-4 board with a thermal resistance of about 8 °C/W for a 0.254-mm diameter, 2-oz. plated via).[7]

RECOMMENDED BOARD LAYOUTS

Cree recommends creating areas of 10-mil (0.254-mm) vias arranged on a 25-mil (0.635-mm) rectilinear grid. The reason for this choice is the combination of cost, performance and manufacturability. According to several PCB manufacturers, 10-mil holes and 25-mil spacing are reasonable and repeatable production choices when used with a 2-oz. plating solution.

When using multiple LEDs, tighter spacing between emitters results in increased heating. The thermal pads can be connected together and additional copper can be added, if possible.

The following sections illustrate minimum recommended pad sizes for the XT, XP, XB, MX and ML packages.

Gerber files

For the ML, MX, XB, XP and XT families of LEDs, Cree revised the Gerber files for a star-shaped, single LED circuit board to include via drilling specifications. The Gerber files are .zip archives posted on Cree's website in the Design Files area of the product pages for each of the XT, XP, XB, MX and ML products.[8]

7 In general, thermal measurement of LEDs is challenging and there are chances for error due to the number of variables involved. Thermocouple placement and subsequent calculations are but two of the concerns. We use these results for their suggestive value rather than their definitive result.

8 At the Products page, select the LED of interest then select the Documentation tab.

FR-4 Boards for XLamp XP and XT LED Packages

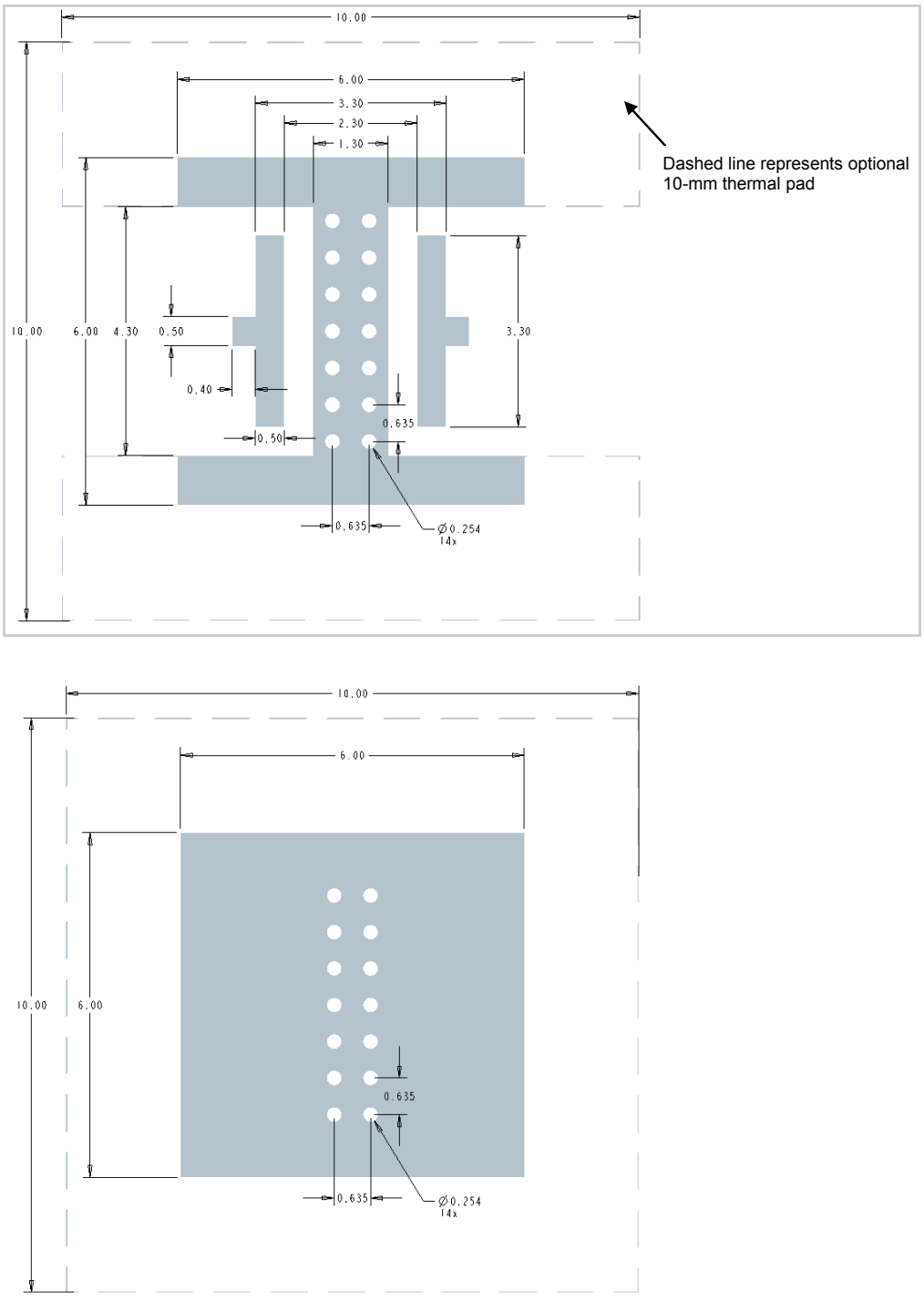

Figure 15: Recommended footprint for XLamp XP and XT family of LEDs on FR-4 PCB (top and bottom)

FR-4 Boards for XLamp XB LED Package

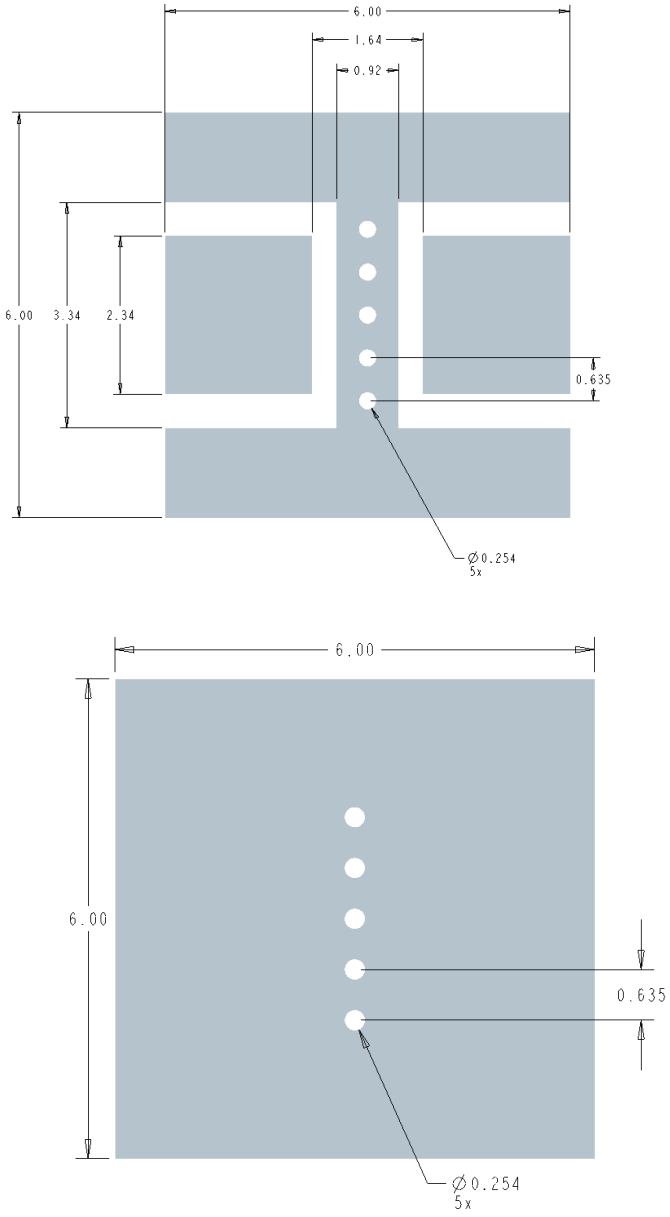

Figure 16: Minimum footprint for XLamp XB family of LEDs on FR-4 PCB (top and bottom)

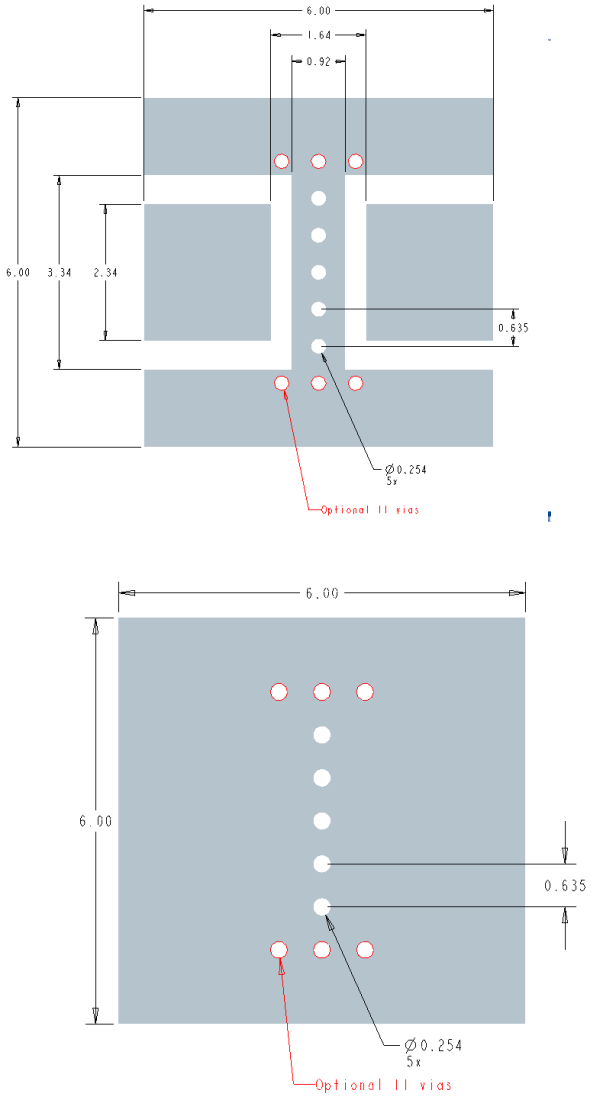

Figure 17: Recommended footprint for XLamp XB family of LEDs on FR-4 PCB (top and bottom)

FR-4 Boards for XLamp MX LED Package

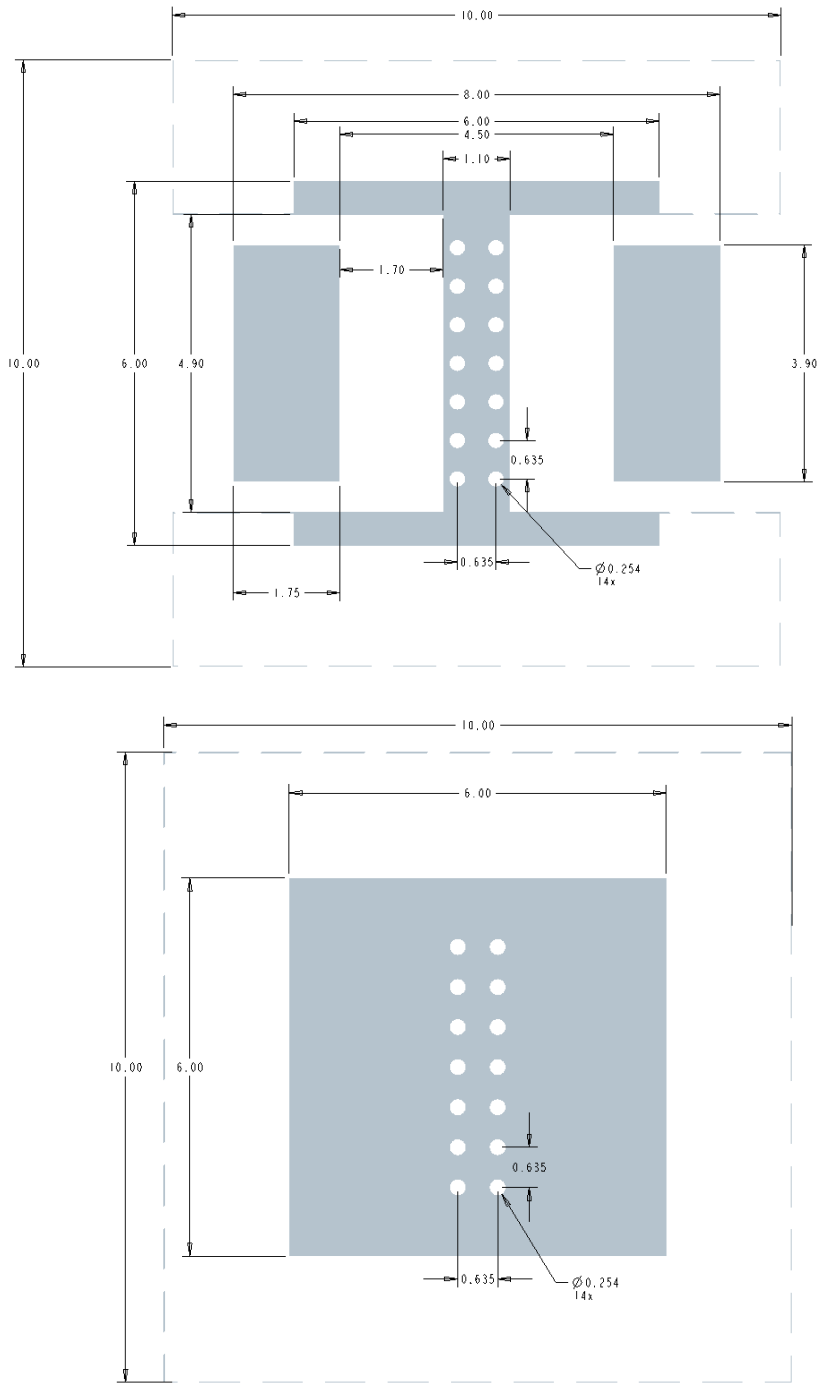

Figure 18: Recommended footprint for XLamp MX package on FR-4 PCB (top and bottom)

FR-4 Boards for XLamp ML LED Package

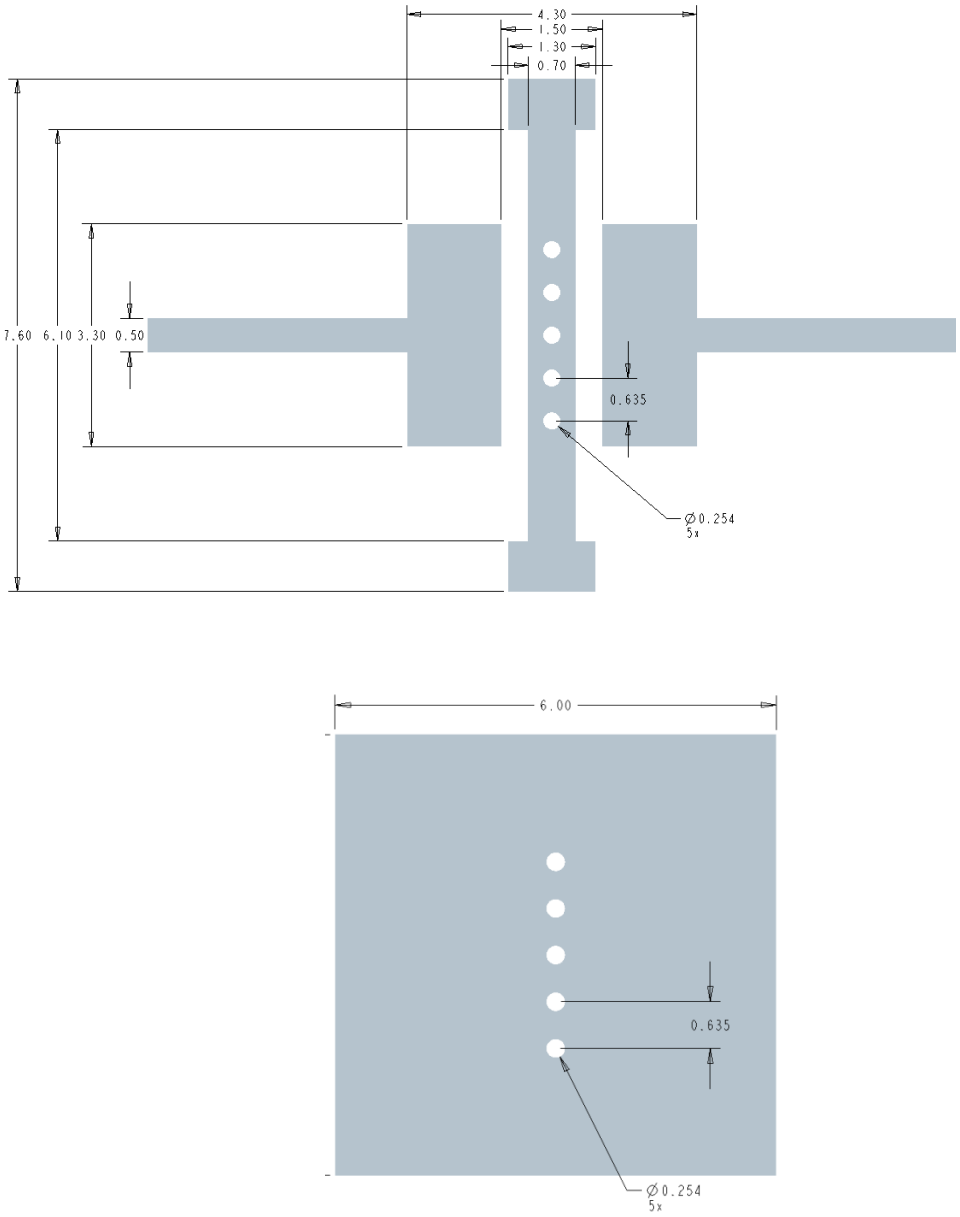

Figure 19: Recommended footprint for XLamp ML package on FR-4 PCB (top and bottom)

CHEMICAL COMPATIBILITY

It is important to verify chemical compatibility when selecting the interface materials to use between the board and the heat sink, as well as other materials to which the LEDs can be exposed. Certain materials from FR-4 board fabrication and assembly processes, e.g., adhesives, solder mask and flux residue, can outgas and react adversely with the materials in the LED package, especially at high temperatures when a non-vented secondary optic is used. This interaction can cause performance degradation and product failure. Each family or individual LED product has an application note identifying substances known to be harmful to Cree LEDs.[10] Consult your PCB manufacturer to determine which materials it uses.

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10 XT Family LEDs Soldering & Handling
XP Family LEDs Soldering & Handling
XB Family LEDs Soldering & Handling
MX Family LEDs Soldering & Handling
ML Family LEDs Soldering & Handling