

EE6320 RF Integrated Circuits

Project: Mixer Design

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Roll No: EE22B003

Mixer Performance Summary Table

	Design Metric	Performance	Specification
Conversion Gain	Minimum Peak Gain in the specified band [$f_{RF} = f_{LO}$]	24.46	>20 dB
	Maximum Peak Gain in the specified band [$f_{RF} = f_{LO}$]	24.53	>20 dB
	Peak Gain flatness in specified band [Max-Min Gain]	0.014	-
	Minimum Band-Edge Gain in the specified band [$f_{RF} = f_{LO} + 10\text{MHz}$]	24.487	>20 dB
	Maximum Band-Edge Gain in the specified band [$f_{RF} = f_{LO} + 10\text{MHz}$]	24.506	>20 dB
Noise Figure	Maximum SSB Noise Figure for $f_{LO} = 925\text{ MHz}$	4.23	$\leq 10\text{ dB}$
	Maximum SSB Noise Figure for $f_{LO} = 942.5\text{ MHz}$	4.31	$\leq 10\text{ dB}$
	Maximum SSB Noise Figure for $f_{LO} = 960\text{ MHz}$	4.34	$\leq 10\text{ dB}$
Linearity - IIP_2	Input power used for extrapolation	-40 dB	-
	Power of Fundamental Tone at output (at chosen input power)	-40 dB	-
	Power of IM_2 Tone at output (at chosen input power)	-152 dBm	-
	Extrapolated IIP_2	54.47 dB	$\geq +30\text{dBm}$
Linearity - IIP_3	Input power used for extrapolation	-60 dB	-
	Power of Fundamental Tone at output (at chosen input power)	-40 dB	-
	Power of IM_3 Tone at output (at chosen input power)	-160 dB	-
	Extrapolated IIP_3	906 m dB	$\geq 0\text{ dBm}$
Power	Mixer DC power consumption [Excluding Bias]	9.78mW	Minimize
	Bias circuit power consumption	0.029mW	Minimize
Other	Sum of all resistances [excluding bias]	1.1 k	-
	Sum of biasing resistances	20k	-
	Sum of all capacitances [Including AC coupling]	8pF	-

	Sum of all inductances	0	
	Load chosen (each R_load)	550 Ohm	-

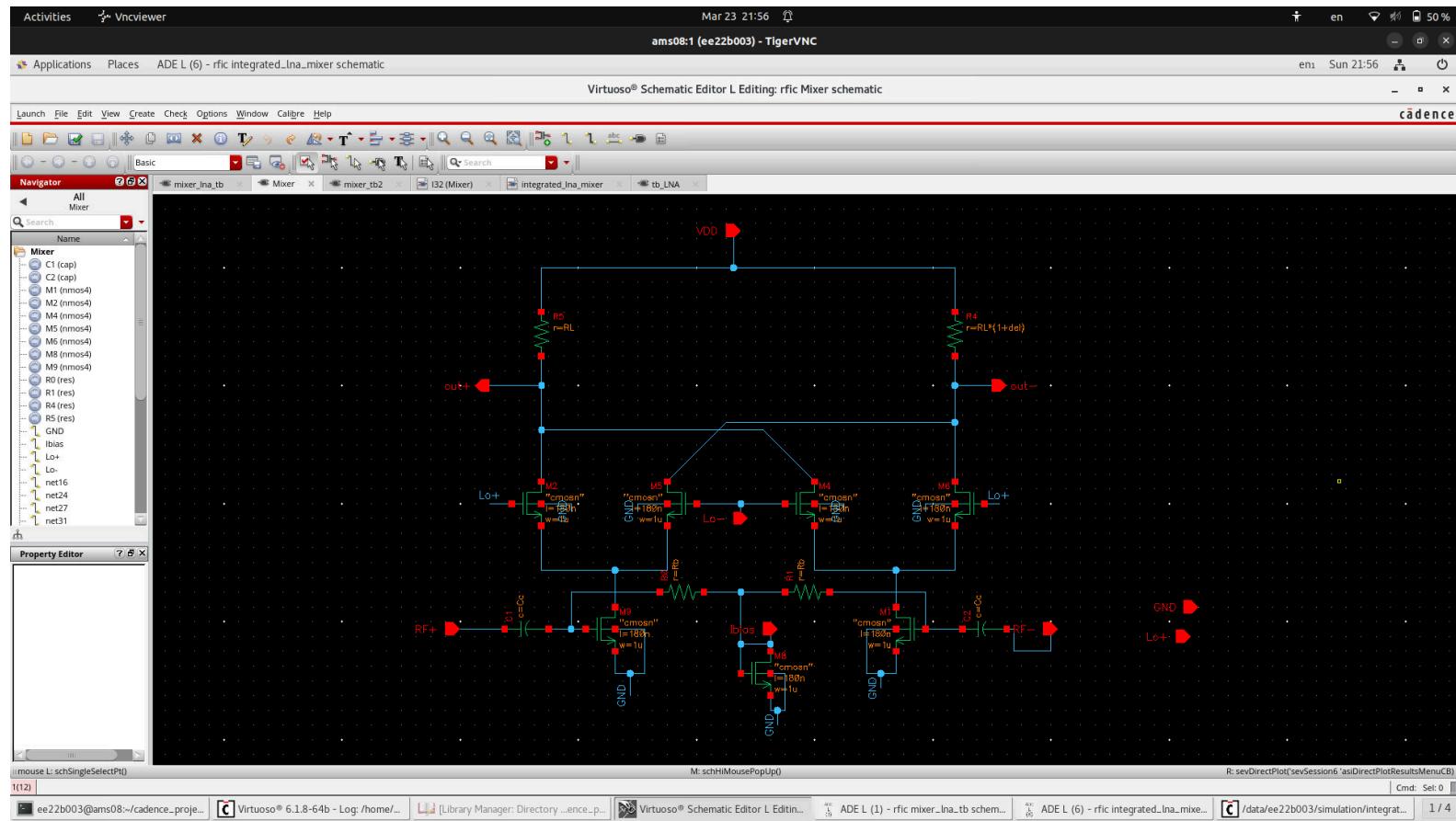
	Differential Mixer Input Capacitance (C_gs Caps)	1.106pF	-
	Simulator Used	Spectre	-

LNA + Mixer Performance Summary Table

	Design Metric	LNA	Mixer	Cascade	
				Expected	Simulated
Conversion Gain	$f_{IN} = f_{LO}, f_{LO} = 925 \text{ MHz}$	27 dB	24 dB	49.5 dB	37.8 dB
	$f_{IN} = f_{LO} + 10\text{MHz}, f_{LO} = 925 \text{ MHz}$	27 dB	24 dB	49.5 dB	37.85 dB
	$f_{IN} = f_{LO}, f_{LO} = 942.5 \text{ MHz}$	28 dB	24 dB	49.5 dB	37.76 dB
	$f_{IN} = f_{LO} + 10\text{MHz}, f_{LO} = 942.5 \text{ MHz}$	28 dB	24 dB	49.5 dB	37.65 dB
	$f_{IN} = f_{LO}, f_{LO} = 960 \text{ MHz}$	27 dB	24 dB	49.5 dB	37 dB
	$f_{IN} = f_{LO} + 10\text{MHz}, f_{LO} = 960 \text{ MHz}$	27 dB	24 dB	49.5 dB	36.7 dB
Noise Figure	$f_{IN} = f_{LO} + 10\text{MHz}, f_{LO} = 925 \text{ MHz}$	1.308 dB	4.23 dB	1.396 dB	1.83 dB
	$f_{IN} = f_{LO} + 10\text{MHz}, f_{LO} = 942.5 \text{ MHz}$	1.336 dB	4.31 dB	1.4 dB	1.83 dB
	$f_{IN} = f_{LO} + 10\text{MHz}, f_{LO} = 960 \text{ MHz}$	1.368 dB	4.34 dB	1.43 dB	1.9 dB
Linearity IIP3	Input power used for extrapolation	-60	-60	-	-60
	Power of Fundamental Tone at output (at chosen input power)			-	
	Power of IM_3 Tone at output (at chosen input power)			-	
	Extrapolated IIP_3			-	
Power	Total power consumption [Excluding Bias]	10.96 mW	19.56 mW	30.12 mW	33.38 mW

	Bias circuit power consumption	22 uW	28.8 uW	508 uW	50.8 uW
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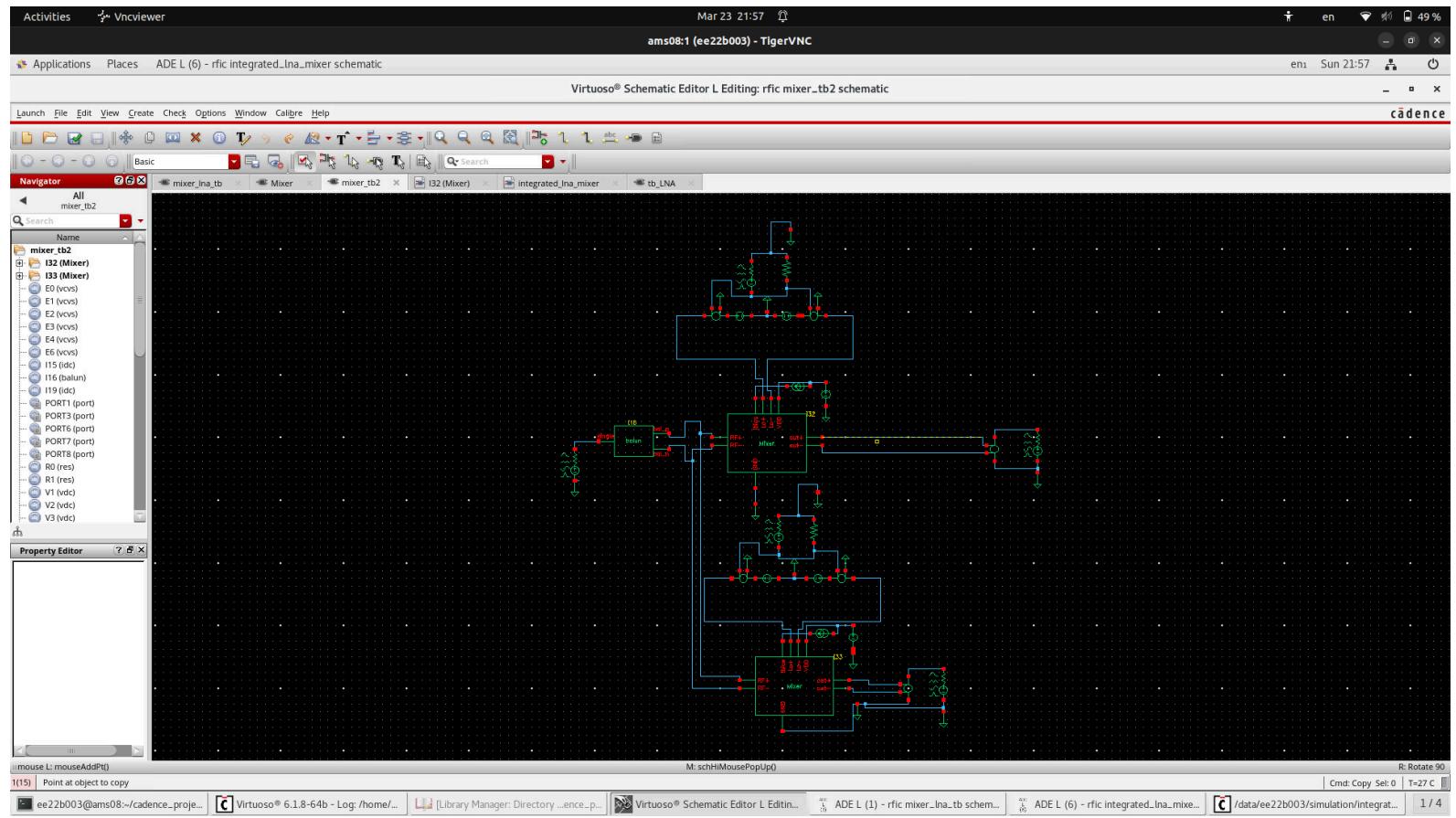
Mixer Schematic



Mixer Testbench

Design Variable Values

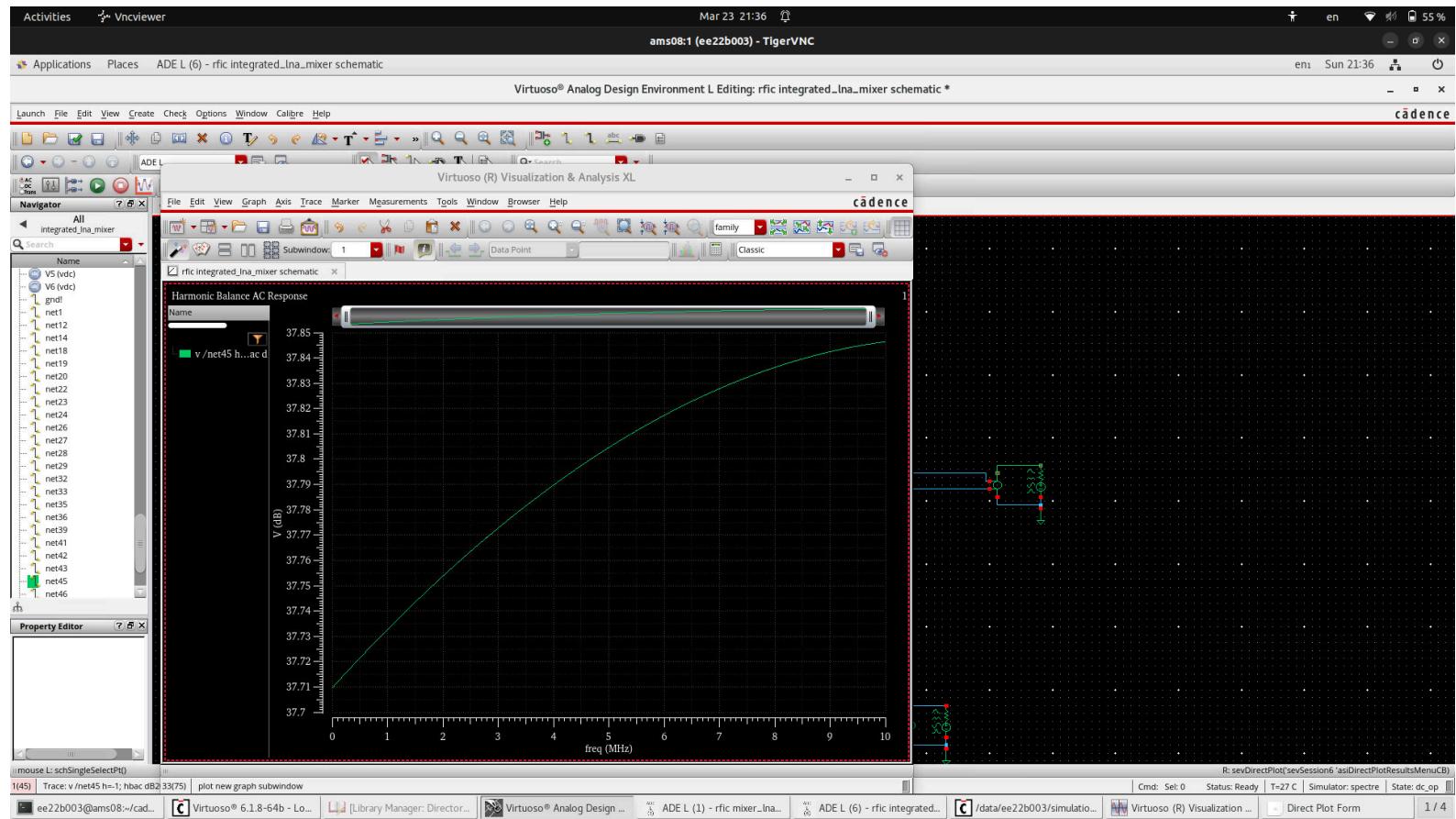
Design Variable	Value
Resistance (load, each side)	550
Length of all MOS	180n
Width of Switch MOS (all 4)	240u
Width of Transconductance MOS (both MOS)	240u
Bias Current	1.355m
V_LO Amplitude	700m



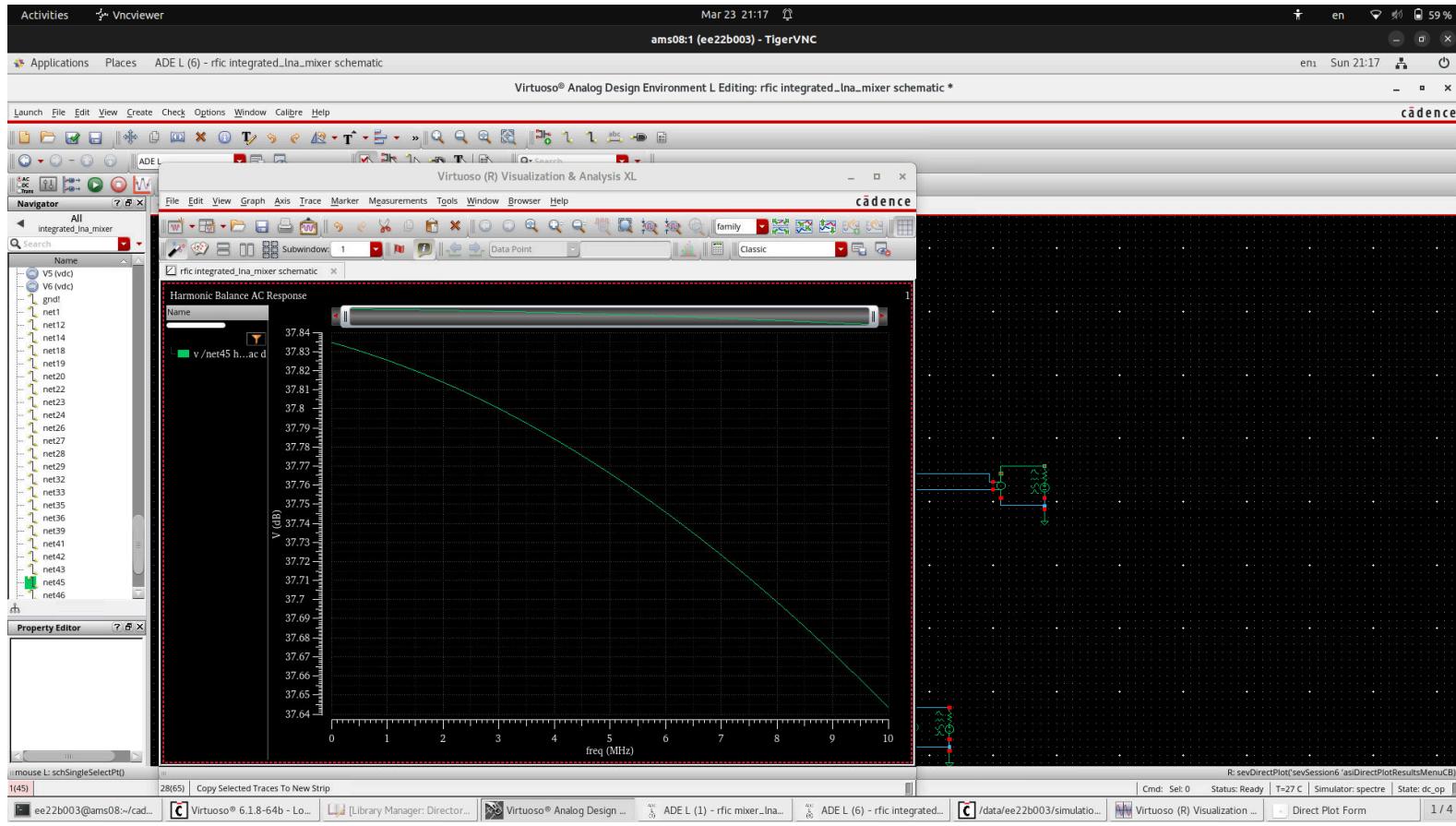
Fixed Constant Parameters

- Transconductance MOS C_gs: 619.4 fF
- Current Mirror MOS: W = 1u , L = 180n
- Coupling capacitances: 2pF (each)
- Bias Resistances: 10 k each

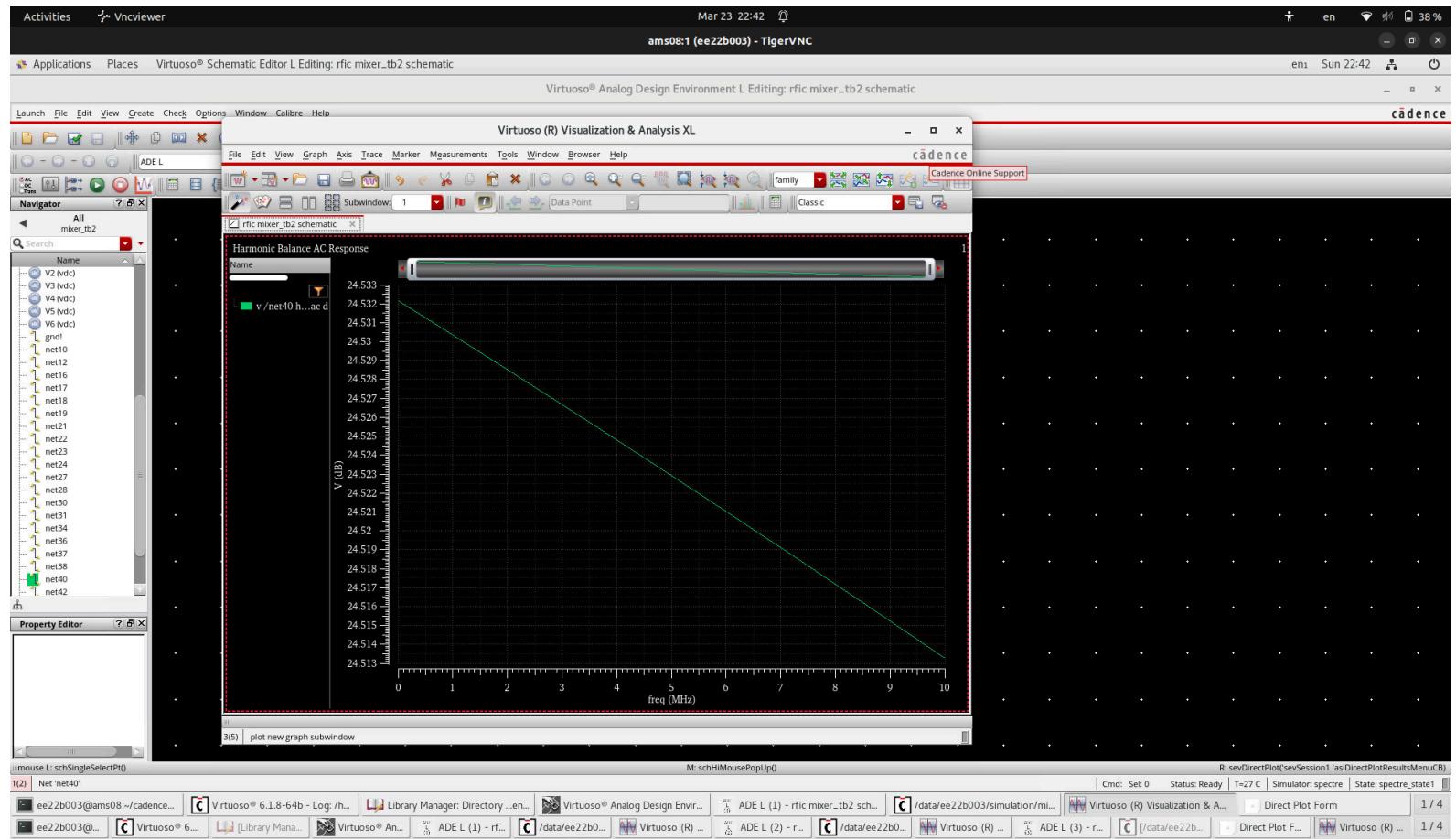
Conversion Gain of Mixer at 925 MHz



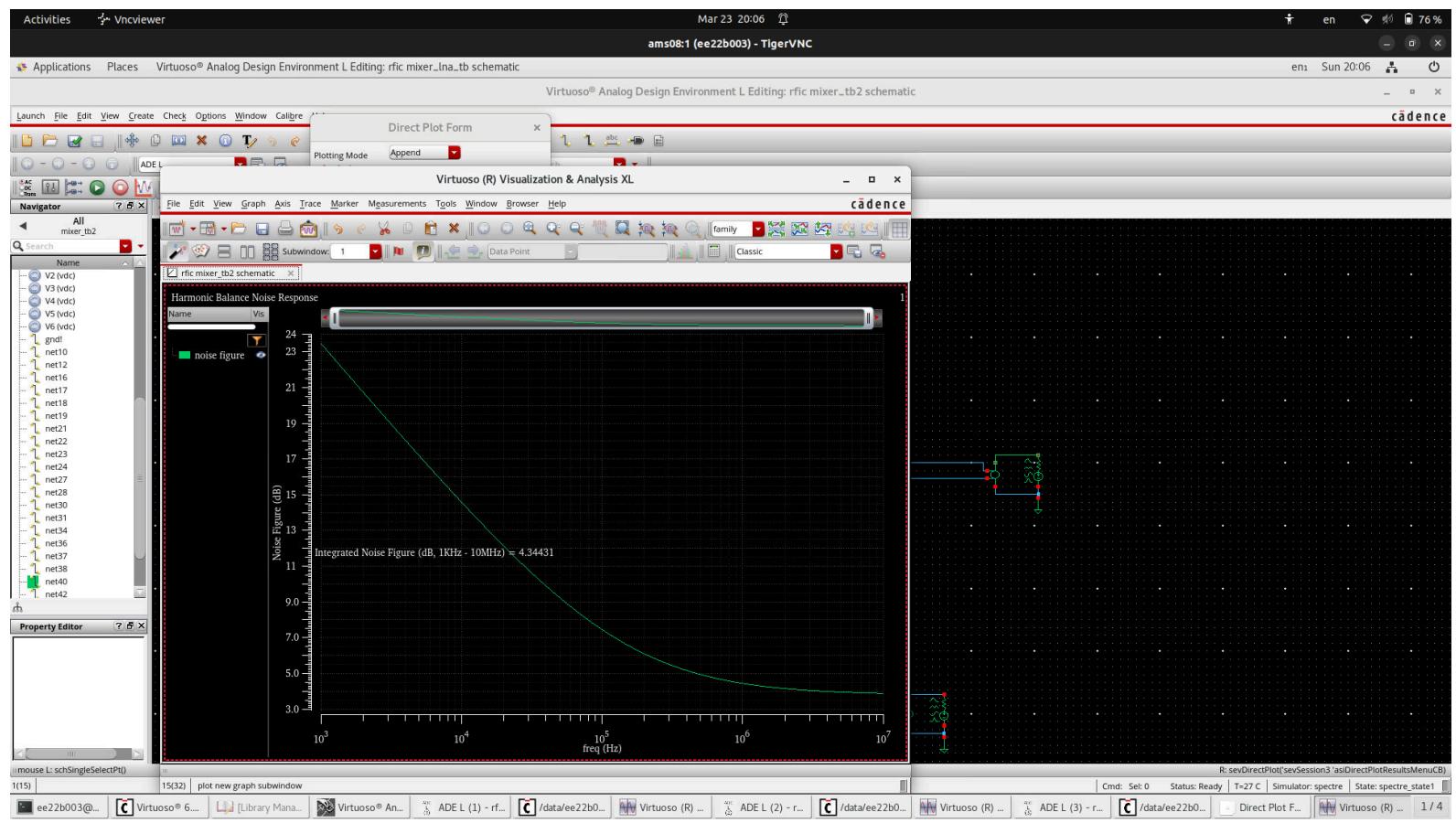
Conversion Gain of Mixer at 942.5 MHz



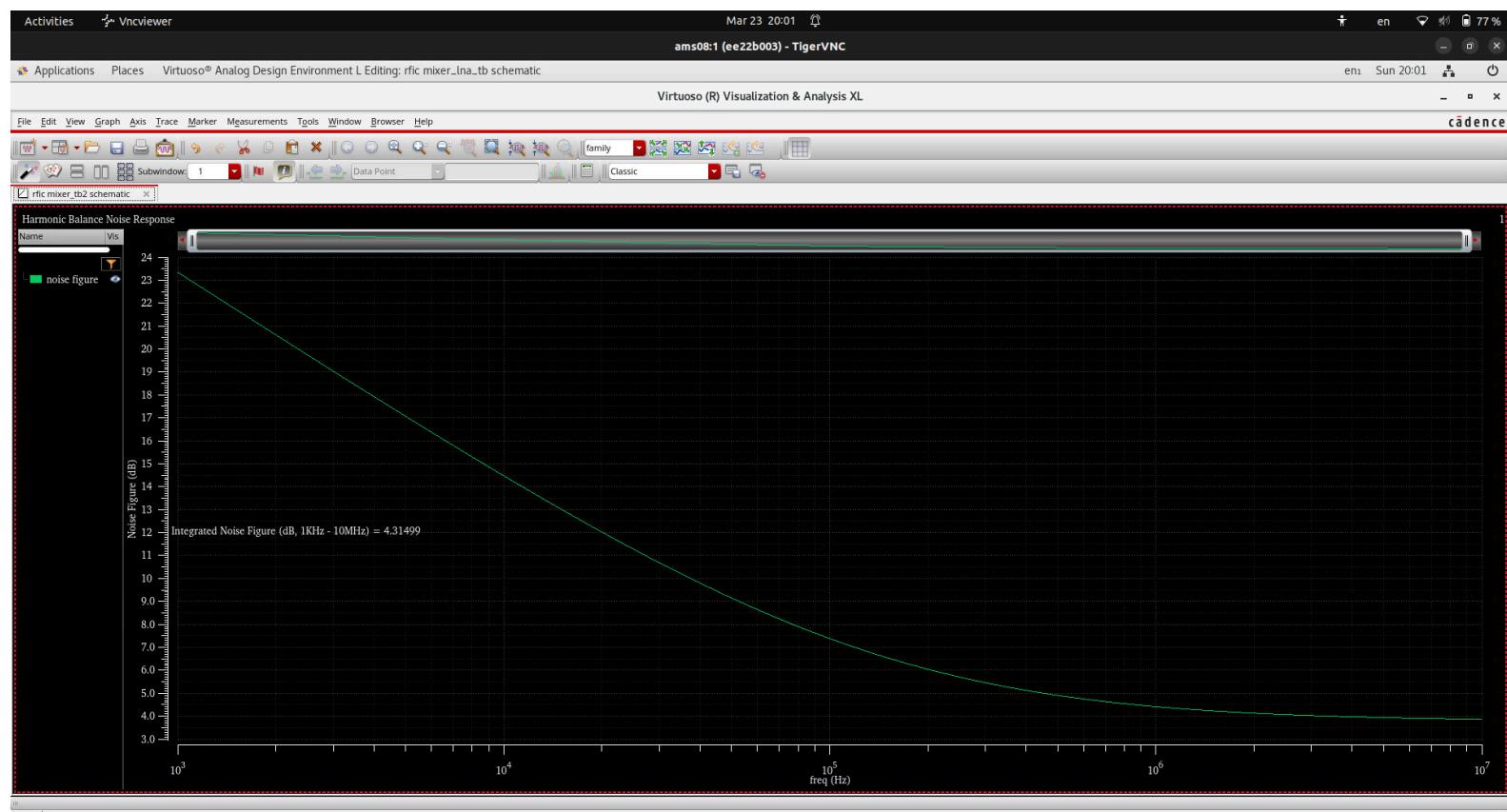
Conversion Gain of Mixer at 960 MHz



Noise Figure of Mixer at 960MHz



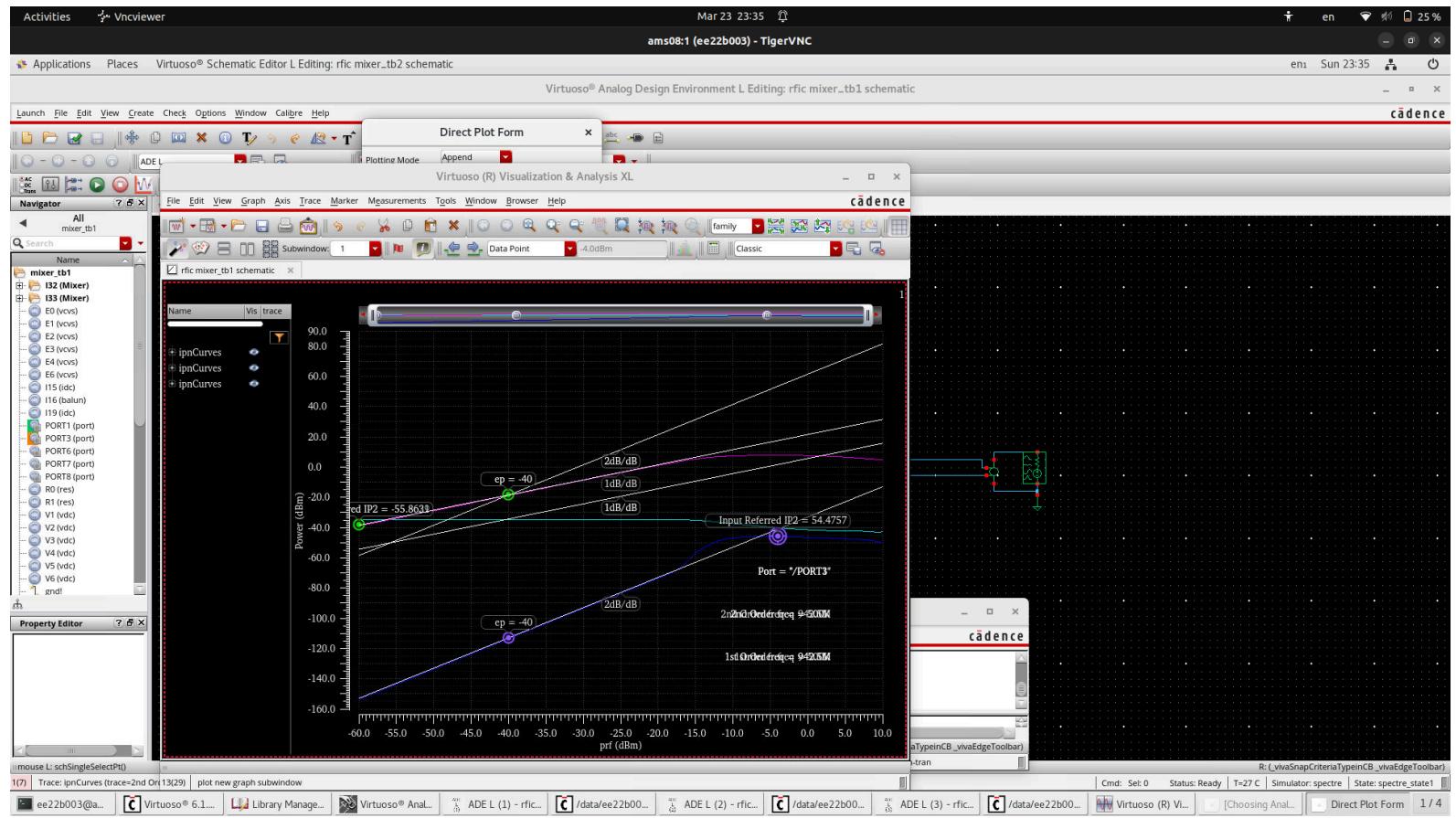
Noise Figure of Mixer at 940 MHz



Noise Figure of Mixer at 925 MHz



Mixer IIP2 Linearity



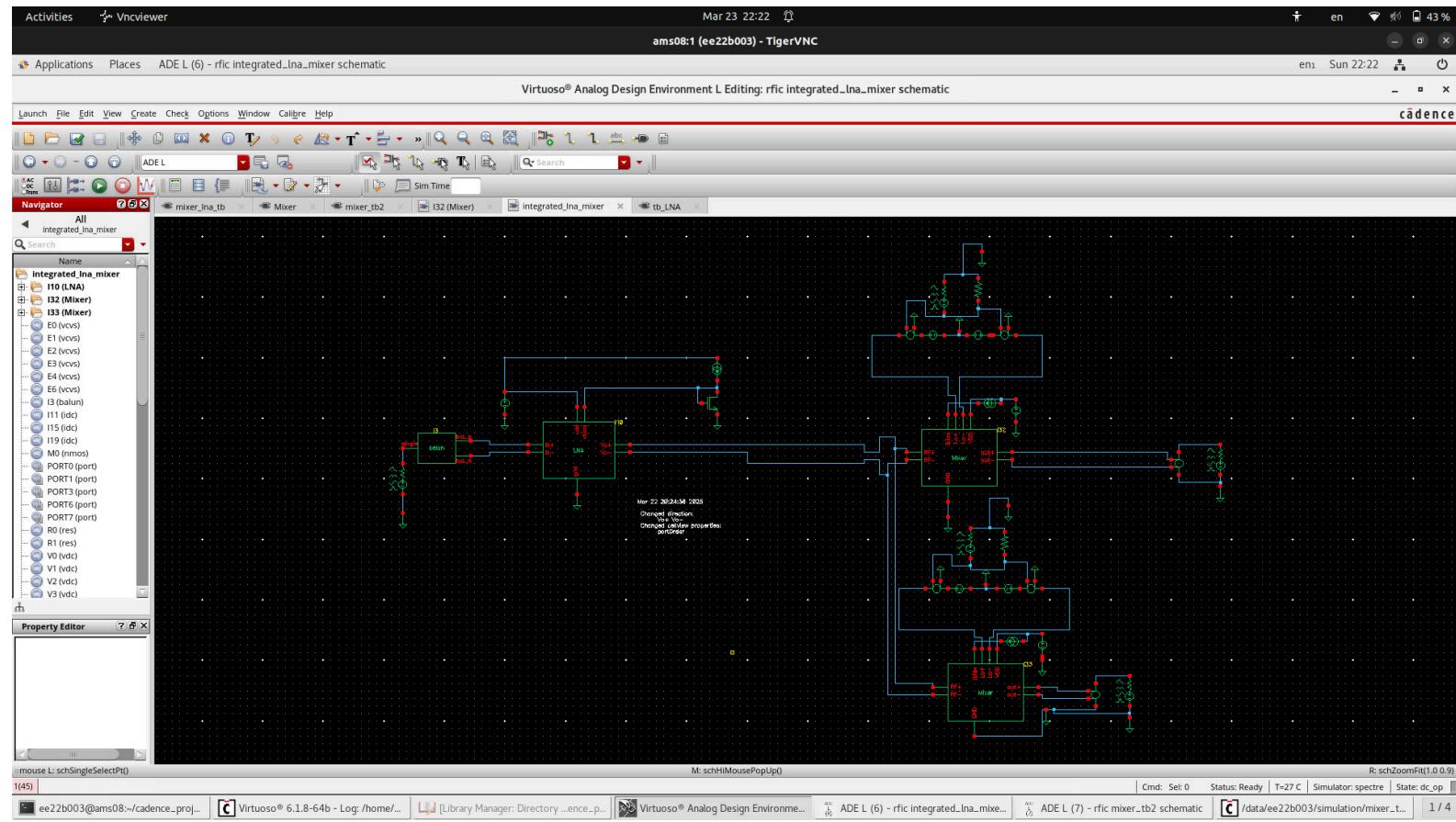
Mixer IIP3 Linearity



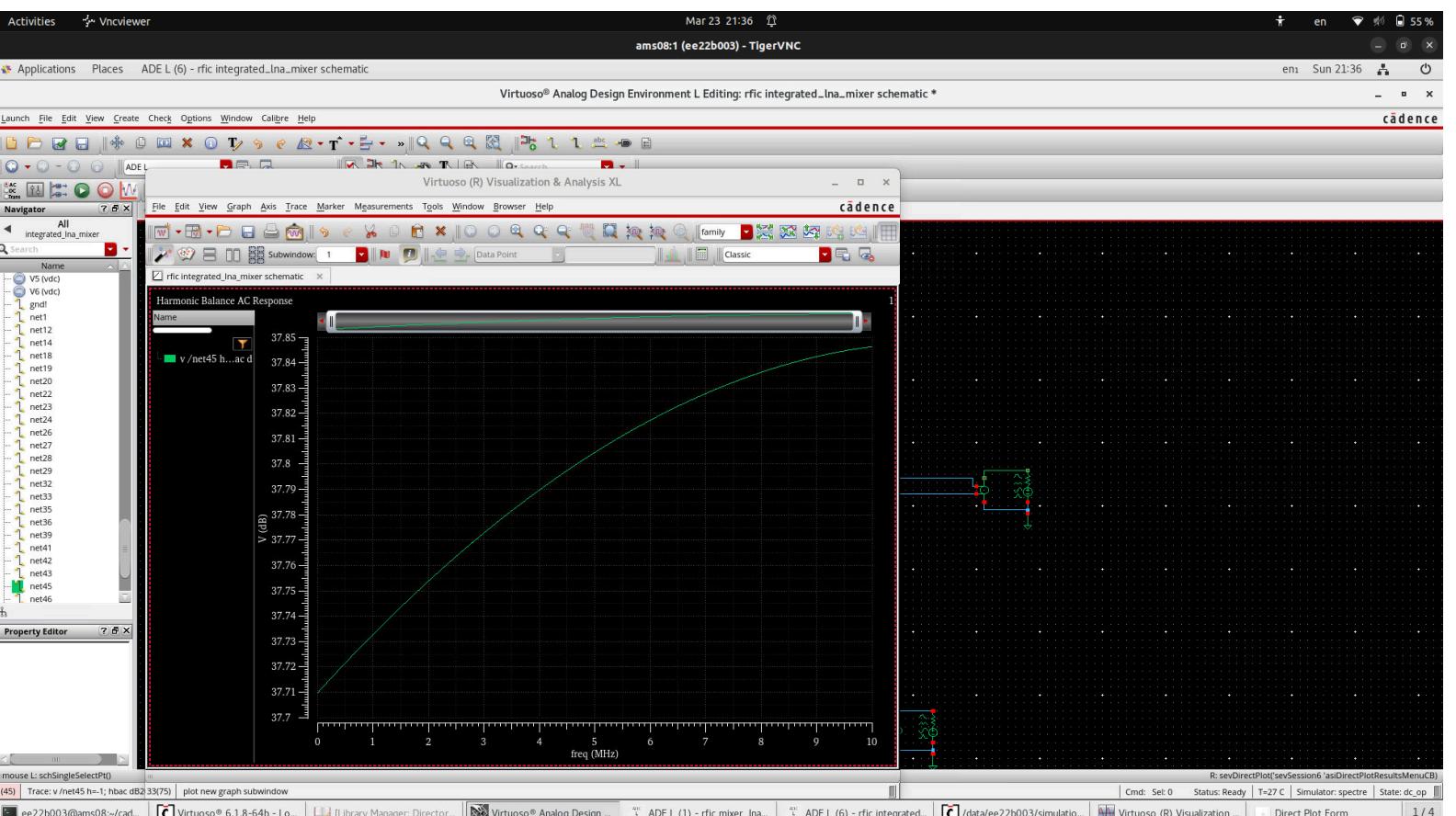
Mixer DC Power Consumption [Excluding Bias]



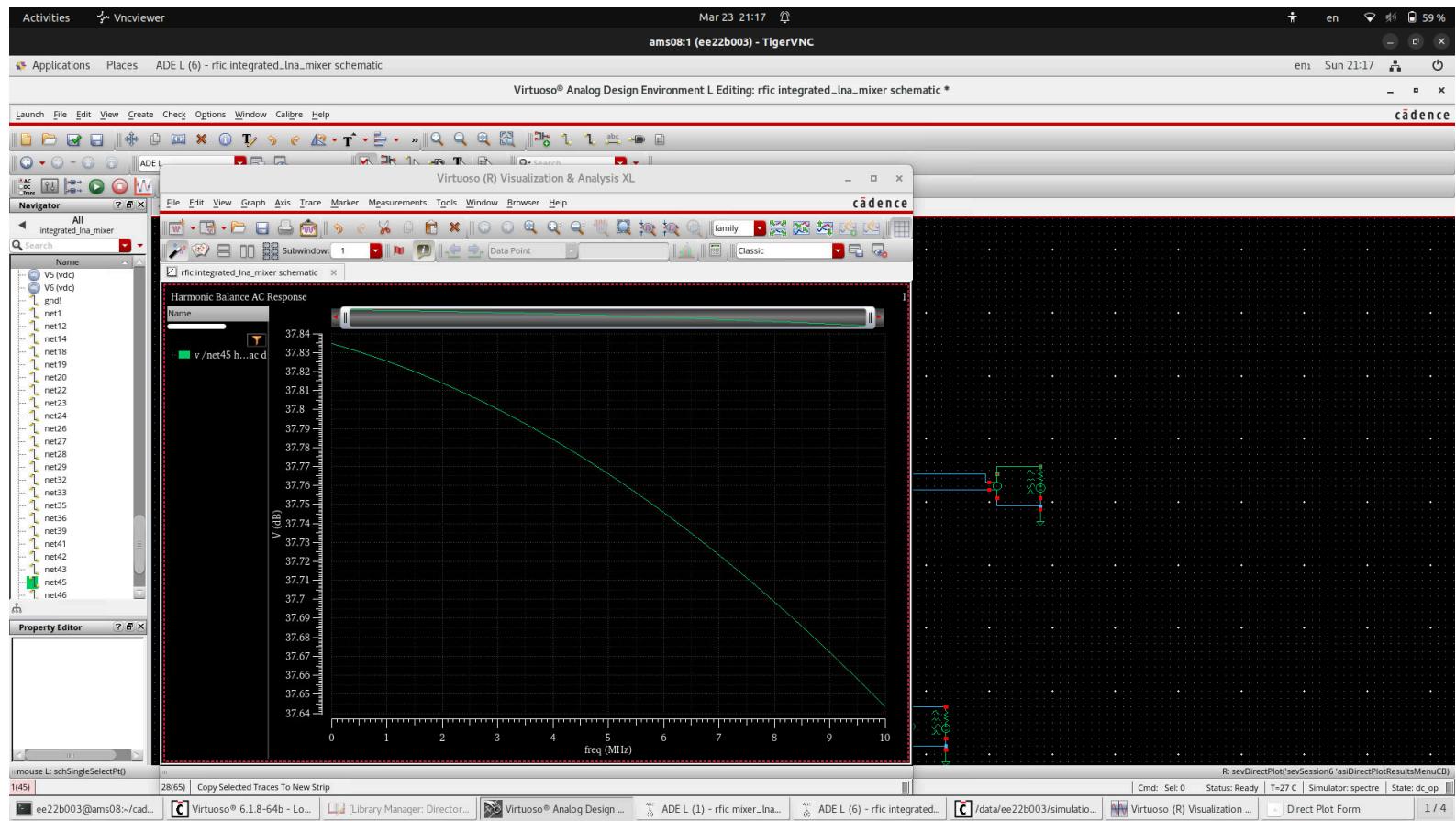
LNA + Mixer Testbench



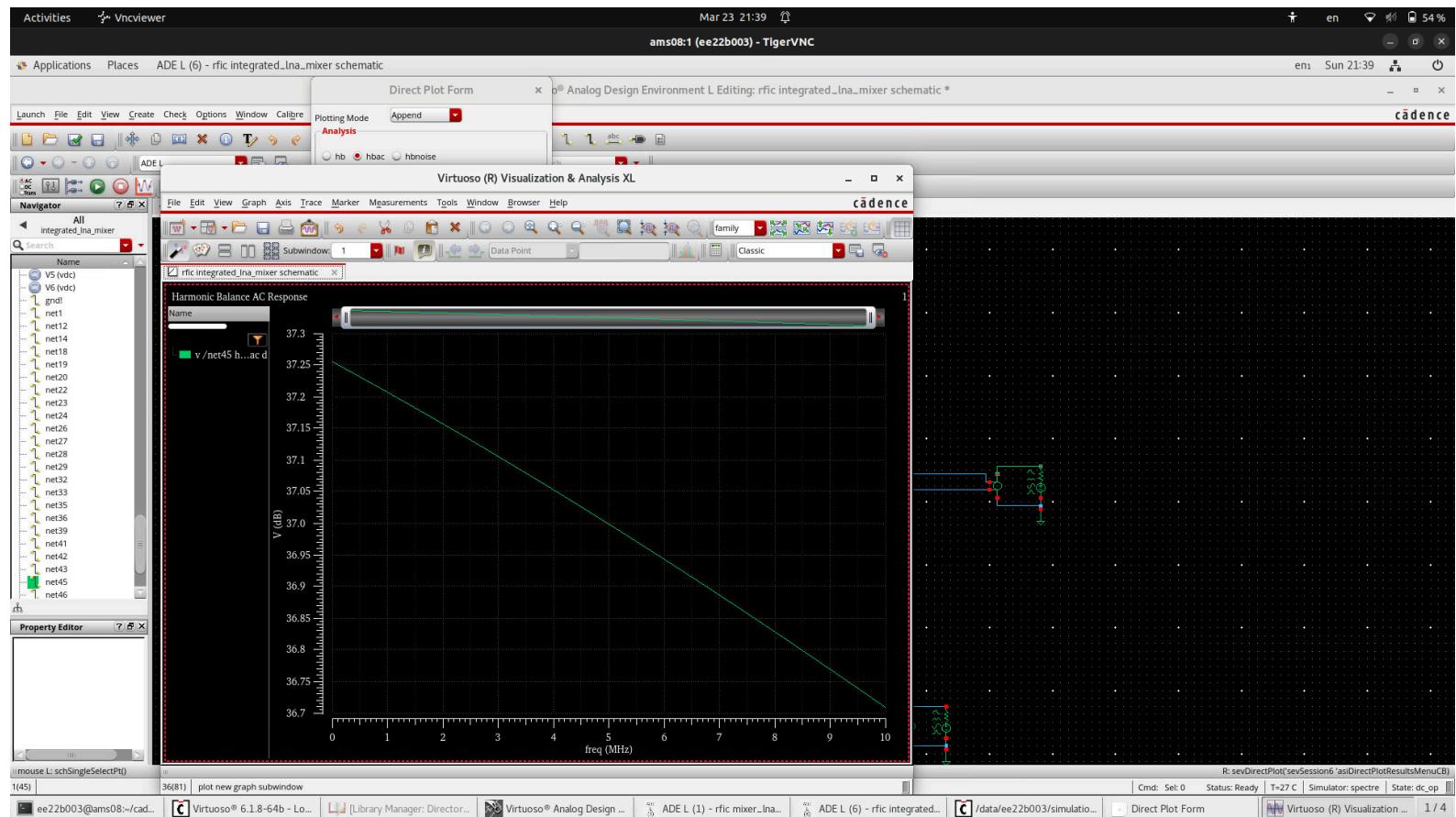
LNA + Mixer Conversion Gain at 925 MHz



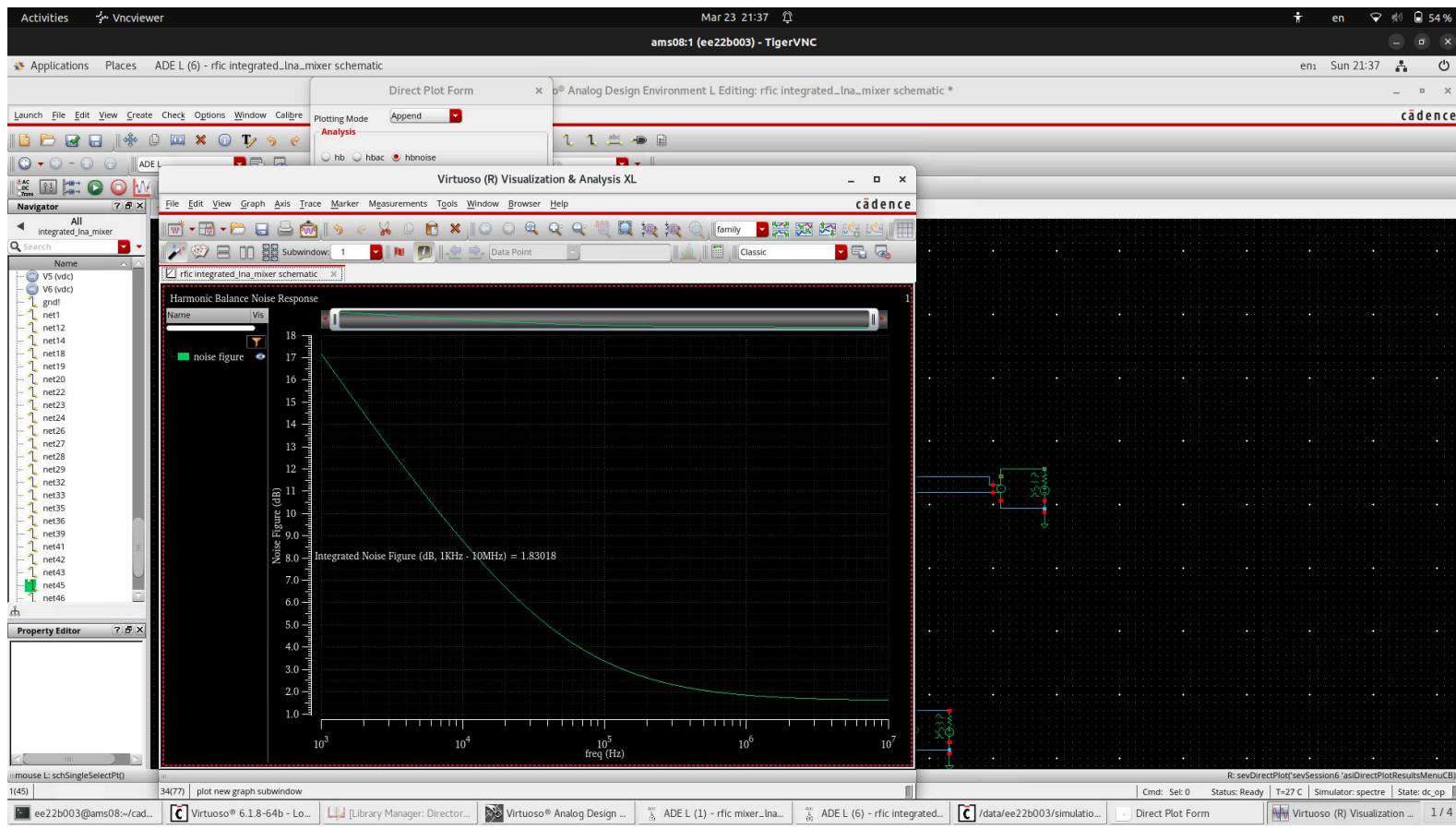
LNA + Mixer Conversion Gain at 942.5 MHz



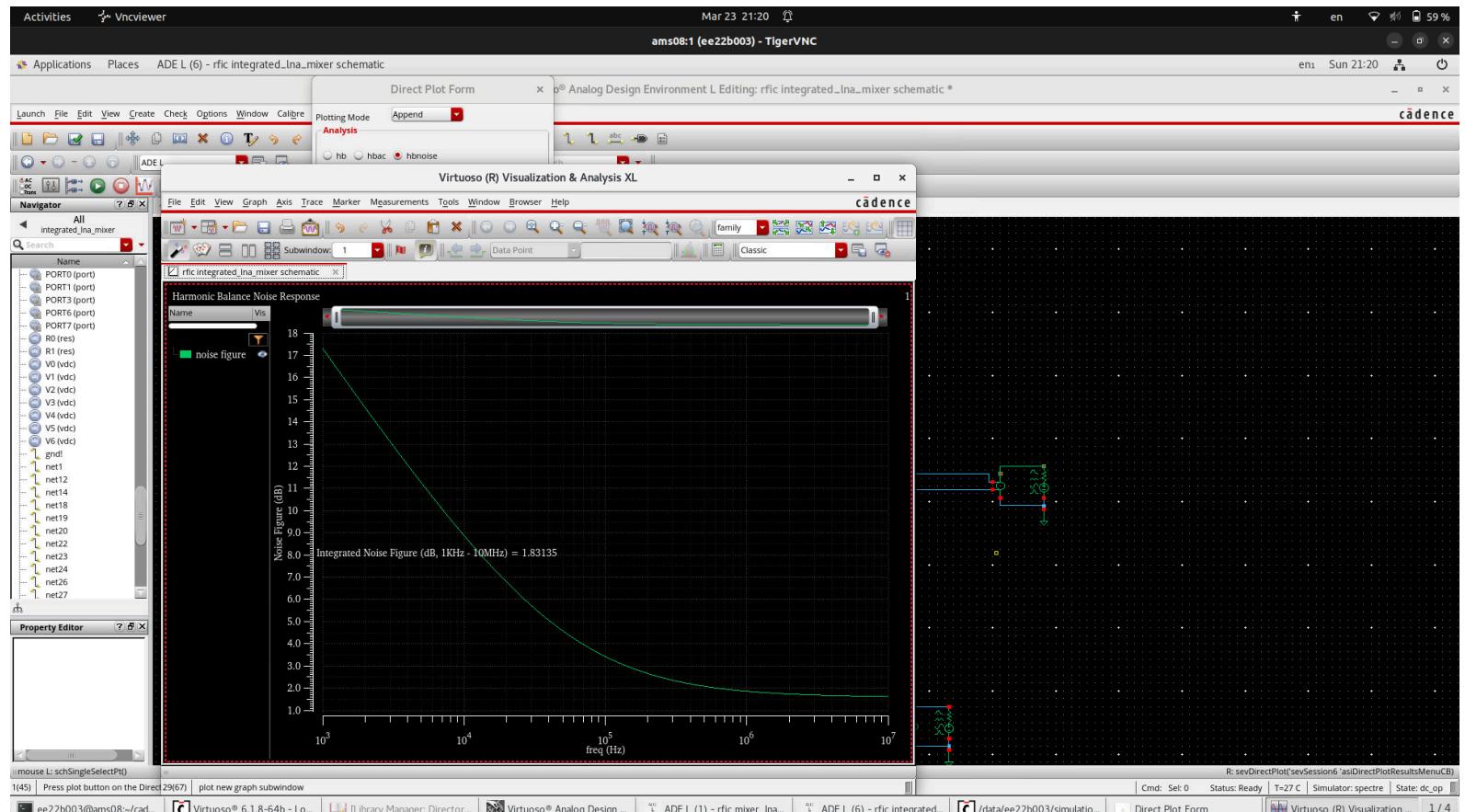
LNA + Mixer Conversion Gain at 960 MHz



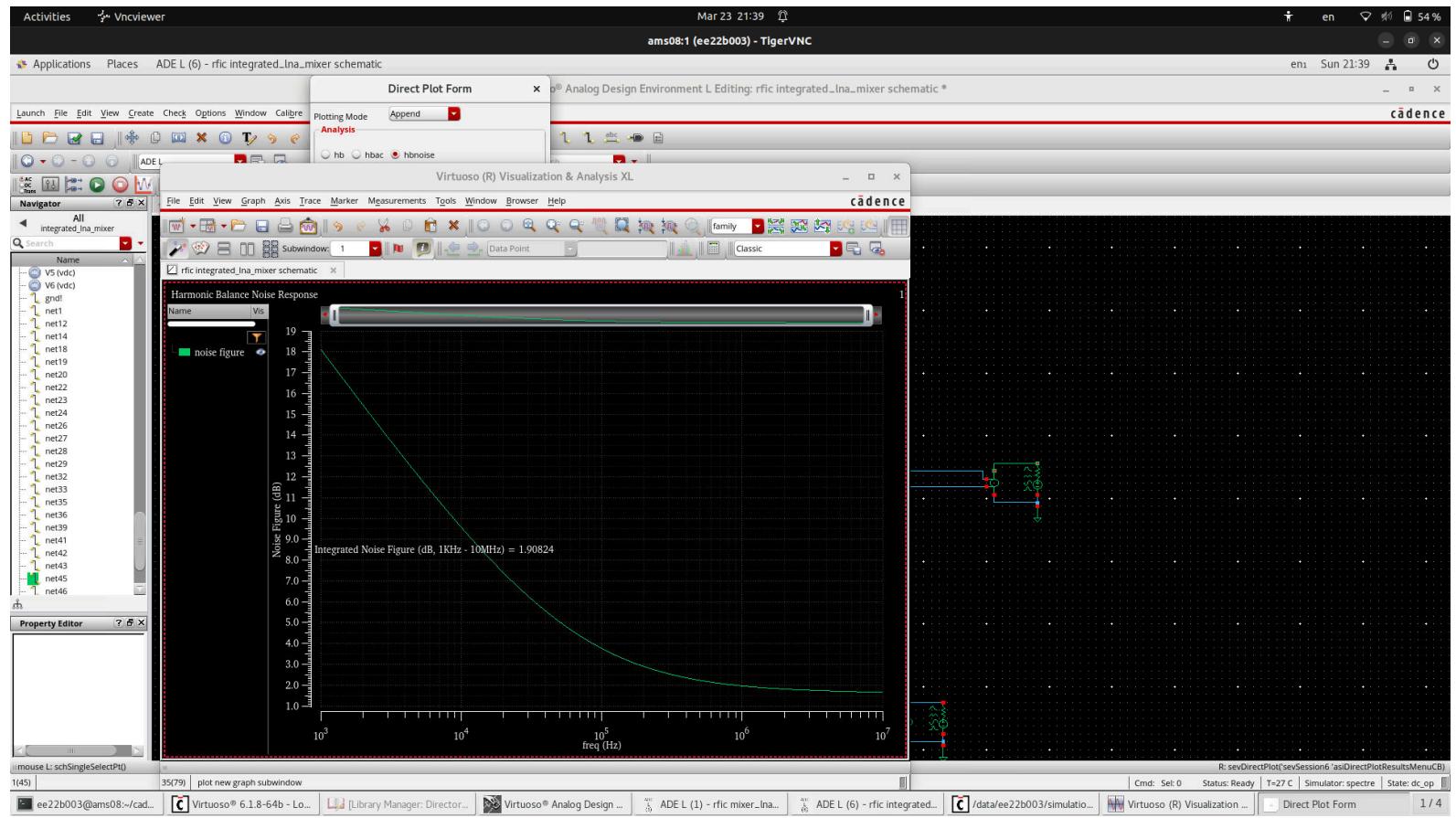
LNA + Mixer Noise Figure at 925 MHz



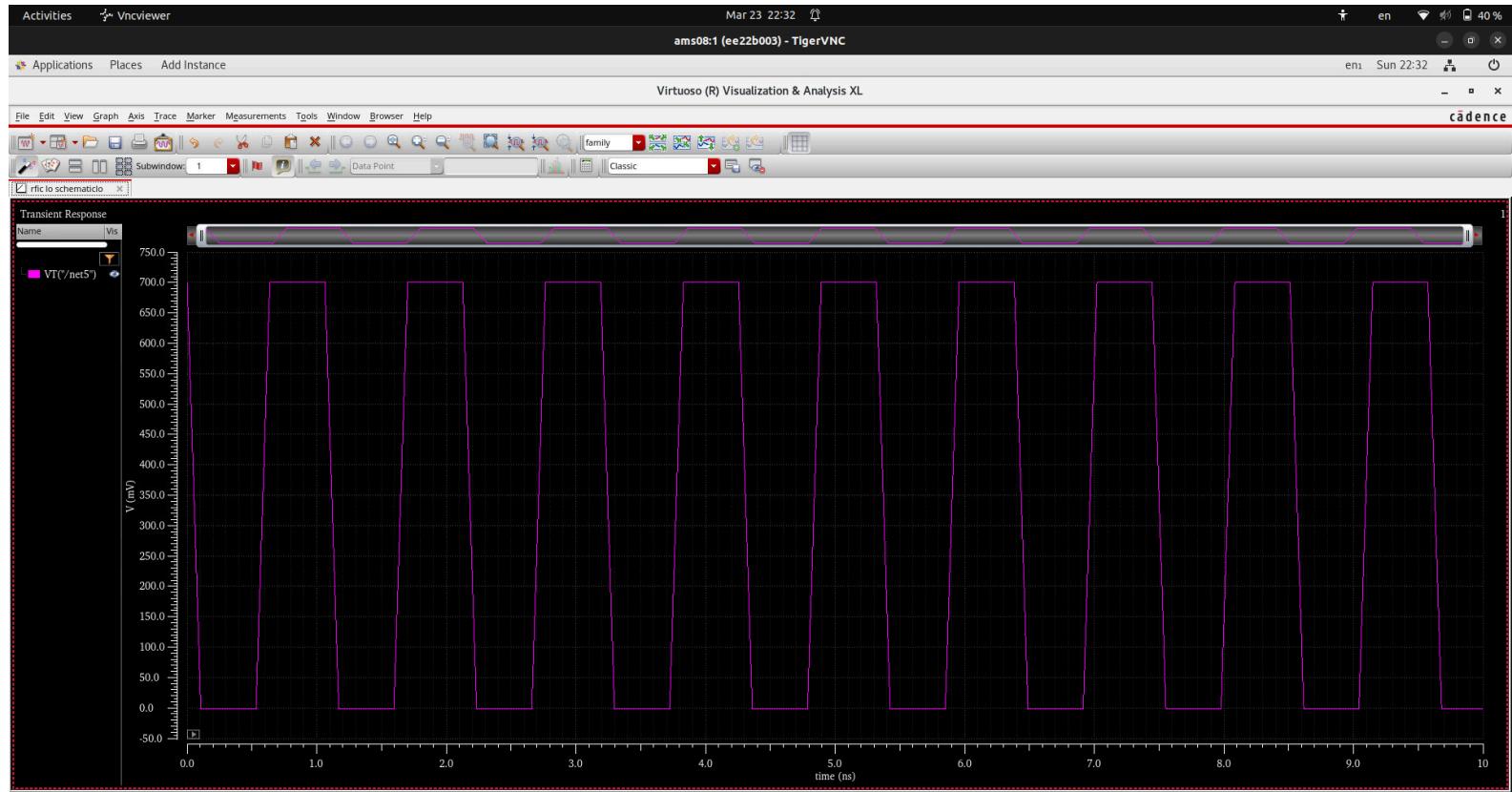
LNA + Mixer Noise Figure at 942.5 MHz



LNA + Mixer Noise Figure at 960 MHz



LO Waveform Characteristics



Characteristics taken are (for generalized manner, as f_{lo} varies for various analysis):

- Frequency: 940MHz
- Time period: 1.064 ns
- Delay time: 0 (for I Lo signal), 266 ps (for Q Lo signal)
- Pulse Width: 425.6 ps
- Rise/Fall Time: 106.4 ps

Calculations done for the Project

For a noise factor of 2, I approximate $NF = 1 + \pi^2 / (8 * gm * R_s)$ taking only the thermal noise of the transconductor into account. Putting R_s as 50 Ohms, $gm = 24mA/V$. So, this gives a theoretical noise factor of 3dB, in practice, 4.3dB is obtained.

Procedure adopted for the Project

First a gm was selected for the mosfet based on noise figure specifications. The bias point was chosen so as to have zero gm_3 of the transconductance Mosfet (610mV). In reality, a smaller bias turned out to be required (~550.7mV). From this, the transistor width was chosen. The switch and transconductor mosfets were chosen to be of the same size so that with the same current when the switch is on, their gate source voltage can be that which give $gm_3=0$. Amplitude of the local oscillator was chosen approximately equal to the simulated V_{ds} of the lower mosfet + the bias voltage that gives $gm_3=0$. Then a load resistor was chosen that gave sufficient output swing, so as not to have any gain expansion at high power, this value was determined from

simulations in increments of 25 Ohms. The value must be large enough to give required conversion gain. Finally, the bias current was adjusted to meet IIP3 > 0 requirement.

Path to the Project Files

~/cadence_project/rfic