Assignment 7

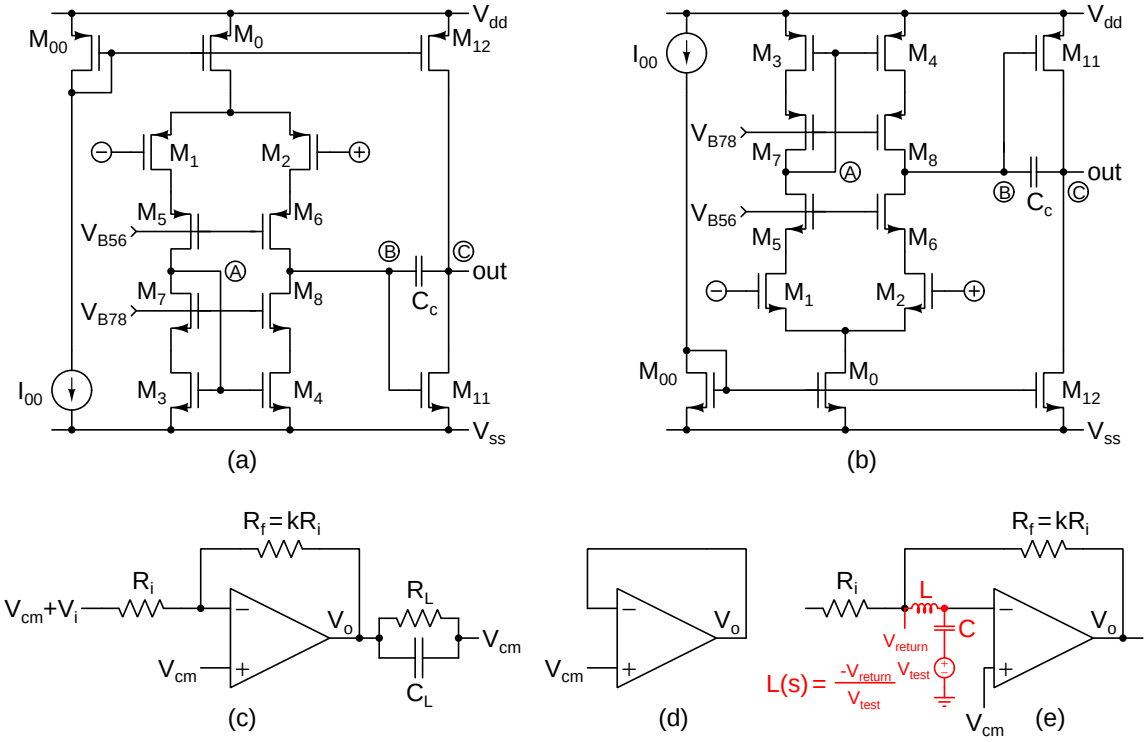

Figure 7.1: Problem 7.1.

7.1. Fig. 7.1 shows two-stage opamps. The first stage is a telescopic cascode stage. (a) uses a pMOS differential pair in the first stage and an nMOS common-source amplifier in the second stage. (b) uses an nMOS differential pair in the first stage and an pMOS common-source amplifier in the second stage.

Realize the inverting amplifier (Fig. 7.1(c)) that you designed in assignment 4 using these opamps. You will be using the same component values here. You will also need the results of MOS characterization to determine the current density.

For simulating the operating point, place the opamp in unity negative feedback as shown in Fig. 7.1(d) or simulate it in open loop with nodes A, B, and C shorted to each other and both inputs at V_{cm}.

- $V_{dd} = 1.8\,\text{V}$, $V_{ss} = 0\,\text{V}$, $V_{cm} = 0.9\,\text{V}$.
- Simulation temperature: 100°C.
- Odd roll numbers: pMOS input pair; Even roll numbers: nMOS input pair.
- $L = 0.3\,\mu\text{m}$ for all transistors.
- Use[1] $V_{DSAT} = 0.15\,\text{V}$ for the first stage transistors except M_0. Use $V_{DSAT} = 0.25\,\text{V}$ for the second stage transistors, M_0, and M_{00}.
- Choosing the V_{DSAT} value fixes the g_m and I_D per $1\,\mu\text{m}/0.3\,\mu\text{m}$ finger. Choose the multiplier m for each transistor to set its g_m or I_D as required.
- For M_{00}, use $m = 2$ and choose I_{00} (integer µA) that sets the desired bias in the first and the second stages.

[1]Choose the current density that sets the V_{DSAT} to within 10 mV of the specified values. Do not aim for microvolt precision.

- All nMOS bulk terminals should be connected to V_{ss}. All pMOS bulk terminals should be connected to V_{dd}.
- Adjust V_{B56} such that the V_{DS} of $M_{1,2}$ is 50 mV above their V_{DSAT}. Similarly, Adjust V_{B78} such that the V_{DS} of $M_{3,4}$ is 50 mV above their V_{DSAT}. i.e., M_{1-4} must be in saturation region with 50 mV margin.

Verify that the operating point (bias currents, voltages, transconductances) are correctly set up before simulating the amplifier.

Present the following results.

Tables:

(a) Specification table with your specific values and all the component values.

(b) Table showing simulation results: closed loop dc gain, closed loop 3-dB bandwidth, unity loop gain frequency, phase margin, rms output noise (integrated from 10 kHz to 100 MHz), fraction of noise variance (integrated from 10 kHz to 100 MHz) contributed by R_i, R_f, first stage, second stage, and R_L, Opamp open loop dc gain, positive and negative slew rates, positive and negative swing limits, HD_3, supply voltage, current consumption. To find the opamp slew rates apply a large input step (from V_{cm} to $V_{cm}+V_{step}$) such that the first stage current is completely switched to one side.

To find HD_3, apply a sinusoidal input that results in a 1 V peak-peak output at a frequency that is 1/4th the bandwidth. Report HD_3, the ratio of the third harmonic to the fundamental (in dB).

Plots:

(a) Loop gain magnitude (dB) and phase (degrees). The unity loop gain frequency and phase margin must be marked. Break the loop as shown in Fig. 7.1(e) to simulate the loop gain. Use large L, C, e.g., $L = 10^6$ H, $C = 1$ F. The frequency range should be from $\sim 0.1\times$ dominant pole to where the loop gain is ~ -20 dB.

(b) Closed loop transfer function magnitude on a log-y scale showing the dc gain and the 3-dB bandwidth.

(c) Closed loop dc transfer curve. Vary V_i from $V_{cm} - 0.5$ V to $V_{cm} + 0.5$ V

(d) Small-signal step response: Output should step from $V_{cm} - 0.05$ V to $V_{cm} + 0.05$ V and back. Use a short rise time ~ 100 ps.

(e) Large-signal step response: Output should step from $V_{cm} - 0.5$ V to $V_{cm} + 0.5$ V and back. Use a short rise time ~ 100 ps. Check to see that the current is completely switched to one side in the first stage.

(f) Output noise PSD and the input referred noise PSD of the closed loop amplifier from 10 kHz to 100 MHz.

(g) Input referred noise PSD of the opamp from 10 kHz to 100 MHz.

(Not for submission):

- Remove the cascodes from the first stage, run the simulations and find out the differences
- Connect C_c to the drain of M_2 or M_4 instead of the drains of $M_{6,8}$. See if there is a difference in phase margin. You can also try connecting $C_c/2$ each to the drains of M_2 and M_4.