

EE6320 RF Integrated Circuits
Project: PA Design

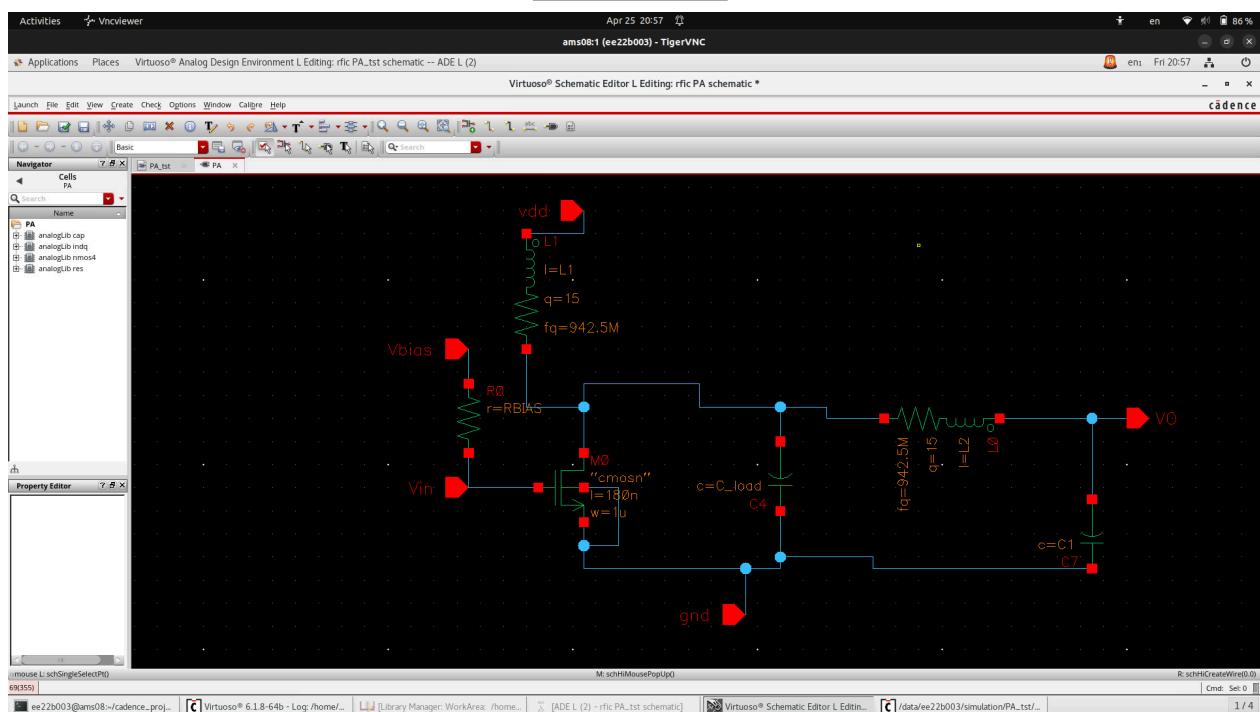
PA Performance Summary Table

Design Parameter	Design Metric	Performance	Specification
Output P1dB	$f_o = 925 \text{ MHz}$	13.001 dBm	$\geq +13 \text{ dBm}$
	$f_o = 942.5 \text{ MHz}$	13.03 dBm	$\geq +13 \text{ dBm}$
	$f_o = 960 \text{ MHz}$	13.05 dBm	$\geq +13 \text{ dBm}$
AM-PM Deviation (at P1dB)	$f_o = 925 \text{ MHz}$	-0.026 degrees	$\leq 3 \text{ degrees}$
	$f_o = 942.5 \text{ MHz}$	-0.013 degrees	$\leq 3 \text{ degrees}$
	$f_o = 960 \text{ MHz}$	0.017 degrees	$\leq 3 \text{ degrees}$
Voltage Gain (from Gate to Drain)	$f_o = 925 \text{ MHz}$	7.7	≥ 2
	$f_o = 942.5 \text{ MHz}$	7.735	≥ 2
	$f_o = 960 \text{ MHz}$	7.764	≥ 2
Power (at 942.5 MHz)	PA Average Consumption (excluding bias)	60.02mW	Minimize
	Bias Circuit Consumption	76 uW	Minimize
Other	Sum of all Capacitances (excluding ac coupling)	7.3 pF	-

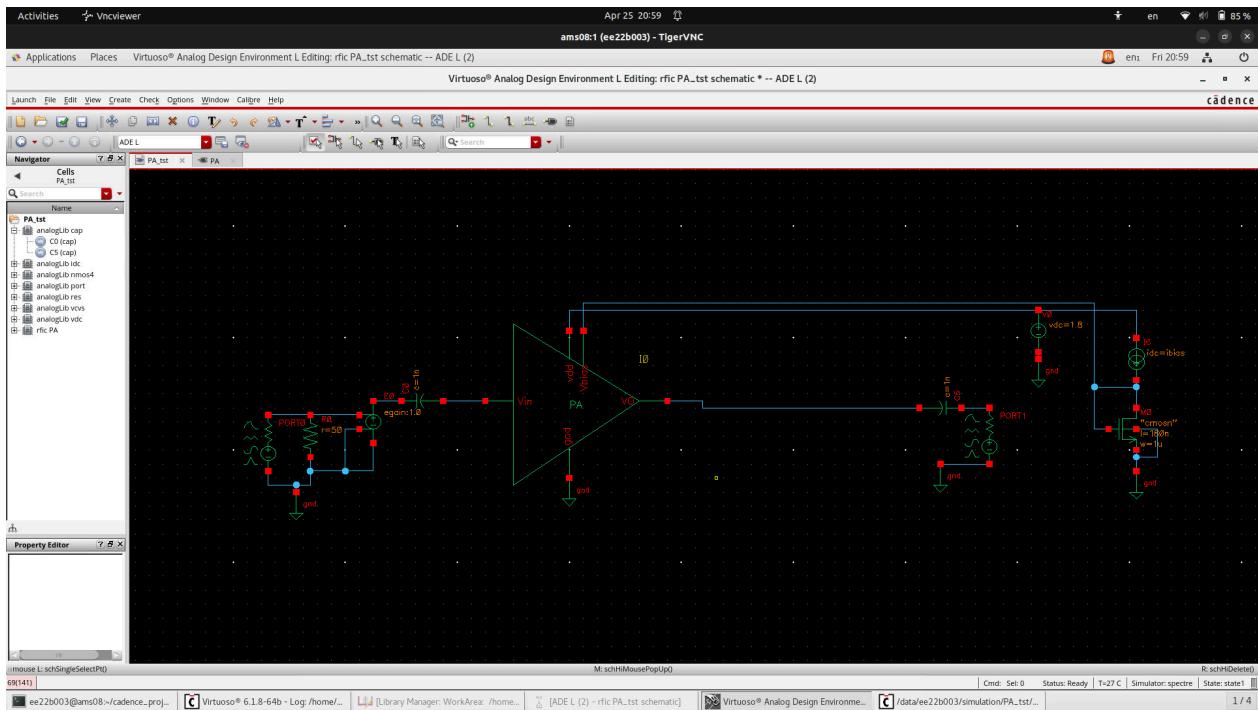
	Total Inductance Used	5.1 nH	-
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Roll No: <your roll number> EE22B003**

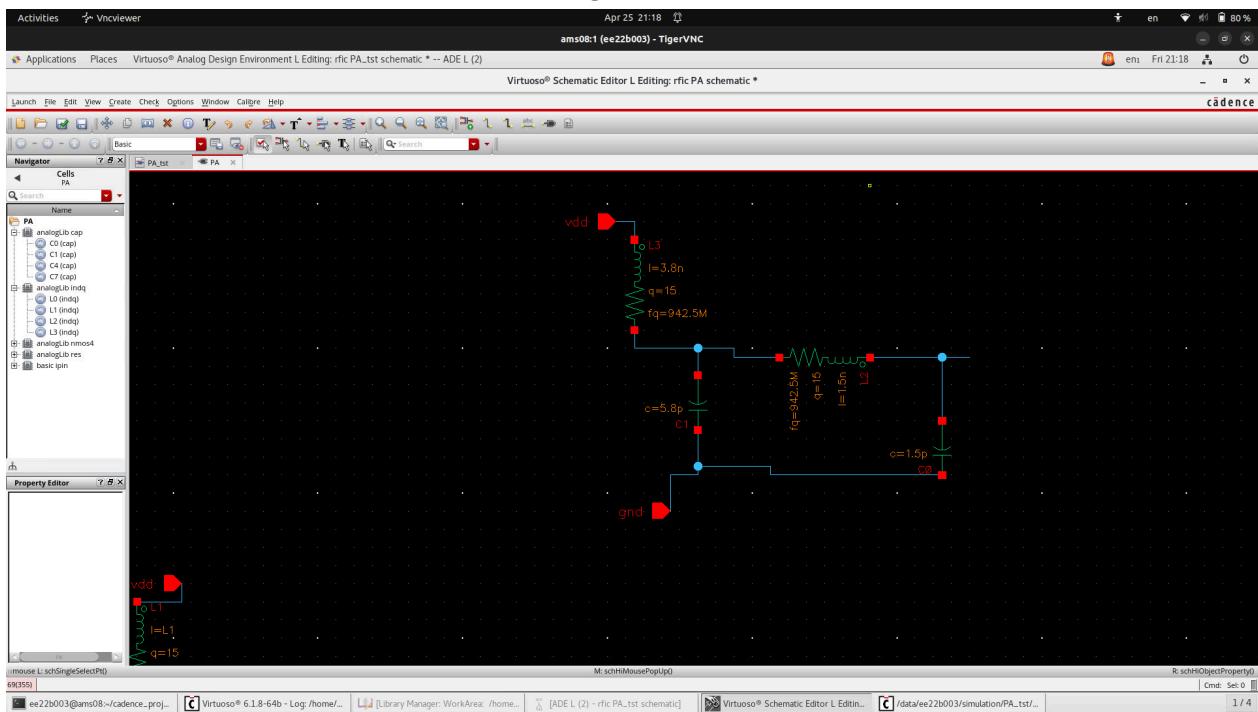
PA Schematic



PA Testbench



PA Matching Network Values



Component Values Table

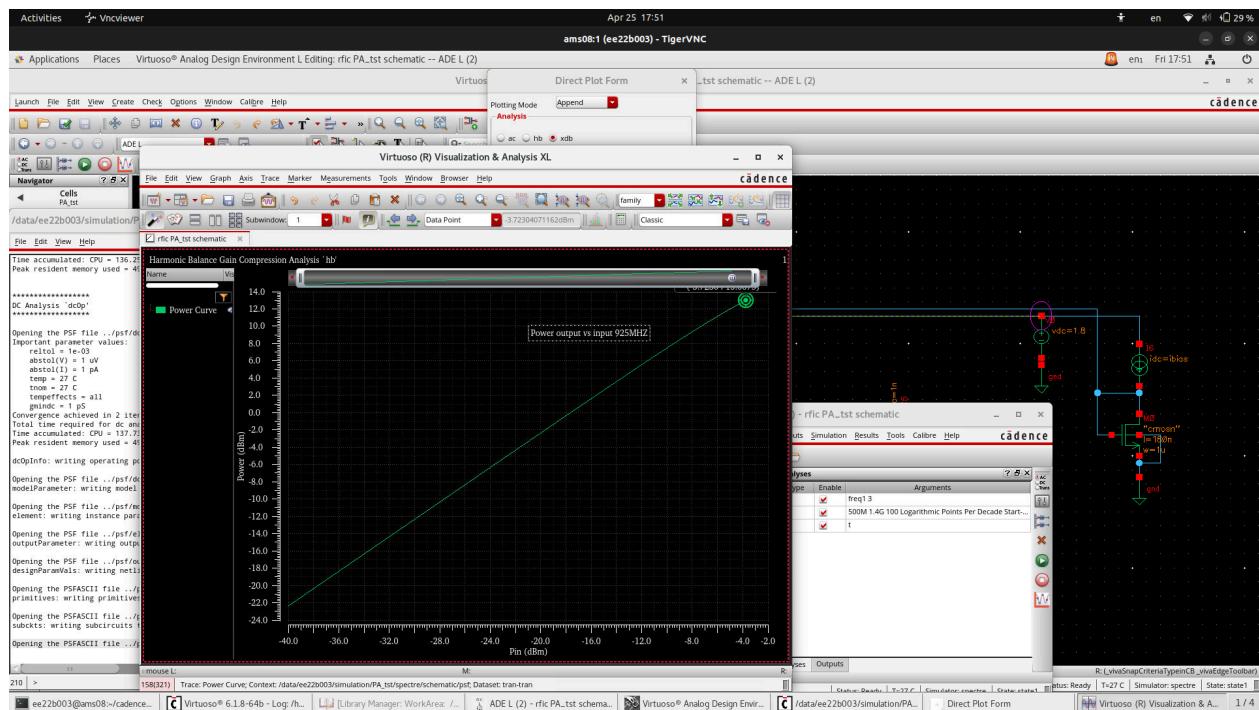
(W, L) MOS Amplifier = 592.4 μ , 180n

Choke inductor = 3.8 nH

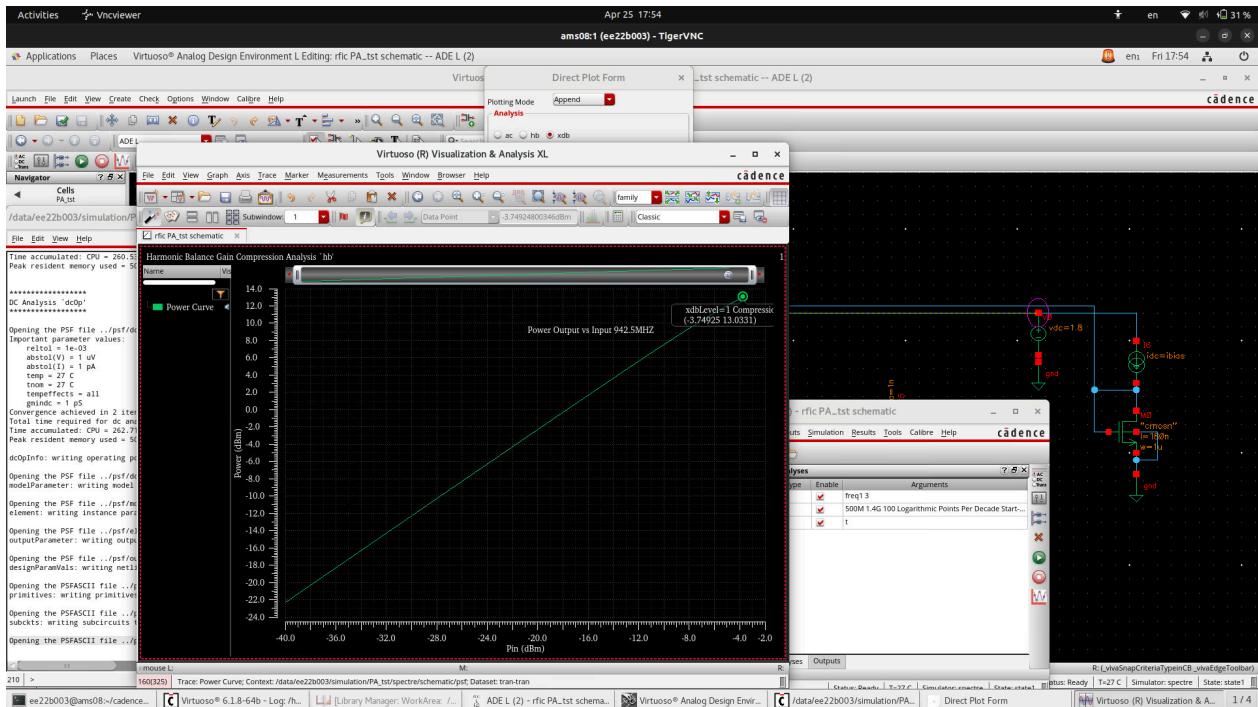
(W, L) Current Mirror MOS = 1u, 180n	Bias Current = 50uA
R_bias = 100 kΩ, C_coupling = 1 nF	V_DD = 1.8V, R_load = 50 Ohs

Output 1dB Compression Point Plots

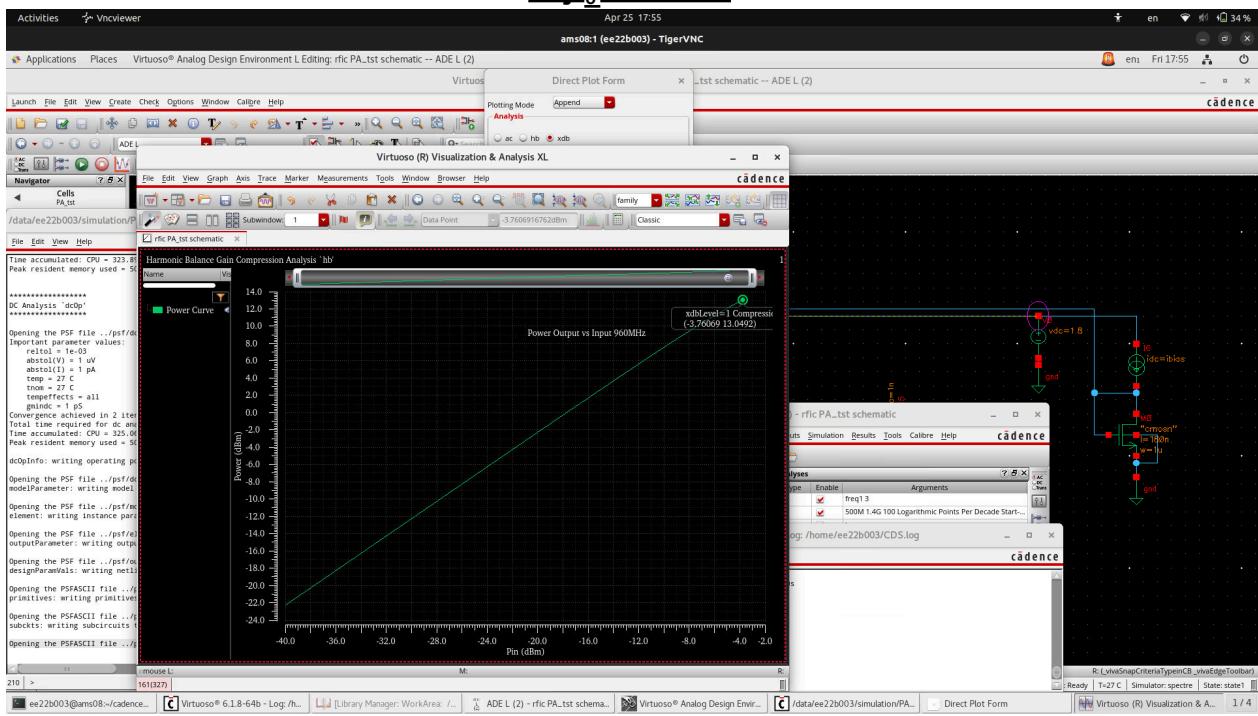
At $f_o = 925$ MHz



At $f_o = 942.5$ MHz



At $f_o = 960$ MHz



AM-PM Deviation Plots

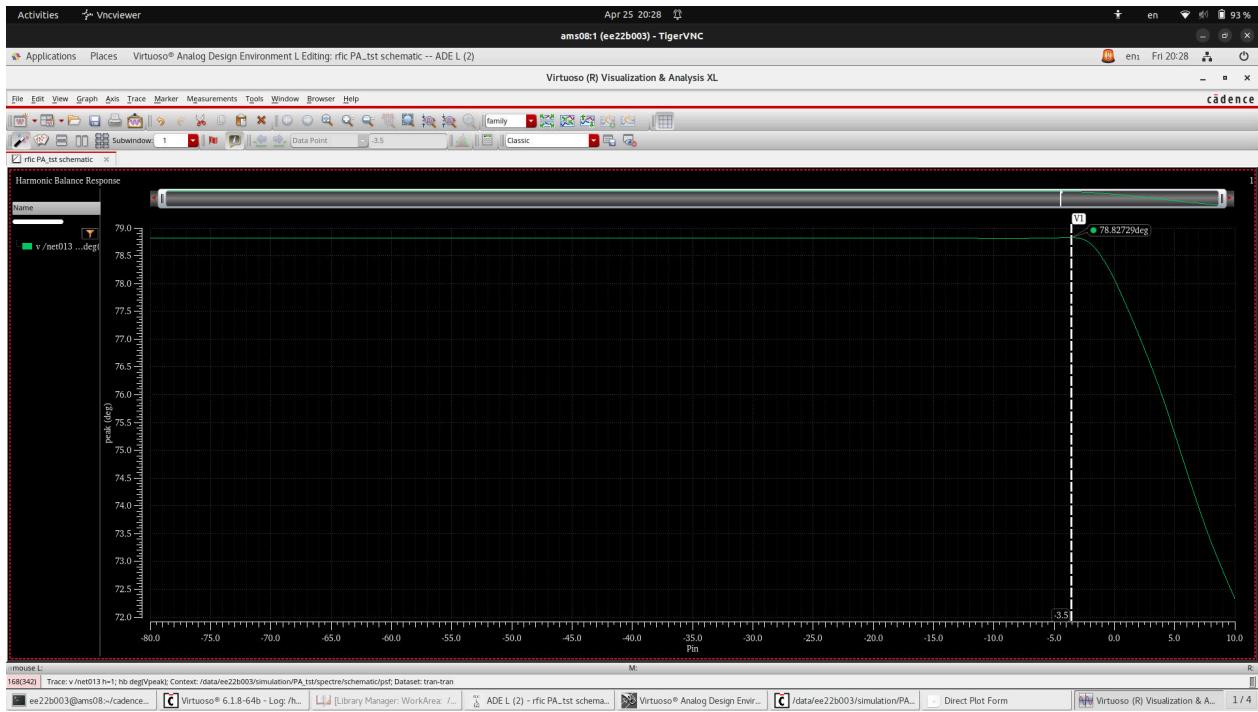
At $f_o = 925$ MHz



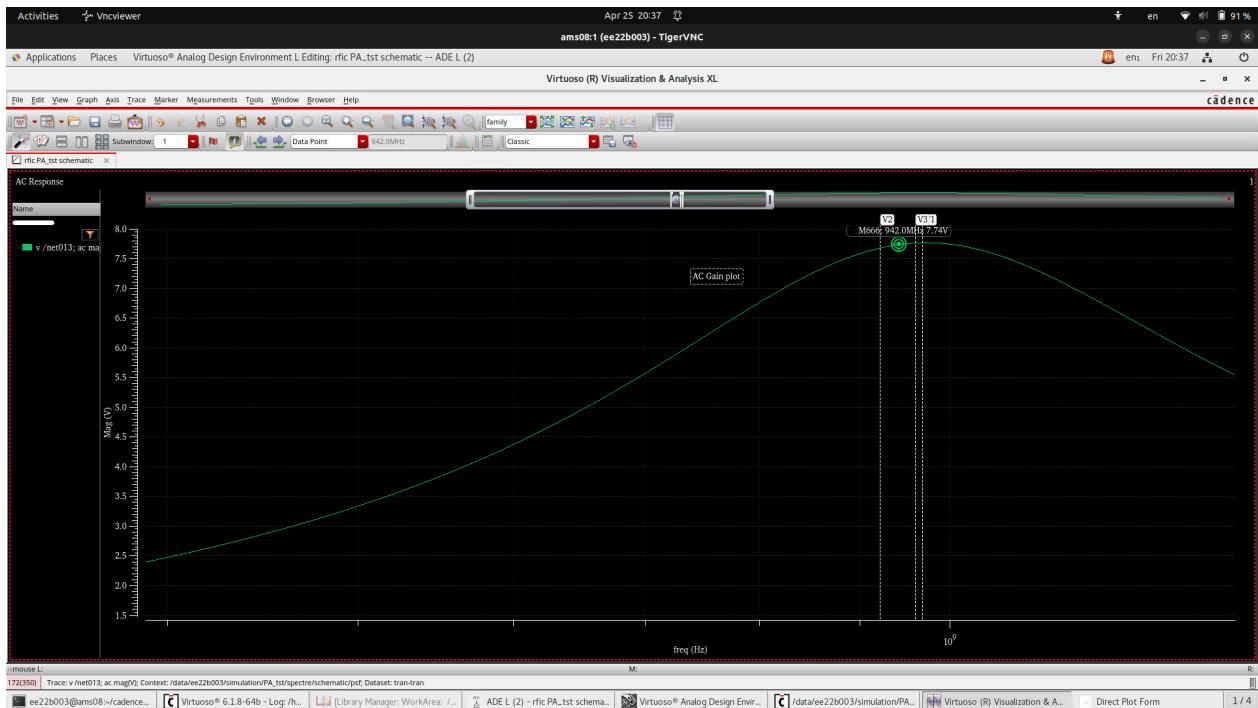
At $f_o = 942.5 \text{ MHz}$



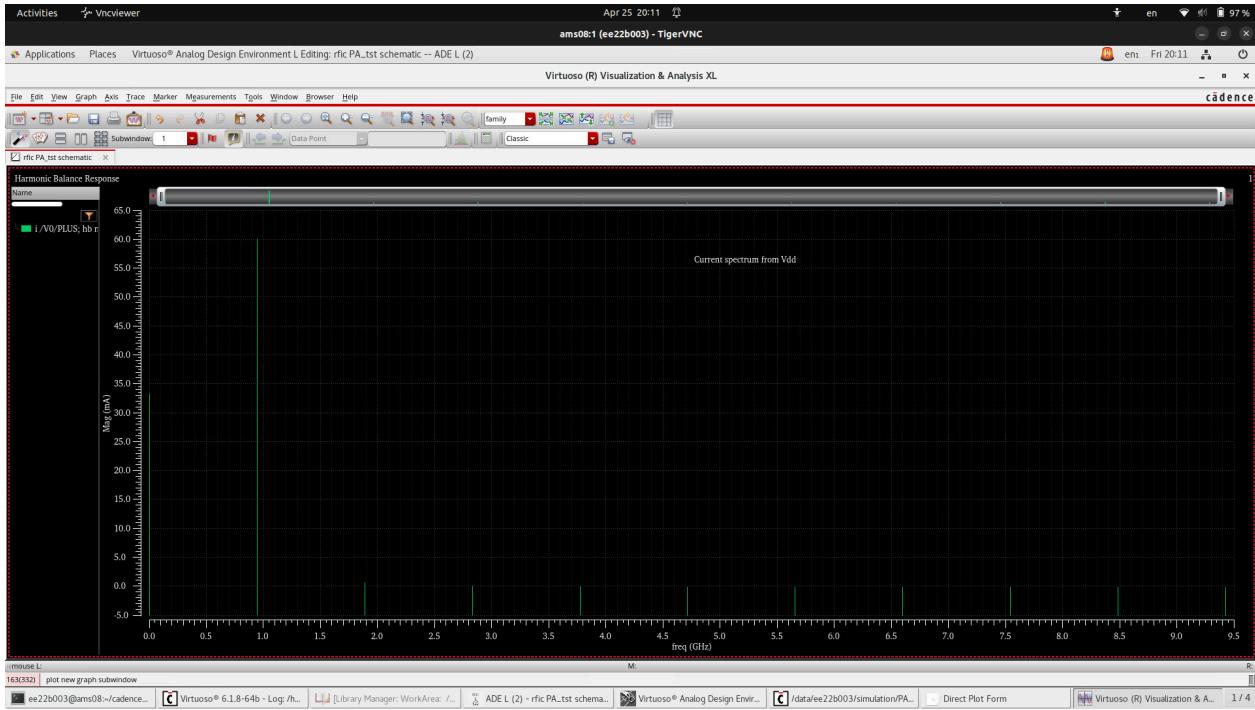
At $f_o = 960 \text{ MHz}$



**PA Voltage Gain Plot
(from Gate to Load)**



**Current through VDD Plot
(f_o = 942.5 MH and at P1dB)**



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Design Procedure

Assuming a V_{dsat} of around 100mV, $(V_{dd} - V_{dsat})^2 / (2 * P_{1dB_output}) = RL$ happens with $RL \sim 70$ Ohms. The required current is calculated as 26 mA, and transistor is sized to produce that current. Next a choke inductor is chosen which is small, but not too small that its parasitic parallel resistance at the operating frequency is of the same order as Load.

Then a capacitor is chosen to resonate with the inductor. This will reduce AM-PM conversion as well as increase the current flowing to load. Next a L match is used between the load and the drain of the mosfet, to convert the load resistance to a value that is slightly smaller (31-11j). The L and C values are adjusted to produce the maximum 1dB compression point output power. Then the mosfet width is increased gradually, until P_{1dB} crosses 13dB. At each mosfet width, the choke inductor and drain capacitor as well as L match network are adjusted for maximum power. This can be done using a parametric sweep in cadence.

Path to Project Files

[~/cadence_project/rfic](#)