EE6320 RF Integrated Circuits
Project: LNA Design

Performance Summary Table

Design metric	Measurement	Simulation Result	Requirement
Input matching	Worst case S11 in the specified band	-15.021	< –15dB
	Band over which S11 ≤ –15dB	890 to 980 MHz	925 to 960 MHz
Voltage Gain	Minimum Gain in the specified band	27.15dB	≥ 20dB
	Maximum Gain in the specified band	28.15dB	≥ 20dB
	Gain flatness in specified band [Max-Min Gain]	1dB	≤ 1dB
	3dB Bandwidth	78.5 MHz	-
	Load Capacitance [Differential]	200fF	200f F
Noise Figure	Maximum Noise Figure in the specified band	1.308dB	≤ 2dB
	Minimum Noise Figure in the specified band	1.368dB	-
	Band over which NF ≤ 3dB	151MHz to 1.42GHz	-
Linearity	IIP3 Tones used	942.5Mhz & 943.5MHz	-
	Input power used for extrapolation	-60	-
	Power of Fundamental Tone at output (at chosen input power)	-31.8dBm	-
	Power of IM3 Tone at output (at chosen input power)	-164dBm	-
	Extrapolated IIP3	8.3dBm	≥ 0 dBm
Power	LNA DC power consumption [Excluding Bias]	10.66 mW	Minimize
	Bias circuit power consumption (power supplied by i_bias)	21.96 uW	Minimize
Other	Sum of all on-chip inductances	10.16nH	-
	Sum of all off-chip inductances (2 Lg's)	19.1nH	-
	Sum of all resistances [Including bias]	2.0036 MOhms	-
	Sum of all capacitances [on chip]	10.29pF	-
	Simulator Used	Spectre	-

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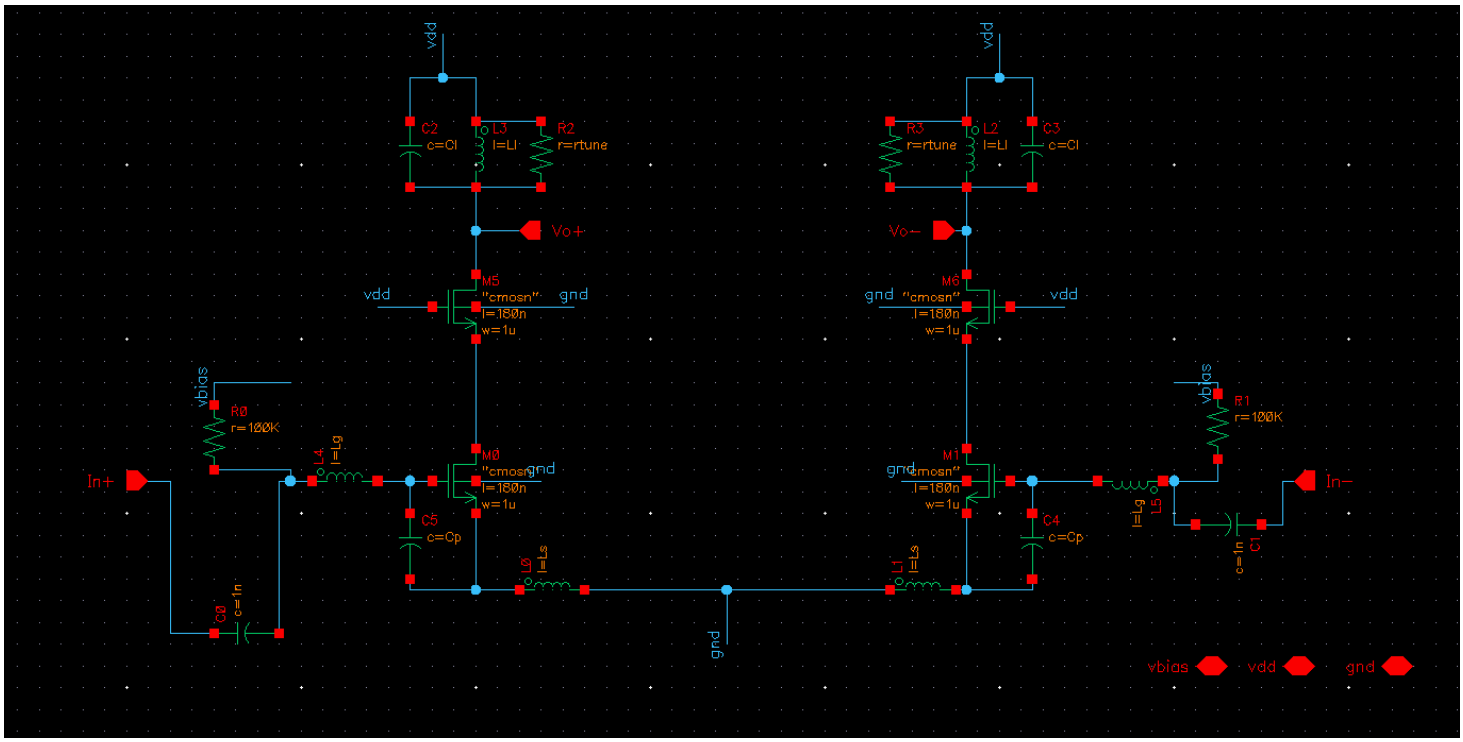
LNA Schematic



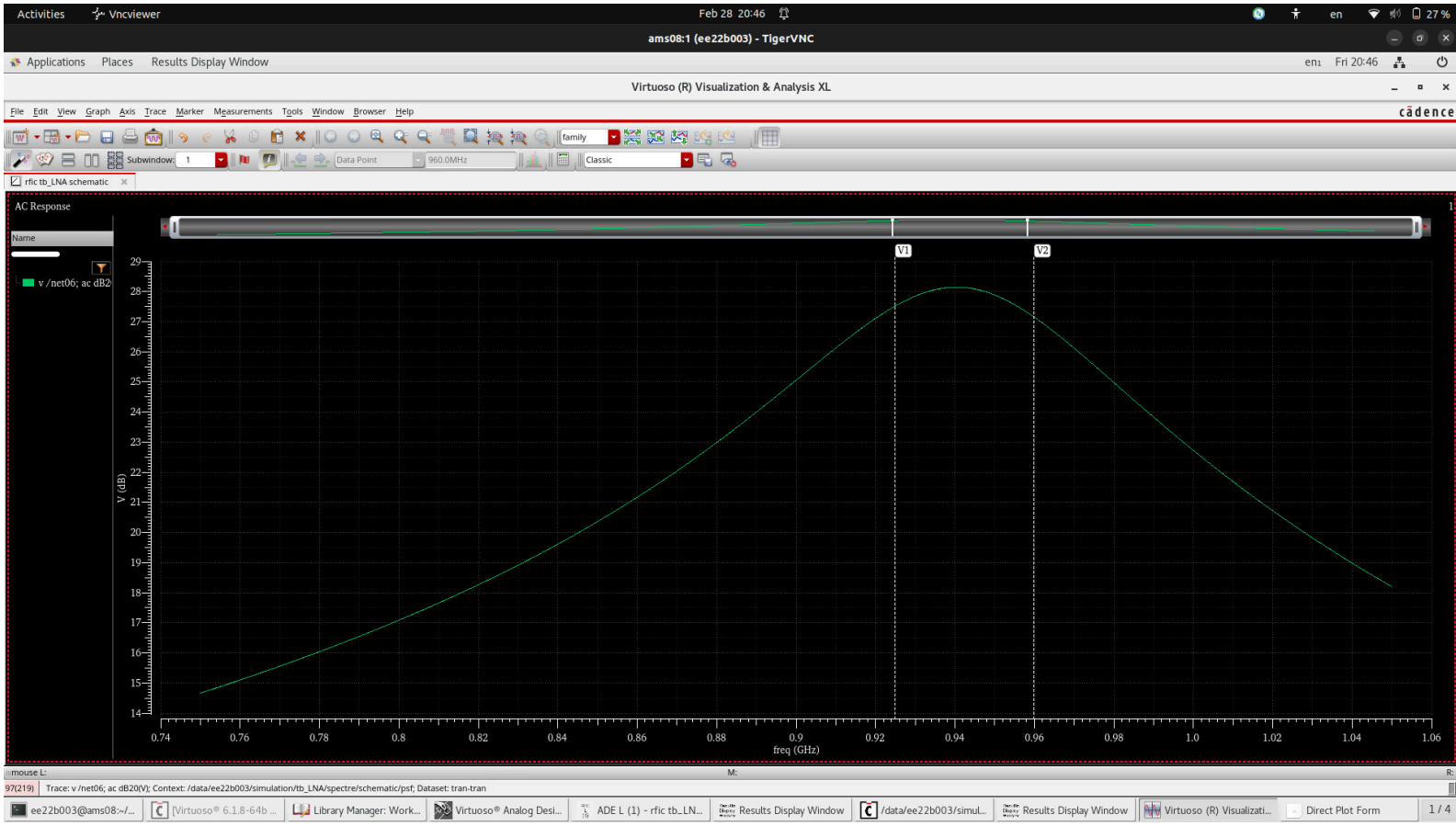
Component Values (one side values)		
Design Component	**Hand Calculated Value**	**Simulated Value**
Lg (gate inductance)	7.285 nH	9.55nH
Ls (source inductance)	2.02 nH	2.02nH
Ld (drain inductance)	3.51 nH	3.51nH
Rd* (drain resistance)	1.8 K Ohm	1.8 K Ohm
R_ls* (res. parallel with Ls)	NA	NA
Cgs (In addition to parasitic Cgg)	2.341pF	2.341pF

Fixed Constant Parameters

- **LNA CS MOS parameters: W = 210.5 um, L = 180 nm**
- **Current Mirror MOS parameters: W = 1um, L = 180nm**
- **I_bias (current): 12.2 uA**
- **LNA Cascode device CMOS parameters: W=450 um, L = 180nm**

*** - intrinsic resistance to respective inductors (doesn't come in net resistance on/off the chip)**

Gain Plot (from AC, only for representation)

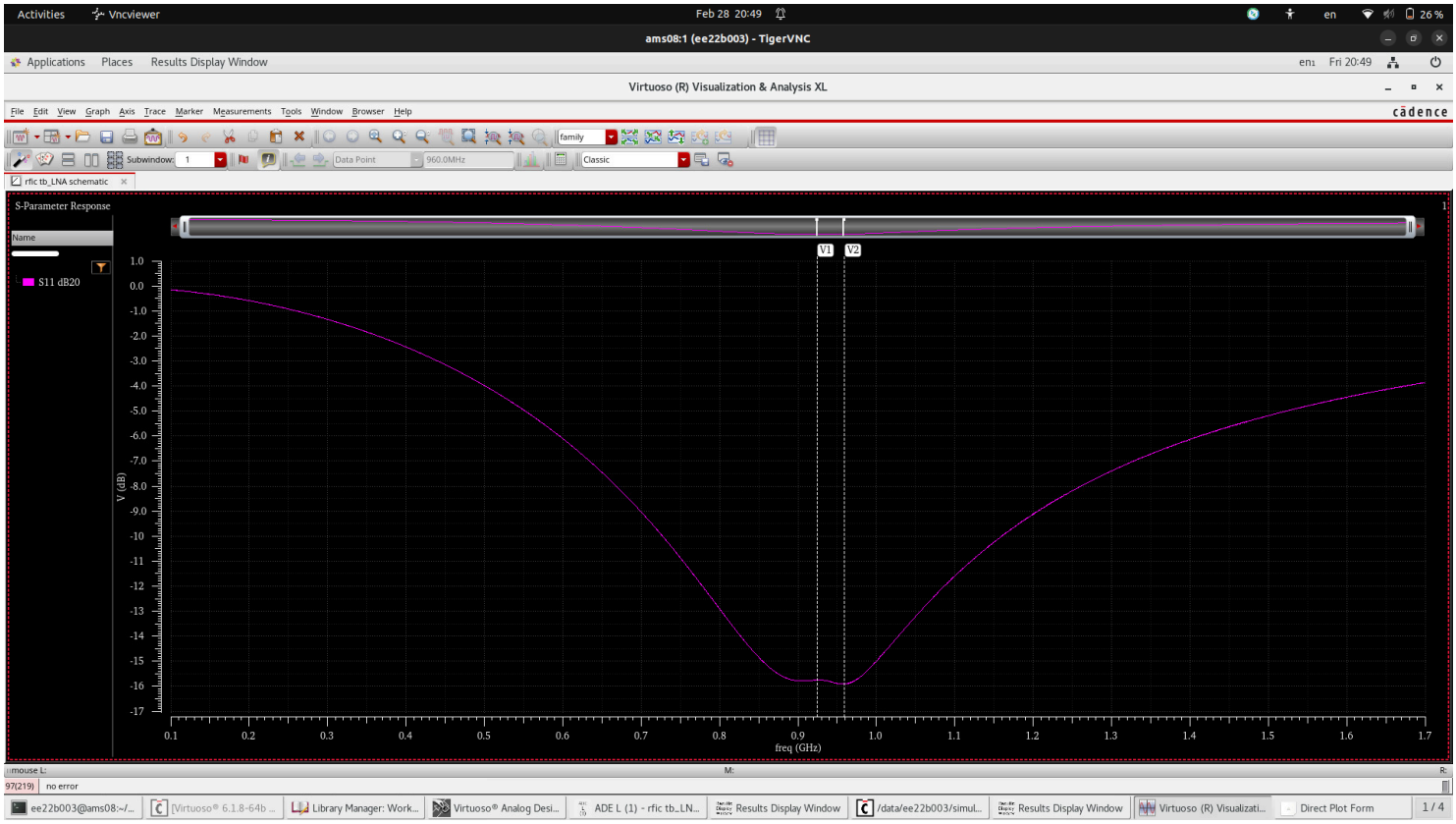

Activities
Vncviewer
Feb 28 20:46
en
27 %
ams08:1 (ee22b003) - TigerVNC
Applications
Places
Results Display Window
en1
Fri 20:46
Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
family
Subwindow:
Data Point
960.0MHz
Classic
rfic tb_LNA schematic
AC Response
Name
v /net06; ac dB2
V1
V2
V (dB)
freq (GHz)
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
0.74
0.76
0.78
0.8
0.82
0.84
0.86
0.88
0.9
0.92
0.94
0.96
0.98
1.0
1.02
1.04
1.06
mouse L:
M:
R:
97(219)
Trace: v /net06; ac dB20(V); Context: /data/ee22b003/simulation/tb_LNA/spectre/schematic/psf; Dataset: tran-tran
ee22b003@ams08:~/...
[Virtuoso® 6.1.8-64b ...
Library Manager: Work...
Virtuoso® Analog Desi...
ADE L (1) - rfic tb_LN...
Results Display Window
/data/ee22b003/simul...
Results Display Window
Virtuoso (R) Visualizati...
Direct Plot Form
1 / 4

Max Gain through hand calculation: = 13 = 22 dB

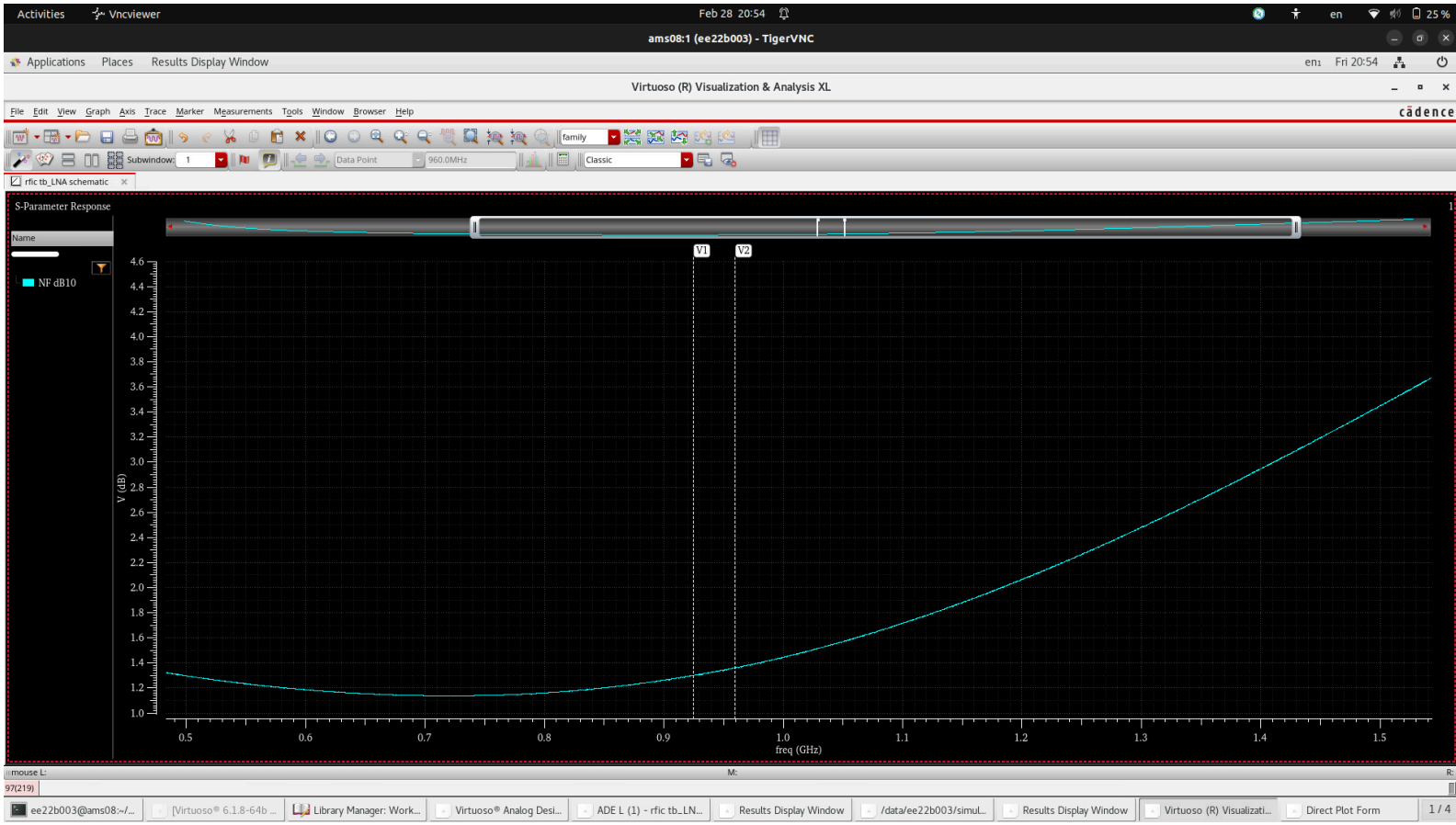
Max Gain from the simulation: 26 = 28.15 dB

From the figure, 3dB bandwidth comes out to be: 78 MHZ

S11 Plot



NF Plot


Activities
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en
25 %
ams08:1 (ee22b003) - TigerVNC
Applications
Places
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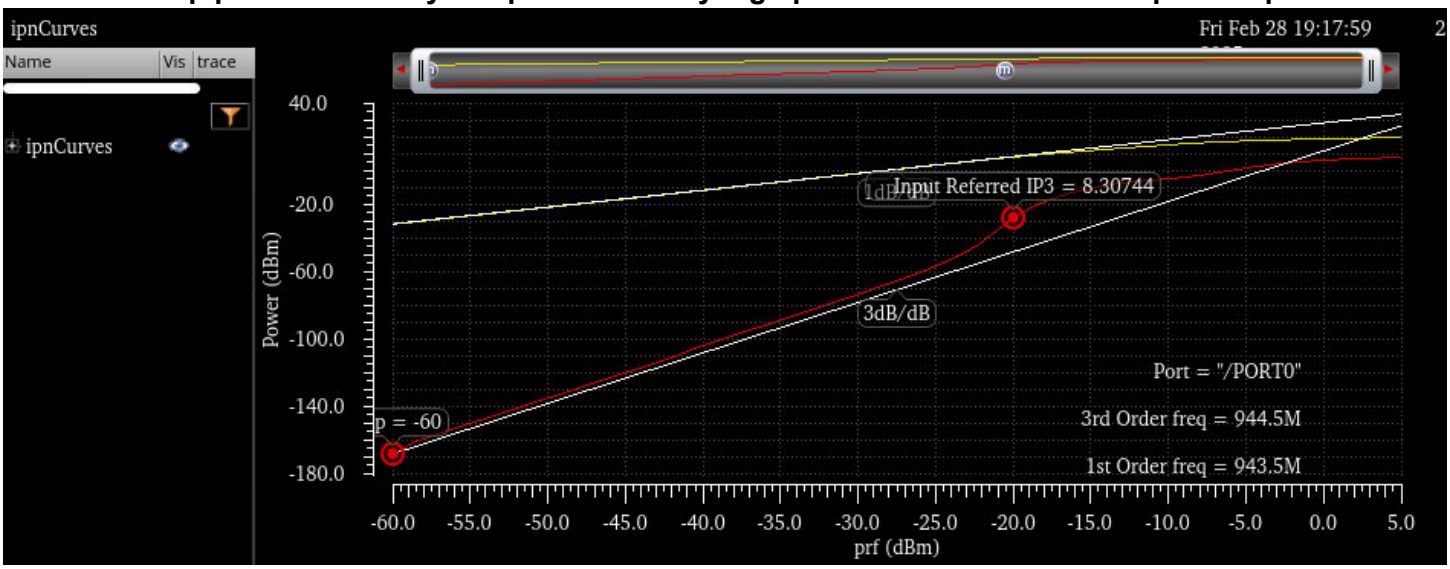
S-Parameter Response
Name
NF dB10
V1
V2
V (dB)
freq (GHz)
mouse L:
M:
R:
97(219)
ee22b003@ams08:~/...
[Virtuoso® 6.1.8-64b ...
Library Manager: Work...
Virtuoso® Analog Desi...
ADE L (1) - rfic tb_LN...
Results Display Window
/data/ee22b003/simul...
Results Display Window
Virtuoso (R) Visualizati...
Direct Plot Form
1 / 4

From hand calculations, NF comes out to be: 1.38

From the plot, NF comes out to be: 1.33

Linearity Plot (IIP3 Computation)

Sweep power from very low powers to very high power and show the extrapolated point

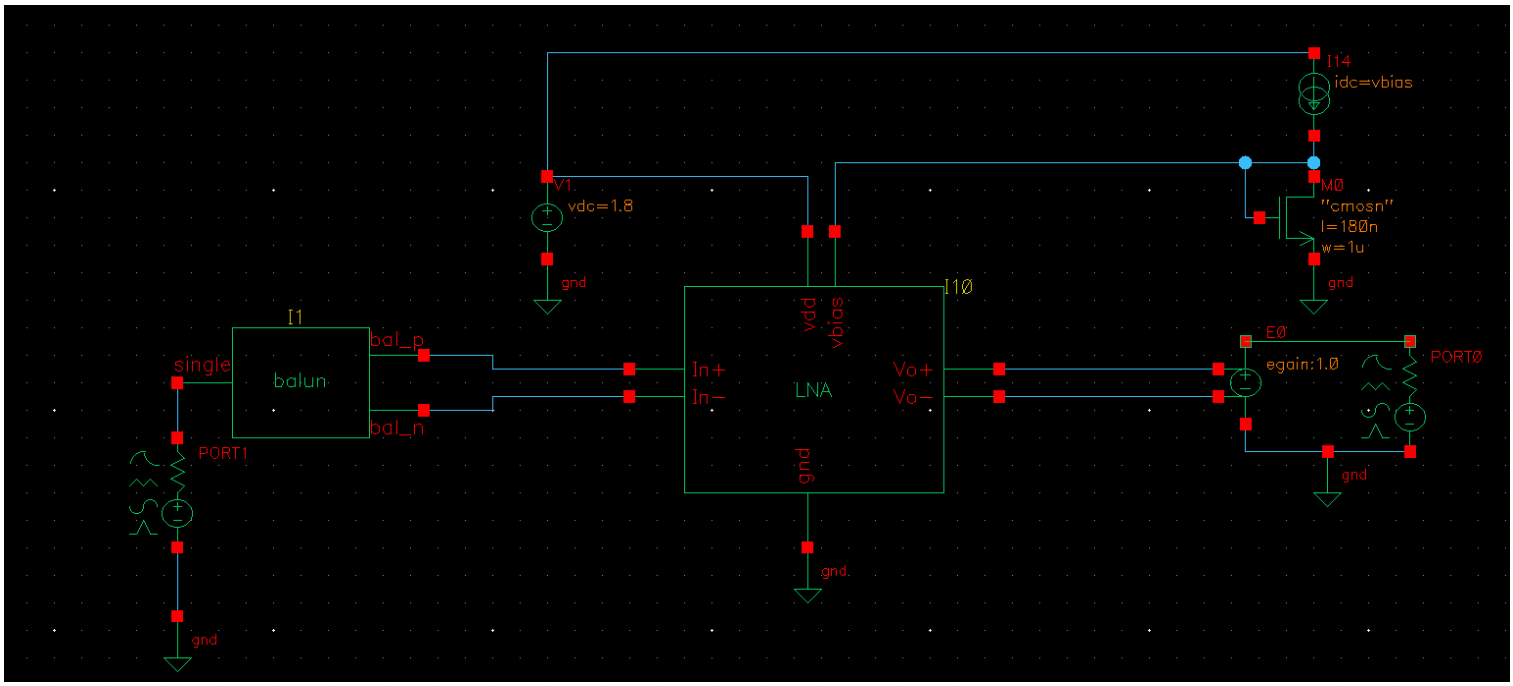


Tones used: 942.5 & 943.5 MHz

IIP3 point comes out to be: 8.3dB

LNA Testbench

This testbench is used for all calculations



Comments

. Due to the presence of parasitic capacitances at drain and source of the LNA mosfet, the required Lg is higher than what was hand calculated

. Due to coupling between input and output resonating circuit through parasitic resistances, 2 minima are seen in S11 vs frequency plot, this improves the bandwidth over which input match is seen due to pole splitting, as well as makes S11 rise more sharply outside the band, despite a really low input quality factor

. Noise figure is minimum at 721 MHz rather than 942.5 MHz. Thus there is a tradeoff between noise figure and input matching

. Noise figure can be improved slightly at the expense of power by increasing bias current

. S11 can also be made smaller in the band by increasing power.

Hand Calculations done for the Project

https://github.com/Armmanoj/RFIC

Design Procedure

. First a moderately small bias point is chosen, and the transistor characterized at that bias.

. Then Lg and extra Cgs is chosen such that the transistor width, and hence power consumption is minimized, while keeping Lg constrained to be lesser than a feasible limit. Adding a Cgs in parallel trades of the transit frequency seen by source inductor for less power and noise. This sets W of CS mosfet too. Qin can be constrained too, to optimize S11. This is done using a python script.

. Then load inductance is chosen such that its parasitic resistance gives more than required gain, so that quality factor can be tuned to get the required gain flatness at the output

. Extra capacitance is added at the output to resonate the load inductor

. Cascode device is chosen with width twice as much as the CS stage mosfet to maximize isolation

. Now Lg is adjusted to account for other parasitic capacitances, and bias voltage is reduced in steps, repeating the above processes till S11 requirement cannot be met anymore. This minimizes power

Path- cadence_project/rfic/LNA