

EE6320 RFIC Project: VCO Design

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Component Values

Component	Value
W,L Current Mirror mosfet	22u, 180n
W,L tail Mosfet	60un 180n
L on each side	1.96 nH
Extra capacitance between Vop and Voq	0fF
C1,C2 Capacitor bank	120fF, 60fF
W,L Cross Coupled Mosfet	180u
Varactor W,L	370u, 1u
Vbias, Ibias	960.9mV,3.67mA

Component Values for Divide by 2 circuit

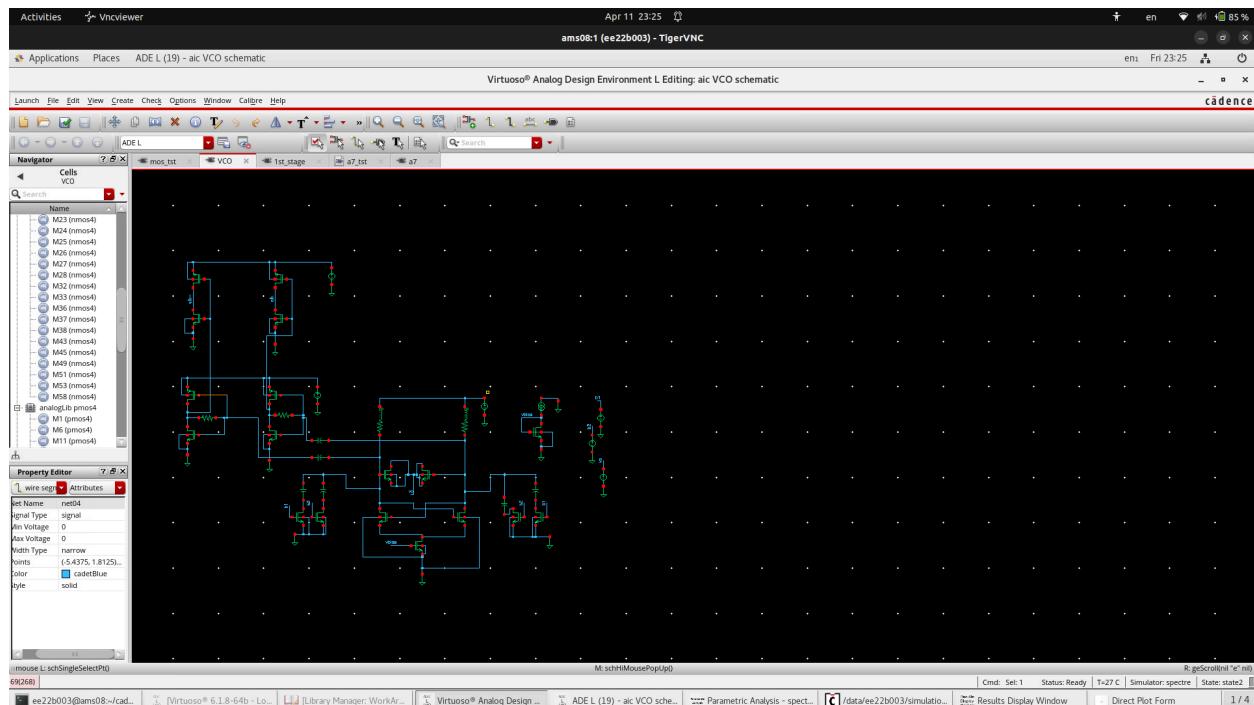
Component	Values
VCO to frequency divider Buffer inverter's multiplier	20
Clock divider multiplier	7
PMOS and NMOS widths	2u,1u
DC coupling R	10 k ohms
C coupling	2pF
Power consumption of frequency Divider Circuit	5.04(FF) mW + 3.9 (Buffer) mW = 8.94mW

VCO Performance Summary

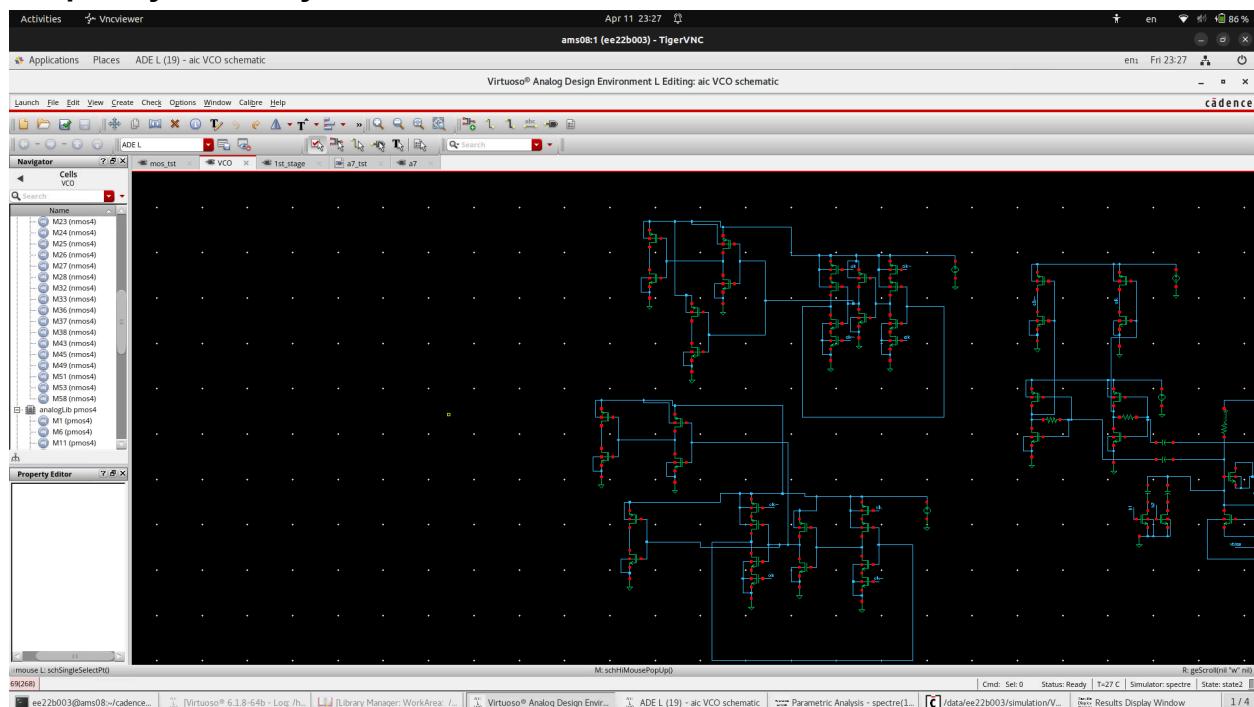
Design Parameter	Design Metric	Performance	Specification
Output Amplitude	-	1.375V	$\geq 1.2V$
Phase noise(1 MHz offset)	freq=1850MHz	-128.9 dBc	$= -125 \text{ dBc}$

	freq=1885 MHz	-131 dBc	=<-125 dBc
	freq=1920 MHz	-128.8dBc	=<-125 dBc
Phase noise (20 MHz offset)	freq=1850 MHz	-159.3 dBc	=<-157 dBc
	freq=1885 MHz	-158.2 dBc	=<-157 dBc
	freq=1920 MHz	-156.6dBc	=<-157 dBc
Tuning Range	Total Tuning Range	920-982 MHz	925-960 MHz
	Voltage range in fine tuning	0.8-1.2 V	-
	Average KVCO	98.7 MHz/V	>=70MHz/V
	Total number of bits in coarse tuning	2	-
	% variation in KVCO	43.5% (Max KVCO-Min KVCO)/2	-
Power Consumption	VCO avg power consumption (excluding bias)	16.66 mW	minimal
	Bias circuit avg power consumption	6.6 mW	minimal
Other	Sum of all capacitances in capacitor bank	180 fF	-
	Net inductance used	3.92nH	-
	Simpulator	Spectre	-

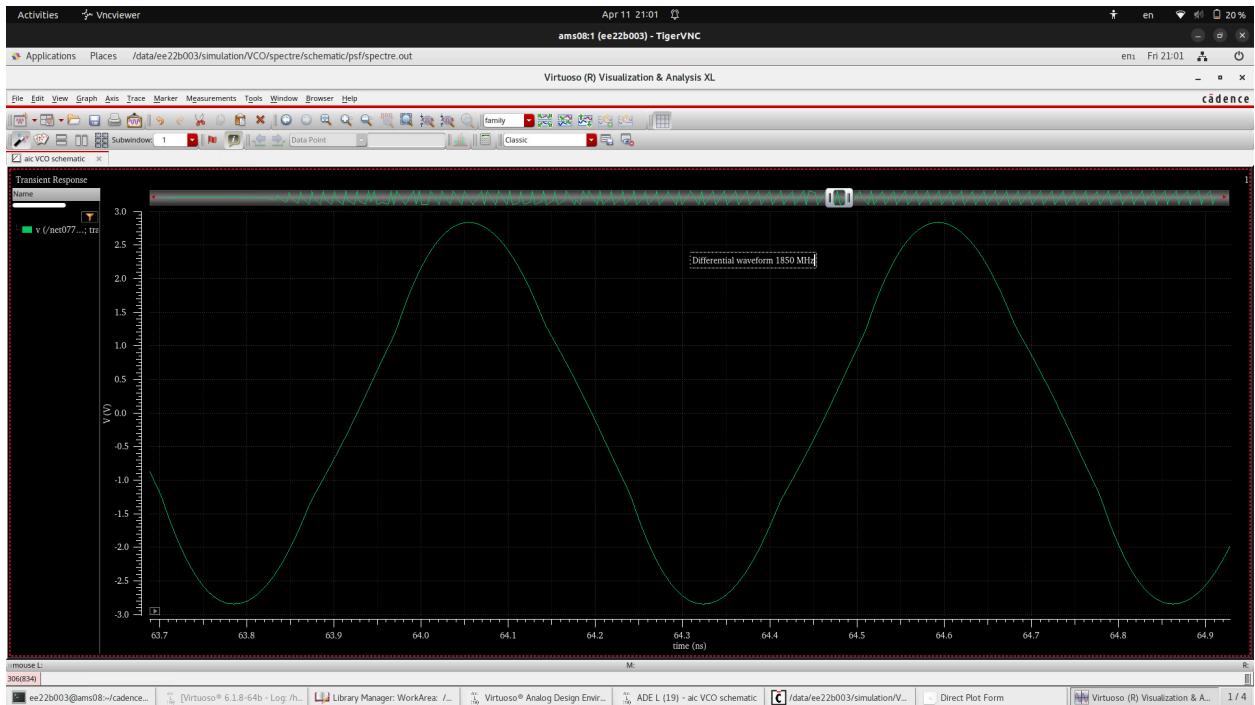
VCO Schematic



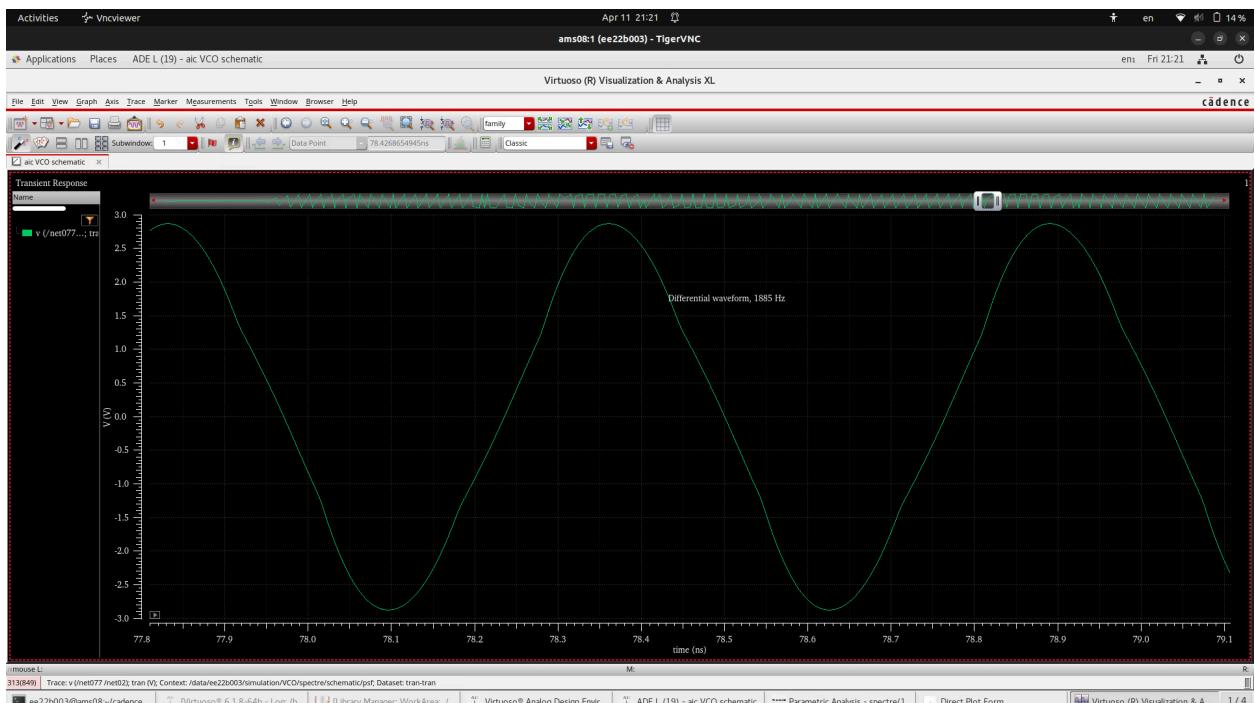
Frequency Divide by 2 circuit



Differential waveform for 1850 MHz

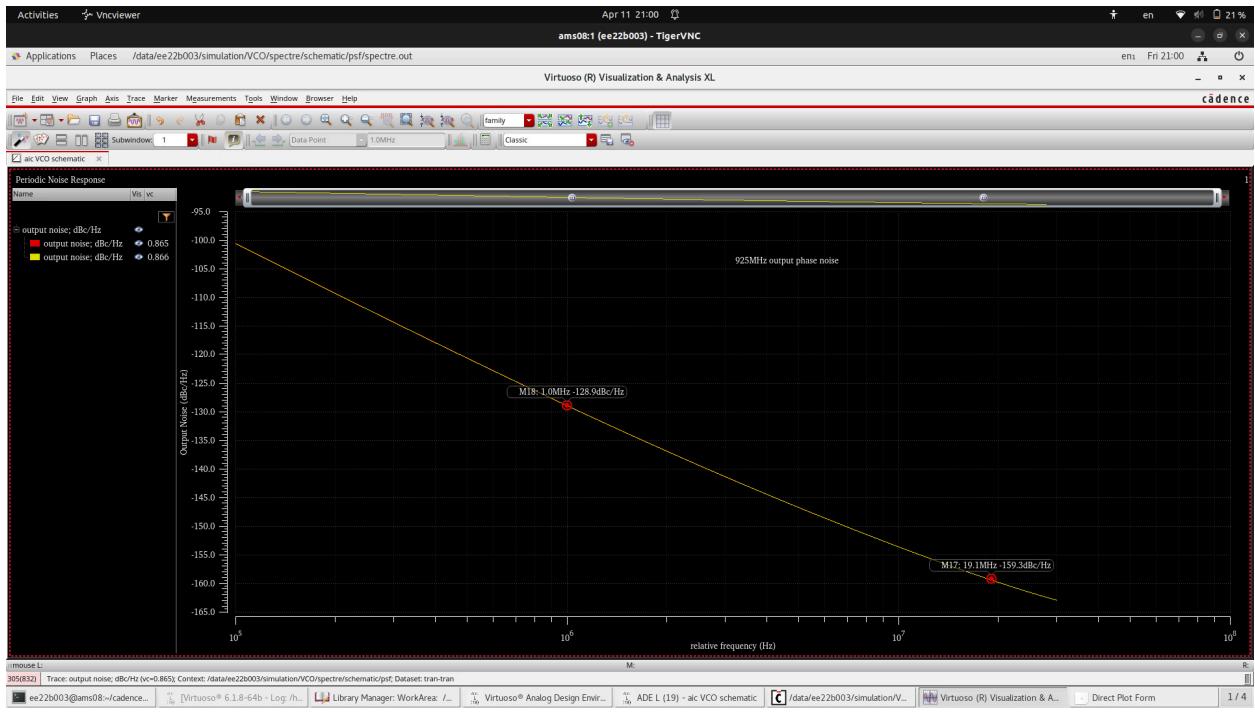


Differential waveform for 1885 MHz

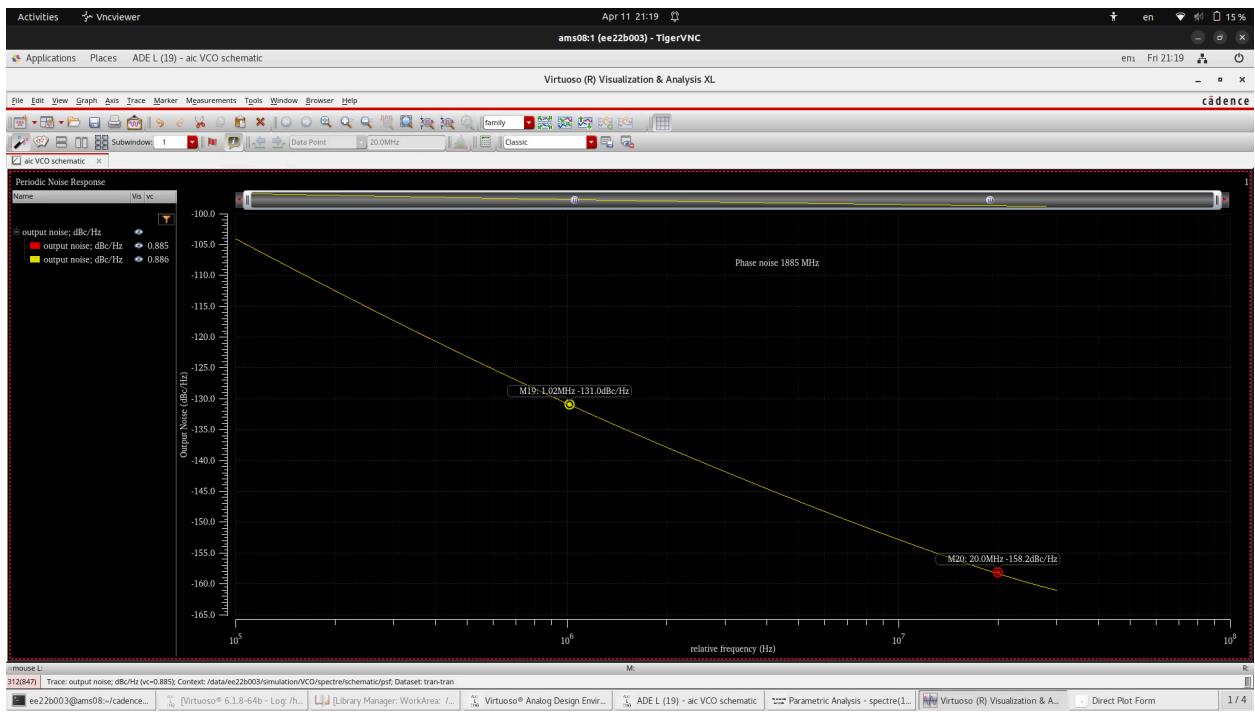


Differential waveform for 1950 MHz

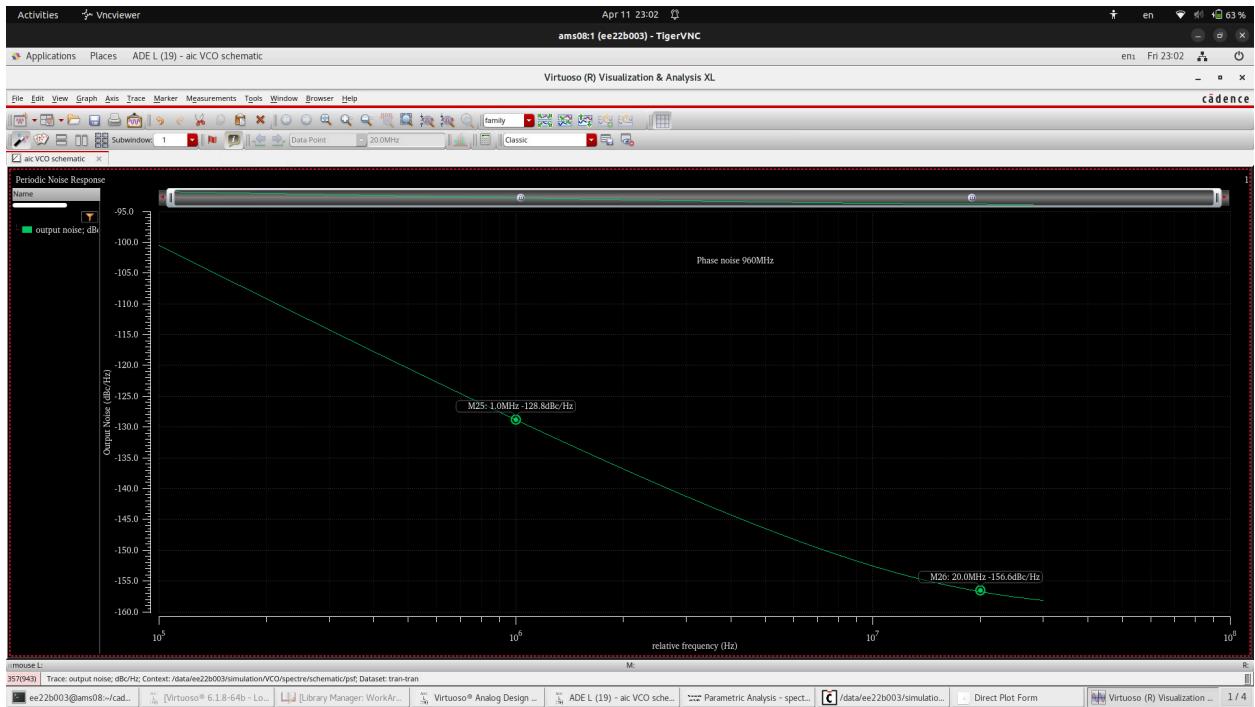
Phase noise 925 MHz



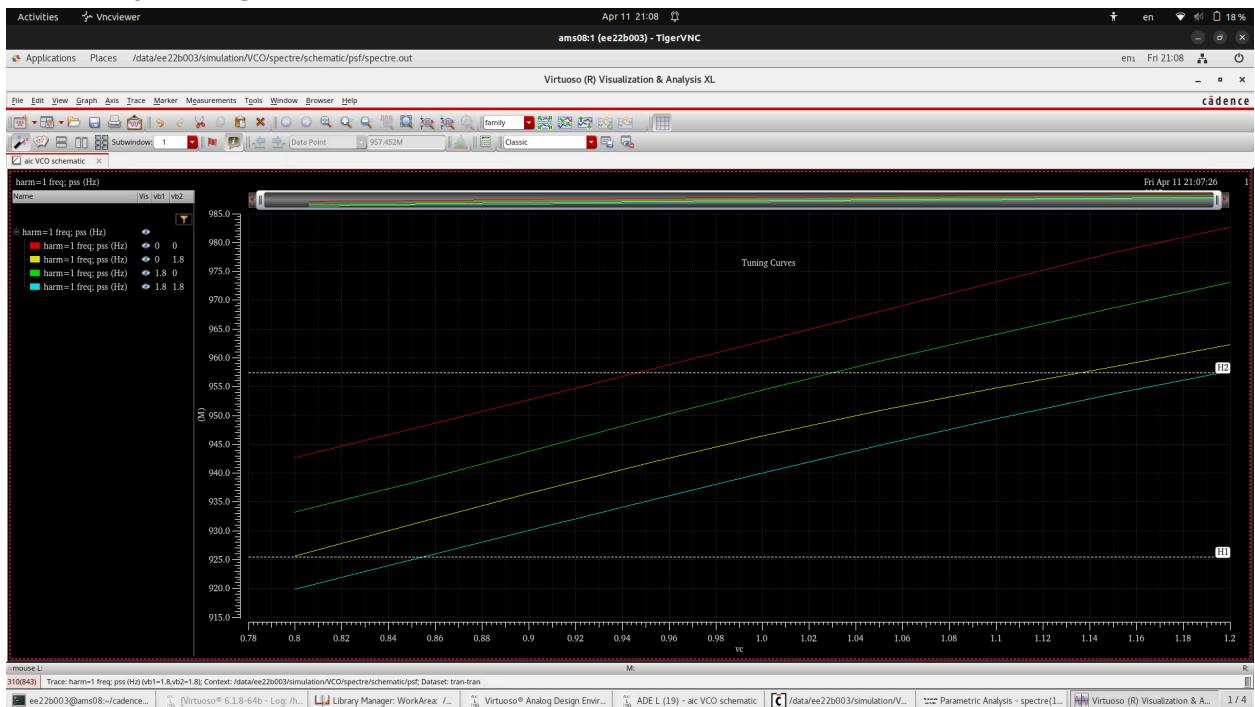
Phase noise 942.5 MHz



Phase noise 960 MHz



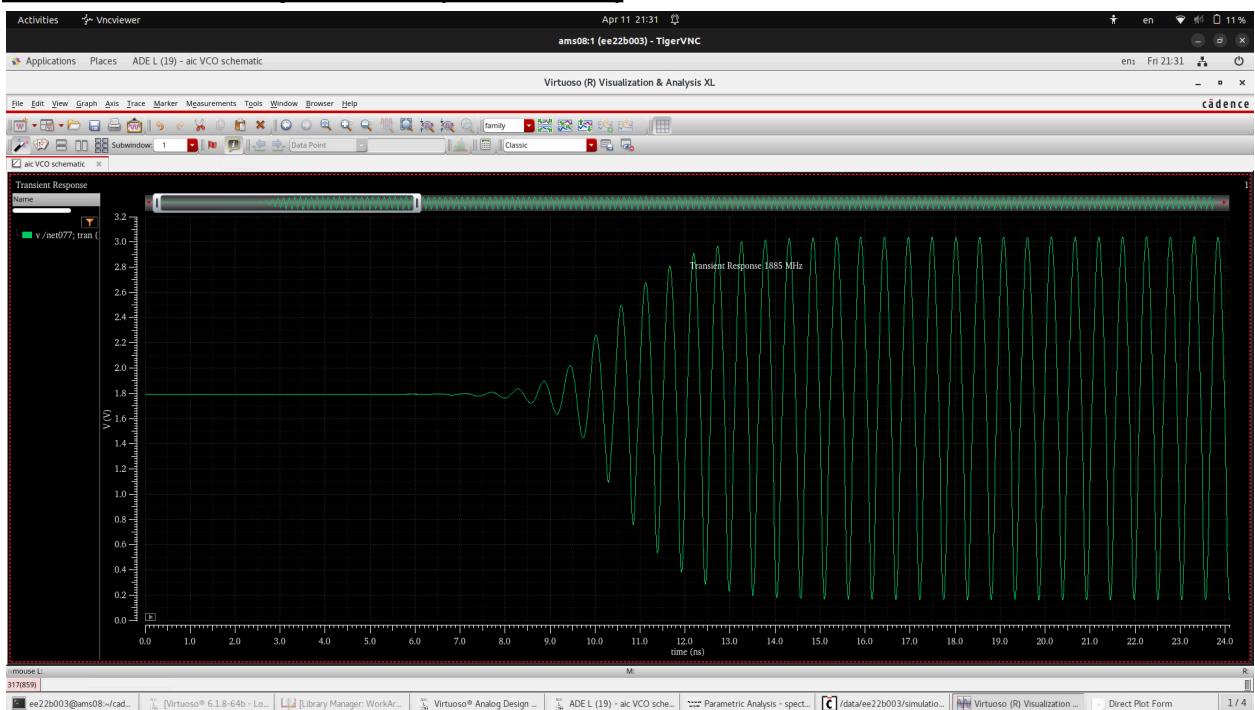
Frequency Tuning plots



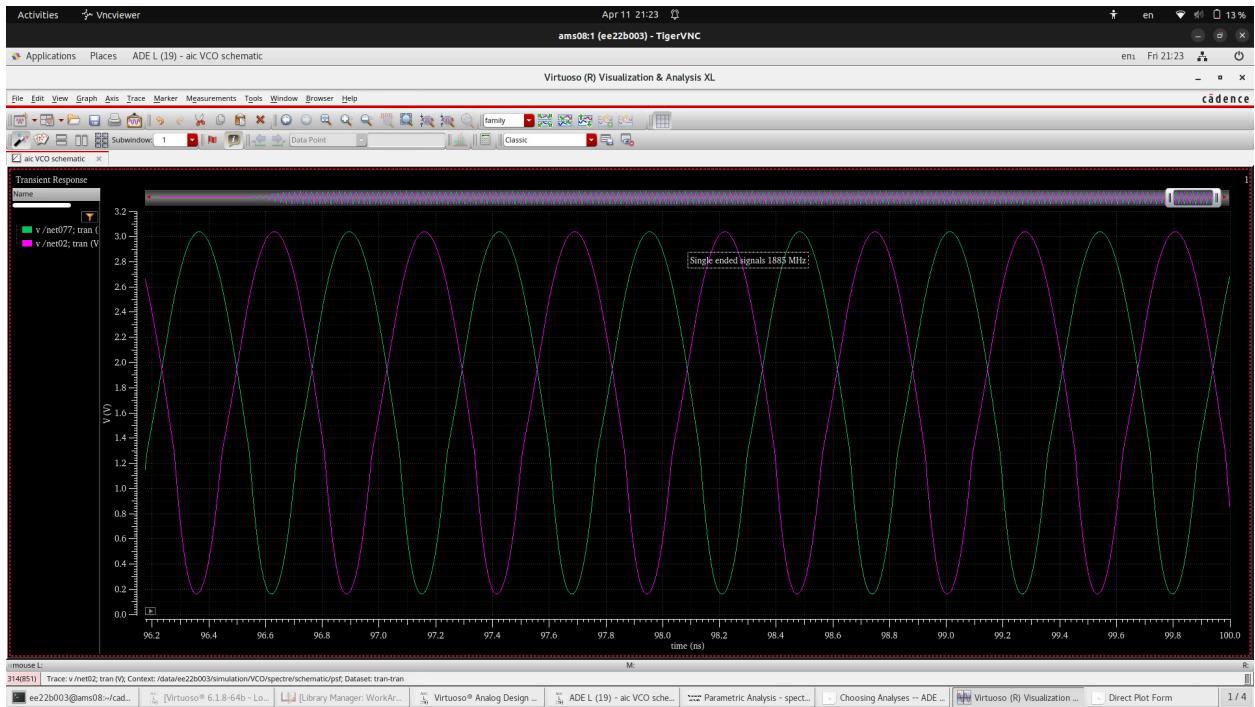
KVCO Plot



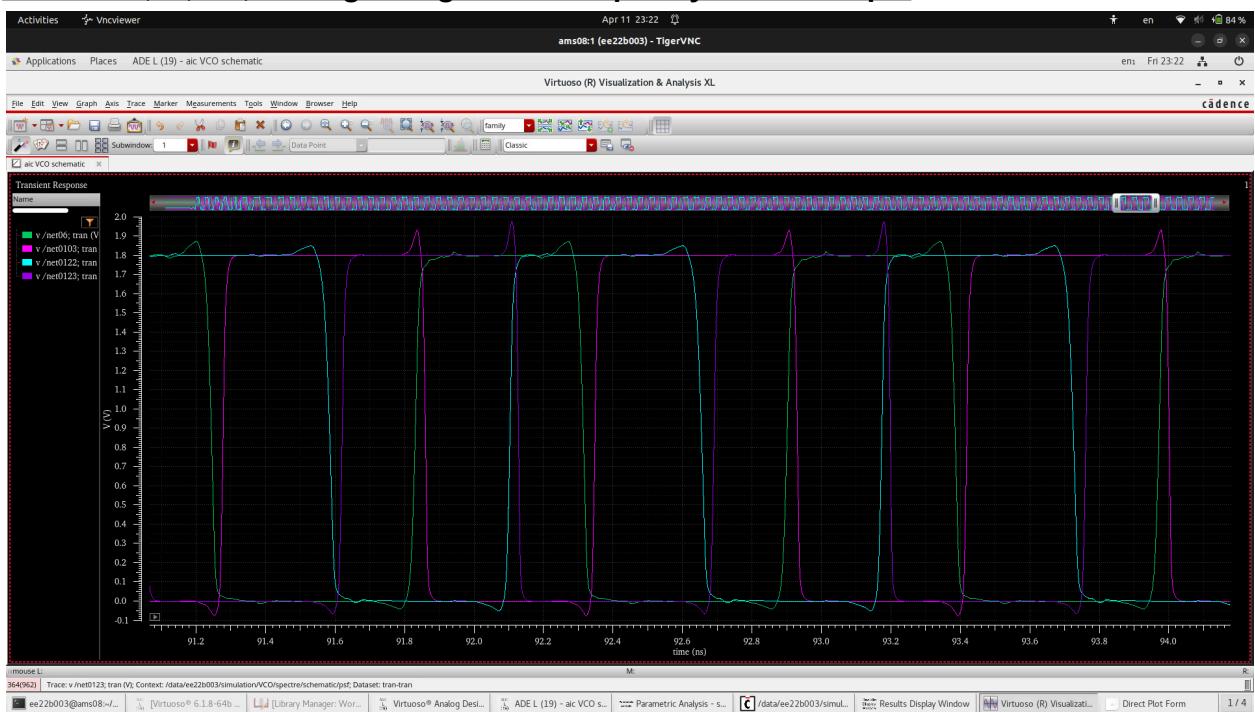
Initial Transient Response Plot (at 1885 MHz)



Single ended Output PPlot (at 1885 MHz)



Plots for 0,90,180,270 degree signals of Frequency Divider output



Design Procedure

I began with designing for achieving phase noise spec, but gave 40dBc margin to account for tail current thermal noise and contribution of clock divider circuit to phase noise. Using Abidi's noise formula, a tank resistance at resonant frequency of 351 ohms was found to give -165dBc of phase noise at 1MHz offset. Using $L=R/(Q^*W)$, and taking Q as 15, $L=1.96\text{ nH}$. Next using

$\omega_0 = 1/\sqrt{LC}$, capacitance was calculated as 3.59pF. Assuming drain capacitances of mosfet as well as capacitor banks add negligible corrections, a varactor of 370u width and 1u length gives this capacitance. Then from 1.2V amplitude requirement, IT is calculated as 10mA. The cross coupled pair's width is chosen as something larger than the tails current, to give a large gm for the given tail current, again to maximize amplitude. Then 2 buffers are added at VCO output, with a coupling capacitor to shift the waveforms DC value to 0.9 V. The sizes are chosen as half of tail mosfet size, to minimize loading of VCO by buffer, as well as not being too small and adding to phase noise. The clock divider circuit is chosen as TSPC latch based divider due the low number of transistors involved, simplicity and hence suitability for high frequencies. As each buffer drives 4 mosfets, the latch is sized smaller than buffer, 7/20th the size mosfets. Then the bias current and current mirror mosfets are scaled up till phase noise constraint is met

Path to project files: ~/cadence_project/aic/VCO