CA Homework4 Report

B08902055 李英華

Development Environment

- Operating System: Windows 10
- Compiler: iverilog

Module Explanation

CPU

Use structural modeling to map the input and output of each module so that they can connect together as a datapath of single cycle processor.

Control

Reads `opcode` from the instruction to determine the control signal (`ALUOp` , `ALUSrc` , `RegWrite`) for Registers, ALU_Control, and MUX32.

ALU_Control

In this homework, we only have two type of `ALUOp` , `Rtype_ALUOp` and `Itype_ALUOp` . For R-type, we use both `funct7` and `funct3` to determine `ALUCtrl` ; for I-type, we use `funct3` to determine `ALUCtrl` , as `addi` and `srai` have different `funct3` .

Sign_Extend

Sign extension into 32 bit number for the immediate value. `imm[11]` is copied 20 times since we need to extend the sign.

ALU

Do arithmetic according to `ALUCtrl` . For the `SRAI_ALUCtrl` , there's only `imm[4:0]` , so we left shift 27 and then right shift 27 bits to get the exact `imm[4:0]` field.

Adder

No branch or jump instruction in this homework, so simply `PC` + 4.

MUX32

According to `ALUSrc` , select between immediate or `reg[rs2]`