HÁSKÓLI ÍSLANDS
Iðnaðarverkfræði-, vélaverkfræði- og tölvunarfræðideild

TÖL401G: Stýrikerfi / Operating Systems · Vormisseri 2022

Assignments 25–26 · Due 19.4.2022, 13:00

You can consider these two assignments as some sort of bonus assignments: solutions will not be presented, otherwise they can be used to contribute to the final grade just like all the other assignments.

Assignment 25

At a disk scheduler (being part of the operating system's disk driver), the following accesses to cylinders of a hard disk have queued up in the following order (entries to the left arrived earlier than those to the right):

2, 15, 20, 18, 13, 4, 30, 35, 26.

Just before, the read/write head of the hard disk has moved from cylinder 8 to cylinder 18, i.e. it is currently located at cylinder 18 and the above queued up request for cylinder 18 is a new request that has not been processed, yet. The following head scheduling strategies are used:

1. First Come, First Served (FCFS),
2. Shortest Seek First (SSF),
3. Elevator/Scan[1].

- For each of the strategies, write down in which order the cylinder accesses are scheduled.
- What is the distance (in terms of cylinders) that the disk head has to move for each of the strategies?
- To move the head from one cylinder to a directly neighbored cylinder, 0.1 ms are required for each cylinder that the head is moved. Once the head has reached the target position, a further delay of 1 ms is introduced, because the head has to "settle" (i.e. a fine positioning is made and the controller has to wait until vibrations/oscillations (due to the movement and sudden stop) of the head settled).
  - How much time does head positioning consume for each of the strategies and the above accesses?
  - To get a feeling how slow I/O is in comparison to a CPU: How many instructions may a CPU with a clock rate of 1 GHz execute during each of these head positioning times? (For simplicity, assume that during one CPU clock cycle, exactly one instruction can be executed.)

[1] Use the unfair variant where a further request for the current cylinder is processed immediately as part of the current "from-high-to-low-cylinder" or "from-low-to-high-cylinder" phase (instead of having to wait to be processed in the forthcoming phase that will be used for the way back).

Assignment 26

Consider the connection of an input/output (I/O) device (or it's device controller respectively) to the main memory:

1. *Briefly* describe why I/O is a *bottleneck* with respect to the overall performance of a computer system!
2. *Briefly* describe why in a *multiprogramming* system *Direct Memory Access* (DMA) helps (in comparison to *Programmed I/O* (PIO)) to reduce the I/O bottleneck!
3. *Briefly* describe why in a *monoprogramming* system DMA does not reduce the I/O bottleneck!

If PIO is used, two approaches are possible to find out whether data needs to be transferred by the OS's devicer driver between the I/O device controller and the RAM:

- *Polling* (the CPU asks periodically the I/O device controller (busy waiting)),
- *Interrupt* (the I/O device controller raises an interrupt).

Which approach should be used if

4. the I/O device is fast? Justify your answer!
5. the I/O device is slow? Justify your answer!

Preparation

Read chapters 12 and 13 as preparation where we will cover material for assignments which are based on these chapters. Examples from each chapter will be explained in videos that are available in Canvas via "Panopto". Report via Ed Discussion any questions that you have, so that we can clarify.