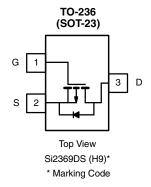




# P-Channel 30 V (D-S) MOSFET

| PRODUCT SUMMARY     |                                      |                                 |                       |  |  |
|---------------------|--------------------------------------|---------------------------------|-----------------------|--|--|
| V <sub>DS</sub> (V) | $R_{DS(on)}\left(\Omega\right)$ Max. | I <sub>D</sub> (A) <sup>a</sup> | Q <sub>g</sub> (Typ.) |  |  |
|                     | 0.029 at V <sub>GS</sub> = - 10 V    | - 7.6                           |                       |  |  |
| - 30                | 0.034 at V <sub>GS</sub> = - 6 V     | - 7                             | 11.4 nC               |  |  |
|                     | 0.040 at V <sub>GS</sub> = - 4.5 V   | - 6.5                           |                       |  |  |



#### **Ordering Information:**

Si2369DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

#### **FEATURES**

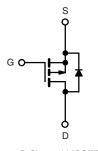
- TrenchFET® Power MOSFET
- 100 % R<sub>g</sub> Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



COMPLIANT HALOGEN FREE

#### **APPLICATIONS**

- · For Mobile Computing
  - Load Switch
  - Notebook Adaptor Switch
  - DC/DC Converter



P-Channel MOSFET

| <b>ABSOLUTE MAXIMUM RATIN</b>                      | IGS (T <sub>A</sub> = 25 °C | , unless othe                     | rwise noted)         |      |
|--|-----------------------------|-----------------------------------|----------------------|------|
| Parameter  |                             | Symbol                            | Limit                | Unit |
| Drain-Source Voltage                               |                             | V <sub>DS</sub>                   | - 30                 | V    |
| Gate-Source Voltage                                |                             | V <sub>GS</sub>                   | ± 20                 | V    |
|  | T <sub>C</sub> = 25 °C      |                                   | - 7.6                |      |
| Continuous Dunin Comment (T., 150 °C)              | T <sub>C</sub> = 70 °C      | 1 . [                             | - 6.1                |      |
| Continuous Drain Current (T <sub>J</sub> = 150 °C) | T <sub>A</sub> = 25 °C      | l lo                              | - 5.4 <sup>b,c</sup> |      |
|  | T <sub>A</sub> = 70 °C      | i – –                             | - 4.3 <sup>b,c</sup> | Α    |
| Pulsed Drain Current (t = 100 μs)                  |                             | I <sub>DM</sub>                   | - 80                 |      |
| Continuos Course Drain Diada Current               | T <sub>C</sub> = 25 °C      |                                   | - 2.1                |      |
| Continous Source-Drain Diode Current               | T <sub>A</sub> = 25 °C      | l <sub>S</sub> –                  | - 1 <sup>b,c</sup>   |      |
|  | T <sub>C</sub> = 25 °C      |                                   | 2.5                  |      |
| Maximum Power Dissipation                          | T <sub>C</sub> = 70 °C      | 1 5 [                             | 1.6                  | 10/  |
|  | T <sub>A</sub> = 25 °C      | P <sub>D</sub>                    | 1.25 <sup>b,c</sup>  | W    |
|  | T <sub>A</sub> = 70 °C      | 1 – –                             | 0.8 <sup>b,c</sup>   |      |
| Operating Junction and Storage Temperature Range   |                             | T <sub>J</sub> , T <sub>stg</sub> | - 55 to 150          | °C   |

| THERMAL RESISTANCE RATINGS                 |              |                   |         |         |      |
|--|--------------|-------------------|---------|---------|------|
| Parameter                                  |              | Symbol            | Typical | Maximum | Unit |
| Maximum Junction-to-Ambient <sup>b,d</sup> | t ≤ 5 s      | R <sub>thJA</sub> | 75      | 100     | °C/W |
| Maximum Junction-to-Foot (Drain)           | Steady State | R <sub>thJF</sub> | 40      | 50      | C/VV |

#### Notes:

- a. Based on  $T_C$  = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. Maximum under steady state conditions is 166 °C/W.

## Vishay Siliconix



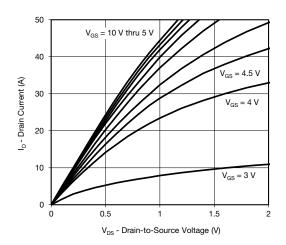
| Parameter         Symbol         Test Conditions         Min.         Typ.         Max.           Static         Drain-Source Breakdown Voltage         V <sub>DS</sub> V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA         -30 <th< th=""><th>V mV/°C V nA μA</th></th<>   | V mV/°C V nA μA |
|---|-----------------|
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$   | wV/°C V nA      |
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$   | wV/°C V nA      |
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$   | V<br>nA         |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$  | V<br>nA         |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$  | nA              |
|   |                 |
|   | μΑ              |
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$   | μΑ              |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$  | 1               |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$  | Α               |
|   |                 |
| Forward Transconductance <sup>a</sup> $g_{fs}$ $V_{DS} = -15 \text{ V}, I_D = -5.4 \text{ A}$ 18 $\begin{array}{ c c c c c c c c c c c c c c c c c c c$   | Ω               |
|   |                 |
|   | S               |
| Output Capacitance $C_{oss}$ $V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ 150Reverse Transfer Capacitance $C_{rss}$ 130Total Gate Charge $V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -5.4 \text{ A}$ 2436   | _               |
| Output Capacitance $C_{oss}$ $V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ 150Reverse Transfer Capacitance $C_{rss}$ 130Total Gate Charge $V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -5.4 \text{ A}$ 2436   | T               |
| Reverse Transfer Capacitance $C_{rss}$ 130 Total Gate Charge $Q_{q}$ $V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -5.4 \text{ A}$ 24 36   | pF              |
| Total Gate Charge   |                 |
| lotal Gate Charge   |                 |
|   | _               |
| Gate-Source Charge $Q_{gs}$ $V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -5.4 \text{ A}$ 3.4   | nC              |
| Gate-Drain Charge Q <sub>gd</sub> 3.8   |                 |
| Gate Resistance R <sub>g</sub> f = 1 MHz 1.5 7.7 15.4   | Ω               |
| Turn-On Delay Time t <sub>d(on)</sub> 13 20   |                 |
| Rise Time $t_r$ $V_{DD}$ = - 15 V, $R_L$ = 3.5 $\Omega$ 4 8   |                 |
| Turn-Off Delay Time $t_{d(off)} \hspace{0.2in} I_{D} \cong \text{-} \hspace{0.1in} 4.3 \hspace{0.1in} A, \hspace{0.1in} V_{GEN} = \text{-} \hspace{0.1in} 10 \hspace{0.1in} V, \hspace{0.1in} R_g = 1 \hspace{0.1in} \Omega \hspace{0.2in} 38 \hspace{0.2in} 57 \hspace{0.2in} 38 \hspace{0.2in} 38 \hspace{0.2in} 57 \hspace{0.2in} 38 0.2i$ |                 |
| Fall Time t <sub>f</sub> 6 12   |                 |
| Turn-On Delay Time t <sub>d(on)</sub> 28 42   | ns              |
| Rise Time $t_r = V_{DD} = -15 \text{ V}, R_L = 3.5 \Omega$ 16 24  |                 |
| Turn-Off Delay Time $t_{d(off)}$ $I_D \cong -4.3 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$ 30 45   |                 |
| Fall Time t <sub>f</sub> 10 20  |                 |
| Drain-Source Body Diode Characteristics   |                 |
| Continuous Source-Drain Diode Current $I_S$ $T_C = 25 ^{\circ}C$ $-2.1$   |                 |
| Pulse Diode Forward Current (t = 100 µs) I <sub>SM</sub> - 80   | A               |
| Body Diode Voltage $V_{SD}$ $I_{S} = -4.3 \text{ A}, V_{GS} = 0 \text{ V}$ $-0.8 -1.2$  | V               |
| Body Diode Reverse Recovery Time t <sub>rr</sub> 15 23  |                 |
| Body Diode Reverse Recovery Charge Q <sub>rr</sub> 1 4 2 A dl/dt 100 A/va T 25 °C 7 14  | ns              |
| Reverse Recovery Fall Time $t_a$ $I_F = -4.3 \text{ A, dl/dt} = 100 \text{ A/µs, T}_J = 25 ^{\circ}\text{C}$ 8  | ns<br>nC        |
| Reverse Recovery Rise Time t <sub>b</sub> 7   |                 |

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

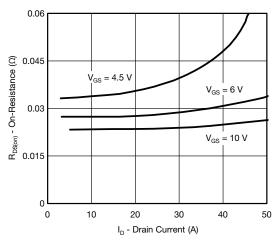
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



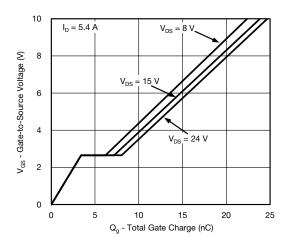
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



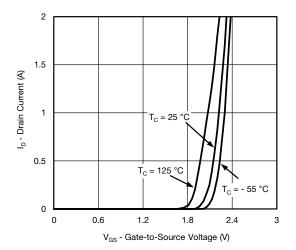
#### **Output Characteristics**



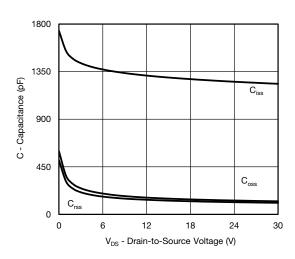
On-Resistance vs. Drain Current



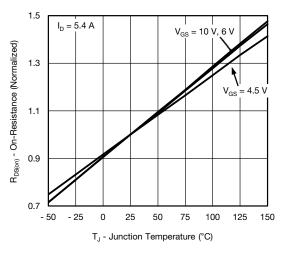
**Gate Charge** 



**Transfer Characteristics** 



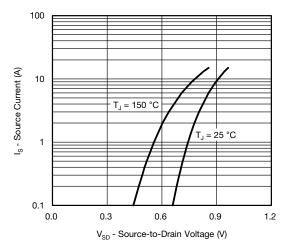
Capacitance



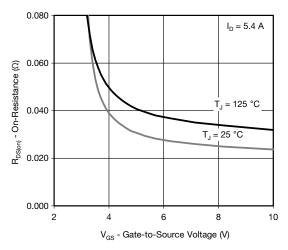
On-Resistance vs. Junction Temperature

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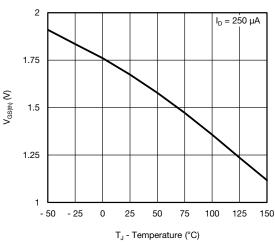
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



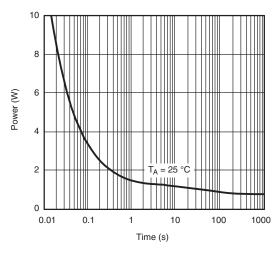
Source-Drain Diode Forward Voltage



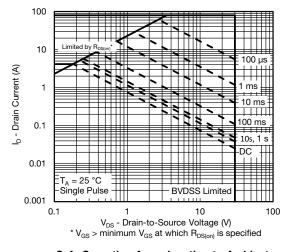
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 



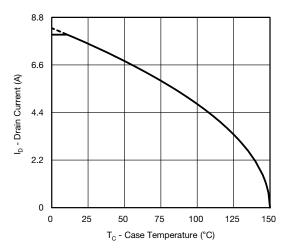
Single Pulse Power (Junction-to-Ambient)



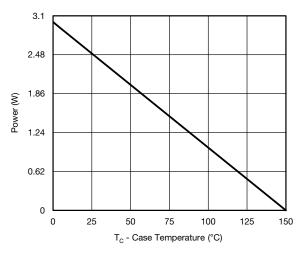
Safe Operating Area, Junction-to-Ambient

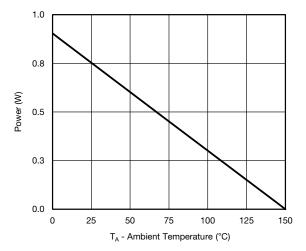


### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



#### **Current Derating\***



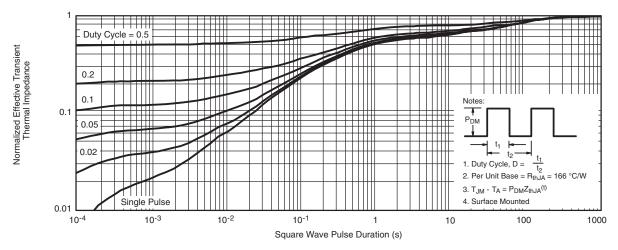


Power, Junction-to-Foot Power, Junction-to-Ambient

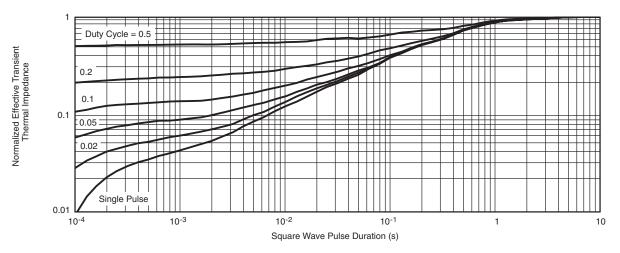
<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max.)}$  = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62865.



### SOT-23 (TO-236): 3-LEAD







| Dim                    | MILLIMETERS |      | INCHES     |       |
|------------------------|-------------|------|------------|-------|
|                        | Min         | Max  | Min        | Max   |
| Α                      | 0.89        | 1.12 | 0.035      | 0.044 |
| A <sub>1</sub>         | 0.01        | 0.10 | 0.0004     | 0.004 |
| A <sub>2</sub>         | 0.88        | 1.02 | 0.0346     | 0.040 |
| b                      | 0.35        | 0.50 | 0.014      | 0.020 |
| С                      | 0.085       | 0.18 | 0.003      | 0.007 |
| D                      | 2.80        | 3.04 | 0.110      | 0.120 |
| E                      | 2.10        | 2.64 | 0.083      | 0.104 |
| E <sub>1</sub>         | 1.20        | 1.40 | 0.047      | 0.055 |
| е                      | 0.95 BSC    |      | 0.0374 Ref |       |
| e <sub>1</sub>         | 1.90 BSC    |      | 0.0748 Ref |       |
| L                      | 0.40        | 0.60 | 0.016      | 0.024 |
| L <sub>1</sub>         | 0.64 Ref    |      | 0.025 Ref  |       |
| S                      | 0.50 Ref    |      | 0.020 Ref  |       |
| q                      | 3°          | 8°   | 3°         | 8°    |
| FCN: S-03946-Rev K 09- | lul-01      | •    |            |       |

ECN: S-03946-Rev. K, 09-Jul-01

DWG: 5479

Document Number: 71196 www.vishay.com 09-Jul-01





# **Mounting LITTLE FOOT® SOT-23 Power MOSFETs**

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs, (http://www.vishay.com/doc?72286), for the basis of the pad design for a LITTLE FOOT SOT-23 power MOSFET footprint. In converting this footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

The electrical connections for the SOT-23 are very simple. Pin 1 is the gate, pin 2 is the source, and pin 3 is the drain. As in the other LITTLE FOOT packages, the drain pin serves the additional function of providing the thermal connection from the package to the PC board. The total cross section of a copper trace connected to the drain may be adequate to carry the current required for the application, but it may be inadequate thermally. Also, heat spreads in a circular fashion from the heat source. In this case the drain pin is the heat source when looking at heat spread on the PC board.

Figure 1 shows the footprint with copper spreading for the SOT-23 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlies the drain pin and provides planar copper to draw heat from the drain lead and start the process of spreading the heat so it can be dissipated into the ambient air. This pattern uses all the available area underneath the body for this purpose.



FIGURE 1. Footprint With Copper Spreading

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low-impedance path for heat to move away from the device.

Document Number: 70739 26-Nov-03



### **RECOMMENDED MINIMUM PADS FOR SOT-23**



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index

APPLICATION NOTE



### **Legal Disclaimer Notice**

Vishay

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Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

Revision: 02-Oct-12 Document Number: 91000