Single Stage Amplifier Simulation
Assignment 2
ELL304

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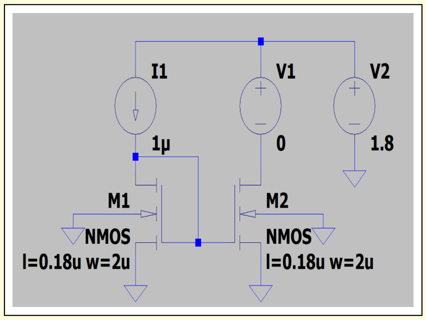
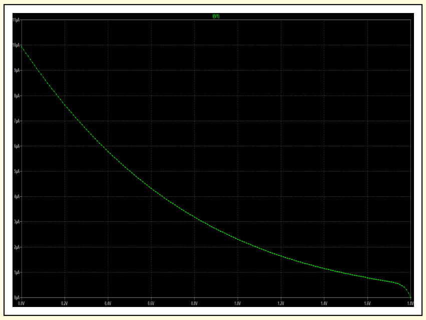
1 Question 1

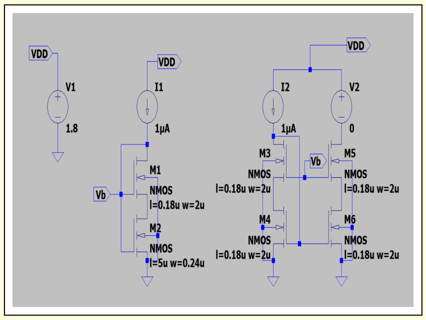
1.1 Part A



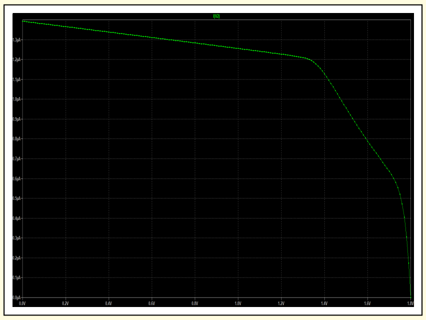
Circuit Schematics (L=0.18u)



I vs V plot

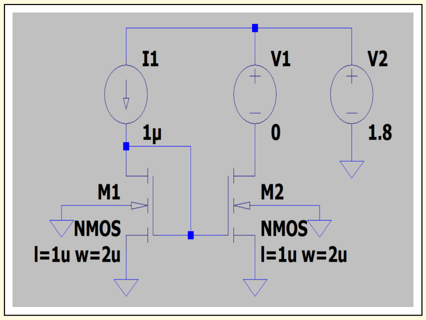


Circuit Schematics (L=0.18u)



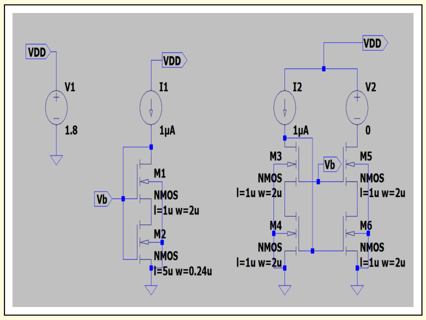
I vs V plot

1.2 Part B

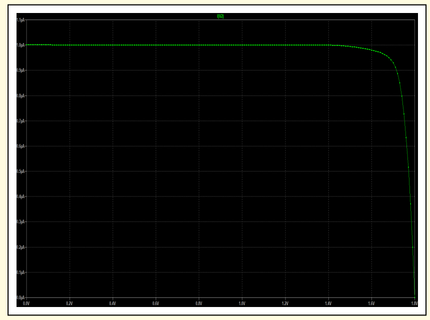


Circuit Schematics (L=1u)

I vs V plot



Circuit Schematics (L=1u)



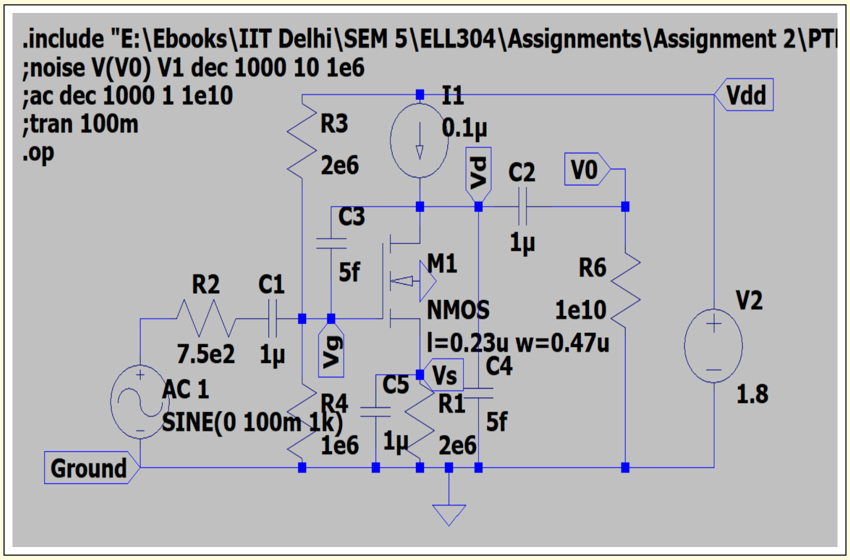
I vs V plot

1.3 Conclusion

- We see that the gain drops due to increase in L and process variations but the waveform of the variation of current remains the same.
- The extra current flows into parasitic capacitances and body of the MOSFETs, hence we can see a lot of non-ideality at edge of process limits (smaller transistors have more mismatches).
- As we increase L, we reduce the extra currents through the parasitic elements and observe more ideal mirroring action. We also have better output impedance.

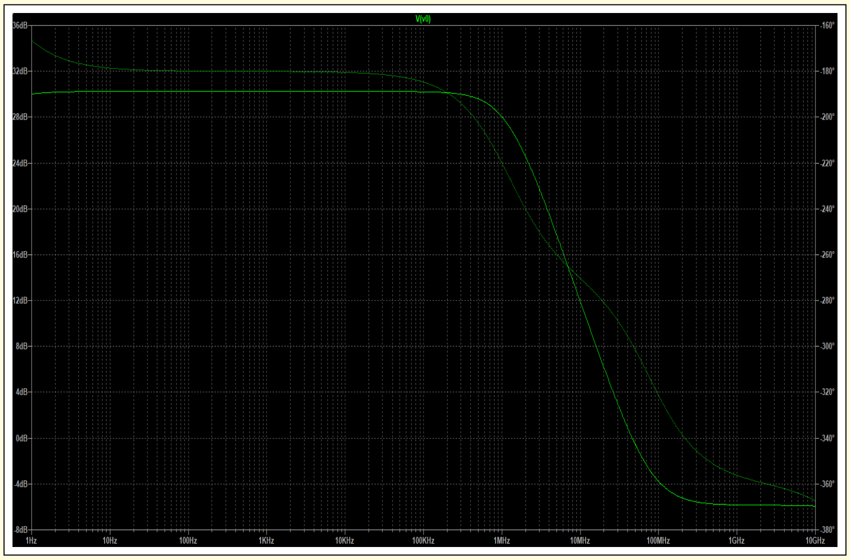
2 Question 2

- We need to design a CS Amplifier for a DC gain of 30dB and a Unity Gain Bandwidth of 50MHz while minimising power dissipation.
- The gain of a common source amplifier is approximately gm*r0
- A gain of 30dB is equivalent to a gain of 31.622 on the linear scale.
- gm*r0= $2/(V_{ov} * \lambda)$, thus we need to reduce the V_{ov} to get a better gain.
- We choose $V_{gs} \approx V_T$ so that $V_{ov} \approx 0$ and we get high gain.
- For low power dissipation, we reduce the MOS Current. Thus we take MOS current as 0.1μ. So that the power requirements are minimised.
- Choose R_L as high as possible so that it doesn't affect the gain of the amplifier. We choose it as $1e10\Omega$.
- We choose values of other resistors and capacitors accordingly to maintain gain and keep the device in saturation.



Circuit Schematics of the Amplifier

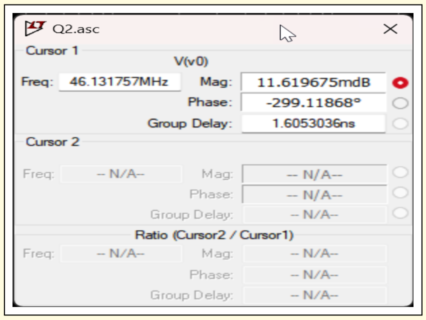
- We adjust C3,C4 so that the UGB is as expected.
- The Device is in Saturation.
- We apply an AC signal of amplitude 1 and plot the AC Characteristics of the ciruit.



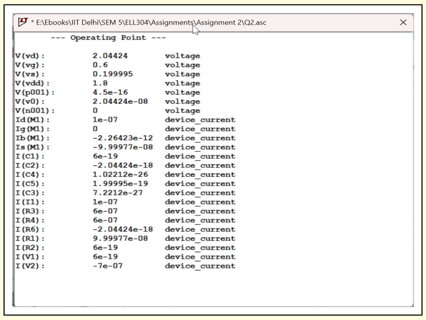
AC Plot of the Circuit

- We observe that the DC Gain of the circuit is around 30dB as expected.

- We also see that the circuit has 2 poles.
- The first pole occurs near 300kHz.
- The UGB of the circuit is near 46Mhz, which is a little less that what we wanted.
- The Phase Margin of the circuit is around 60degrees which is great for the stability of the device.

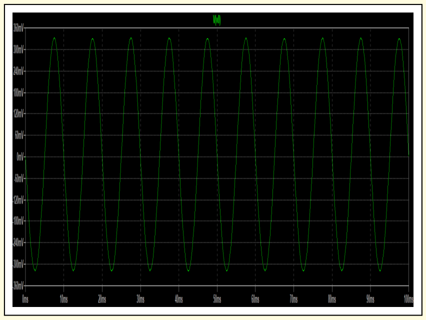


UGB and Phase Margin

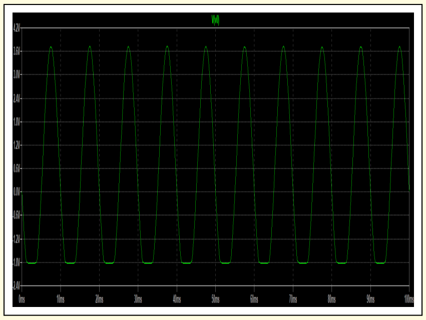


Operating Points of the Circuit

- The Operating Points show that the device is in Saturation
- Id: 1.00e-07; Vgs: 4.00e-01; Vds: 1.84e+00
- Vbs: -2.00e-01; Vth: 5.39e-01; Vdsat: 4.43e-02
- Gm: 2.56e-06; Gds: 7.86e-08; Gmb 5.48e-07
- The Power Dissipation is around $1.3\mu W$.
- Thus, we designed the amplifier as expected.

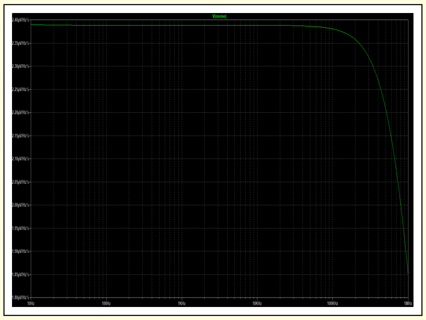


Response for Input 0.01V

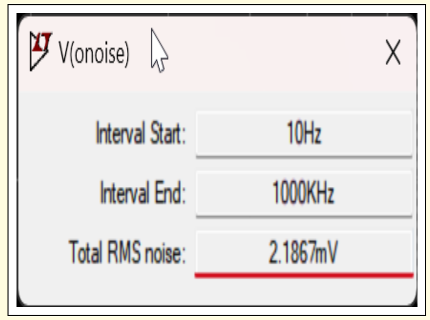


Response for Input 0.1V (Clipped)

3 Question 3



Noise Plot of the circuit



RMS value of the Noise

- Input Referred Noise $= \frac{(1+\gamma g_m(r0||R_L))kT}{g_m^2(r0||R_L)^2 C_L}$
- The input noise is a white spectrum and the output noise is a combination of low frequency flicker noise and noise due to capacitive load.
- The Noise due to bias resistors is very very low.
- When we integrate the output noise over a 1MHz bandwidth, LTSpice gives us a value of 0.0021867. This is in V.
- Therefore, the noise power is $6.06mV^2$
- From the analytical expression, we get total output noise as $1.102mV^2$, which is slightly less than the simulated value as we have not considered the non-idealities of the process and body effect.