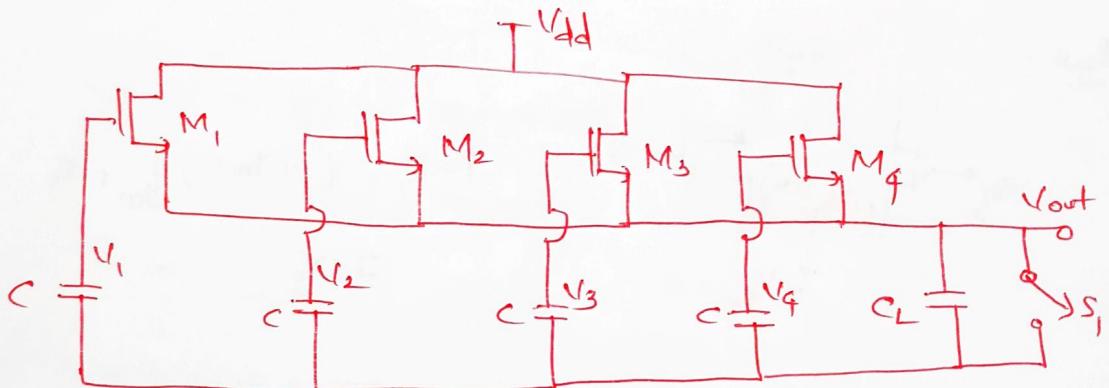


Tutorial - 4

Q4) In the circuit given below $V_{DD} = 18V$ and M_1-4 are NMOS transistors with $V_{TN} = 0.47V$. At $t=0$, switch S_1 turns ON and discharges C_L . At $t=t_1$, the switch turns OFF and shortly after that ($t=t_1^+$) inputs $V_1 = 0.69V$, $V_2 = 0.89V$, $V_3 = 1.45V$ and $V_4 = 0.67V$ are applied on capacitors c at gates of M_1-4 respectively. What will be the value of V_{out} (in V) at $t=\infty$, given that the devices show ideal behavior in the "cutoff" region.



Sol.: The given circuit is an example of a "winner takes all" circuit. It is used to identify $\max(V_1, V_2, \dots, V_k)$

Operation: At $t=t_1^+$ $V_{out} = 0V$

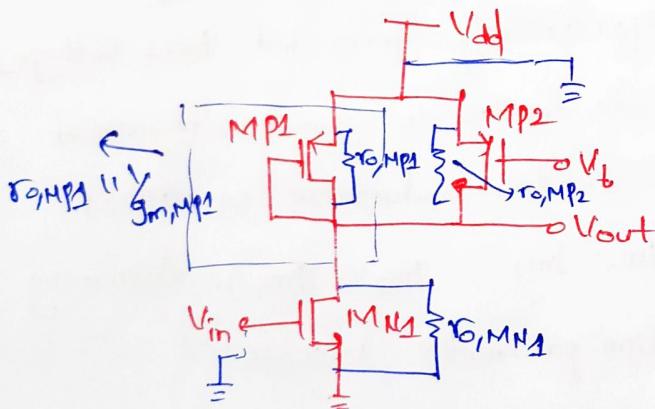
All MOSFETs with $V_g > 0$ turns ON,

$\Rightarrow I_D$ increases $\Rightarrow V_{out}$ increases $\Rightarrow V_{as}$ decreases

After, a finite amount of time all MOSFETs with gate voltage other than $\max(V_{th}/4)$ will turn off and the MOSFET with the highest gate voltage turns off at last

$$\begin{aligned} \therefore V_{out}(t=\infty) &= \max(V_1, V_2, V_3, V_4) - V_{th} \\ &= 1.45 - 0.47 \\ &= 0.98 \text{ V} \end{aligned}$$

Q2) Find the small signal DC gain of the circuit given below considering $MN1$ & $MP2$ are biased in the saturation region of operation, with DC bias current of 17 mA and 9.69 mA flowing through them respectively. Consider $\lambda = 0.001$, $g_{m1} \gg 1$, $\mu_n = \mu_p$ and (W/L) of all transistors equal to 10.



Sol: $A_v = G_m R_{out}$

For G_m , short output to ground and find short circuit o/p current (I_{sc})

$$G_m \approx -g_{m, MN1}$$

$$\left[\text{Same as } Y_{21} = \frac{I_2}{V_1} \Big|_{V_2=0} \right]$$

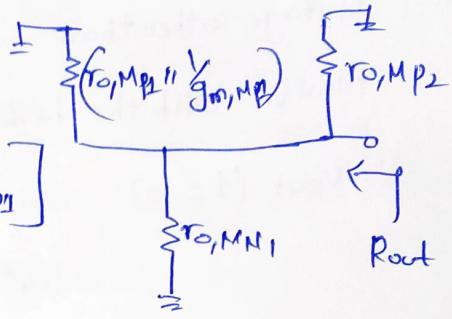
\downarrow
 G_m

R_{out}: short V_{in} to ground & V_{dd} also

$$R_{out} = \cancel{ }$$

$$\approx \frac{1}{g_{m,Mp1}} \left[r_{o,MN1} \parallel r_{o,Mp2} \parallel r_{o,Mp1} \parallel \frac{1}{g_{m,Mp1}} \right]$$

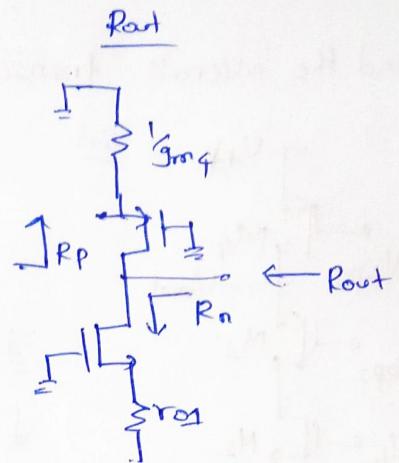
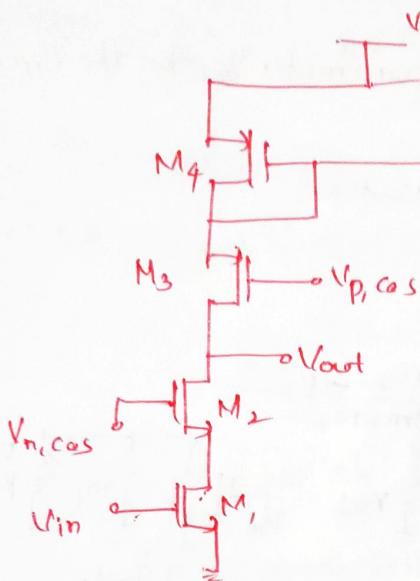
$\left[r_o \gg \frac{1}{g_m} \right]$



$$A_V \approx -\frac{g_{m,MN1}}{g_{m,Mp1}} = -\frac{\sqrt{2 I_D n \mu_n C_{ox} \frac{W}{L}}}{\sqrt{2 I_D p \mu_p C_{ox} \frac{W}{L}}} = -\sqrt{\frac{I_D n}{I_D p}} = -\sqrt{17}$$

$$A_V = -1.525$$

Q3) Consider that in the circuit shown below, the DC bias for M₁ is adjusted until 465 uA starts flowing through R₁. V_{n, cas} and V_{p, cas} are appropriately generated bias voltages to keep M₂ & M₃ cascode devices in saturation region of operation and such that the transconductance of NMOS & PMOS are matched ($g_{m1} = g_{m2}$; $g_{m3} = g_{m4}$). Assuming channel length modulation parameter $\lambda = 0.015 \text{ V}^{-1}$, $\mu_n C_{ox} = \mu_p C_{ox} = 200 \text{ nA/V}^2$; W/L for all NMOS as $200/\mu$ and $(W/L)_3 = (W/L)_4 = 800/\mu$ and $(W/L)_5 = 400/\mu$; calculate the output impedance from port V_{out} (in M_Ω).



$$\text{Sol!} \quad R_{\text{out}} = R_p \parallel R_n$$

$$R_n = (1 + g_{m2} r_{o3}) r_{o1} + r_{o2}, \quad R_p = (1 + g_{m3} r_{o3}) \frac{1}{g_{m4}} + r_{o3}$$

$$\begin{aligned} R_{\text{out}} &= \underbrace{(g_{m2} r_{o2} r_{o1} + r_{o2})}_{\text{Very large}} \parallel \underbrace{\left(\frac{g_{m3}}{g_{m4}} + 1\right) r_{o3}} \\ &\approx \left(\frac{g_{m3}}{g_{m4}} + 1\right) r_{o3} \approx 2r_{o3} \quad \text{if } \frac{g_{m3}}{g_{m4}} = 1 \quad (\text{Same Current &} \\ &\quad \text{w/L for } M_3 \text{ & } M_4) \end{aligned}$$

$$r_{o3} = \frac{1}{\lambda I_{D3}} = \frac{1}{(0.015) I_{P3}}$$

$$r_{o3} = 0.717 \text{ M}\Omega$$

$$I_{D3} = I_{DS} \frac{(W/L)_3}{(W/L)_S} = 46.5 \times \frac{4}{2} = 93 \mu\text{A}$$

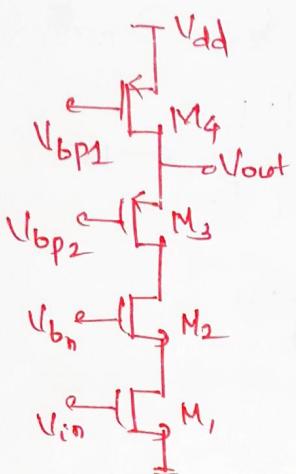
$$\boxed{R_{\text{out}} = 1.434 \text{ M}\Omega}$$

4) Assume that all of the transistors M_{1-4} are biased in the saturation region. The small signal parameters are as follows:

$$1) g_{m1} = g_{m2} = g_{m3} = g_{m4} = 1.5 \text{ ms}$$

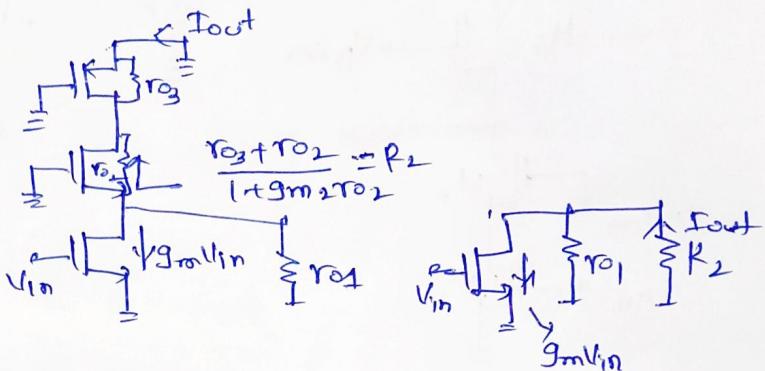
$$2) r_{ds1} = r_{ds4} = 28 \text{ k}\Omega, r_{ds2} = r_{ds3} = 597 \text{ k}\Omega$$

Find the overall transconductance parameter Y_{21} for the circuit.



Sol

$$G_m = \frac{I_{out}}{V_{in}} \quad | V_{out} = 0$$

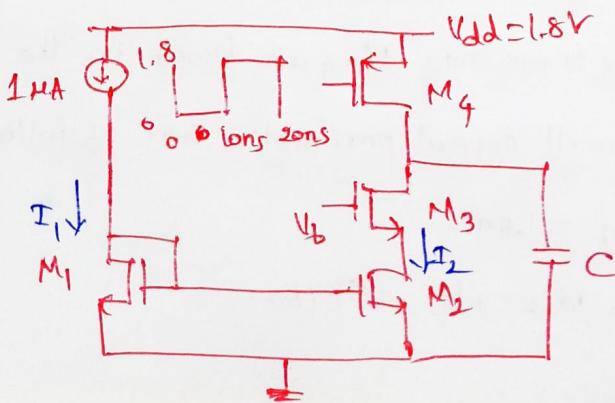


$$I_{out} = g_m V_{in} R_01$$

$$R_2 = \frac{R_03 + R_02}{1 + g_m R_02} = \cancel{\frac{(597\text{K}) R_02}{(1.5)(597\text{K})}} = \cancel{0.8} \approx \frac{2 R_02}{g_m R_02} \approx \frac{2}{g_m} = 1.33\text{K}$$

$$\frac{I_{out}}{V_{in}} = 1.5 \frac{28}{28 + 1.33} = 1.432 \text{ mS}$$

Q5) In the circuit shown below, calculate V_{DS3} (in V) after 19.7ns. Assume the pulse given at the gate of M_4 starts at $t=0s$. Given $(W/L)_1 = (W/L)_2 = (W/L)_3 = 1$, $\mu_n C_o x = 200\text{nA}$, $V_b = 0.7$, $V_{th} = 0.5\text{V}$ and $C = 32\text{fF}$)



Sol: $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 \Rightarrow I_1 = I_2 = I_3$

$$I_3 = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_3 (V_b - V_s - V_{TH})^2$$

$$14 = \frac{1}{2} \times 200 \times (0.2 - V_s)^2$$

$$0.2 - V_s = \frac{1}{\sqrt{100}} = 0.1 \Rightarrow V_s = 0.1 \text{ V}$$

M_4 acts as a switch as pulse is given as input.

When $V_{G4} = 0 \Rightarrow M_4$ ON, $V_{G4} = 1.8 \Rightarrow M_4$ OFF

upto $t=0$, M_4 ON $\Rightarrow V_{D3} = 1.8 \text{ V}$

after $t=0$, M_4 OFF; C starts to discharge

$$V_D = 1.8 - \frac{I A t}{C} = 1.8 - \frac{1 \times 10^{-6} \times 9.7 \times 10^{-9}}{32 \times 10^{-15}}$$

$$\boxed{V_D = 1.497 \text{ V}}$$

$$V_{DS3} = 1.497 - 0.1 = 1.397 \text{ V.}$$

Q6) In the circuit shown below, transistors M_1 & M_2 are perfectly matched and biased in saturation. The resistor R and Supply Voltage V_{DD} are set to $10 \text{ k}\Omega$ and 5 V . Ignoring channel length modulation effect, determine the change in bias current I_{BIAS} (in μA) if the supply voltage fluctuates and increases by 39.6 mV from its nominal value.

Take: $(\frac{W}{L})_1 = (\frac{W}{L})_2 = 1$, $V_{TN} = 1V$, $\mu_n C_{ox} = 100 \mu A/V^2$

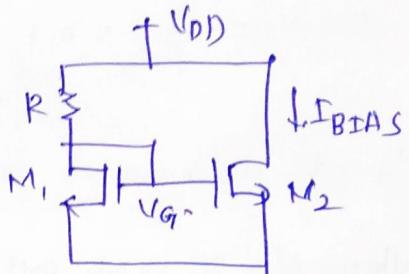
Sol:

This question can be solved by two approaches

i) Repeating the DC analysis again with $V_{DD} \pm \Delta V$

ii) Small signal analysis

-



DC analysis

$$I_{BIAS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_G - V_{TN}]^2, \quad V_G = 5 - I_{BIAS}(10k)$$

$$I_{BIAS} = 50 \mu A / V^2 [4 - (10k) I_{BIAS}]$$

$$(10k) I_{BIAS} = 16 + 100k^2 I_{BIAS}^2 - (80k) I_{BIAS}$$

$$(100k)^2 I_{BIAS}^2 - (10k) I_{BIAS} + 16 = 0$$

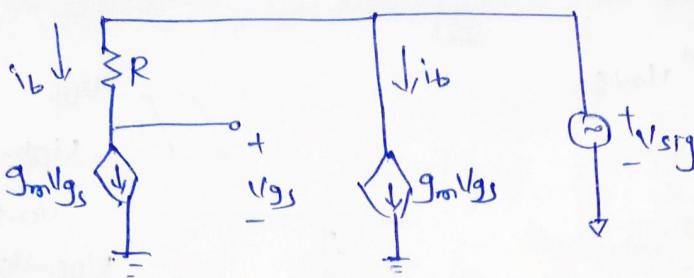
$$I_{BIAS} = \frac{10k \pm \sqrt{(10k)^2 - (4 \times 16 \times 100k^2)}}{2 \cdot (100k^2)}$$

$$= 0.2 \text{ mA}, \quad 0.8 \text{ mA}$$

$I_{BIAS} = 0.2 \text{ mA}$ not possible (V_G is negative)

Supply voltage increases by 39.6 mV Small Signal

Small Signal analysis



$$V_{sig} = i_b R + V_{gs} = i_b R + \frac{i_b}{g_m} \quad (\because i_b = g_m V_{gs})$$

$$V_{sig} = i_b \left[R + \frac{1}{g_m} \right] = i_b \left[\frac{g_m R + 1}{g_m} \right]$$

$$\Rightarrow i_b = V_{sig} \left[\frac{g_m}{1 + g_m R} \right] = 39.6 \text{ mV} \frac{200 \mu\text{s}}{(1 + 200 \mu\text{s})(10k)} = 2.64 \text{ mA}$$

→ Instead of small signal analysis, we can also get ans by repeating DC analysis again with V_{DD} as $V_{DD} \pm \Delta V$

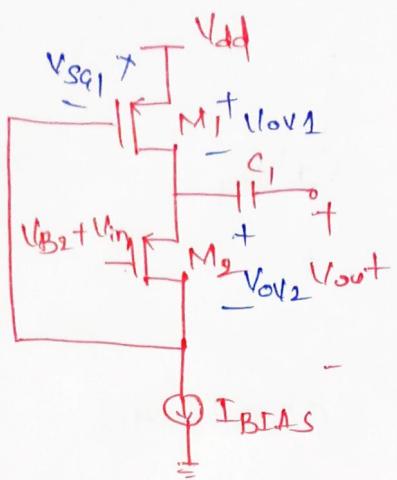
Q7) In the circuit shown below, determine the bias voltage V_{B2} (in V) to obtain a symmetrical signal swing at the output while keeping all the transistors in saturation region.

Ignore channel length modulation effect and take

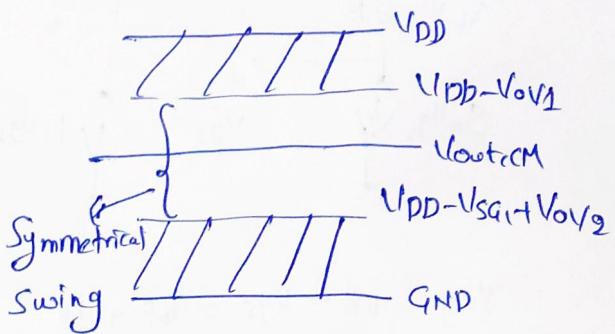
$$V_{DD} = 10 \text{ V}, \left(\frac{W}{L}\right)_1 = 4 \quad \left(\frac{W}{L}\right)_2 = 64 \quad |V_{TP}| = 1 \text{ V}$$

$$\mu_{pCO} = 25 \text{ nA/V}^2 \quad I_{BIAS} = 236 \text{ nA}$$

Assume C_1 to be large coupling capacitor



Sol



$$V_{OV1} = \sqrt{\frac{2I_{BIAS}}{\mu_p C_o(\frac{W}{L})}} = 2.172 \text{ V}, \quad V_{OV2} = \sqrt{\frac{2I_{BIAS}}{\mu_p C_o(\frac{W}{L})}} = 0.543 \text{ V}$$

$$V_{SG1} = V_{OV1} + |V_{tp}| = 3.172 \text{ V}$$

$$V_{out,CM} = \frac{(V_{DD} - V_{SG1} + V_{OV2}) + (V_{DD} - V_{OV1})}{2} = 7.6 \text{ V}$$

$$V_{B2} = V_{out,CM} - V_{SG2} = V_{out,CM} - [V_{OV2} + |V_{tp}|] \\ = 6.057 \text{ V}$$

- Q8). In the circuit given below, find the small signal voltage gain V_{out}/V_{in} . Consider resistors R_1, R_2 & R_D to be $8\text{k}\Omega, 168\text{k}\Omega$ & $47\text{k}\Omega$. $V_{DD} = 12\text{V}$, $V_{B3} = 6\text{V}$, $I_{BIAS} = 100\text{mA}$

$$\frac{W}{L} \text{ of all transistors} = 1, \quad V_{TN} = 1\text{V}, \quad \mu_{nC_ox} = 200\text{mA/V}^2$$

Assume C_L to be large coupling capacitor and ignore channel length modulation effect.

Sol: M_1 is diode connected MOSFET
 \Rightarrow saturation

$$V_{G1} = V_{out} + V_{TN} = V_{as2} = V_{as3}$$

$$V_{out} = \sqrt{\frac{2 I_{BIAS}}{\mu_n C_o \frac{W}{L}}} = \sqrt{\frac{2 \times 100}{200 \times 1}} = 1$$

$$V_{G1} = V_{out} + V_{TN} = 1 + 1 = 2V$$

$$V_{D3} = V_{DD} - I_{BIAS} R_D = 12 - 4.7 = 7.3$$

For M_3 to be in Sat $V_{B3} \geq V_{as3} - V_{TN}$ $7.3 \geq 5 \Rightarrow$ saturation

For M_2 to be in sat $V_{D2} \geq V_{as2} - V_{TN}$

$$V_{D2} = V_{B3} - V_{as2} = 6 - 2 = 4 \Rightarrow 4 \geq 1 \Rightarrow$$
 saturation

$$g_{m1} = g_{m2} = g_{m3} = g_m = \sqrt{2 I_{BIAS} \mu_n C_o \frac{W}{L}} = 200 \mu S$$

Small Signal

$$V_y = -g_m V_s R_o \quad R_o \approx \frac{1}{g_m}$$

$$\boxed{V_y = -V_s}$$

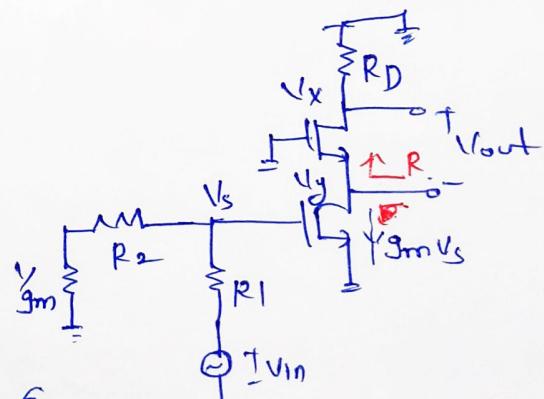
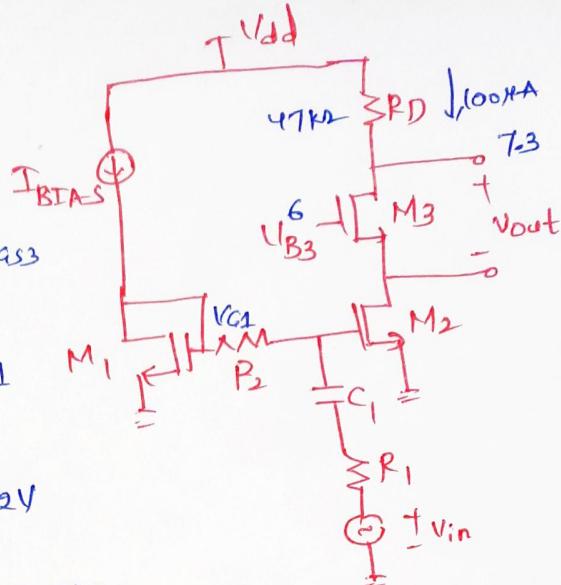
$$V_x = -g_m V_s R_D = -g_m R_D V_s$$

$$V_{out} = V_x - V_y = [-g_m R_D + 1] V_s = -(g_m R_D - 1) V_s$$

$$V_s = V_{in} \frac{R_2 + g_m}{R_1 + R_2 + \frac{1}{g_m}}$$

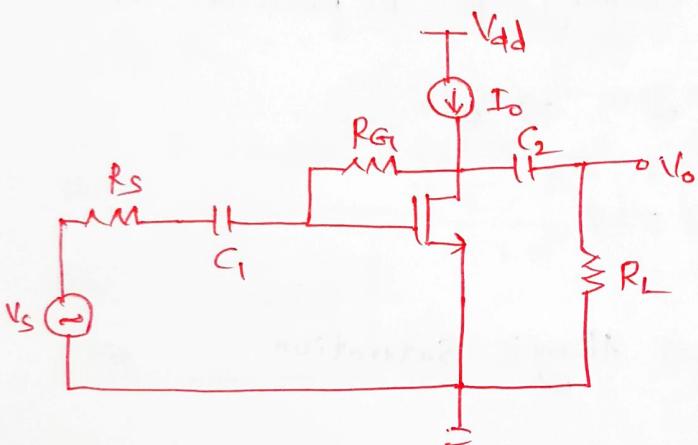
V_{out}

$$\frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_s} \times \frac{V_s}{V_{in}} = -(g_m R_D - 1) \frac{R_2 + g_m}{R_1 + R_2 + \frac{1}{g_m}} = -5.653$$

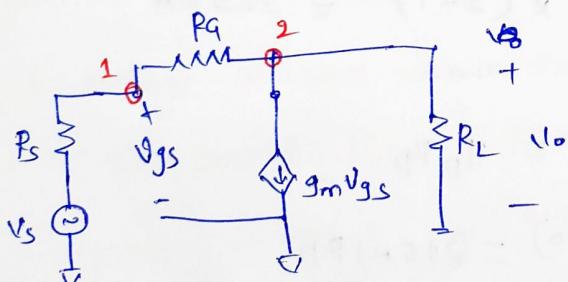


Tutorial-4

Q19) In the circuit shown below, $I_o = 408 \mu A$, $R_s = 37 k\Omega$, $R_L = 90 k\Omega$, $V_{dd} = 3V$ and Mos parameters are $\mu_n C_{ox} = 100 \mu A/V^2$, $V_{TH} = 0.5 V$, $(W/L) = 10$. To achieve gain V_o/V_s very close to $-g_m R_L$ constraint on R_G is $R_G \gg R$ (R is the minimum value of R_G). Find value of R in $M\Omega$. Assume C_1 & C_2 are very large. (Accuracy ± 0.001)



Sol: Small signal model:



KCL at node ①

$$\frac{V_{gs} - V_s}{R_s} + \frac{V_{gs} - V_o}{R_G} = 0$$

$$V_{gs} \left(\frac{1}{R_s} + \frac{1}{R_G} \right) = \frac{V_o}{R_G} + \frac{V_s}{R_s}$$

$$V_{gs} = \frac{V_o R_s}{R_G + R_s} + V_s \frac{R_G}{R_G + R_s} \rightarrow ①$$

KCL at node ②

$$\frac{v_o}{R_L} + g_m v_{gs} + \frac{v_o - v_{gs}}{R_G} = 0$$

$$v_o \left(\frac{1}{R_L} + \frac{1}{R_G} \right) + v_{gs} \left(g_m - \frac{1}{R_G} \right) = 0$$

$$v_o \left(\frac{R_G + R_L}{R_G R_L} \right) + v_{gs} \left(\frac{g_m R_G - 1}{R_G} \right) = 0 \quad \text{---} ①$$

Substitute ① in ②

$$v_o \left(\frac{R_G + R_L}{R_G R_L} + \frac{(g_m R_G - 1) P_S}{R_G (R_G + P_S)} \right) = -v_s \quad \frac{R_G}{P_S + P_S} \left(\frac{g_m R_G - 1}{R_G} \right)$$

$$v_o \left(\frac{(R_G + R_L)(P_S + P_S) + (g_m R_G - 1) P_S R_L}{R_G R_L (R_G + P_S)} \right) = -v_s \quad \frac{(g_m R_G - 1)}{P_S + P_S}$$

$$\begin{aligned} \frac{v_o}{v_s} &= - \frac{(g_m R_G - 1) R_L R_G}{R_G^2 + P_S P_S + P_S R_L + R_S P_S + g_m R_S P_S R_L - P_S R_L} \\ &= - \frac{(g_m R_G - 1) R_L R_G}{R_G [P_S + P_S + R_L + g_m R_S R_L]} \end{aligned}$$

$$\frac{v_o}{v_s} = - \frac{(g_m R_G - 1) R_L}{R_G + P_S + P_S + g_m P_S R_L}$$

if $R_G \gg g_m P_S R_L, P_S, R_L \implies [R_G \gg g_m P_S R_L]$

$$\boxed{\frac{v_o}{v_s} \approx - \frac{g_m R_G R_L}{R_G} \approx -g_m P_L}$$

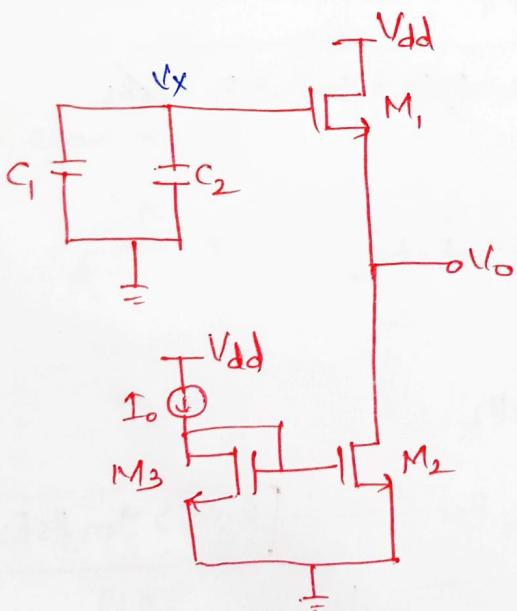
$$g_m = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}}$$

$$= \sqrt{2 \times 408 \times 100 \times 10}$$

$$g_m = 903.327 \text{ nS}$$

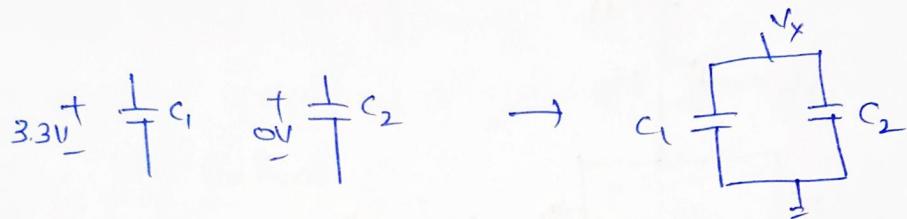
$$R_g \gg g_m R_L R_S = 903.327 \times 37 \times 90 = 3.008 \text{ M}\Omega$$

Q10) In the circuit shown below, C_1 is initially charged to 3.3V. Later C_1 and C_2 are connected together. To get $V_o = 2.4V$, Find W/L of M_1 . Given $V_{dd} = 3.3V$, $I_o = 2 \text{ nA}$, $C_1 = 350 \text{ fF}$, $C_2 = 35 \text{ fF}$, $\frac{W}{L}$ of $M_3 = 1$, W/L of $M_2 = 5$ and MOS parameters are $\mu_n C_{ox} = 100 \text{ nA/V}^2$, $V_{TH} = 0.5V$. (Accuracy ± 0.001)



Sol: As C_1 is initially charged to 3.3V, C_2 is not charged so its voltage means it is 0V.

Charge conservation happens when we connect both capacitors. Let us assume that node voltage as V_x



$$(3.3V)C_1 + (0V)C_2 = V_x(C_1 + C_2)$$

$$V_x = \frac{3.3C_1}{C_1 + C_2} = 3.3 \cdot \frac{350}{350 + 35} = 3V$$

$$V_o = V_x - V_{GS} \Rightarrow V_{GS} = V_x - V_o = 3 - 2.4 = 0.6$$

$$V_{GS} \text{ of } M_1 = \sqrt{\frac{2 I_{D1}}{\mu_n C_{O2} \frac{W}{L}}} + V_{TH}$$

$$I_{D1} = I_{D2} = \frac{(W/L)_1}{(W/L)_2} I_0$$

$$= 5 I_0 = 10mA$$

$$0.6 = \sqrt{\frac{2 \times 10}{100 \times 0.1 \frac{W}{L}}} + 0.5$$
 ~~$= 0.2 + 0.5 = 0.7$~~

$$\Rightarrow \frac{W}{L} = \frac{20}{100 \times (0.1)^2} = 20$$

~~$V_o = V_x - V_{GS} = 3 - 0.6 = 2.4$~~
 ~~$\frac{W}{L} = \frac{(0.1)^2 \times 100}{20} = 0.1$~~

~~$\frac{W}{L} = \frac{(0.1)^2 \times 100}{20} = 0.1$~~