

TUTORIAL - 2 SOLUTIONS

- Q1) In an NMOS transistor, the drain current $I_D = 1\text{mA}$, when the drain-source voltage (V_{DS}) is 5V . If the drain-source voltage is increased to 6.91V while keeping the gate-source voltage constant, the drain current gets increased by $20\mu\text{A}$. Calculate the channel length modulation parameter λ (in V^{-1}) (with atleast 1% accuracy).

in a MOSFET

Solution → Channel length modulation effect is observed in saturation region.

So, equation of drain current (I_D) in saturation region must be used.

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_{TN}]^2 (1 + \lambda V_{DS})$$

↑
includes the
effect of channel
length modulation.

$$\therefore I_{D1} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS1} - V_{TN}]^2 [1 + \lambda V_{DS1}] \quad -(1)$$

$$\text{and, } I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS2} - V_{TN}]^2 [1 + \lambda V_{DS2}] \quad -(2)$$

$$\frac{I_{D1}}{I_{D2}} = \frac{1 + \lambda V_{DS1}}{1 + \lambda V_{DS2}}$$

Given : $I_{D1} = 1\text{mA}$, $V_{DS1} = 5\text{V}$, $I_{D2} = 1.02\text{mA}$, $V_{DS2} = 6.91\text{V}$

$$\frac{1}{1.02} = \frac{1 + \lambda_5}{1 + \lambda_6 \cdot 91}$$

$$\Rightarrow \boxed{\lambda = 0.011 \text{ (ans)}}$$

voltage

(2) Find the magnitude of the small signal gain $|V_{out}/V_{in}|$ of the circuit shown below.

Consider :

Supply voltage (V_{DD}) = 4V

$\mu_{pcox} = 100 \mu A/V^2$, $\mu_{ncox} = 200 \mu A/V^2$

$$|V_{TP}| = V_{TN} = 1V$$

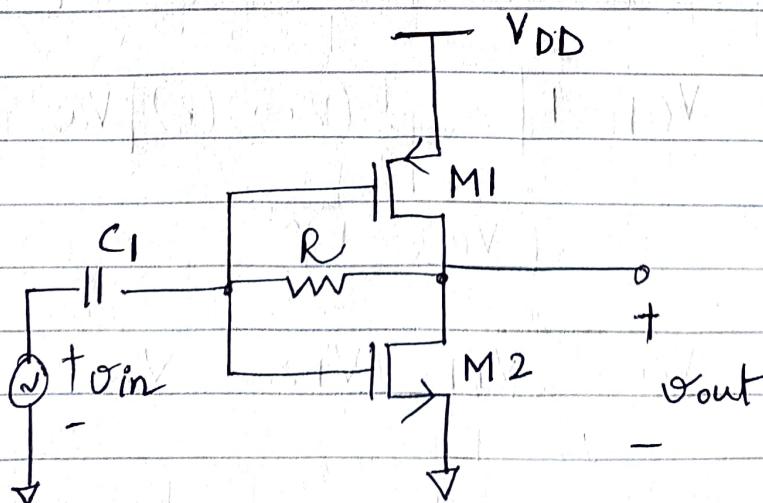
$$(\frac{W}{L})_1 = 4, (\frac{W}{L})_2 = 2$$

Resistor R equals $2.9 M\Omega$

Assume C_1 to be a large coupling capacitor.

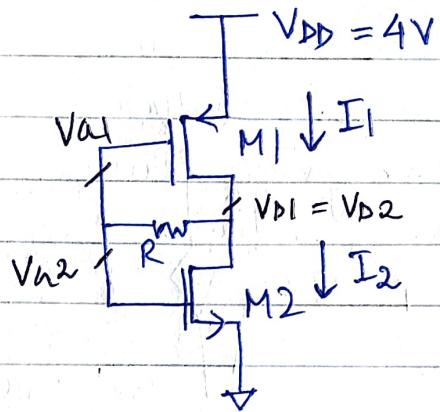
Ignore channel length modulation effect.

Give answer correct up to 3 decimal places.



Solution :

Performing DC analysis to find operating current (I). Coupling capacitor C_1 (large) behaves like open circuit in DC picture.



$$(i) I_1 = I_2 = I$$

(As no current can flow into gate terminal)

(ii) Also notice, voltage drop across R is 0V (due to reason (i)).

So, for both M_1 and M_2 , gate and drain terminals are shorted.

$\therefore M_1$ and M_2 are in saturation region of operation.

$$I_1 = I_2$$

$$\Rightarrow \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right) \left[V_{SG1} - |V_{TP}| \right]^2 = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) \left[V_{SG2} - |V_{TN}| \right]^2$$

$$\Rightarrow \frac{1}{2} (100)(4) \left[4 - V_{G1} - 1 \right]^2 = \frac{1}{2} (200)(2) \left[V_{G2} - 1 \right]^2$$

$$\Rightarrow (3 - V_{G1})^2 = (V_{G2} - 1)^2$$

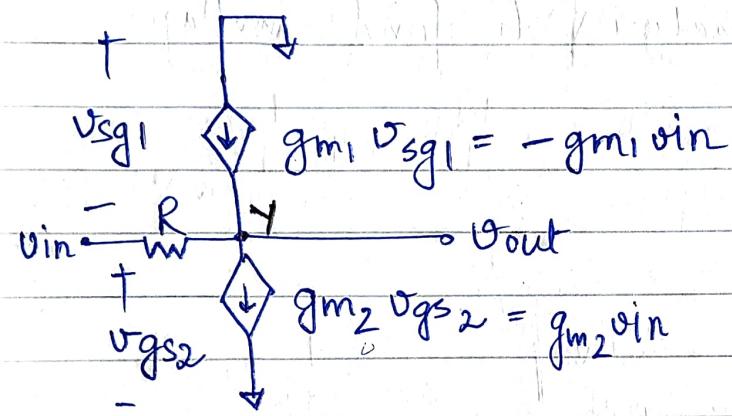
where, $V_{G1} = V_{G2} = V_{D1} = V_{D2} = V_x$

$$\Rightarrow (3 - V_x)^2 = (V_x - 1)^2$$

$$\boxed{V_x = 2V}$$

and, $I_1 = I_2 = I = 200 \mu A$ ← using either M1 or M2's current equation and using $V_{G1} = V_{G2} = 2V$.

Performing small signal analysis to find $\left| \frac{v_{out}}{v_{in}} \right|$.



Applying KCL at Y,

$$\frac{v_{out} - v_{in}}{R} + g_{m2} v_{in} + g_{m1} v_{in} = 0$$

$$\Rightarrow \frac{v_{out}}{v_{in}} = - \left[g_{m1} + g_{m2} - \frac{1}{R} \right] R$$

$$\Rightarrow \left| \frac{v_{out}}{v_{in}} \right| = \left[g_{m1} + g_{m2} - \frac{1}{R} \right] R$$

$$g_{m1} = \sqrt{2 I \mu_p \lambda \left(\frac{W}{L} \right)_1} = 400 \mu S$$

$$g_{m2} = \sqrt{2 I \mu_n \lambda \left(\frac{W}{L} \right)_2} = 400 \mu S$$

$\Rightarrow g_{m1} = g_{m2} = g_m$.

$$\left| \frac{v_{out}}{v_{in}} \right| = (2g_m R - 1)$$

$$\Rightarrow \left| \frac{v_{out}}{v_{in}} \right| = (2 \times 400 \times 2.9) - 1 = 2319 \text{ (Ans)}$$

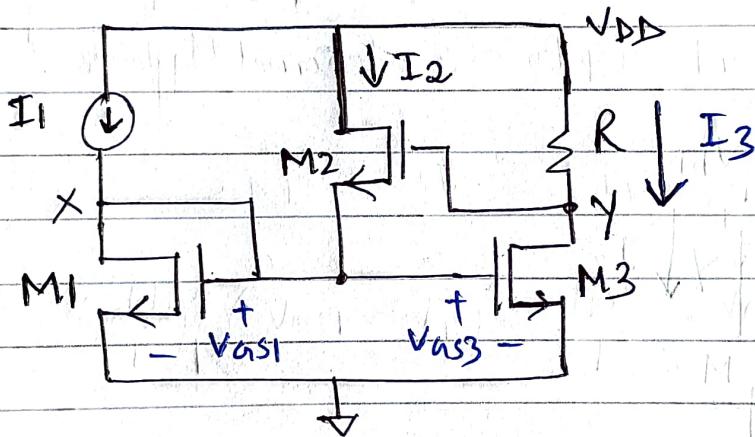
$\uparrow \quad \uparrow$
4S MSL

Q3) In the circuit shown below, transistors M1 and M3 are in saturation and current I_1 equals 10mA . Ignoring channel length modulation effect, calculate the aspect ratio of transistor M2 to support a current I_2 of 40mA through it. Consider $R = 2.3K\Omega$ and threshold voltages of all transistors to be 0.7V . Other parameters are:

Supply voltage (V_{DD}) = 2V , $\mu_n C_{ox} = 250\text{nA/V}^2$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_3 = 10$$

(Give answer correct upto 3 decimal places).



Solution: (i) I_2 cannot flow into gates of M3 and M1.
(ii) So, $(I_1 + I_2)$ will flow through M1 and $V_{DS1} = V_x$ is generated corresponding to drain-source current $(I_1 + I_2)$ in M1.

$$I_1 + I_2 = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 [V_x - V_{TN}]^2$$

$$\Rightarrow 50 = \frac{1}{2} (250) (10) [V_x - 0.7]^2$$

$$\Rightarrow \boxed{V_x = 0.9 \text{ V}}$$

Now, it can be seen that $V_{GS1} = V_{GS3} = V_x$
 And, all transistors are in saturation (mentioned).

So, $I_3 = 50 \mu A$ [Transistors are in saturation and there is no channel length modulation effect. So $I_D = f(V_{GS})$ only.]

$$\therefore V_y = V_{DD} - (I_3)R$$

$$V_y = 2 - ((50)(2.3) \times 10^{-3})$$

$$\boxed{V_y = 1.885}$$

For M2,

$$I_2 = \frac{1}{2} \mu_{n,ox} \left(\frac{W}{L} \right)_2 [V_{GS2} - V_{TN}]^2$$

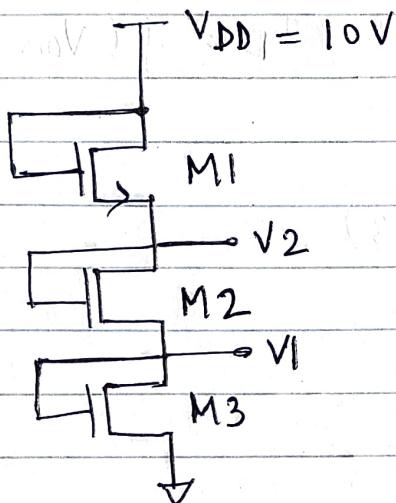
$$\Rightarrow 40 = \frac{1}{2} (250) \left(\frac{W}{L} \right)_2 [V_y - V_x + 0.7]^2$$

$$\Rightarrow 40 = \frac{1}{2} (250) \left(\frac{W}{L} \right)_2 [1.885 - 0.9 - 0.7]^2$$

$$\Rightarrow \boxed{\left(\frac{W}{L} \right)_2 = 3.939} \quad (\text{Ans})$$

- Q4) For the circuit given below, assume that for each MOSFET $\mu_{n,ox} = 120 \mu A/V^2$ and threshold voltage is $V_{TN} = 1.2 V$ and power supply (V_{dd}) is 10 V. In order to have a DC bias current of $600 \mu A$ and V_1 and V_2 equal to 2.5 V and

6V respectively, the aspect ratio ($\frac{W}{L}$) of each transistor needs to be adjusted. The sum of three required aspect ratio is : (Give at least 3 decimal places in your answer).



Solution : $I_{D1} = I_{D2} = I_{D3} = 600 \mu A = 0.6 \text{ mA}$

$$\frac{0.6 \text{ mA} \times 2}{4n60x} = \left(\frac{W}{L}\right)_1 (V_{GS1} - V_T)^2 = \left(\frac{W}{L}\right)_2 (V_{GS2} - V_T)^2 = \left(\frac{W}{L}\right)_3 (V_{GS3} - V_T)^2$$

$$\Rightarrow \left(\frac{W}{L}\right)_1 (V_{GS1} - V_T)^2 = \left(\frac{W}{L}\right)_2 (V_{GS2} - V_T)^2 = \left(\frac{W}{L}\right)_3 (V_{GS3} - V_T)^2 = \frac{0.6 \text{ mA} \times 2}{120 \mu A / V^2} = 10$$

$$\therefore \left(\frac{W}{L}\right)_1 (2.5 - 1.2)^2 = 10 \Rightarrow \left(\frac{W}{L}\right)_1 = 5.917$$

$$\therefore \left(\frac{W}{L}\right)_2 (6 - 2.5 - 1.2)^2 = 10 \Rightarrow \left(\frac{W}{L}\right)_2 = 1.890$$

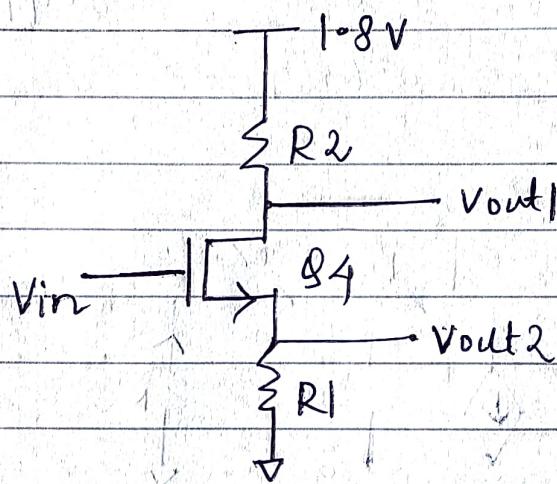
$$\therefore \left(\frac{W}{L}\right)_3 (10 - 6 - 1.2)^2 = 10 \Rightarrow \left(\frac{W}{L}\right)_3 = 1.275$$

$$\therefore \boxed{\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2 + \left(\frac{W}{L}\right)_3 = 9.082} \quad (\text{Ans})$$

Q5) Assume that the short channel length transistor Q4 is kept in saturation region always by a DC biasing circuit omitted from the schematic shown below.

If the quiescent DC drain current is 101.4A , channel length modulation parameter (λ) = 0.01V^{-1} , $\mu_{n,\text{ext}} = 111\text{mA/V}^2$, $V_{TN} = 1\text{V}$, $\frac{w}{L} = 13\mu\text{m}/500\text{nm}$, $R_2 = 11.5\text{k}\Omega$,

$R_1 = 6.9\text{k}\Omega$, find the ratio V_{out1}/V_{out2} .



Solution: For this question, both the following approaches are considered correct.

$$a) \frac{V_{out1}}{V_{out2}} = \frac{\text{Operating voltage } V_{out1}}{\text{Operating voltage } V_{out2}}$$

$$b) \frac{V_{out1}}{V_{out2}} = \frac{\text{small signal voltage } v_{out1}}{\text{small signal voltage } v_{out2}}$$

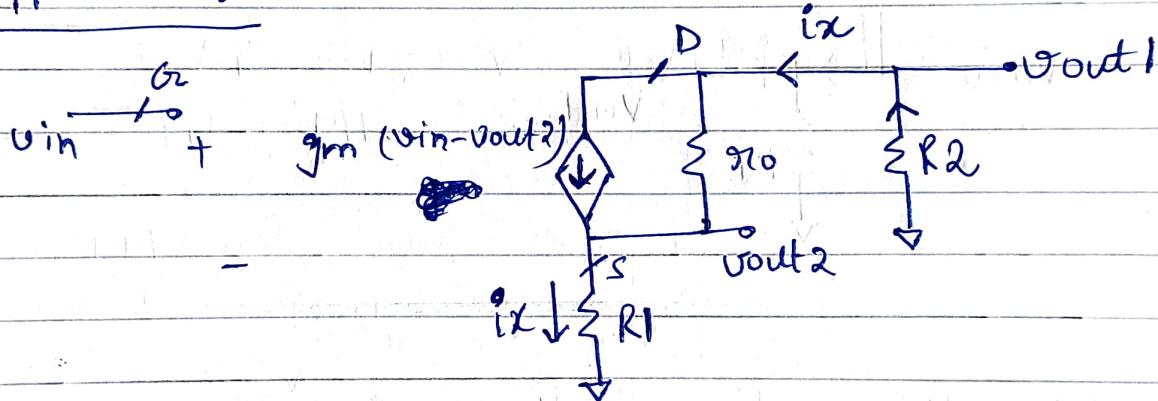
Approach a) : $I_D = 101 \mu A$

$$\frac{V_{OUT1}}{V_{OUT2}} = \frac{V_{DD} - (I_D)(R_2)}{I_D R_1}$$

$$\Rightarrow \frac{V_{OUT1}}{V_{OUT2}} = \frac{1.8 - (101 \mu A)(11.5 k\Omega)}{(101 \mu A)(6.9 k\Omega)}$$

$$\Rightarrow \frac{V_{OUT1}}{V_{OUT2}} = \frac{0.6385}{0.6969} = 0.9162 \text{ (Ans)}$$

Approach b) :



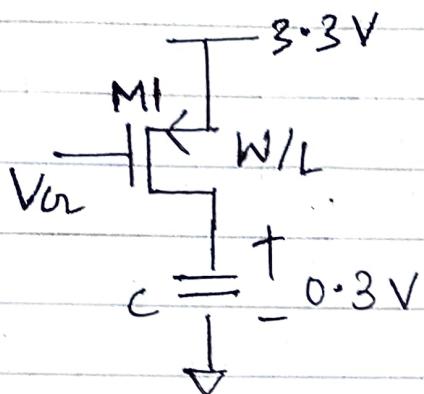
$$\frac{0 - V_{OUT1}}{R_2} = \frac{V_{OUT2}}{R_1}$$

$$\Rightarrow \frac{V_{OUT1}}{V_{OUT2}} = - \frac{R_2}{R_1} = - \frac{11.5 k\Omega}{6.9 k\Omega} = -1.667 \text{ (Ans)}$$

Q6) In the circuit shown below, $V_{DD} = 3.3 V$, $V_{GS} = 0.3 V$, $W/L = 7$, $\mu C_{ox} = 50 \mu A/V^2$, $|V_{TH}| = 0.5 V$, $C = 25 pF$.

Assume the capacitor C is initially charged to $0.3 V$.

Find out the time instant at which M1 will be at the edge of saturation in μsec (Accuracy ± 0.001)

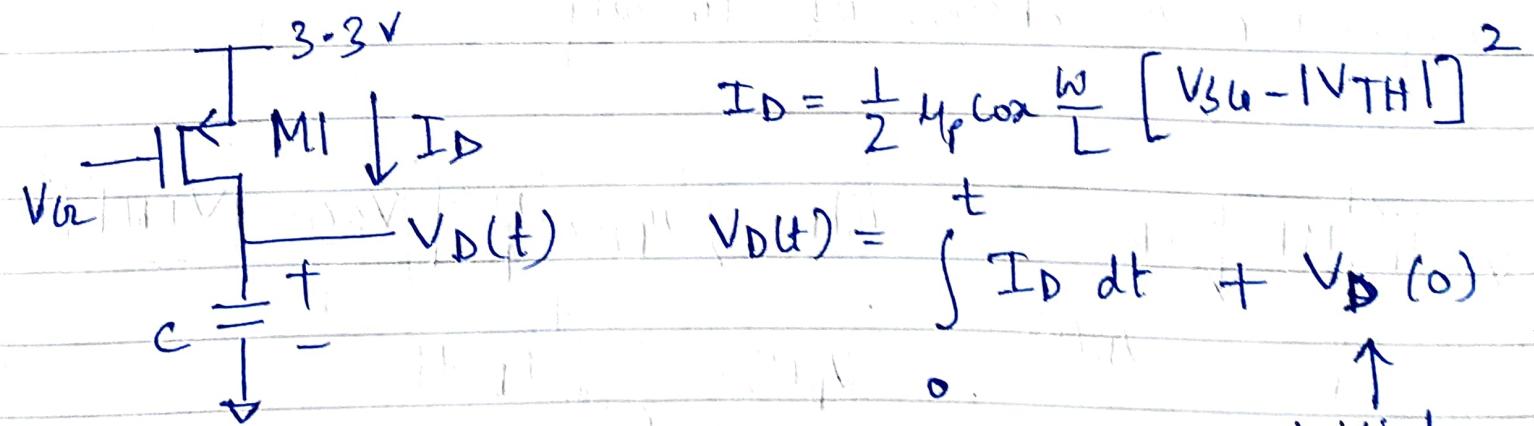


Solution: $V_S = 3.3V$, $V_A = 0.3V$, $V_D = 0.3V$, $|V_{TH}| = 0.5V$

$$\therefore V_{SD} = 3V, V_{SD} - |V_{TH}| = 2.5V$$

\therefore PMOS M1 is initially in saturation region.

So, M1 acts like a constant current source and capacitor C charges up linearly.



$$I_D = \frac{1}{2} \mu_p C_o x \frac{W}{L} [V_{SD} - |V_{TH}|]^2$$

$$V_D(t) = \int_0^t I_D dt + V_D(0)$$

↑
initial stored voltage.

As capacitor C charges up, V_D mode increases and edge of saturation happens when:

$$V_{SD} = V_{S0} - |V_{TH}|$$

$$\Rightarrow V_D = V_{S0} + |V_{TH}|$$

Let's assume at time instant $t = t_0$, edge of sat occurs.

$$\therefore V_D(t_0) = \frac{1}{C} \int_0^{t_0} I_D dt + V_D(0)$$

$$\Rightarrow V_{D0} + |V_{TH}| = \frac{1}{C} \int_0^{t_0} \frac{1}{2} \mu_p C_{ox} \frac{W}{L} [V_{SD} - |V_{TH}|]^2 dt + 0.3$$

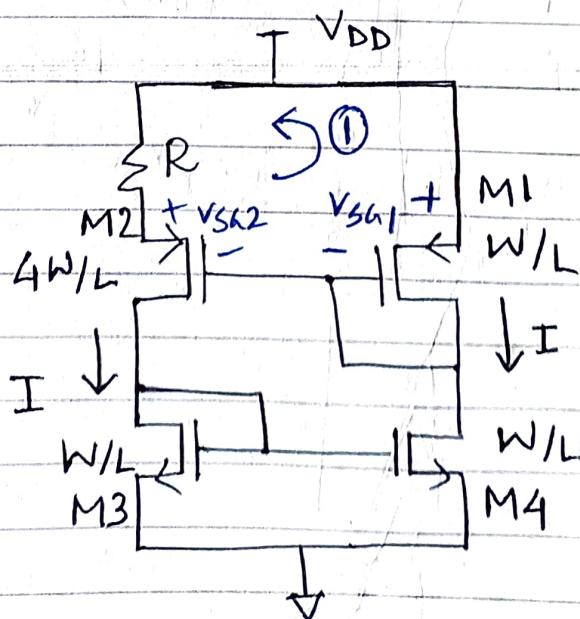
$$\Rightarrow \frac{1}{2} (50 \mu A/V^2) (7) (2.5)^2 t_0 = (0.3 + 0.5 - 0.3) 25PF$$

$$\Rightarrow t_0 = \frac{(0.5)(25PF)}{\frac{1}{2} (50 \mu A/V^2) (7) (2.5)^2} = 0.0114 \mu\text{sec}$$

(Ans)

Q7) In the circuit shown below, $V_{DD} = 3.3V$, $\mu_n C_{ox} = 2 \mu_p C_{ox} = 50 \mu A/V^2$, $|V_{THN}| = |V_{THP}| = 1V$, $W/L = 1$ and $R = 15k\Omega$.

Assume currents through both branches are equal and all transistors are in saturation. Find the transconductance (g_m) of M1 in μS . (Accuracy required: $\pm 0.1\%$.)



Solution: Applying KVL in Loop ①,

$$V_{S1} = IR + V_{S2} \\ \Rightarrow V_{S1} - V_{S2} = IR \quad \text{--- (1)}$$

$$V_{S1} = \sqrt{\frac{2I}{\mu_{pox} \frac{W}{L}}} + |V_{THP}| \quad \text{--- (2)}$$

$$V_{S2} = \sqrt{\frac{2I}{\mu_{pox} \left(\frac{4W}{L}\right)}} + |V_{THP}| \quad \text{--- (3)}$$

Putting (2) & (3) in (1),

$$(V_{S1} - V_{S2})^2 = (IR)^2$$

$$\Rightarrow \left[\sqrt{\frac{2I}{\mu_{pox} \frac{W}{L}}} + |V_{THP}| - \sqrt{\frac{2I}{\mu_{pox} \frac{W}{L}} + |V_{THP}|} \right]^2 = (IR)^2$$

$$\Rightarrow \frac{2I}{\mu_{pox} \frac{W}{L}} \left[1 - \frac{1}{2} \right]^2 = (IR)^2$$

$$\Rightarrow \frac{2I}{\mu_{pox} \frac{W}{L}} \left[1 + \frac{1}{4} - 1 \right] = I^2 R^2$$

$$\Rightarrow I = \frac{1}{2R^2 \mu_{pox} \frac{W}{L}}$$

$$\text{Transconductance of M1} = g_m = \sqrt{2 I_{\text{D}} \mu_{\text{FET}} \frac{W}{L}}$$

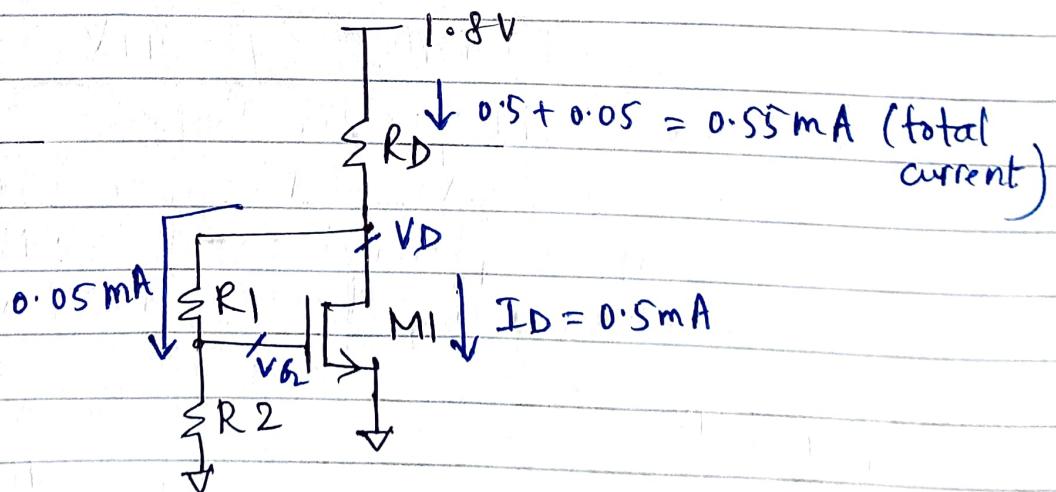
$$\Rightarrow g_m = \sqrt{2 \cdot \frac{1}{2 R^2 \mu_{\text{FET}} \frac{W}{L}}} \cdot \mu_{\text{FET}} \frac{W}{L}$$

$$\Rightarrow g_m = \boxed{\frac{1}{R}}$$

$$\Rightarrow g_m = \frac{1}{15k\Omega} = 66.667 \mu\text{s} \quad (\text{Ans})$$

Q8) In the following circuit, the drain current of the MOSFET is 0.5 mA . Calculate the ratio of R_1 and R_2 such that the current flowing through resistors equals one-tenth of the drain current. Given $\mu_{\text{FET}} = 200 \mu\text{A/V}^2$, $V_{\text{TH}} = 0.4 \text{ V}$, $R_D = 865 \Omega$, $W = 50 \mu\text{m}$ and $L = 180 \text{ nm}$. (Give atleast correct upto 2 decimal places).

Solution :



$$V_D = 1.8 - (0.55 \text{ mA})(R_D)$$

$$\Rightarrow V_D = 1.8 - (0.55 \text{ mA})(865 \Omega)$$

$$\Rightarrow V_D = 1.324 \text{ V.}$$

Assuming M1 is in saturation,

$$I_D = \frac{1}{2} \mu n C_{ox} \frac{W}{L} [V_{DS} - V_{TH}]^2$$

$$\Rightarrow 0.5 \text{ mA} = \frac{1}{2} (200 \mu \text{A}/\text{v}^2) \left(\frac{50 \mu \text{m}}{0.18 \mu \text{m}} \right) [V_D - 0.4]^2$$

$$\Rightarrow \boxed{V_D = 0.534 \text{ V}}$$

$(V_{DS} > V_{DS} - V_{TH}) \rightarrow M1 \text{ is in saturation.}$
Above assumption is valid.

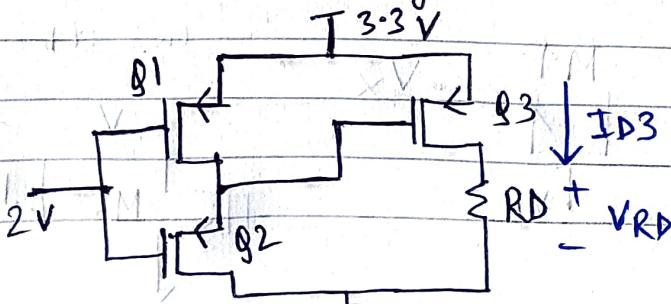
$$\therefore R_1 = \frac{V_D - V_A}{0.05 \text{ mA}} = \frac{1.0324 - 0.534}{0.05 \text{ mA}} = 15.8 \text{ k}\Omega$$

$$\text{And, } R_2 = \frac{V_A}{0.05 \text{ mA}} = 10.68 \text{ k}\Omega$$

$$\boxed{\frac{R_1}{R_2} = \frac{15.8 \text{ k}\Omega}{10.68 \text{ k}\Omega} = 1.479 \quad (\text{Ans})}$$

Q9) In the circuit shown below, the transistors are all identical. Calculate the value of V_{DS3} (in Volts), given that $|V_{TP}| = 1 \text{ V}$, $(\frac{W}{L})_1 = (\frac{W}{L})_3 = 0.45 (\frac{W}{L})_2$.

If $V_{SG2} > 1 \text{ V}$ is always true. Consider $R_D = 7 \text{ k}\Omega$.



Solution : Given $V_{SA2} > 1V$ always.

$$V_{S2} > 1 + V_{A2}$$

$$\Rightarrow V_{S2} > 1 + 2$$

$$\Rightarrow V_{S2} > 3V \leftarrow \text{always}$$

$$\text{and, } V_{S2} = V_{A3}$$

$$\therefore V_{SA3} = 3 \cdot 3 - V_{A3}$$

$$\text{if } V_{A3} > 3V, \text{ then } V_{SA3} < 0.3V$$

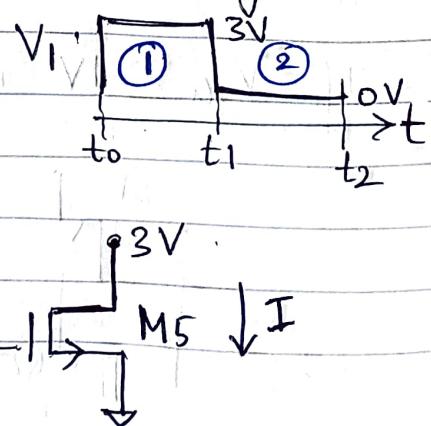
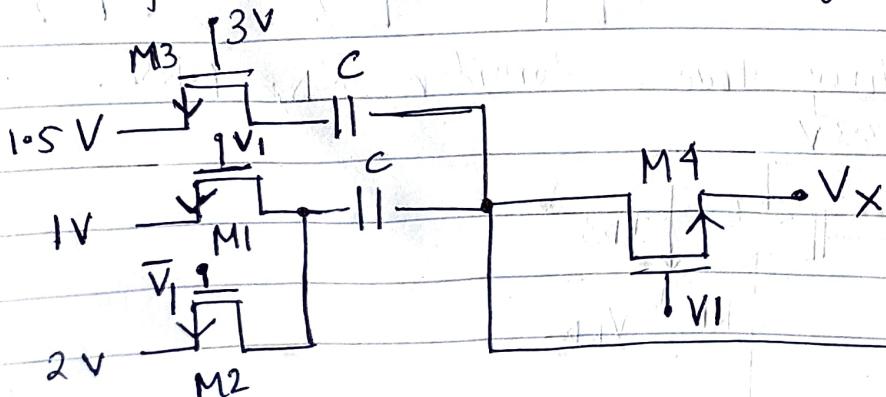
$$\text{Given } |V_{TP}| = 1V$$

$$\therefore V_{SA3} < |V_{TP}| \rightarrow Q_3 \text{ is in cutoff.}$$

$$\text{So, } I_{D3} = 0A, V_{RD} = 0V.$$

$$\text{and, } V_{DS3} = -3.3V \quad \underline{\text{Ans}}$$

Q10) In the circuit shown below, $V_x = 0.9V$ and $C = 80fF$, V_{TH} of all transistors = $0.5V$, $\mu_{nCOX} = 50mA/N^2$, aspect ratio of $M_5 = 8$, V_I is a pulse varying from $3V$ to $0V$. Find the current through M_5 after time t_1 in μA . (Consider R_{ON} of all transistors to be negligible). (Accuracy $\pm 0.1\%$.)

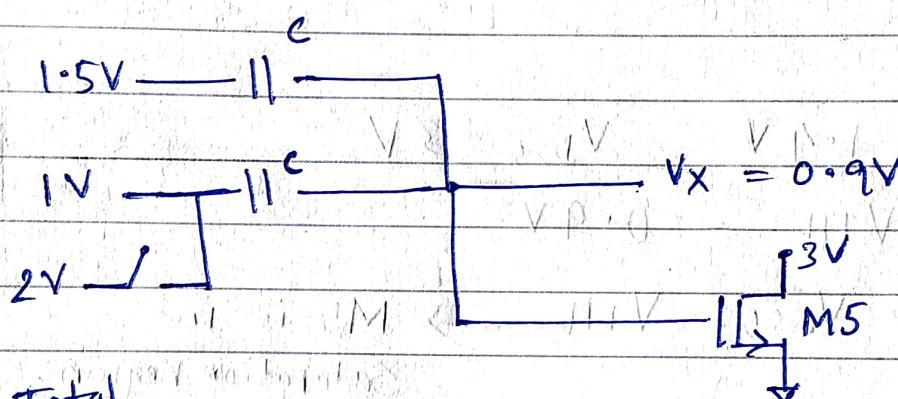


Solution :

Transistors M1, M2, M3 and M4 are acting as switches.
ON \rightarrow Linear region, OFF \rightarrow cutoff region.

Phase ① ($t_0 < t < t_1$)

$$V_1 = 3V, \bar{V}_1 = 0V$$



Total

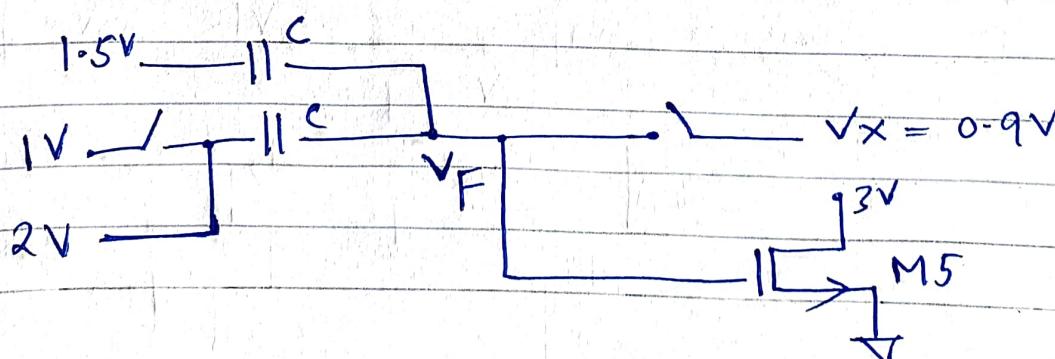
\therefore Charge stored in the capacitors in phase 1,

$$\begin{aligned} Q_{\text{tot1}} &= (1.5 - V_x)C + (1 - V_x)C \\ &= (1.5 - 0.9)C + (1 - 0.9)C \end{aligned}$$

$$Q_{\text{tot1}} = 0.7C$$

After time t_1 , (Beginning of phase ②)

$$V_1 = 0V, \bar{V}_1 = 3V$$



Total charge has to be conserved at floating node ' V_F ' from phase ① to phase ②,

$$\therefore (1.5 - V_F) C + (2 - V_F) C = Q_{\text{tot}}$$

$$\Rightarrow \cancel{(3.5 - 2V_F)C} = 0.7C$$

$$\Rightarrow V_F = 1.4 \text{ Volts}$$

For M5,

$$V_{GS5} = 1.4 \text{ V}, \quad V_{DS5} = 3 \text{ V}$$

$$V_{GS5} - V_{TH} = 0.9 \text{ V}$$

$\therefore V_{DS5} > V_{GS5} - V_{TH} \rightarrow M5 \text{ is in Saturation region.}$

$$\begin{aligned} \therefore I &= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS5} - V_{TH}]^2 \\ &= \frac{1}{2} \left(\frac{50 \mu A}{V^2} \right) (8) (1.4 - 0.5)^2 \end{aligned}$$

$$I = 162 \mu A$$