# ELL304 Assignment 2

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## Contents

# 1 DC sweep

## 1.1 Part 1a

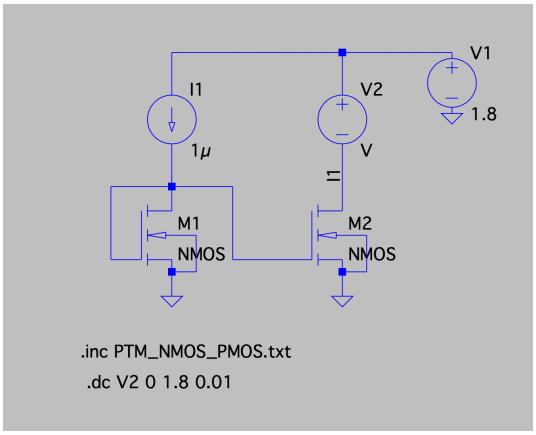


Figure 1: Circuit Diagram of a current mirror.

- We plot the current $I_d$ through $M_2$ as we vary $V_2$ from 0V - 1.8V.
- The dimensions of $M_1$ and $M_2$ are $\frac{W}{L} = \frac{2\mu}{0.18\mu}$

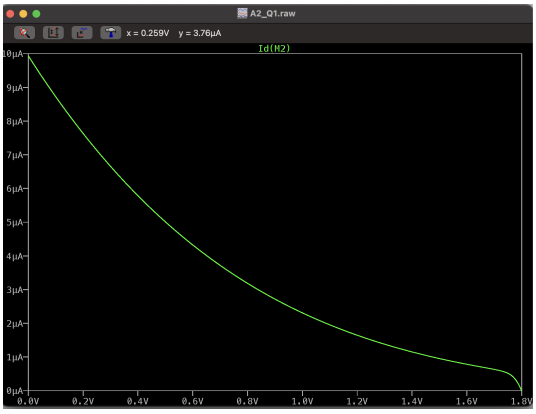


Figure 2: Variation of $I_d$ flowing into $M_2$ as we vary $V_2$.

## 1.2 Part 1b

- Change the L of $M_1$ and $M_2$ from $0.18\mu$ to $1\mu$ and repeat.


Figure 3: Variation of $I_d$ flowing into $M_2$ as we vary $V_2$ after changing dimensions of L.

- We see that the gain drops due to increase in L and process variations but the waveform of the variation of current remains the same.
- The extra current flows into parasitic capacitances and body of the MOSFETs, hence we can see a lot of non-ideality at edge of process limits (smaller transistors have more mismatches).
- As we increase L, we reduce the extra currents through the parasitic elements and observe more ideal mirroring action. We also have better output impedance.

## 1.3 Part 2a

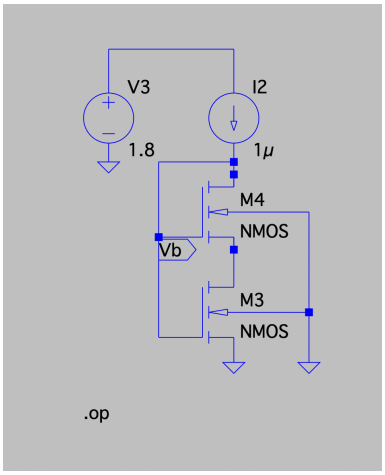


Figure 4: Circuit Diagram of a current mirror.

- The MOSFET $M_4$ will be in saturation and $M_3$ will be in linear region.
- The bias Voltage $V_b$ turns out to be 0.839V.

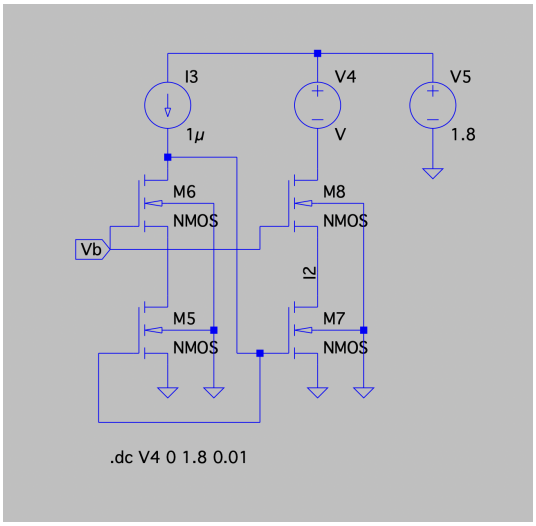


Figure 5: Circuit Diagram of a low swing cascode current mirror.

- We plot the current $I_d$ through $M_7$ as we vary $V_4$ from 0V - 1.8V.
- The dimensions of all MOSFETs except $M_3$ are $\frac{W}{L} = \frac{2\mu}{0.18\mu}$
- The dimensions of $M_3$ are $\frac{W}{L} = \frac{0.24\mu}{5\mu}$


Figure 6: Variation of $I_d$ flowing into $M_7$ as we vary $V_4$.

### 1.4 Part 2b

- We change the dimensions of all MOSFETs except $M_3$ to $\frac{W}{L} = \frac{2\mu}{1\mu}$ and repeat.
- The bias Voltage $V_b$ changes to 0.854V.

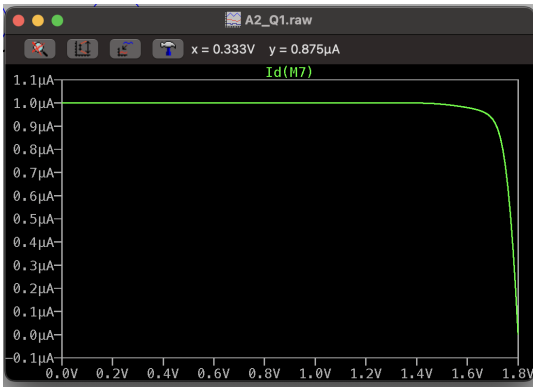


Figure 7: Variation of $I_d$ flowing into $M_7$ as we vary $V_4$ after changing dimensions.

- We see that the gain drops due to increase in L and process variations but the waveform of the variation of current remains the same.
- We again see same pattern in low-swing cascode current mirror and reduce non-ideality as we increase L.

## 2 CS Amplifier Design

- We need to design a CS Amplifier for a DC gain of 30dB and a Unity Gain Bandwidth of 50MHz while minimising power dissipation.
- The gain of a common source amplifier is approximately $g_m(R_D||R_L)$
- A gain of 30dB is equivalent to a gain of 31.622 on the linear scale.
- If we start with the design of $g_m \approx 5mS$, for sufficient swing, if we keep the gate overdrive voltage as 0.2V, we get that $I_D$ is 0.5mA.
- But the problem is that the drain voltage can fall only 1 threshold below the gate voltage, therefore, $V_{DD} - I_D R_D > V_{overdrive}$. Therefore, we get $R_D$ ¡ $3.2k\Omega$. But this amount to a gain of only 24.08 dB.
- We see that the condition of the MOSFET being in saturation is limiting our gain. Therefore we should decrease our drain current. We can achieve this by decreasing the overdrive voltage but this is traded off with limited input and output swings.

- $$g_m = \frac{2I_D}{V_{GS} - V_T} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)$$
- Lets start with the overdrive voltage of 0.01V, i.e

  $$V_G = V_T + 0.01 = 0.39 + 0.01 = 0.4V$$

  . Note that this is seriously limiting our input voltage swing.
- From the MOS I-V characteristics, as we have the MOSFET changing it's threshold with operating points as well, we approximate the $g_m$ should be in the order of $\mu$S.
- If we include a little body effect, $g_m + g_{m_b}$ can be in 10's of $\mu$S and $I_D$ will be in 100's of nA ($10^-7$).
- Therefore for a gain of 31.62, we need $R_D||R_L \approx 30M\Omega$.
- But $R_D$ is limited as we need to ensure the MOSFET is in saturation. Therefore if $I_D$ is in 100's of nA, $R_D$ cannot be higher than $10M\Omega$.
- From the MOS I-V characteristics, $\mu_n C_{ox} \frac{W}{L} \approx 10^-3$.
- With a little bit of trial and error, we see that choosing $R_D = 3.5M\Omega$ gives us satisfactory gain. We need to choose $R_L$ sufficiently large so that $R_D||R_L \approx R_D$ as well ($R_L >> R_D, R_L = 100R_D$).
- We chose $V_G = 0.4V$, therefore $R_2 = 3.5M\Omega$ and $R_1 = 1M\Omega$. We need to choose large values of resistive voltage divider as well as we do not desire large voltage drop across $R_S$ in the small signal model.
- We give the small signal input with a coupling capacitor of $1\mu$F and observe output across $R_L$ through another capacitor to reject the DC component.
- The coupling capacitor initially cuts the small frequencies as it provides an impedance of $1/sC_{cc}$ which is in the order of $M\Omega$ below 100Hz.
- If we do not consider $R_S$ in the input voltage source, the circuit will have only 1 pole and 1 zero and the gain will never drop below zero but the phase will cross $-360^\circ$ making the system unstable. Therefore we take an $R_S$ of $100\Omega$.

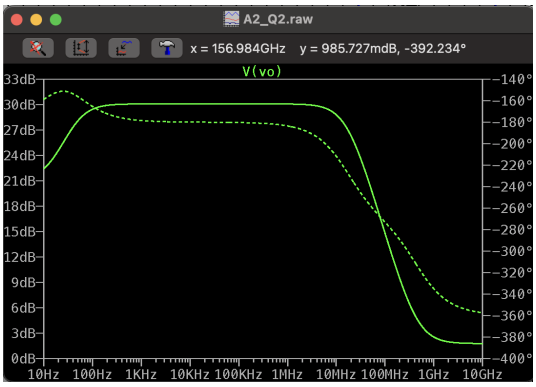


Figure 8: AC Magnitude and phase plot if $R_S = 0$

- Therefore, the circuit for the amplifier is :

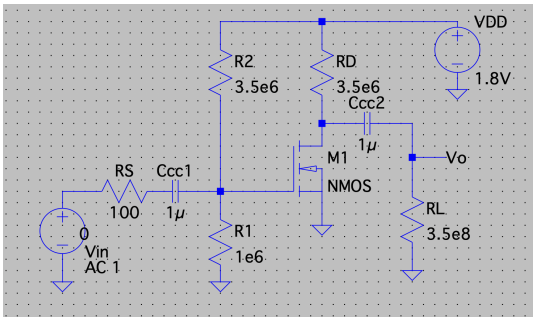


Figure 9: CS Amplifier

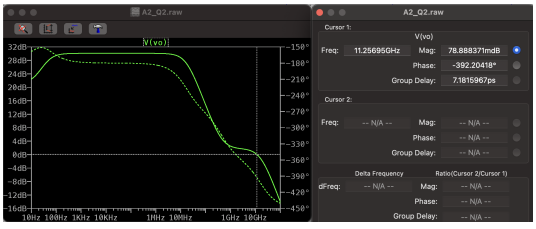


Figure 10: AC Magnitude and phase response.

- From the above plot, we can see that even if we consider $R_S$, the output pole is much further than the zero and the magnitude is not falling fast enough which leads to phase crossover before gain crossover, hence making the system unstable. Therefore, we need to compensate the system with poles to get the desired frequency response.

- If we compensate the system with a miller-cap, we move the input pole closer and the output pole further. If we compensate with $C_{GD}$,

$$\omega_{in} = \frac{1}{R_S(C_{GS} + (1 + g_m(R_D||R_L)C_{GD}))}$$

$$\omega_{out} = \frac{1}{R_D(C_{DB} + C_{GD})}$$

  for our MOSFET model, $C_{DB} = 0, C_{GS} = 2.72fF$. The miller-cap introduces a zero in the system as well. Therefore, to make the system stable, we need to sacrifice on the bandwidth.

- We notice that we cant keep the value of $C_{GD}$ too large as that will cause extremely low bandwidth and low gain. We also notice that just compensating with a miller-cap causes the frequency response to be around 0dB for a long time before the output pole so we will have very less phase margin which is again undesireable.

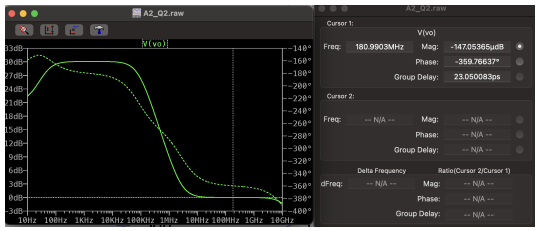


Figure 11: AC Magnitude and phase response of compensated system with miller-cap $C_{GD} = 600fF$.

  As we can see, we have a PM of less than 0.3°.

- If we keep increasing the miller-cap, the BW decreases very fast and we will not be able to achieve a UGB of 50MHz as the input pole keeps moving closer and closer. So we will try to move the output pole closer to get a good PM and satisfactory UGB as well. Therefore, we will add a capacitor $C_{DS}$

- The $C_{DS} gets added in parallel to the C_{GD} after miller multiplication.$

- Compensating with $C_{GD} = C_{DS} = 15fF$ gives us a good response with UGB of 57MHz and a Phase Margin of 57° (PM of 60° is ideal as it has fast response as well as very low overshoot).

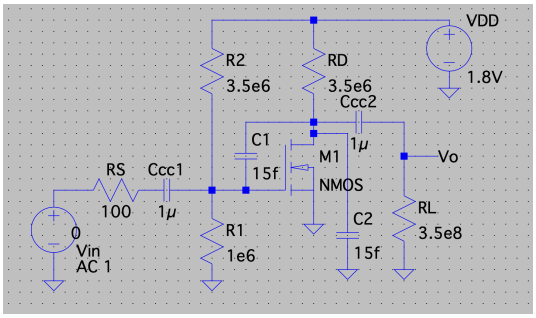


Figure 12: Compensated CS Amplifier

- The operating points are,
  $I_D = 0.442\mu A$
  $V_{GS} = 0.4V$
  $V_T = 0.391V$
  $V_{DS} = 0.254V$
  $g_m = 8.34\mu S$

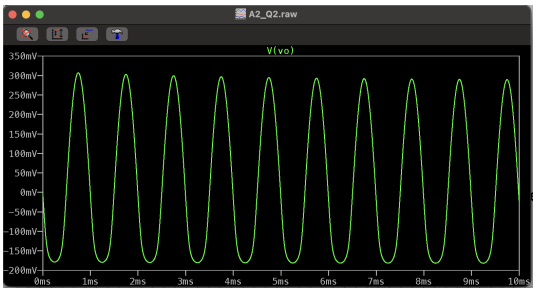


Figure 13: Transient response with input voltage amplitude of 0.01

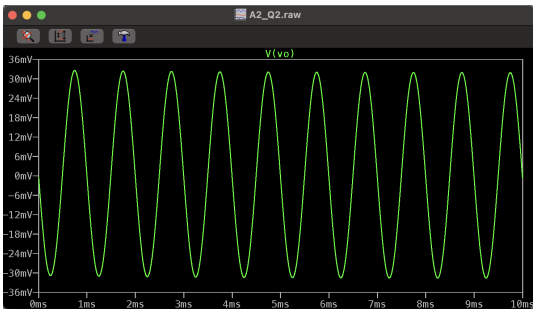


Figure 14: Transient response with input voltage amplitude of 0.001

- Clearly, we can see that the output is clipped as the MOSFET is entering into linear region indicating low swing.

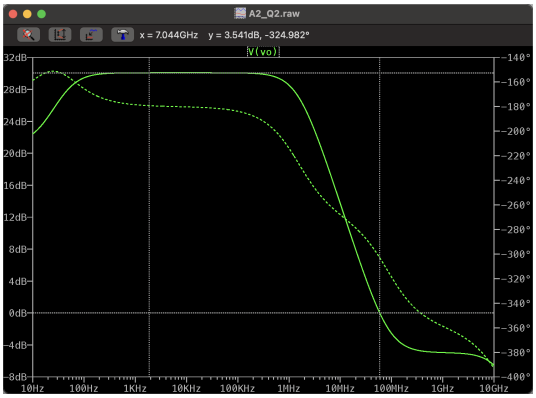


Figure 15: AC Magnitude and phase response.

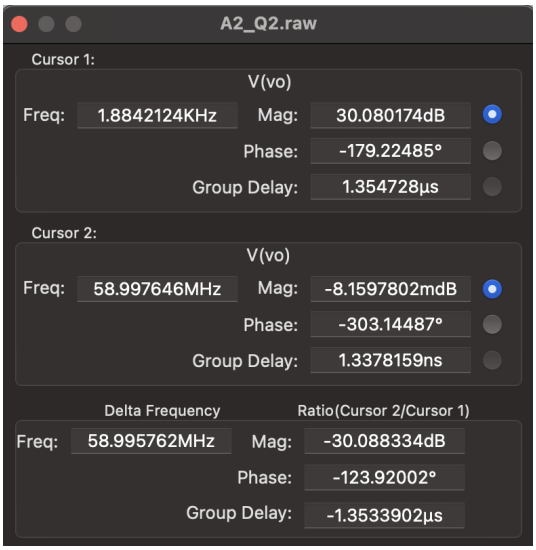


Figure 16: DC gain and PM

# 3 Noise Analysis

– For a CS Amplifier driving a capacitive load, the input referred noise per unit bandwidth is :

$$V_{n,in}^2 = \frac{4kT}{g_m(R_D||R_L)^2} + \frac{4kT\gamma}{g_m}$$

Therefore, the total noise at the output is :

$$V_{n,out,tot}^2 = \int_0^\infty (V_{n,in})^2 (g_m(R_L||R_D))^2 |H(f)|^2 df$$

$$V_{n,out,tot}^2 = \int_0^\infty (4kT(R_D||R_L) + 4kT\gamma g_m(R_D||R_L)^2) \frac{1}{1+4\pi^2(R_D||R_L)^2 C_L^2} df$$

$$V_{n,out,tot}^2 = (1+\gamma g_m(R_D||R_L)) \frac{kT}{C_L}$$

Therefore the total input referred noise is :

$$V_{n,in,tot}^2 = \frac{1+\gamma g_m(R_D||R_L)}{g_m^2(R_D||R_L)^2} \frac{kT}{C_L}$$

– On performing the noise analysis on the CS amplifier, we can plot the input and output referred noise voltages.

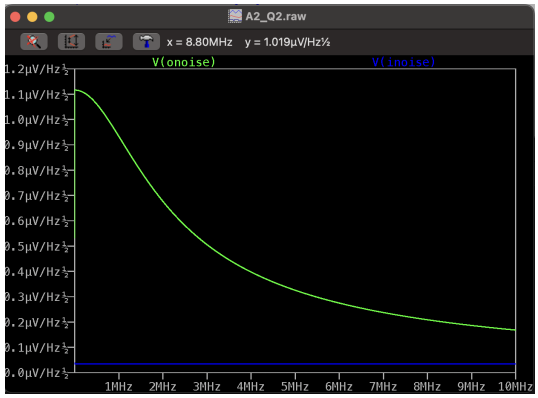


Figure 17: Output and input noise

– The input noise is a white spectrum and the output noise is a combination of low frequency flicker noise and noise due to capacitive load.
– The Noise due to bias resistors is very very low.
– When we integrate the output noise over a 1MHz bandwidth, we LTSpice gives us a value of 0.0024617. This is in V.
– Therefore, the noise power is $6.06mV^2$.
– From the analytical expression, plugging in the values of $C_L = 15fF$, T = 298K, $\gamma = 2/3$ for a long-channel MOSFET, we get total output noise as $1.102mV^2$ which is slightly less than the simulated value as we have not considered the non-idealitites of the process and body effect.