

ELL 304: Lab 1 Report

Device Characterization

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1 Aim

- To get acquainted with MOS device.
- Observe I_D vs V_{GS} characteristics for nMOS and pMOS
- CMOS Inverter ...?

2 Apparatus Required

- CD4007 IC
- Breadboard
- Oscilloscope
- DC Source Generator
- Function Generator
- Resistances

3 Theory

- The drain current through a MOSFET is given as:

$$I_D = \begin{cases} 0 & , V_{GS} < V_{Th} \\ \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{Th}) V_{DS} - \frac{V_{DS}^2}{2} \right) & , V_{GS} > V_{Th}, V_{DS} < (V_{GS} - V_{Th}) \\ \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2 & , V_{GS} > V_{Th}, V_{DS} > (V_{GS} - V_{Th}) \end{cases}$$

:Cut-off region
:Triode region
:Saturation region

The above equation is for nMOS. But similar equation can be written for pMOS.

- When gate and drain are shorted in a MOSFET, the MOSFET when ON is always in saturation region.

- CMOS inverters are designed as a combination of pMOS and nMOS with a common gate and common drain. A biasing voltage is applied at the source terminal of pMOS and source of nMOS is grounded. The common gate terminal acts as input terminal and common drain terminal acts as output terminal.

When a low input voltage is applied to CMOS, pMOS is switched ON and nMOS is switched OFF. Hence it allows a flow of current through the output terminal producing high output (ON).

Similarly, when high input is applied to CMOS, then PMOS is switched OFF and NMOS is switched ON. Hence, the resulting output voltage is low (OFF).

- The CD4007 integrated circuit contains 3 n-channel and 3 p-channel MOS devices as per the diagram below.

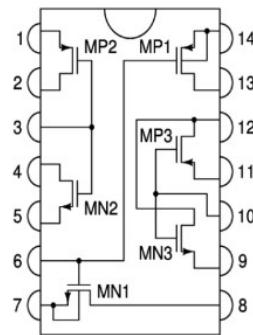


Figure 1: CD4007 IC Pin diagram

4 Procedure

4.1 Part 1

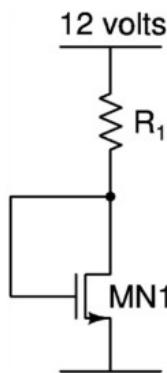


Figure 2: Circuit Diagram for part 1

- Circuit was connected as shown in circuit diagram. Pin 7 (source) was connected to ground and pins 6 (gate) and 8 (drain) were shorted. Pin 8 was then connected to resistor R_1 , whose other end was connected to source V_{DD}
- Oscilloscope probes were connected to pin 8 and ground respectively and voltage was measured.

- Readings were taken for different values of R_1 .

4.2 Part 2

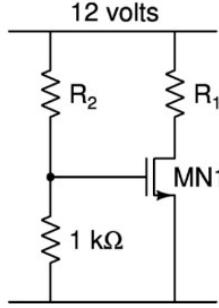


Figure 3: Circuit Diagram for part 2

- Circuit was connected as shown in circuit diagram. Pin 7 (source) was connected to ground. Pin 8 (drain) was connected to resistor R_1 . Pin 6 (gate) was connected to two resistors R_2 and $1\text{K}\Omega$. The other ends of resistors were connected as shown.
- Oscilloscope probes were connected at pin 8 and ground respectively and voltage readings were taken.
- Readings were taken for different values of R_2 , varying R_1 for each.

4.3 Part 3

4.3.1 Part a

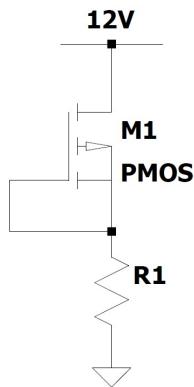


Figure 4: Circuit Diagram for part 3a

- Connections were made similar to part 1, as shown in circuit diagram. Pin 14 was connected to supply V_{DD} . Pins 6 (gate) and 13 (drain) were shorted and resistor R_1 was connected to pin 13.
- Oscilloscope probe was connected at pin 13 and ground respectively and voltage readings were taken.
- Readings were taken for different values of R_1 .

4.3.2 Part b

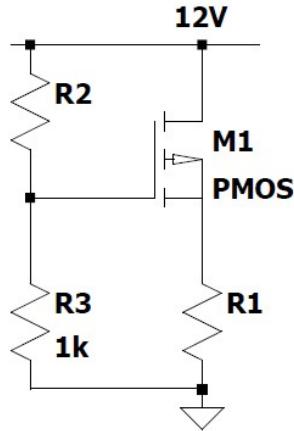


Figure 5: Circuit Diagram for part 3b

- Connections were made similar to part 2, as shown in circuit diagram. Pin 14 was connected to supply V_{DD} . Pin 13 was connected to resistor R_1 . Pin 6 (gate) was connected to resistors R_2 and $1K\Omega$. The other ends of resistors were appropriately connected.
- Oscilloscope probe was connected at pin 13 and ground respectively and voltage readings were taken.
- Readings were taken for different values of R_2 , varying R_1 for each.

4.4 Part 4

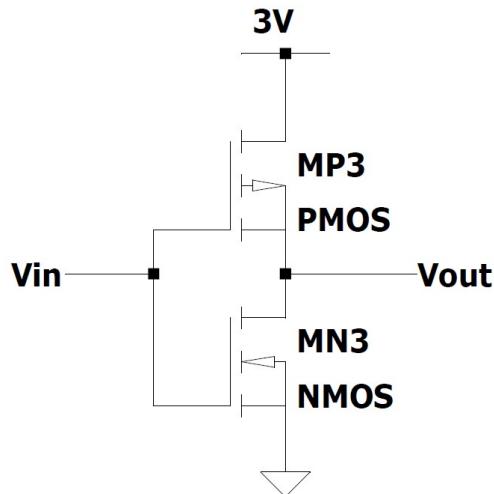


Figure 6: Circuit Diagram for part 4

- MP1 and MP3 are configured as CMOS inverter. The pins were correctly connected as per circuit diagram shown.
- Different DC voltages were applied at gate and the drain voltages were noted.
- Now, a triangular wave from function generator was applied at gate and frequency was increased till the output at drain was no longer a square wave.

5 Results and Calculations

5.1 Readings

5.1.1 Part 1

$V_{DD} = 12 \text{ V}$

R_1 (Ω)	V_{GS} (V)	$I_D = \frac{V_{DD}-V_{GS}}{R_1}$ (mA)
82	10.1	23.17073
220	8.12	17.636
330	7.33	14.15152
560	6	10.7143
1000	4.8	7.2
3300	3.11	2.6939
4700	2.8	1.9574
8200	2.39	1.1719
10000	2.25	0.975
220000	1.23	0.0489

Table 1: Measurements of V_{GS} and calculation of corresponding I_D

5.1.2 Part 2

$V_{DD} = 12 \text{ V}$

R_1 (Ω)	R_2 (Ω)	V_{DS} (V)	I_D (mA)	V_{GS} (V)
470	470	4.33	16.31914894	8.163265306
1000	470	2.64	9.36	8.163265306
3300	470	1.27	3.251515152	8.163265306
4700	470	0.854	2.371489362	8.163265306
10000	470	0.303	1.1697	8.163265306
470	1000	6.8	11.06382979	6
1000	1000	3.64	8.36	6
3300	1000	1.45	3.196969697	6
4700	1000	1.02	2.336170213	6
10000	1000	0.343	1.1657	6
470	3300	10.1	4.042553191	2.790697674
1000	3300	9.52	2.48	2.790697674
3300	3300	4	2.424242424	2.790697674
4700	3300	2.06	2.114893617	2.790697674
10000	3300	0.712	1.1288	2.790697674
470	4700	11	2.127659574	2.105263158
1000	4700	10	2	2.105263158
3300	4700	7.83	1.263636364	2.105263158
4700	4700	5.99	1.278723404	2.105263158
10000	4700	1.95	1.005	2.105263158
470	10000	12	0	1.090909091
1000	10000	12	0	1.090909091
3300	10000	11.9	0.03030303	1.090909091
4700	10000	11.8	0.042553191	1.090909091
10000	10000	10.7	0.13	1.090909091

Table 2: Measurements of V_{DS} and calculation of corresponding I_D

5.1.3 Part 3

Measurement of I_D vs V_{SG} : $V_{DD} = 12$ V

R_1 (Ω)	V_G (V)	$V_{SG} = V_{DD} - V_G$ (V)	$I_D = \frac{V_G}{R_1}$ (mA)
27	0.8	11.2	29.6296
220	3.6	8.4	38.182
330	4.88	7.12	21.576
470	5.4	6.6	14.0425
1000	7.3	4.7	4.7
3300	9.14	2.86	0.867
4700	9.53	2.47	0.525
10000	10.1	1.9	0.19
33000	10.7	1.3	0.039
330000	11.3	0.7	0.0021

Table 3: Measurements of V_{SG} and calculation of corresponding I_D

Measurement of I_D vs V_{SD} : $V_{DD} = 12$ V

R_1 (Ω)	R_2 (Ω)	V_{SD} (V)	I_D (mA)	V_{SG} (V)
470	470	6.82	14.5106383	5.18
1000	470	9.38	9.38	2.62
3300	470	11.2	3.393939394	0.8
4700	470	11.4	2.425531915	0.6
10000	470	11.8	1.18	0.2
470	1000	4.8	10.21276596	7.2
1000	1000	8.4	8.4	3.6
3300	1000	11	3.333333333	1
4700	1000	11.2	2.382978723	0.8
10000	1000	11.8	1.18	0.2
470	3300	1.2	2.553191489	10.8
1000	3300	2.43	2.43	9.57
3300	3300	7.02	2.127272727	4.98
4700	3300	8.84	1.880851064	3.16
10000	3300	11.2	1.12	0.8
470	4700	0.64	1.361702128	11.36
1000	4700	1.35	1.35	10.65
3300	4700	4	1.212121212	8
4700	4700	5.37	1.142553191	6.63
10000	4700	9.32	0.932	2.68
470	10000	0	0	12
1000	10000	0	0	12
3300	10000	0.364	0.11030303	11.636
4700	10000	0.4	0.085106383	11.6
10000	10000	0.8	0.08	11.2

Table 4: Measurements of V_{SD} and calculation of corresponding I_D

5.1.4 Part 4

V_G	V_D
2	4.2
3	3.6
4	3.41
5	3.4
6	1.69
7	1.12
8	0.808
9	0.531
10	0.205
11	0.009
12	0.0083

Table 5: Gate voltage vs Drain voltage for CMOS

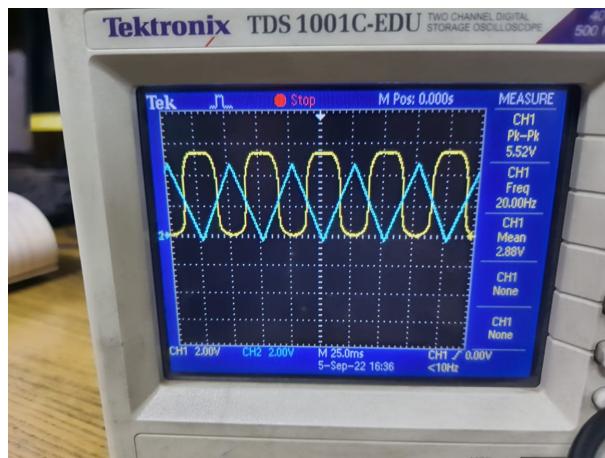


Figure 7: CMOS Input and Output at 20Hz

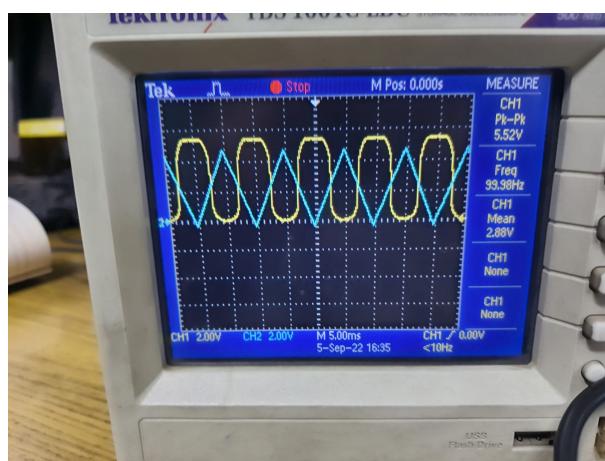


Figure 8: CMOS Input and Output at 100Hz

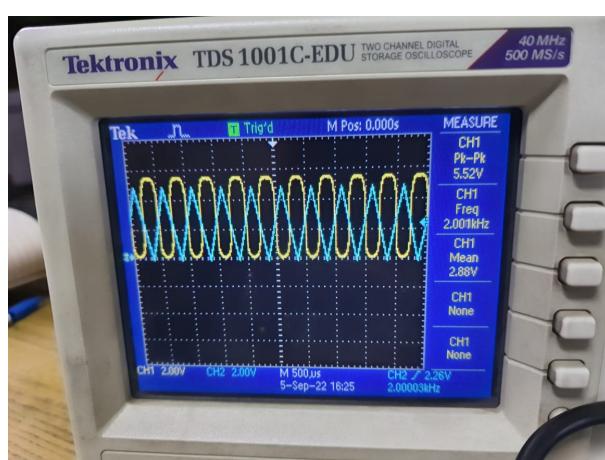


Figure 9: CMOS Input and Output at 2kHz

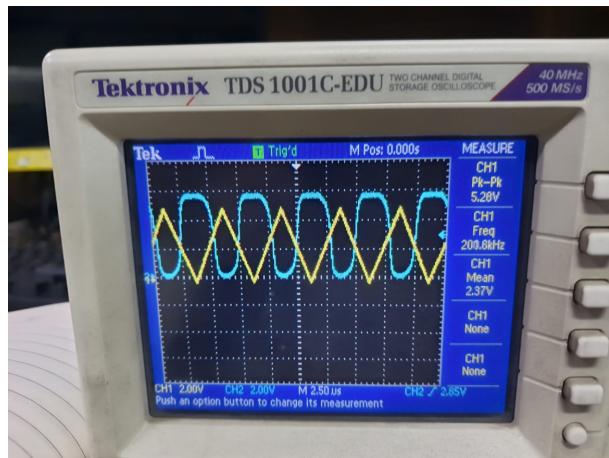


Figure 10: CMOS Input and Output at 200kHz

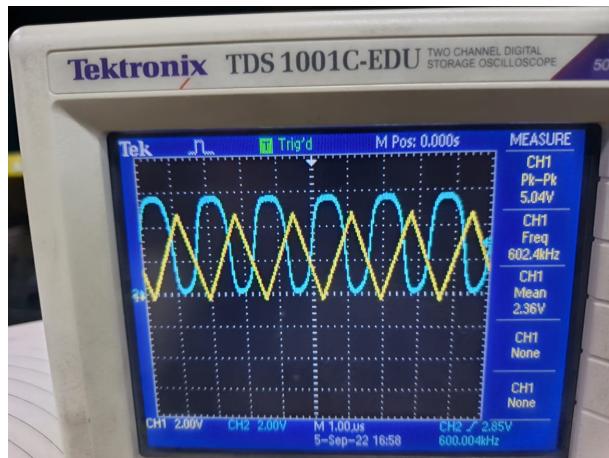


Figure 11: CMOS Input and Output at 600kHz

5.2 Graphs

5.2.1 Part 1:

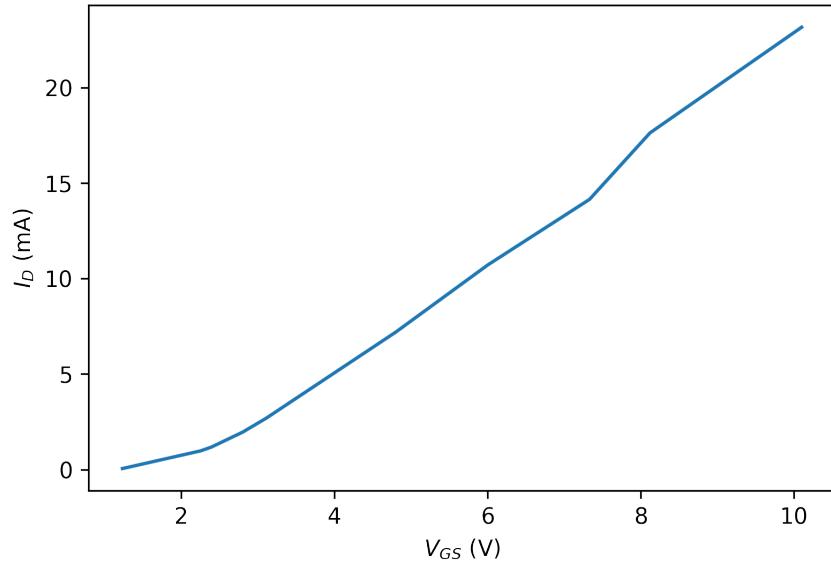


Figure 12: nMOS I_D vs V_{GS} characteristics

5.2.2 Part 2:

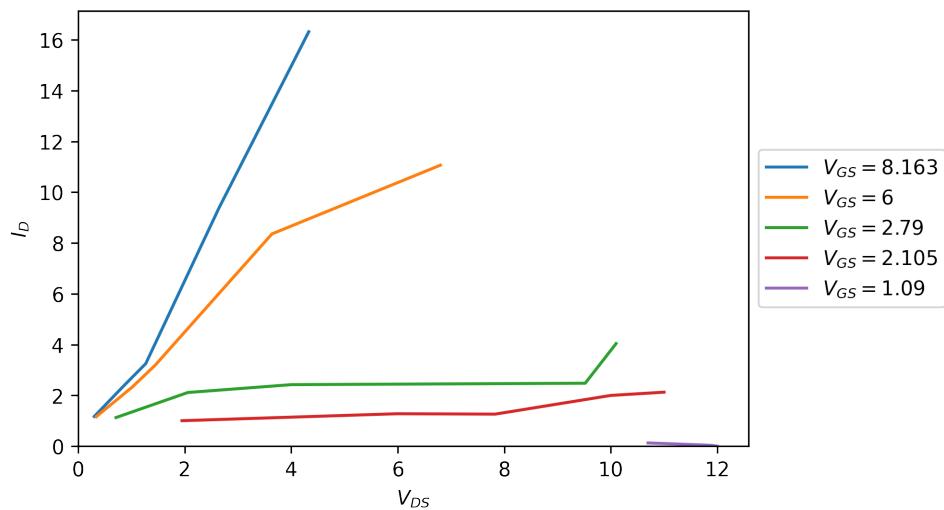


Figure 13: nMOS I_D vs V_{DS} characteristics

5.2.3 Part 3:

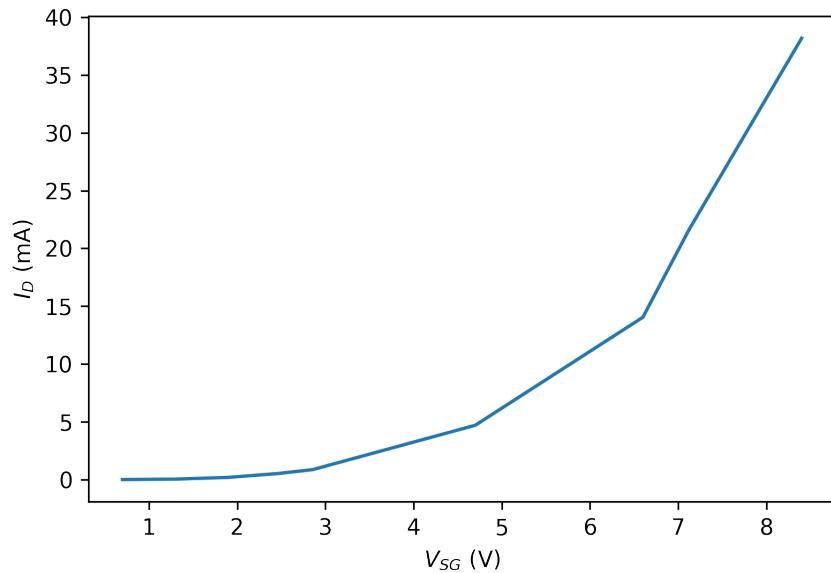


Figure 14: pMOS I_D vs V_{SG} characteristics

Part a:

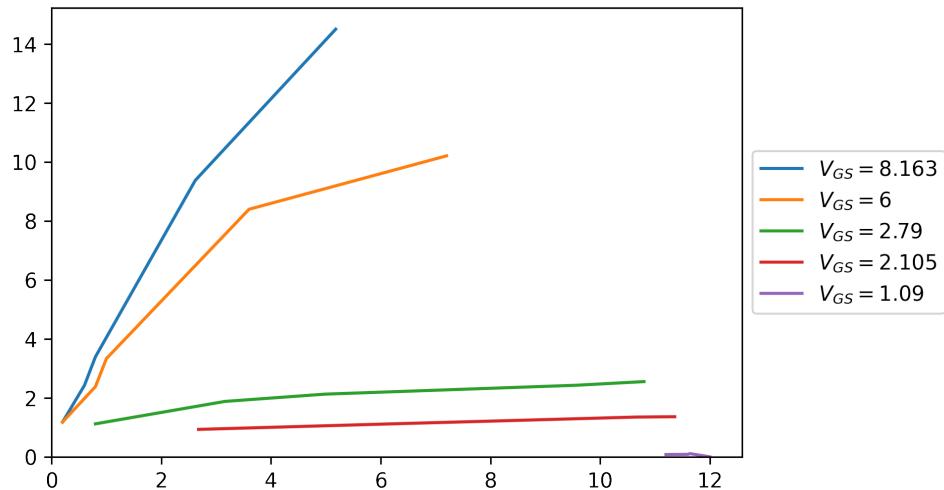


Figure 15: pMOS I_D vs V_{SD} characteristics

Part b:

5.2.4 Part 4:

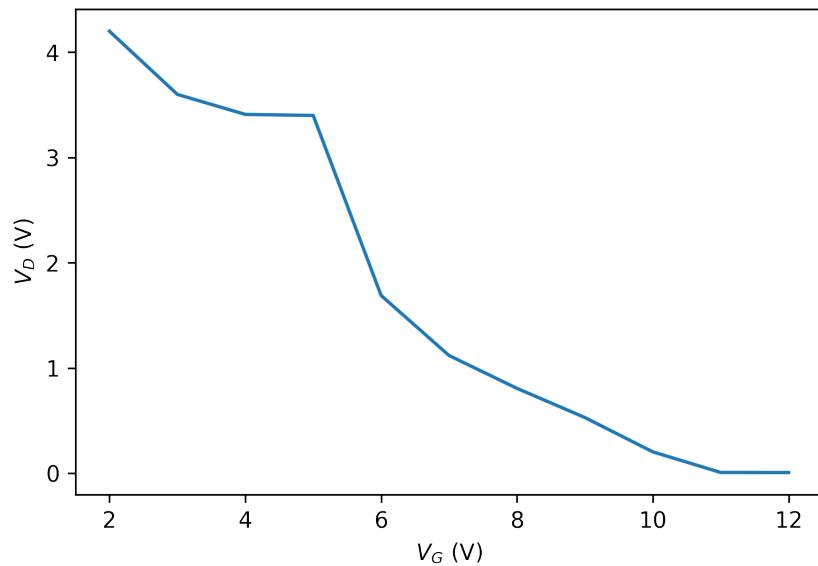


Figure 16: cMOS V_G vs V_D characteristics

5.3 Circuit Snapshots

5.3.1 Part 1:

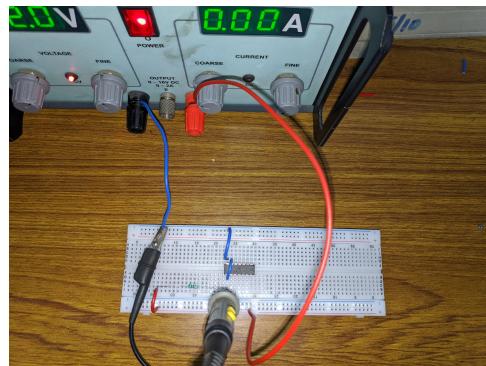


Figure 17: Connections snapshot for Part 1

5.3.2 Part 2:

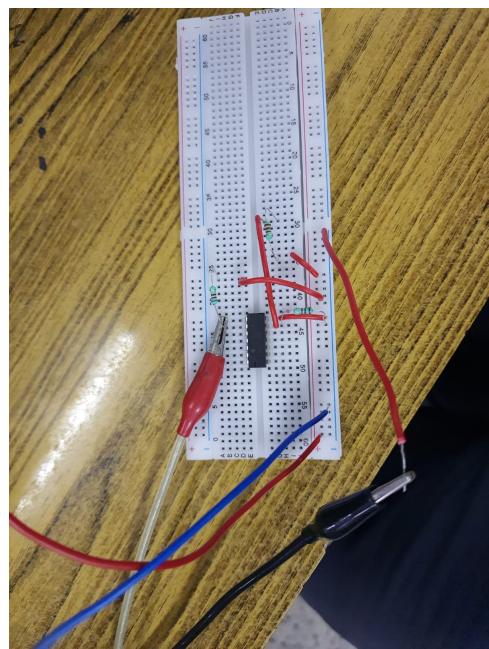


Figure 18: Connections snapshot for Part 2

5.3.3 Part 3:

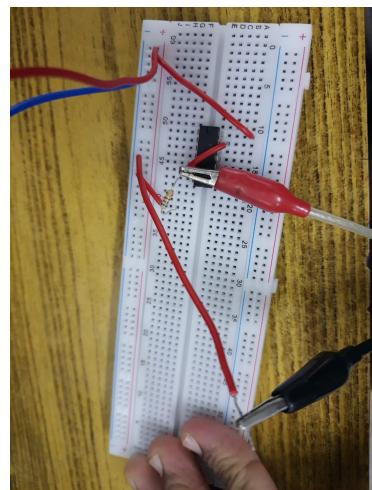


Figure 19: Connections snapshot for Part 3a

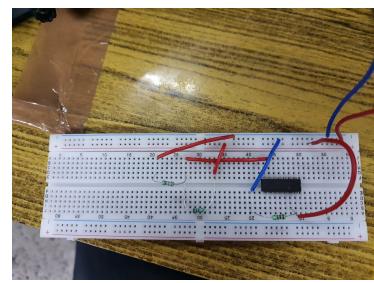


Figure 20: Connections snapshot for Part 3b

5.3.4 Part 4:

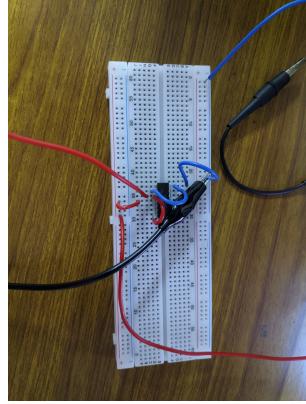


Figure 21: Connections snapshot for Part 4

6 Observation

- From part 1 and part 3a, we observe that, in saturation region, I_D increases with V_{GS}/V_{SG} in both nMOS and pMOS and the relation is almost quadratic as expected theoretically.
- From part 2 and part 3b, we observe that I_D increases with V_{DS} till it reaches saturation for a fixed value of V_{GS} . This is again true in both nMOS and pMOS.
- In part 4, we see that the CMOS inverter output is opposite (inverted) of input in phase. Also, the output is initially a square wave, which on higher frequencies becomes sinusoidal.

7 Conclusion

- From the graph of $\sqrt{I_D}$ and V_{GS} , we calculated the V_{Th} for the nMOS as: 0.19V

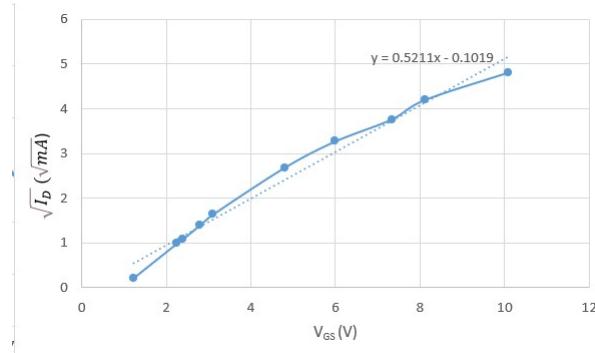


Figure 22: $\sqrt{I_D}$ and V_{GS} for nMOS

- From the graph of $\sqrt{I_D}$ and V_{SG} , we calculated the V_{Th} for the pMOS as: 0.933V

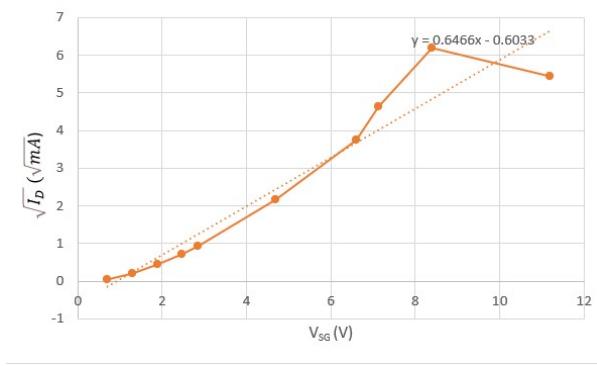


Figure 23: $\sqrt{I_D}$ and V_{SG} for pMOS

- No current flows in the drain for the time that V_{DS} is below threshold voltage implying that the MOSFET is in OFF region.
- The curves obtained for the pMOS, nMOS and CMOS characteristics comply with the theoretical graphs for the same.
- In CMOS inverter at high frequency, time period of the circuit approaches time constant of the RC circuit, hence the output waveform gets skewed at high frequency.