ELL 304: Lab 4 Report
Differential Circuits

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1 Aim

To design a differential MOS circuit to be used as a differential MOS amplifier.

2 Apparatus Required

- CD4007 IC
- Breadboard
- Oscilloscope
- DC Source Generator
- Function Generator
- Resistances

3 Theory

- A differential amplifier is an amplifier topology which senses input from two terminals and produces an amplified output from two terminals. The difference of outputs from the two terminals is the total differential output which is the amplified version of the difference of input of two terminals.

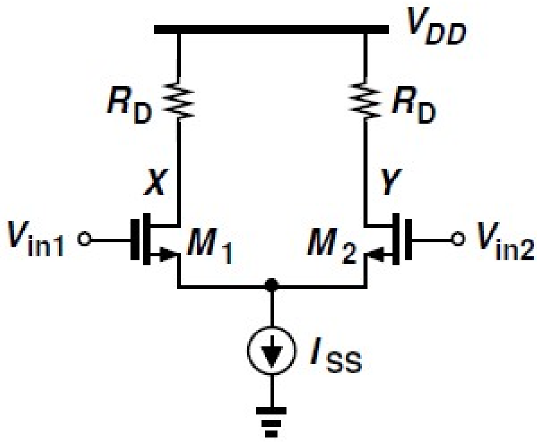

Figure 1: A differential amplifier using nMOS

- The differential gain of the amplifier above on the application of a small signal is given by:

$$A_d = \frac{v_X - v_Y}{V_{in1} - V_{in2}} = -g_m R_D$$

- The common mode gain is a measure of the change in DC output when there is variation in the DC input. We ideally want this to be zero. But since ideal current sources don't exist, we get some tail resistance in parallel with the current source I_{SS}. Due to this, the common mode gain is given by:

$$A_{cm} = \frac{v_X - v_Y}{(V_{in1} + V_{in2})/2}$$

  Also, it is given theoretically by:

$$A_{cm} \approx \frac{R_D}{2R_S}$$

- The common mode rejection ratio is given by:

$$CMRR = \frac{A_d}{A_{cm}}$$

4 Procedure

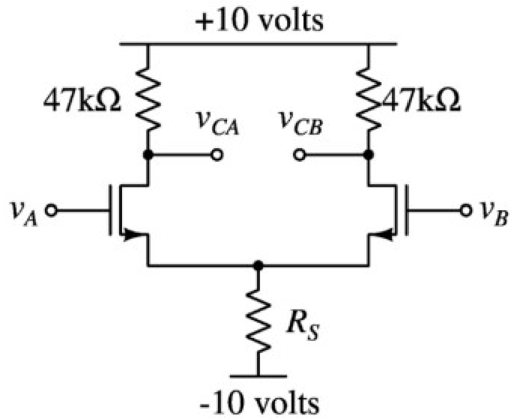

Figure 2: Circuit Diagram

- Circuit was connected as shown in circuit diagram. Body and source of the nMOS were shorted.
- V_A and V_B were initially connected to 0 volts.
- R_S was changed so as to get a current of 0.1mA through the nMOS devices.
- All node voltages were measured to ensure the devices are in saturation.
- All node voltages and currents were reported.
- Now, V_A was increased to 100mV and V_B still at zero. Again the node voltages and currents were reported.
- Now, V_B was increased to 100mV and V_A back to zero. Again the node voltages and currents were reported.
- Differential mode gain and common mode gain were calculated using the formulae:

$$\text{Differential gain, } A_d = \frac{v_{ca} - v_{cb}}{v_a - v_b}$$

$$\text{Common Mode gain, } A_{cm} = \frac{v_{ca} - v_{cb}}{(v_a + v_b)/2}$$

- Now, a small input signal of frequency 1kHz was applied to V_A and 0 to V_B, and differential and common mode gain was measured.

5 Readings

$V_A = V_B = \mathbf{0}$

$R_S = \mathbf{10k}\Omega$

- Voltage across 47kΩ = 14.2V
- Current = (14.2)/47000 = 0.302mA

R_S **= 50kΩ**

- Voltage across 47kΩ = 4.53V
- Current = (14.2)/47000 = 0.096mA

R_S **= 47kΩ**

- Voltage across 47kΩ = 5.15V
- Current = (14.2)/47000 = 0.109mA

Hence, the required value of the R_S is 47kΩ. We will use this resistance in the further experiment.

With this resistance, following are the node voltages:

	Left nMOS	right nMOS
V_D	$(= V_{CA})$ 4.85V	$(= V_{CB})$ 4.66V
V_G	$(= V_A)$ 50mV	$(= V_B)$ 50mV
V_S	-1.3V	-1.3V
I	0.109mA	0.115mA

V_A **100mV, =** V_B **= 0**

	Left nMOS	right nMOS
V_D	$(= V_{CA})$ 5.35V	$(= V_{CB})$ 6.18V
V_G	$(= V_A)$ 100mV	$(= V_B)$ 50mV
V_S	-1.12V	-1.12V
I	0.098mA	0.081mA

Differential gain, $A_d = \frac{5.35-6.18}{0.1-0.05}$ = -16.6

Common mode gain, $A_{cm} = \frac{5.35-6.18}{(0.1+0.05)/2} = 11.067$

Common mode gain (theoretically), $A_{cm} = \frac{R_D}{2R_S} = 0.5$

V_A **= 0,** V_B **= 100mV**

	Left nMOS	right nMOS
V_D	$(= V_{CA})$ 6.38V	$(= V_{CB})$ 5.36V
V_G	$(= V_A)$ 50mV	$(= V_B)$ 105mV
V_S	-1.12V	-1.12V
I	0.077mA	0.098mA

Differential gain, $A_d = \frac{6.38-5.36}{0.05-0.1}$ = -18.54

Common mode gain, $A_{cm} = \frac{5.35-6.18}{(0.1+0.05)/2}$ = -13.16

Common mode gain (theoretically), $A_{cm} = \frac{R_D}{2R_S} = 0.5$

1kHz small signal input to v_A, $v_B = 0$:

Differential Gain
Input, $v_A = 200$mV.
Differential Output = 3.44V

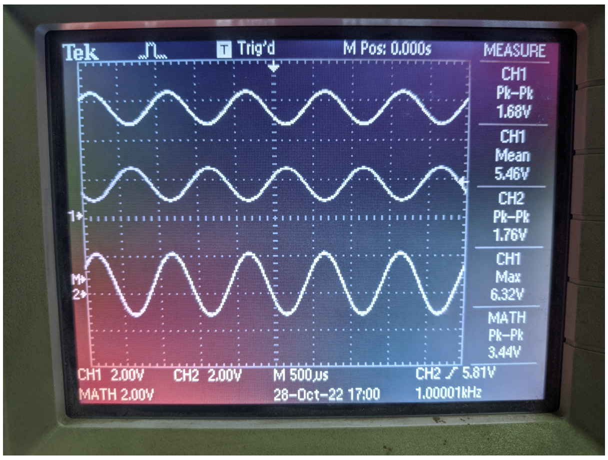

Figure 3: Differential Mode output using MATH mode

Differential Gain, experimentally= 17.2

Common mode gain
Input = 200mV
Common mode Output = 102mV
Hence, common mode gain = 0.51

6 Circuit Snapshot

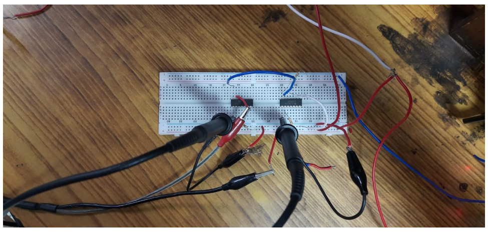

Figure 4: Connections snapshot

7 Observations and Conclusions

- **DC Operating point measurement when $V_A = V_B = 0$:**
  Q: What should the voltages at v_{CA} and v_{CB} been? How different are they from your expectations and why? Ans: When we measured the DC operating point, we observed that V_{CA} and V_{CB} are 4.85V and 4.66V. Theoretically, we expect them to be equal symmetrically when symmetrically equal inputs are applied to both sides. There is a small difference in the values of both sides. This can be

attributed to many things. Firstly, the transistors may not be perfectly matched. Also, the resistors on both sides may not be perfectly equal. There may also be other non-idealities in the circuit (parasitic capacitances, capacitances in the breadboard lines, temperature effects etc.).

- **100mV DC applied to one input, other input grounded**:

  The differential gain obtained from the node voltage calculations is: -16.6 and -18.54 in both cases.

  The common mode gain obtained from the node voltage calculations is: 11.076 and -13.16

- **Small signal input from function generator**: The differential gain measured is 17.2.
- We see that the differential gain measured experimentally is nearly same as calculated from node voltages. Hence, our experimantal observations match the theory.
- The common mode gain measured is 0.51.
- Hence, common mode gain measured is close to the experimental value from theory. But the expression from node voltages seem to be incorrect.
- **CMRR** Hence. the CMRR is = 30.55917 dB
- Hence, in this experiment, we learned the operation and characteristics of a differential amplifier and enhanced our understanding.