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## Solutions for practice problems

1.
  - a. All NMOS devices  $V_{GS}$  is same and 1V, except the device with W/L of 4. Device with W/L of 4 has 0.75 V. All NMOS devices drain current is same and 0.25mA, except tail current source and output NMOS device. Tail current is 0.5mA and output NMOS drain current is 2.8125mA. All PMOS devices has same  $V_{SGP}$  of 1V and drain current is 0.25 mA except output PMOS device, which has 2.8125 mA.
  - b. All NMOS devices  $g_m$  is same and 1mS except W/L=4 device which has 2 mS and tail current source has 2 mS and output NMOS device has 5 mS. All PMOS devices  $g_m$  is same and 1mS, except output PMOS device. Output PMOS device  $g_m$  is 5 mS.

All NMOS devices  $g_{ds}$  is same and 20uS except W/L of 4 size device which has 40 uS and tail current source has 40 uS and output NMOS device has 100 uS. All PMOS devices  $g_m$  is same and 20uS, except output PMOS device. Output PMOS device  $g_m$  is 100uS.

- c. Differential DC gain is 2500. CM gain =  $g_m / (1 + g_m / g_{ds}) * (1/g_m) * g_{mro} = 0.98$  and CMRR is ~ 2500.
  - d.  $p_1 = 2g_{ds} / 50C_c$ ,  $g_{ds}$  is the  $g_{ds}$  of diff pair MOS and  $p_2 = 2g_m / C_L$ , where  $g_m$  is the  $g_m$  of output NMOS.  $z_1 = 2g_m / C_c$  in right half plane.
  - e.  $wp_1 / wp_2 = \tan 30 / 2500$  implies  $wp_2 = wp_1 * 4.33e3$ .
  - f.  $C_c$  of 1.73 pF.
  - g. R of 1kohm is needed in series with  $C_c$ .
  - h.  $U_{GB} = 5.8$  Grad/sec.
2.
  - a. All NMOS devices  $V_{GS}$  is same and 1V, except the device with W/L of 4. Device with W/L of 4 has 0.75 V. All NMOS devices drain current is same and 0.25mA, except tail current source and is 0.5mA. All PMOS devices has same  $V_{SGP}$  of 1V and drain current is 0.25 mA except W/L =2 PMOS devices, which has 0.5 mA.
  - b. All NMOS devices  $g_m$  is same and 1mS except W/L of 4 size device which has 2 mS and tail current source has 2 mS. All PMOS devices  $g_m$  is same and 1mS except W/L=2 PMOS devices has a  $g_m$  of 2mS.

All NMOS devices  $g_{ds}$  is same and 20uS except W/L of 4 size device which has 40 uS and tail current source has 40 uS. All PMOS devices  $g_m$  is same and 20uS except W/L =2 PMOS devices and is 40uS.

- c. Differential DC gain is 625. CM gain is 16.67 and CMRR is 37.5.

- d.  $p_1 = 4g_{ds}^2/gm/(C_c + C_L)$  and other poles and zeros much far.  $C_L$  is much larger than the device capacitances on each node in signal path.
- e. Phase margin of 60 deg is guaranteed with a  $C_L$  of 5 pF.
- f.  $C_c$  of zero.
- g. Right half plane zero is much far away from zero
- h.  $U_{GB} = gm/CL = 1m/5p = 1/5$  G rad/sec.
- 3.
  - a.  $wp_2 = wp_1 * Dc_{gain}/\tan(15deg)$
  - b.  $wp_2 = U_{GB}/\tan(90-PM) = 373Mrad/sec$ ,  $wp_1 = U_{GB}/DC_{gain} = 100M/2500 = 40kHz$ .
  - c.  $wp_2 = gm_2/CL = 373Mrad/sec$ ,  $gm_2 = 1.12mS$ , assuming  $gm_1$  is same as  $gm_2$ . For the Figure 4,  $gm_2$  needed is 0.06 mS.
  - d. W/L of the output stage is 1 for all transistors and use half of the current in the figure 4.
  - e. Possible designs are given below:

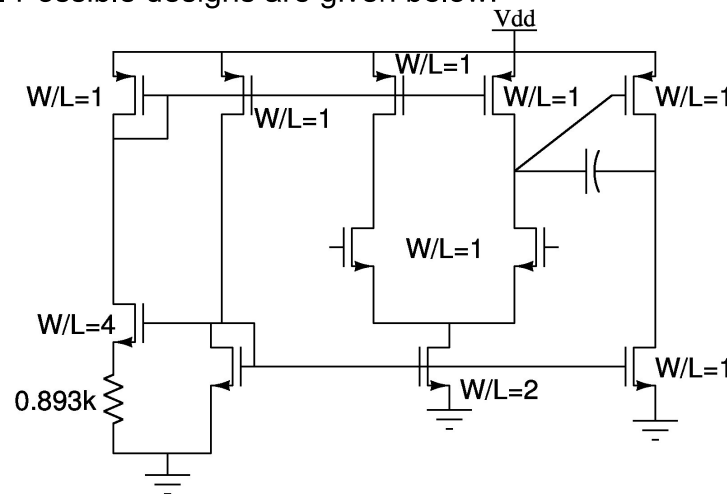


Figure 3

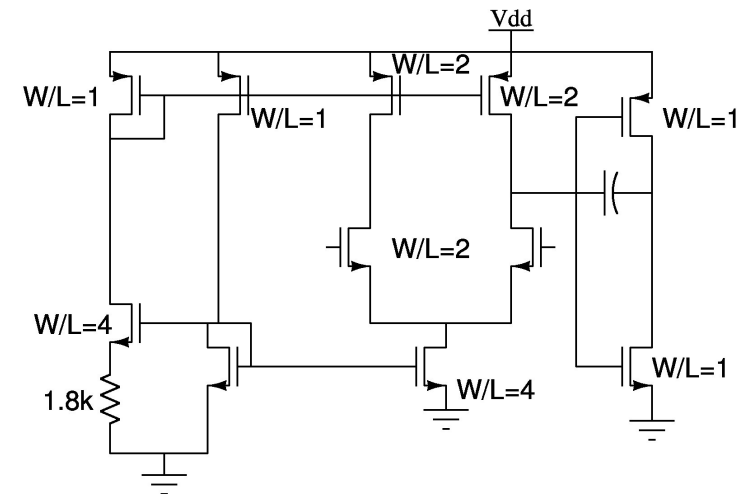
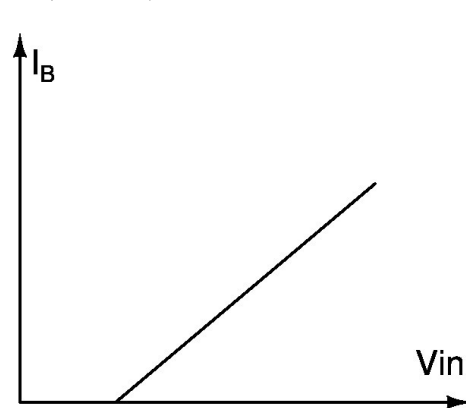


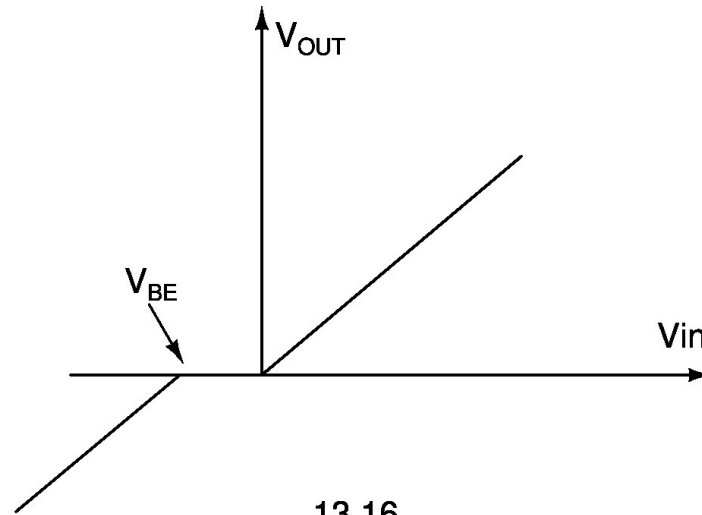
Figure 4

- f.  $4 * 1.12mA = 4.48mA$  (Figure 3) and 3.92 mA (Figure 4)
- g. Approximately doubles.
- 4. 13.1: a. 12.5mA
- b. New gain at peak is 0.9577
- 5. 13.3: 7 mW can be delivered.

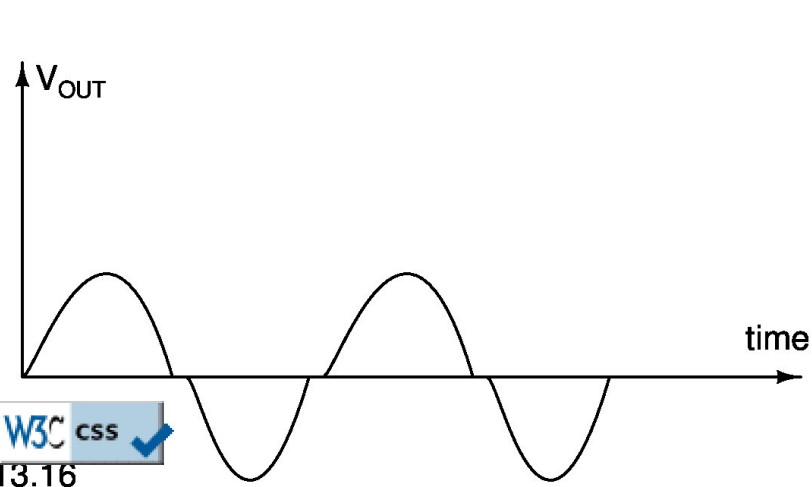
6. 13.8 , 13.16, 13.19 are below.



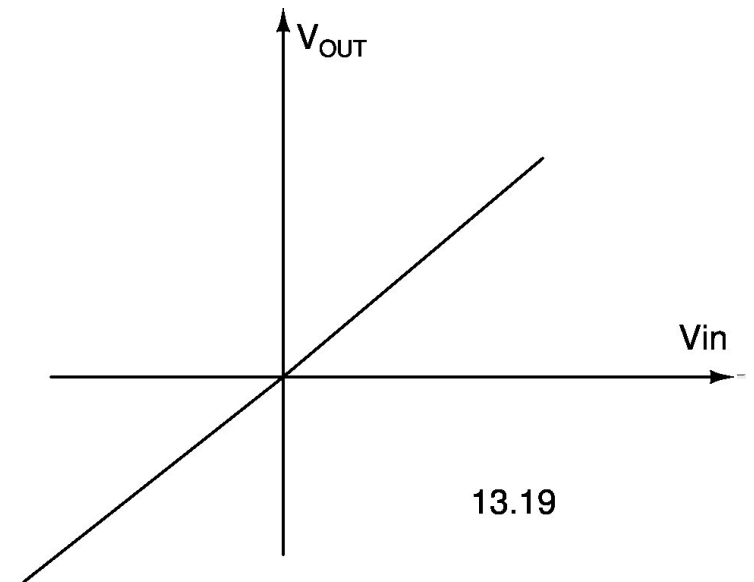
13.8



13.16



13.16



13.19



Last updated on October 19 2016 at 13:35 IST

7. 13.17 -0.329 V of  $V_B$  is needed.