

ELL 304: Lab 3 Report

Current Mirrors

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1 Aim

To design a circuit to use a MOS device as a current source and design a current mirror using the same. And, to design different amplifier topologies using the current mirrors for biasing.

2 Apparatus Required

- CD4007 IC
- Breadboard
- Oscilloscope
- DC Source Generator
- Function Generator
- Resistances
- Capacitors

3 Theory

- A MOSFET is in saturation region when, it is biased such that $V_{DS} > V_{GS} - V_{Th}$ (for an nMOS) or $V_{SD} > V_{SG} - |V_{Th}|$ (for a pMOS).
- A gate-drain connected MOSFET is always in saturation when ON, since now $V_D = V_G$. Therefore, $V_{DS} = V_{GS} > V_{GS} - V_{Th}$.
- At a constant operating point, this gate-drain connected MOSFET has a constant V_{GS} . Hence, it can be used to bias another MOSFET. When the gate of another MOSFET is connected to the gate of this gate-drain connected MOSFET, we get a current mirror setup.
- If the biasing is proper such that both the MOSFETs in the current mirror are in saturation, then, since V_{GS} is same for both the MOSFETs, so the current ratio in them will be that of aspect ratio of both the MOSFETs. ($I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2$).

- This current mirror setup can now be used as a current source for current based biasing of an amplifier.

4 Basic Current Mirror

4.1 Procedure

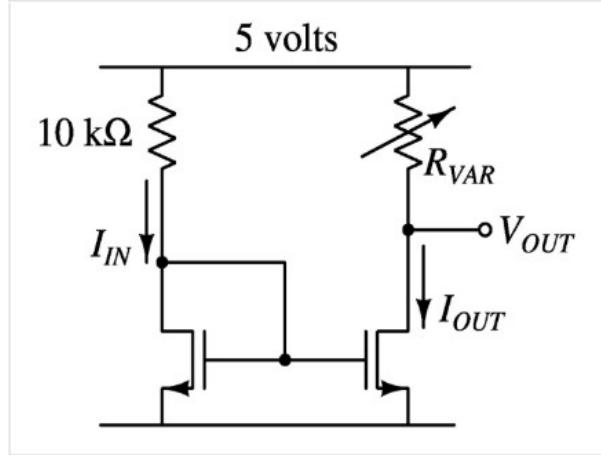


Figure 1: Circuit Diagram for part 1

- Circuit was connected as shown in circuit diagram.
- R_{VAR} was varied from $1\text{k}\Omega$ to $100\text{k}\Omega$ and readings were taken for V_{out} and gate voltage.

Measurement of R_{out} : For measurement of output impedance, the previous measurements with varying R_{VAR} were only used. The readings of I_{out} vs V_{out} were plotted and it was observed that the graph had two regions. Our region of interest is the saturation region. The slope of the saturation region was measured and its reciprocal would give the value of output impedance.

Other schematics with two sources etc. were not used for reasons of change in operating conditions, poorer accuracy, etc.

4.2 Readings

$$V_{DD} = 5 \text{ V}$$

R_{var}	V_{out}	V_{d1}	i_{in}	i_{out}	i_{out}/i_{in}
1000	4.64	1.63	0.337	0.36	1.068249258
2000	4.28	1.63	0.337	0.36	1.068249258
5000	3.24	1.63	0.337	0.352	1.044510386
6800	2.69	1.63	0.337	0.339705882	1.008029324
8200	2.27	1.63	0.337	0.332926829	0.98791344
10000	1.82	1.63	0.337	0.318	0.943620178
12740	1.25	1.63	0.337	0.294348509	0.873437711
16500	0.67	1.63	0.337	0.262424242	0.778706951
20000	0.376	1.63	0.337	0.2312	0.686053412
33000	0.18	1.63	0.337	0.146060606	0.433414261
50000	0.114	1.63	0.337	0.09772	0.289970326
100000	0.061	1.63	0.337	0.05	0.148367953

Table 1: Measurements of V_{out} and V_{D1} and calculation of corresponding I_{out} and I_{in}

4.3 Circuit Snapshot

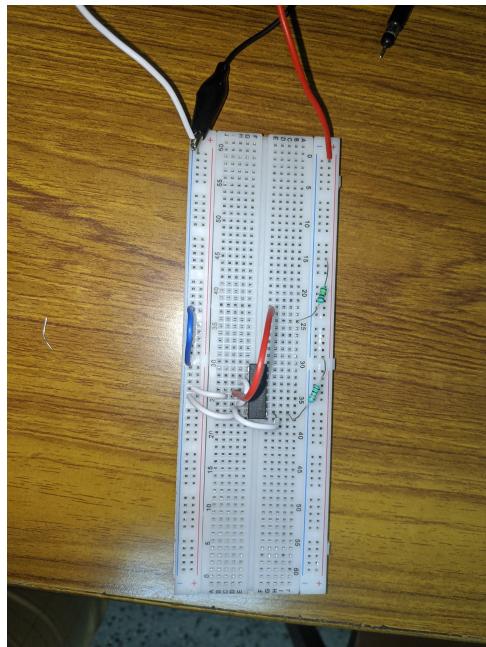


Figure 2: Connections snapshot for Part 1

4.4 Graphs

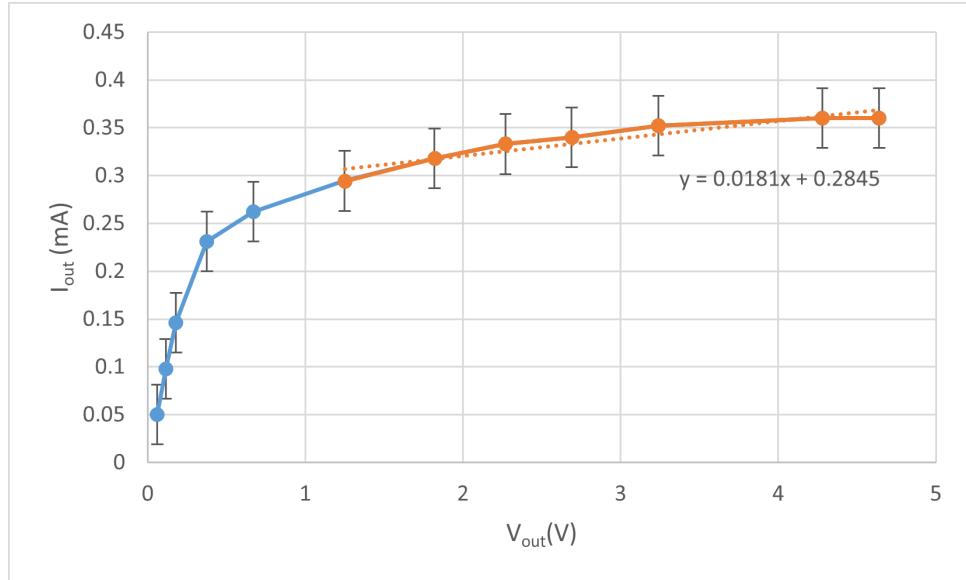


Figure 3: I_{out} vs V_{out}

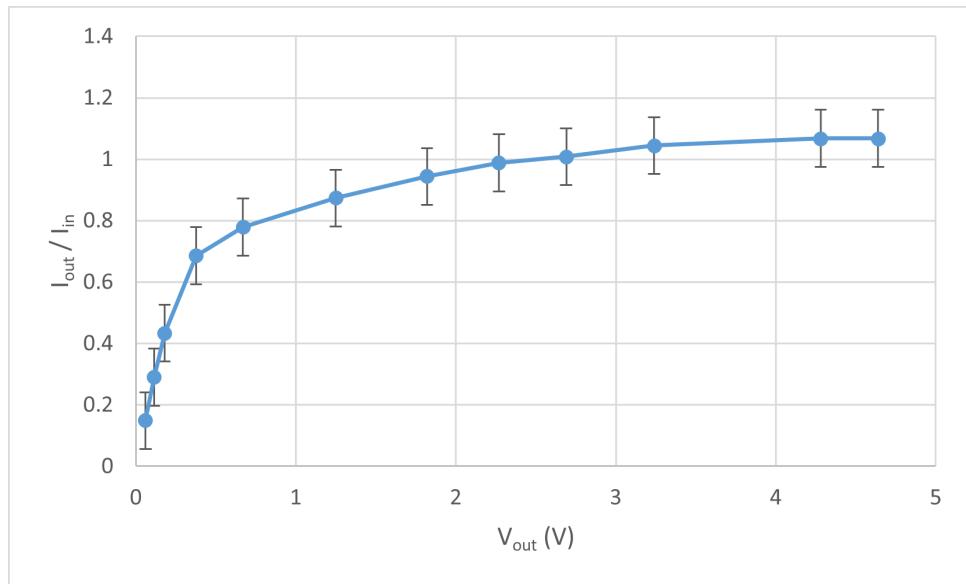


Figure 4: I_{out}/I_{in} vs V_{out}

4.5 Observations

- When both the transistors are in saturation, we see that the graph of output current I_{out} vs output voltage V_{out} is very flat.
- In this saturation region, the ratio of current in both the MOSFETs, I_{out}/I_{in} is nearly constant.
- The slope of best fit line for the saturation region is found to be = 0.0181 mA/V. Hence, the value of **output impedance** is found to be = **55248.62** Ω .

5 Amplifier biased using current mirror

5.1 Schematic 1

5.1.1 Procedure

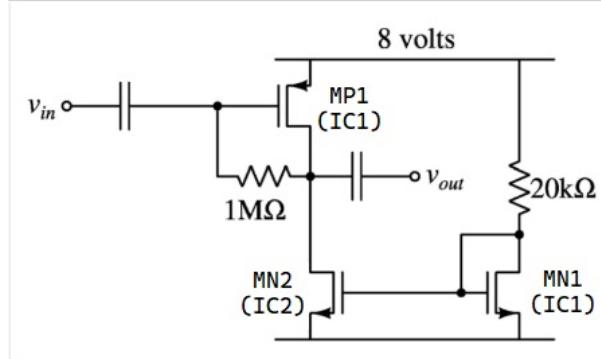


Figure 5: Circuit Diagram for 1st amplifier schematic

- Connections were made as shown in circuit diagram.
- DC operating voltages were measured of all the nodes.
- It was observed that the **amplifier is not in saturation for the above connection**. So the resistance $1M\Omega$ is replaced with $100k\Omega$.
- DC node voltages were again measured and it was verified that all the MOSFETs are in saturation.
- A 100mV pk-pk 100Hz sine wave was injected at v_{in} . And voltage gain was measured from v_{out}/v_{in} .
- Source frequency was increased till 1MHz and the above measurement was repeated each time.

5.1.2 Readings

DC operating point :

- **MP1 (IC2):**
 - $V_S = 8.02V$
 - $V_G = 6.27V$
 - $V_D = 6.33V$
 - Therefore, $V_{SD} = 1.69V$ and $V_{SG} = 1.75V$.
 - Hence, $V_{SD} > V_{SG} - |V_{Th}|$
- **MN1 (IC1):**
 - $V_S = 0.008V$
 - $V_G = 1.6V$

- $V_D = 1.6V$
- Therefore, $V_{DS} \approx 1.6V$ and $V_{GS} \approx 1.6V$.
- Hence, $V_{DS} > V_{GS} - V_{Th}$

- **MN2 (IC2):**

- $V_S = 0.008V$
- $V_G = 1.6V$
- $V_D = 6.33V$
- Therefore, $V_{DS} \approx 6.33V$ and $V_{GS} \approx 1.6V$.
- Hence, $V_{DS} > V_{GS} - V_{Th}$

$$\text{Current in reference branch} = \frac{8-1.6}{20000} = 0.32mA$$

Small signal readings : $v_{in} = 100\text{mV}$ pk-pk sine, $V_{DD} = 8 \text{ V}$

Frequency(Hz)	$V_{in}(\text{V})$	$V_{out}(\text{V})$	Gain	Gain(dB)
100	100	1040	10.4	20.34066679
200	100	1040	10.4	20.34066679
400	100	1000	10	20
600	100	1000	10	20
800	100	1000	10	20
1000	100	1000	10	20
2000	100	1000	10	20
4000	100	1120	11.2	20.98436045
6000	100	1120	11.2	20.98436045
8000	100	1120	11.2	20.98436045
10000	100	1120	11.2	20.98436045
20000	100	1120	11.2	20.98436045
40000	100	1040	10.4	20.34066679
60000	100	1000	10	20
80000	100	960	9.6	19.64542466
100000	100	880	8.8	18.88965344
200000	100	560	5.6	14.96376054
400000	100	366	3.66	11.26962171
600000	100	260	2.6	8.299466959
800000	100	220	2.2	6.848453616
1000000	100	200	2	6.020599913

Table 2: Measurements of v_{out} and calculation of corresponding gain for first schematic

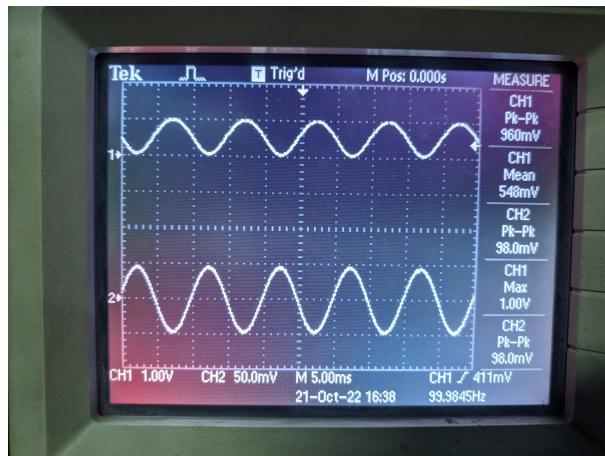


Figure 6: Amplifier Output at 100Hz

5.1.3 Circuit Snapshot

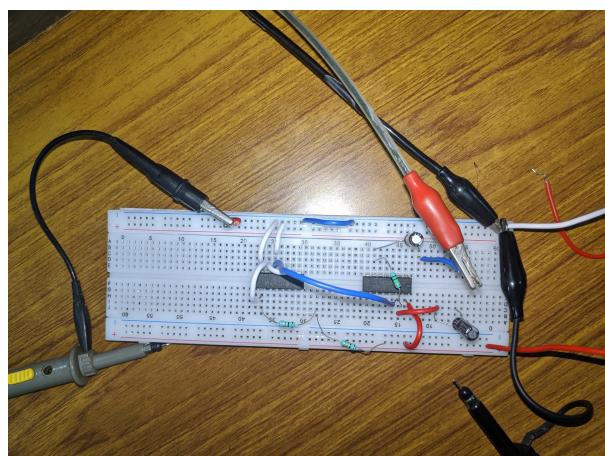


Figure 7: Connections snapshot for Part 2a

5.1.4 Graphs

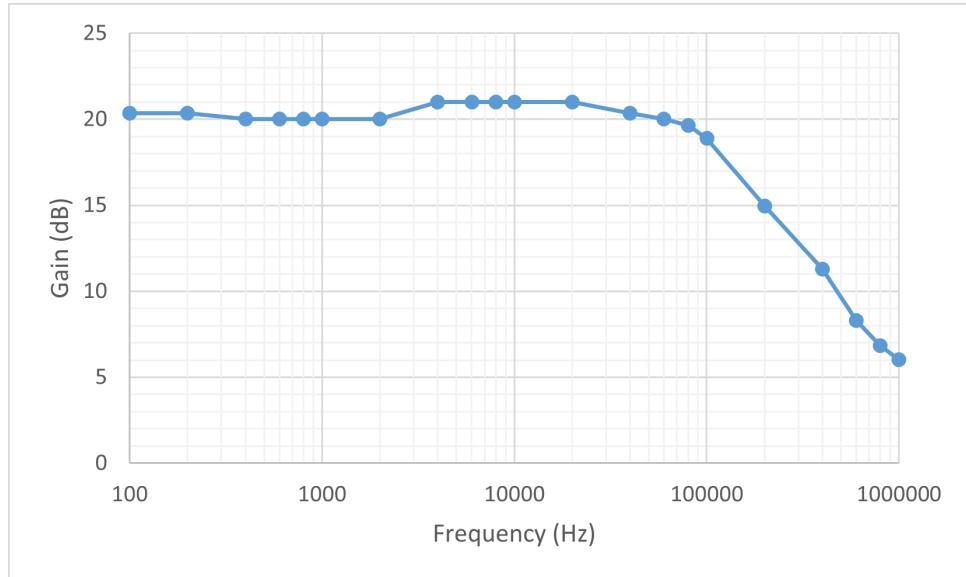


Figure 8: Gain (dB) vs $\log_{10}(\text{frequency})$ (Hz) plot

5.1.5 Observations

- We observe that we get a small signal gain of 10.4.
- Initially, the gain is almost unchanging on changing frequency.
- We also observe that after around 100kHz, on increasing frequency, the gain decreases drastically.

5.2 Schematic 2

5.2.1 Procedure

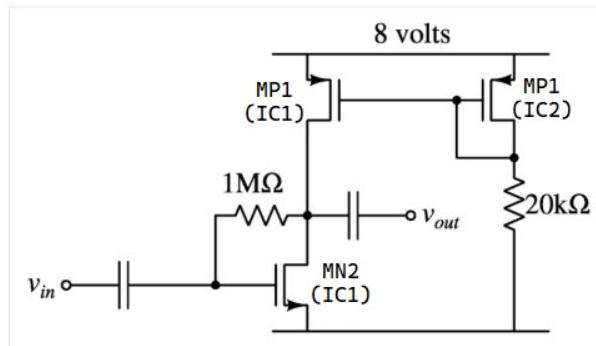


Figure 9: Circuit Diagram for 2nd amplifier schematic

- Connections were made as shown in circuit diagram.
- DC operating voltages were measured of all nodes and it was ensured all the MOS-FETs were in saturation.

- A 100mV pk-pk 100Hz sine wave was injected at v_{in} . And voltage gain was measured from v_{out}/v_{in} .
- Source frequency was increased till 1MHz and the above measurement was repeated each time.

5.2.2 Readings

DC Operating point :

- **MN2 (IC1):**

- $V_S = 0.003V$
- $V_G = 1.71V$
- $V_D = 1.82V$
- Therefore, $V_{DS} \approx 1.82V$ and $V_{GS} \approx 1.71V$.
- Hence, $V_{DS} > V_{GS} - V_{Th}$

- **MP1 (IC1):**

- $V_S = 8.16V$
- $V_G = 6.41V$
- $V_D = 1.8V$
- Therefore, $V_{SD} = 6.26V$ and $V_{SG} = 4.61V$.
- Hence, $V_{SD} > V_{SG} - |V_{Th}|$

- **MP1 (IC2):**

- $V_S = 8.16V$
- $V_G = 6.41V$
- $V_D = 6.41V$
- Therefore, $V_{SD} = 1.75V$ and $V_{SG} = 1.75V$.
- Hence, $V_{SD} > V_{SG} - |V_{Th}|$

$$\text{Current in reference branch} = \frac{6.41}{20000} = 0.3205mA$$

Small signal readings : $v_{in} = 100mV$ pk-pk sine, $V_{DD} = 8 V$

Frequency(Hz)	V_{in} (V)	V_{out} (V)	Gain	Gain(dB)
100	100	1320	13.2	22.41147862
200	100	1320	13.2	22.41147862
400	100	1320	13.2	22.41147862
600	100	1320	13.2	22.41147862
800	100	1320	13.2	22.41147862
1000	100	1320	13.2	22.41147862
2000	100	1320	13.2	22.41147862
4000	100	1320	13.2	22.41147862
6000	100	1320	13.2	22.41147862
8000	100	1320	13.2	22.41147862
10000	100	1320	13.2	22.41147862
20000	100	1300	13	22.27886705
40000	100	1240	12.4	21.8684337
60000	100	1160	11.6	21.28915978
80000	100	1080	10.8	20.66847511
100000	100	980	9.8	19.82452151
200000	100	616	6.16	15.79161424
400000	100	344	3.44	10.73116885
600000	100	228	2.28	7.15869694
800000	100	176	1.76	4.910253356
1000000	100	148	1.48	3.405234308

Table 3: Measurements of v_{out} and calculation of corresponding gain for second schematic

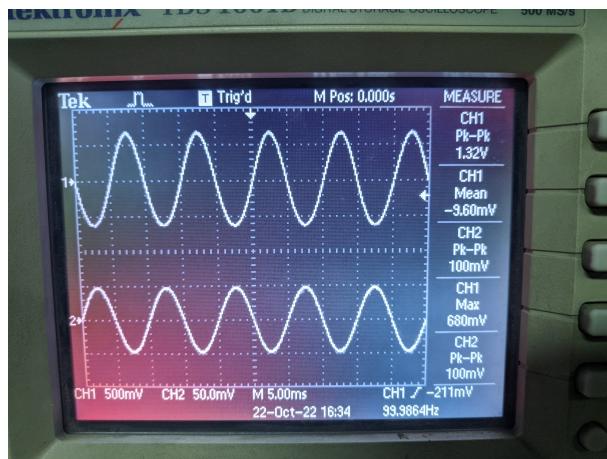


Figure 10: Amplifier Output at 100Hz

5.2.3 Circuit Snapshot

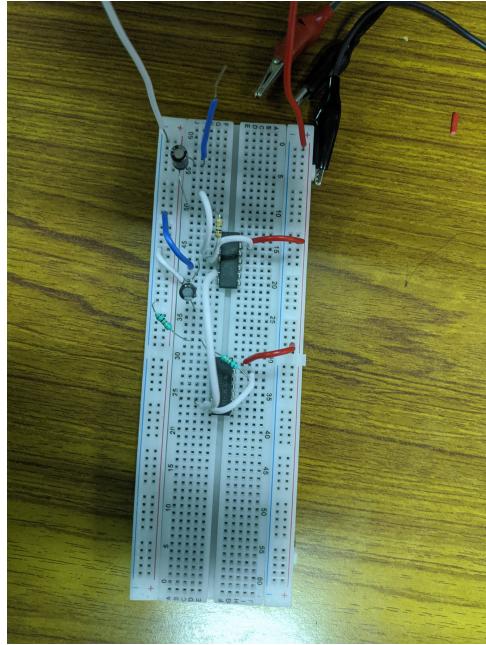


Figure 11: Connections snapshot for Part 2b

5.2.4 Graphs

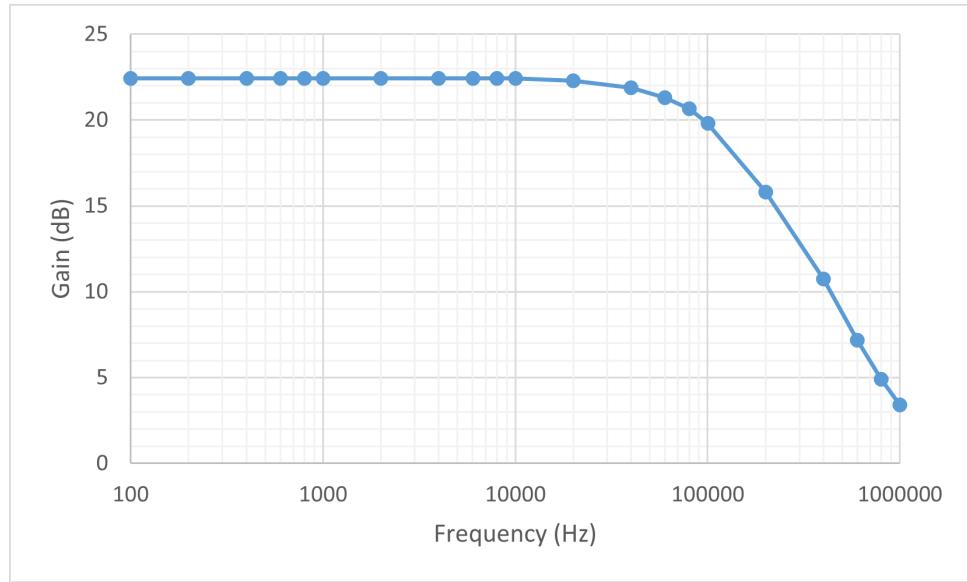


Figure 12: Gain (dB) vs $\log_{10}(\text{frequency})$ (Hz) plot

5.2.5 Observations

- We observe that we get a small signal gain of 13.2.
- Just like previous case, here also the gain drops close to zero at very high frequencies. Here, above 100kHz, there is a significant drop in gain.

Difference between schematic 1 and 2: The main difference between the two parts is that nMOSes and pMOSes have been flipped. That is, now the pMOSes form the current mirror which bias the nMOS amplifier now. Hence now the circuit is flipped.

Comparison of results of schematic 1 and 2: We get a slightly higher gain in the second circuit than the first. The circuits for both are almost identical, save for the different V_{Th} for nMOS and pMOS. This causes a slight difference in the operating point, and consequently, in gain. The threshold voltage for pMOS is smaller, and hence the current mirror in circuit 2 is able to provide a higher current.

5.3 Schematic 3

5.3.1 Procedure

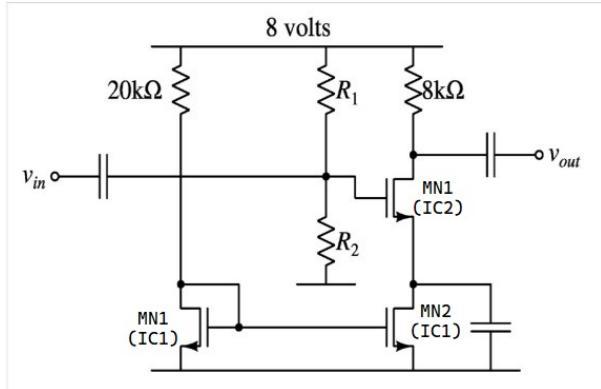


Figure 13: Circuit Diagram for common drain amplifier

- Connections were made as shown in circuit diagram.
- The resistance values used were $R_1=100\text{k}\Omega$ and $R_2=330\text{k}\Omega$.
- DC operating point voltages were measured of all the nodes and it was ensured that all the MOSFETs were in saturation.
- A 100mV pk-pk 100Hz sine wave was injected at v_{in} . And voltage gain was measured from v_{out}/v_{in} .
- Source frequency was increased till 1MHz and the above measurement was repeated each time.

5.3.2 Readings

DC operating point :

- MN1 (IC2):
 - $V_S = 4.57\text{V}$
 - $V_G = 5.8\text{V}$

- $V_D = 5V$
- Therefore, $V_{DS} = 0.43V$ and $V_{GS} = 1.23V$.
- Hence, $V_{DS} > V_{GS} - V_{Th}$

- **MN1 (IC1):**

- $V_S = 0.198V$
- $V_G = 1.79V$
- $V_D = 1.79V$
- Therefore, $V_{DS} = 1.59V$ and $V_{GS} = 1.59V$.
- Hence, $V_{DS} > V_{GS} - V_{Th}$

- **MN2 (IC1):**

- $V_S = 0.198V$
- $V_G = 1.79V$
- $V_D = 4.57V$
- Therefore, $V_{DS} = 4.37V$ and $V_{GS} = 1.59V$.
- Hence, $V_{DS} > V_{GS} - V_{Th}$

$$\text{Current in reference branch} = \frac{8-1.79}{20000} = 0.3105mA$$

Small signal readings : $v_{in} = 100\text{mV}$ pk-pk sine, $V_{DD} = 8 \text{ V}$

Frequency(Hz)	$V_{in}(\text{V})$	$V_{out}(\text{V})$	Gain	Gain(dB)
100	100	624	6.24	15.90369179
200	100	624	6.24	15.90369179
400	100	624	6.24	15.90369179
600	100	624	6.24	15.90369179
800	100	624	6.24	15.90369179
1000	100	624	6.24	15.90369179
2000	100	624	6.24	15.90369179
4000	100	648	6.48	16.23150012
6000	100	648	6.48	16.23150012
8000	100	648	6.48	16.23150012
10000	100	648	6.48	16.23150012
20000	100	648	6.48	16.23150012
40000	100	632	6.32	16.01434157
60000	100	624	6.24	15.90369179
80000	100	616	6.16	15.79161424
100000	100	600	6	15.56302501
200000	100	496	4.96	13.90963353
400000	100	328	3.28	10.31747687
600000	100	240	2.4	7.604224834
800000	100	180	1.8	5.105450102
1000000	100	140	1.4	2.922560714

Table 4: Measurements of v_{out} and calculation of corresponding gain for third schematic

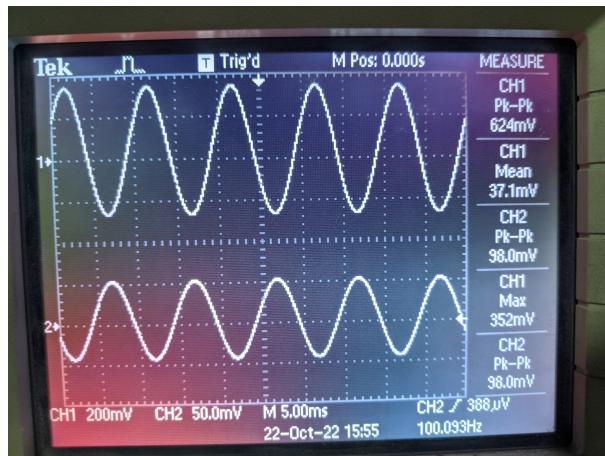


Figure 14: Amplifier Output at 100Hz

5.3.3 Circuit Snapshot

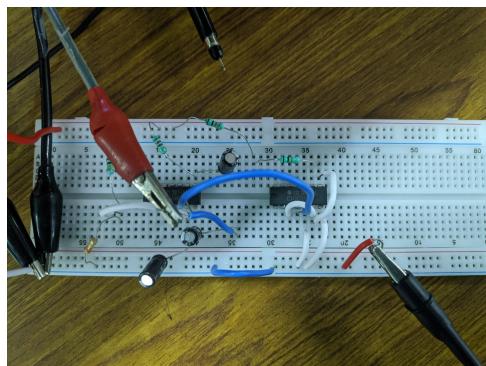


Figure 15: Connections snapshot for Part 2c

5.3.4 Graphs

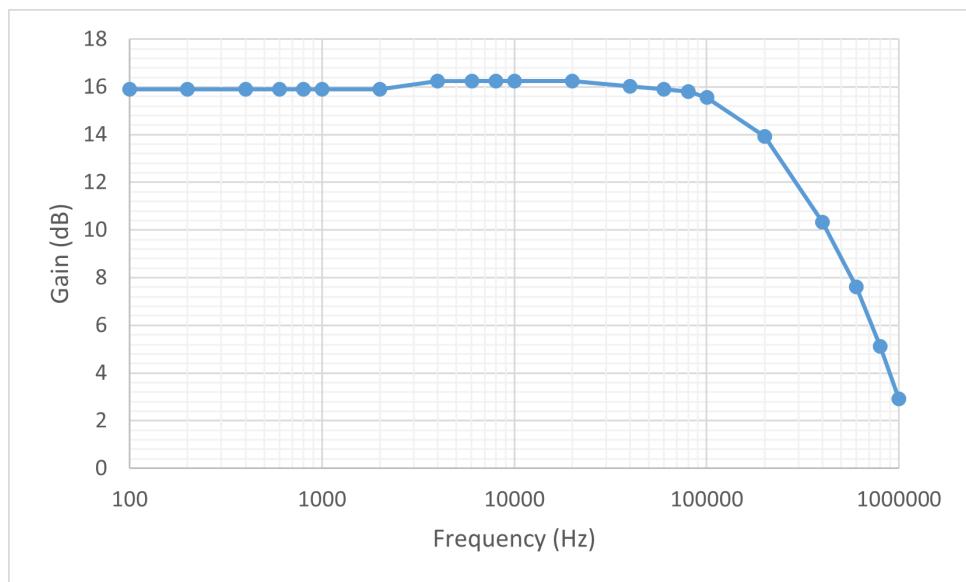


Figure 16: Gain (dB) vs $\log_{10}(\text{frequency})$ (Hz) plot

5.3.5 Observations

- We get a small signal gain of 6.24.
- Again, the gain drops significantly at higher frequencies after 100kHz.

Difference from previous two schematics: There are two major differences between this schematic and the previous two. Firstly, here we are using all nMOS transistors in the circuit. Secondly, and majorly, the DC biasing of gate of amplifier is very different in this schematic. In the previous two, the amplifier transistor's gate was DC shorted with the drain using a very large resistor. So they were gate-drain connected for large signal. But now, in this schematic, we are providing DC bias to the gate of the amplifier transistor using a resistive divider. Hence, we can choose the value of gate voltage as per our will. As per previous two, the amplifier is as a whole current biased using the current mirror. So, here the source and the drain voltage are adjusted automatically as per the current.

Comparison of performance from previous two schematics: The gain now is significantly reduced than previous two schematics. We see that the drain voltage is now 8200 k Ω . Which causes the overall output impedance to decrease. Theoretically, the overall output impedance is now the output impedance of current mirror in parallel with 8.2k Ω . Hence, we see a decrease in overall gain.

6 Conclusion

- **Basic Current Mirror:** With proper biasing and ensuring saturation, we achieved almost accurate current mirroring with i_{out}/i_{in} close to 1.
- **Amplifier biased using current mirror:**
 - The gain in schematic 1 is 10.4
 - The gain in schematic 2 is 13.2
 - The gain in schematic 3 is 6.24

The gain obtained in order with expected gain from theory within practical bounds. We also see that gain decreases by about 3dB somewhere between 100kHz and 200kHz.

We also see that the amplification is inverted as expected from a common source amplifier.

- We observed that the gain in all the three configurations is nearly constant in lower frequencies and then suddenly drops considerably when frequency is increased. We can see this in the graphs plotted which resemble a low pass filter. This can be explained by the parasitics. At higher frequencies, the parasitic capacitances start to show their effect. The impedances of parasitic capacitance of the MOSFET become comparable to the biasing impedances in the circuit. Hence, all the current now does not flow through the load resistors and hence the output voltage also decreases.

- In schematic 2, the **gain obtained is slightly higher** than the first schematic. We also saw that the currents in the reference branch is almost same in both the circuits. Hence, the only difference is the different V_{Th} for nMOS and pMOS. We also know that a pMOS is a better current source than nMOS and nMOS is a better current sink than pMOS. This difference is enabling second schematic to provide a higher gain since here nMOS is a sink and pMOS is source.
- The **gain in third schematic is significantly reduced** than previous two schematics. The output impedance in this case, as noted previously, has decreased significantly. Hence, we see a decrease in overall gain.