2 Stage Operational Amplifier Simulation
Assignment 3
ELL304

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2021EE10638

November 15, 2023

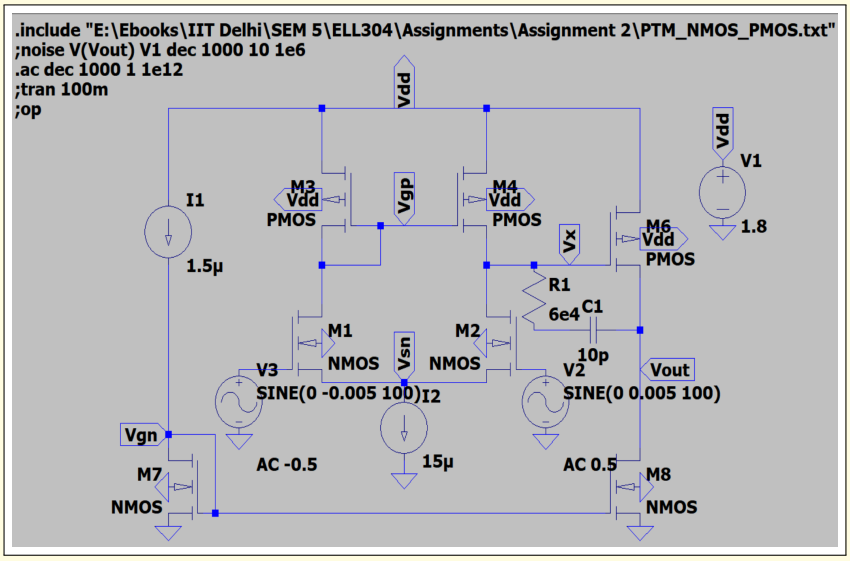
Contents

1 Requirements

Design and simulate a 2-stage opamp using LT-Spice software in 180 nm technology. Highlight the frequency compensation technique used. The specifications are the following -

1. DC gain $\geq$ 55 dB
2. Unity gain frequency, UGF $\geq$ 100 MHz
3. Phase margin $\geq$ 55 degree
4. Supply voltage, VDD = 1.8 V
5. Power Budget $\leq$ 300 µW
6. The output swing should be as high as possible

2 Schematics and Aspect Ratio

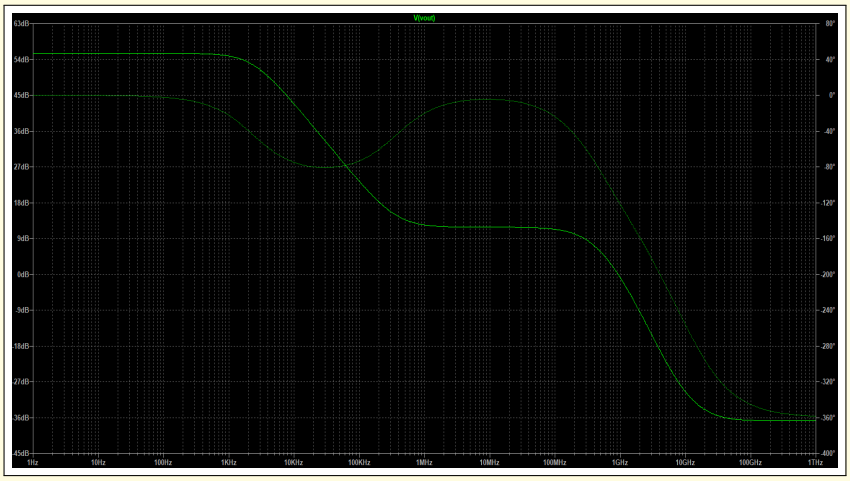


Circuit Schematics of the OpAmp
M1: Length=0.5u Width=2u; W/L= 4
M2: Length=0.5u Width=2u; W/L= 4
M3: Length=0.5u Width=2u; W/L= 4
M4: Length=0.5u Width=2u; W/L= 4
M5: Length=0.5u Width=5u; W/L= 10
M6: Length=0.5u Width=2u; W/L= 4
M7: Length=0.5u Width=1u; W/L= 2

3 Operating Points

Name:	m1	m2	m7	m5	m3	m4	m6
Model:	nmos	nmos	nmos	nmos	pmos	pmos	pmos
Id (μA):	7.14	7.14	1.5	7.81	7.14	7.14	7.81
Vgs:	0.45	0.45	0.52	0.52	0	0	0.379
Vds:	1.53	1.53	0.52	0.702	0.719	0.719	1.1
Vbs:	0.45	0.45	0	0	0.719	0.719	1.1
Vth:	0.385	0.385	0.495	0.495	-0.473	-0.473	-0.473
Vdsat:	0.0965	0.0965	0.0792	0.0792	-0.182	-0.182	-0.182
Gm (mS):	0.102	0.102	0.0261	0.135	0.0567	0.0567	0.0615
Gds (μS):	1.25	1.25	0.339	1.69	1.76	1.76	1.75
Gmb (μS):	20.5	20.5	8.12	42.1	15.3	15.3	16.6

4 AC Magnitude and Phase Response

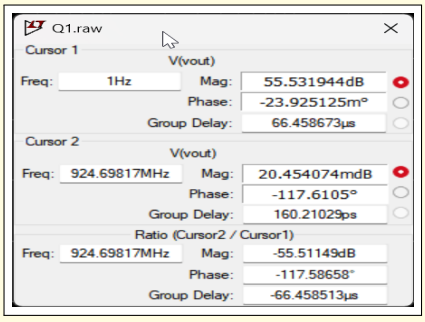


AC Response of the circuit

DC Gain= 55.53dB $\approx 55dB$.

UGF=925MHz which is more than the required 100MHz.

Phase Margin $\approx 62degrees$, which is excellent.

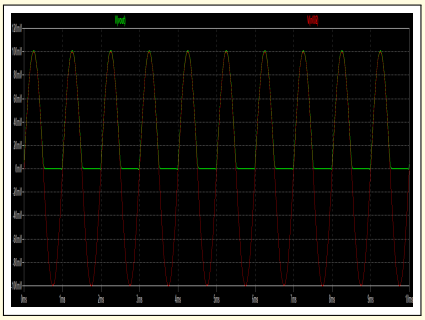


UGB, Phase Margin and DC Gain

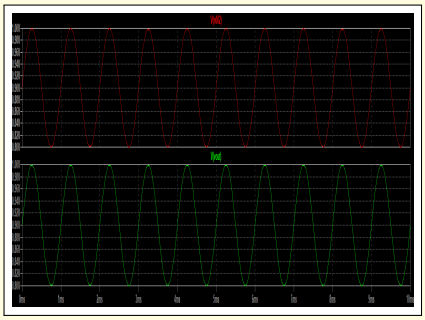
5 ICMR and OCMR

- ICMR = $V_{CM-MAX} - V_{CM-MIN}$
- $V_{CM-MAX} = V_{DD} - V_{SG-3} + V_t$ = 1.08+0.385=1.42V
- $V_{CM-MIN} = V_{GS-1}$ = 0.45V
- ICMR= 1.42-0.45= 0.97V
- OCMR= $V_{OCM-MAX} - V_{OCM-MIN}$
- $V_{CM-MAX} = V_{DD} - V_{SG-6} + V_t$ = 1.08+0.473=1.55V
- $V_{CM-MIN} = V_{GS-5} - V_t$ = 0.025V
- OCMR= 1.55-0.025=1.53V

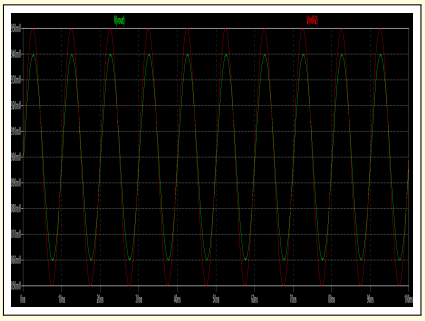
6 Unity Gain Operation



Clipping of output due to 0 DC Offset



DC Offset:0.9V; Freq=1kHz



DC Offset:0.9V; Freq=100MHz

DC Offset:0.9V; Freq=1GHz

- We notice that the output is clipped since the DC Offset is 0. We set DC Offset to 0.9V.

- We observe the transient output at 1kHz frequency. The gain is unity and both input and output signals overlap.
- At 100Mhz, we see our gain has dropped from unity. This is because of presence of poles in the system.
- When we applied a frequency more than the UGB (925Mhz), we not only observe that the gain drops, but we see some Phase shift as well. Due to presence of poles, our AC phase response starts decreasing as well, thus we see a phase shift at output.

7 Conclusion

- We designed a 2 stage Operational Amplifier as per the required specifications.
- DC Gain of $\approx$ 55dB was achieved.
- UGB of the amplifier was 925Mhz, 9 folds above the required value.
- Phase Margin of the circuit was around 62.
- The Power dissipated in the circuit is around $50\mu W$, which is 6 folds less than the maximum permissible value.
- The output Swing of the device is around 700mV, after which M5 goes into Linear Region.