भारतीय प्रौद्योगिकी संस्थान दिल्ली

INDIAN INSTITUTE OF TECHNOLOGY DELHI

मुख्य परीक्षा उत्तर पुस्तिका

MAJOR TEST ANSWER BOOK

नाम
Name: T PRATHAM

अनुक्रमांक
Entry No.: 2 0 2 0 E E 1 0 5 5 9

पाठ्यक्रम सं.
Course No.: E L L 3 0 4

ग्रुप संख्या
Group No.: 0 1

पाठ्यक्रम शीर्षक
Course Title: Analog Integrated Circuits

दिनांक
Date: 19-11-2022

प्रयोग किए गए अनुवर्ती पृष्ठों की संख्या
No. of continuation sheets used:

प्रश्न सं. Q. No.	प्राप्त अंक Marks
1.	3.5
2.	1
3.	4.5
4.	5
5.	4
6.	
7.	
8.	
9.	
10.	
11.	
12.	
कुल TOTAL	18

पाठ्यक्रम निर्धारक के हस्ताक्षर और दिनांक
Signature of Course Co-ordinator and date

अनुचित साधनों का प्रयोग करने वाले छात्रों को निलम्बित/निष्कासित किया जा सकता है।
Students using unfair means are liable to be punished by Suspension/Expulsion

परीक्षा केन्द्र में सेलफोन, काम्युनिकेटर्स व पीडीए साधनों का प्रयोग करना सख्त मना है।
Use of cell-phones, Communicators & PDAs in the Examination Hall is Strictly prohibited.

Q5.

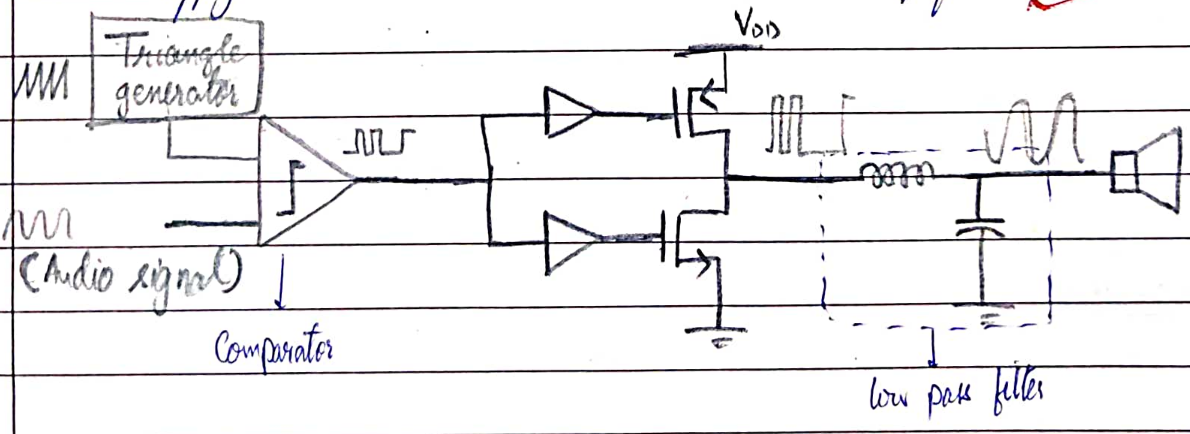
a) Question: Which amplifier is used in most of the audio amplification systems? Design one such basic amplifier. What are its advantages and disadvantages over other type of amplifiers?

3

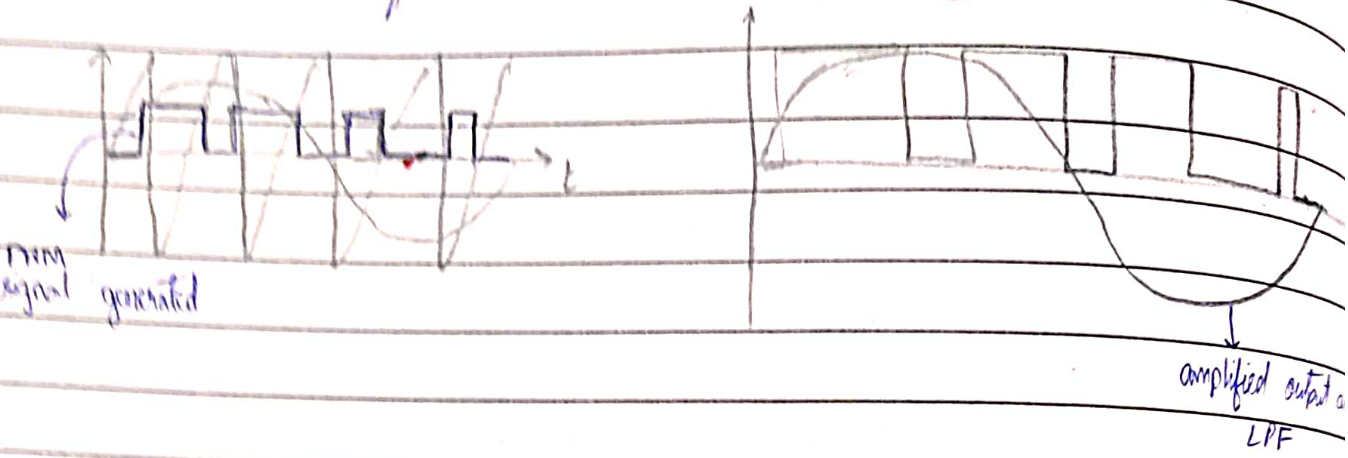
Answer:

A "class-D amplifier" or a "switching amplifier" is used in most of audio amplification systems today. It finds its application ~~from~~ in mobile phone speakers, hearing aids, home theater systems, sub woofers, bass amplifiers, RF amplifiers, etc.

In a class-D amplifier, the amplification device (MOSFET) acts as a switching device instead of a linear gain device as we have seen till now. It is fed a pulse width modulated (PWM) signal and its output rapidly switches between the supply rails. A basic class-D amplifier is shown below:



An audio signal is fed into a comparator along with a high frequency triangular or sawtooth signal to generate a PWM signal, which is then fed into MOSFETs. We can see that ~~a~~ at a particular instant, only one of the nMOS or pMOS is ON depending on the PWM signal. And the output is one of the supply rails. Hence we get an amplified digital signal which is then passed through a low pass filter to remove the high frequency PWM carrier and we get an amplified audio signal which can be fed into a speaker.



The primary advantage of class-D amplifiers over class-A amplifiers (the ones which we have seen in class) is efficiency. Class-A amplifiers dissipate a lot of power and their efficiency is around 20-25% for most amplifiers. Whereas class-D amplifiers are as high as 90% efficient. This is particularly helpful where we want to transfer most of the power to the speaker, esp. in low power devices. ~~More~~ But its primary disadvantage is a higher THD.

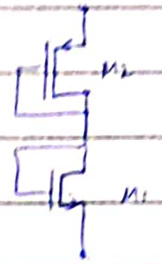
More detailed analysis is beyond my time constraints here.

Justification: We have seen here a very helpful application of class-D amplifiers, and its particular usefulness in low power devices, as well as high power devices. Hence it is very flexible in its range of application.

b) As stated earlier, the amplifier described here is a class-D amplifier. The ideal characteristics of this amplifier is zero current (I_D) when it is OFF ($V_{GS}=0$) and very low V_{DS} (ideally zero) when it is ON, and instantaneous switching between ON and OFF regions ideally. That is it acts as an ideal switch.

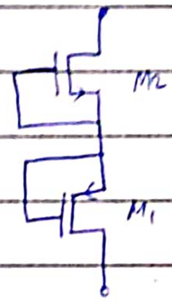
Q1.

a) In figure 1 a), both the MOSFETs are gate-drain connected, hence can be replaced by $1/g_{m_1}$ and $1/g_{m_2}$ respectively.



Hence total resistance $= \frac{1}{g_{m_1}} + \frac{1}{g_{m_2}}$

In figure 1 b) gate and source are shorted, which will only leave their ~~channel~~ drain-source resistances in series as the MOSFETs are OFF.



Hence total resistance $= r_{o1} + r_{o2}$

1.5

So, the resistance in circuit b) is much larger than in a) b/w nodes X and Y.

b) In this circuit, M2 is in ~~saturation~~ linear region ~~since its gate will adjust to allow~~.

1

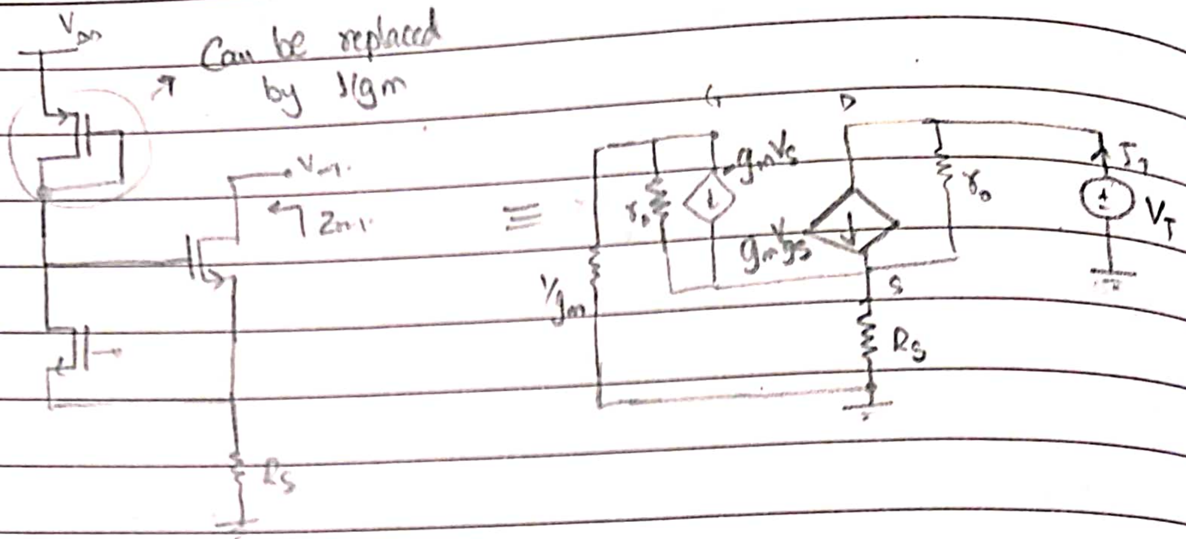
For M_1, gate-drain are shorted : $V_{DS} = V_{GS}$ and $V_{GS} > V_{Th}$

Now V_{GS} of ~~M2~~ M1 is V_{GD} of M2 $\rightarrow$ $V_{GD,2} > V_{Th}$

$\Rightarrow V_{G_2} - V_{D_2} > V_{Th}$

$\Rightarrow V_{GS_2} - V_{Th_2} > V_{DS_2} \rightarrow$ linear region

c) Can be replaced by $1/g_m$



KCL: $I_T = g_m V_{gs} + \frac{(V_T - V_S)}{r_o}$ — ①

$g_m V_g + \frac{(V_g - V_s)}{r_o} - g_m V_s = 0$ — ②

$I_T + \frac{(V_g - V_S)}{r_o} - g_m V_S - \frac{V_S}{R_S} = 0$ — ③

From ②: $V_g \cancel{\left(\frac{1}{r_o} + g_m\right)} = V_s \cancel{\left(g_m + \frac{1}{r_o}\right)}$

$\Rightarrow V_g = V_s$ or $V_{gs} = 0$

③ : $I_T = \left(g_m + \frac{1}{R_S}\right) V_S$

① : $I_T = \frac{V_T}{r_o} - \frac{V_S}{r_o}$ 1

$= \frac{V_T}{r_o} - \frac{I_T R_S}{(1+g_m R_S) r_o}$

$\Rightarrow I_T \left(\frac{(1+g_m R_S) r_o + R_S}{(1+g_m R_S) \cancel{r_o}}\right) = \frac{V_T}{\cancel{r_o}}$

$\Rightarrow \frac{V_T}{I_T} = Z_{out} = \frac{g_m r_o R_S + r_o + R_S}{1 + g_m R_S}$

$\therefore$ Output impedance $= \frac{g_m r_o R_S + r_o + R_S}{1 + g_m R_S}$

Q2.

a) **ICMR:-**

$$V_{cm,max} = V_{DD} - V_{SD2,sat} - V_{SD4,sat} - V_{SG5}$$
$$= V_{DD} - 3V_{ov} - V_{Th}$$

assuming V_{ov} & V_{Th} for all are equal.

$$V_{cm,min} = V_{GS,7} + V_{Th}$$
$$= V_{ov} + 2V_{Th}$$

$$\therefore \text{ICMR} = V_{DD} - 4V_{ov} - 3V_{Th}$$

OCMR:-

$$\cancel{V_{out,max} = V_{DD} - V_{SD7,sat} - V_{SD4,sat} - V_{SG6}}$$
$$\cancel{= V_{DD} - 3V_{ov} - V_{Th}}$$

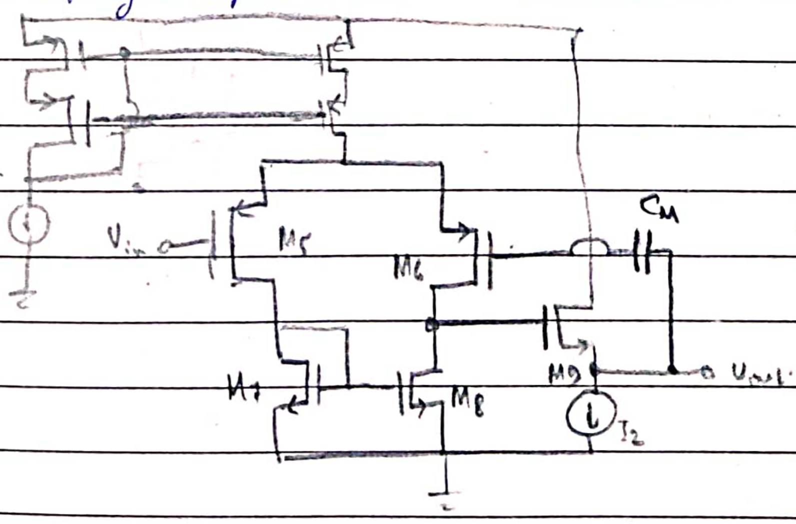
$$V_{out,max} = V_{DD} - V_{DS9,sat}$$
$$= V_{DD} - V_{ov}$$

$$V_{out,min} = V_{DS8,sat} + V_{GS9}$$
$$= 2V_{ov} + V_{Th}$$

1

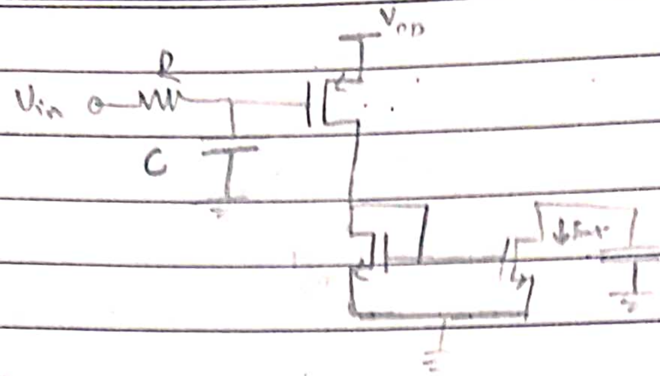
$$\text{OCMR} = V_{DD} - 3V_{ov} - V_{Th}$$

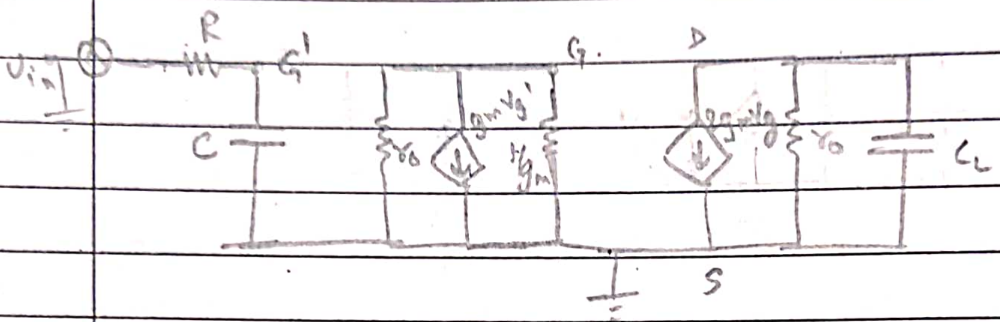
Frequency compensation:-



→ Miller b/w ~~input~~ & output of ~~inverting~~ amp.

b)





Output pole, $\omega_p = \frac{1}{r_o C_L}$

Q3.

a) DC current in $M_7 = I_0 + I_1$ (assuming same aspect ratio of all) +0.5

Small signal current in $M_1 = -g_{m_2} V_{in}$ +0.5

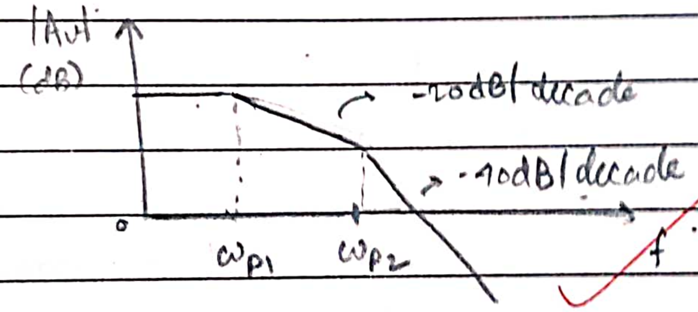
$\therefore I_a = I_0 + I_1 - g_{m_2} V_{in}$

Output current, $I_b = -g_{m_2} V_{in}$ +0.5

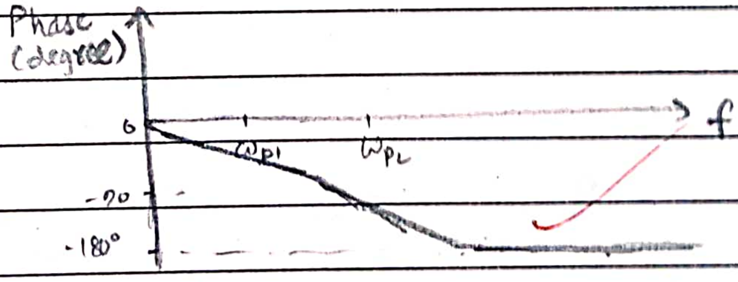
~~Bet~~ Drain of M_5 is a better current sensing node because in this type of current mirror, drain of M_1 is a virtual ground.

Reason not correct

b) a):

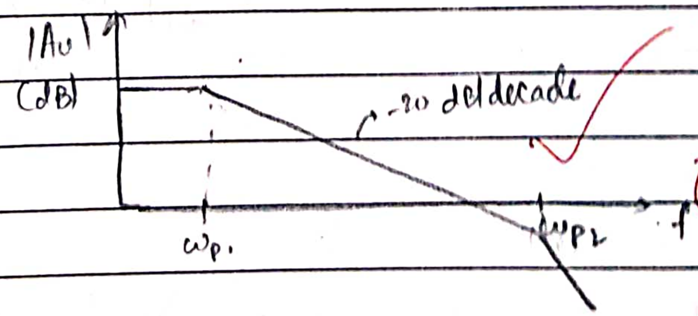


+0.5

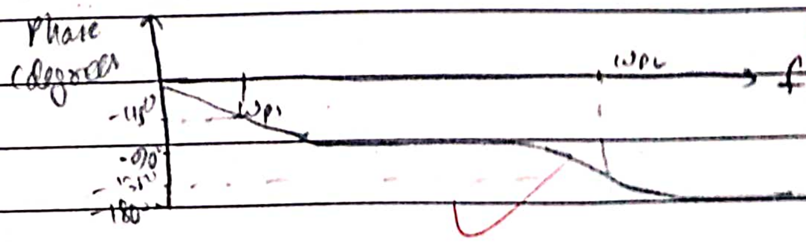


+0.5

b)



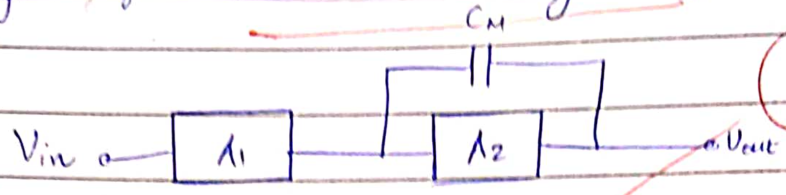
+0.5



+0.5

Configuration (a) might require frequency compensation

Assuming stage A_2 is inverting stage :-

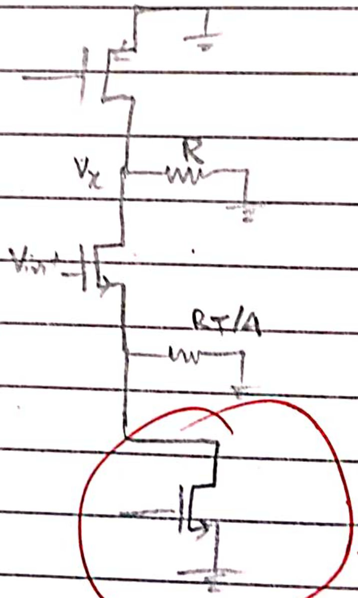


+1

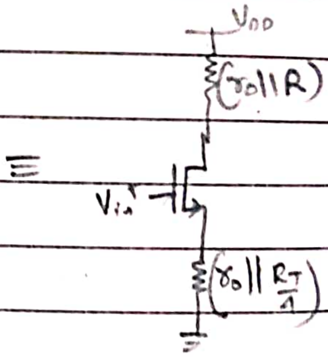
Q4. a)

i) Half diff. ckt. :

Assuming r_o equal for all & resistance of transistor in linear region R_T,



$\equiv$



does not appear in diff

we have a source degenerated circuit.

Hence small signal gain

$$= \frac{g_m R_D}{1 + g_m R_S}$$

$$= \frac{g_m (r_o \| R)}{1 + g_m (r_o \| \frac{R_T}{4})}$$

2

ii) On node X :

$V_{X,max} = V_{DD} - V_{SD,3}$

$= V_{DD} - V_{ov} - V_{Th}$ } from above

$V_{X,min} = V_{DS,sat_1} = V_{ov}$ } from below

$\therefore$ OCMR = $V_{DD} - 2V_{ov} - V_{Th}$ which is quite high indeed (assuming V_{ov} is same for all).

~~Also~~ Symmetrically we can see on Y as well.

1

Hence, I agree that output swing available is quite high.

Reason is wrong

iii) M_7 : Current source & biases M_6

M_8 : load

M_9 : load

M_{10} : Current mirror

M_{11} : Current source and matches load for M_{10}

(X)

Sets $V_{O,CM} = V_{REF}$ using -ve feedback

iv) If output common mode variation is zero, then V_G of M_9 is also zero.

Since in common mode, V_x & V_y have same potential.

Hence current in each R is zero.

Hence, V at between of R is same as V_x which is zero.

2