Quiz

$\frac{2v}{r_o} + g_m v_g \ldots$

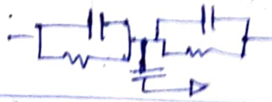
$$\frac{4kT\gamma g_{mn} + 4kT\gamma g_{mp}\,(r_{on}\,\cancel{\| r_{op}})^2}{(g_{mn}^2)\, r_{on} \cancel{\ldots}\,(\cancel{r_{on}\| r_{op}})^2}$$

$I = \frac{\beta}{2}(V_{GS}-V_T)^2$

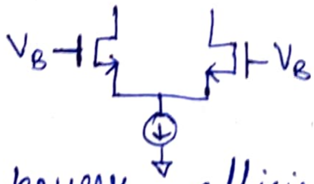
Oly

$$V_n^2 = \frac{4kT\gamma(g_{mn}+g_{mp})\,(r_{on}}{g_{mn}^2}$$

~~Why~~ Why does cap divider not lead to a pole



Q Why do we use ½ DC picture to analyse differential ~~po~~ part here?



- Transistor is more power efficient when closer to cutoff.

Subthreshold → ~~V_{SS}~~ Weak inversion

$V_{GS} < \cancel{V_{\xi}}\, V_T$

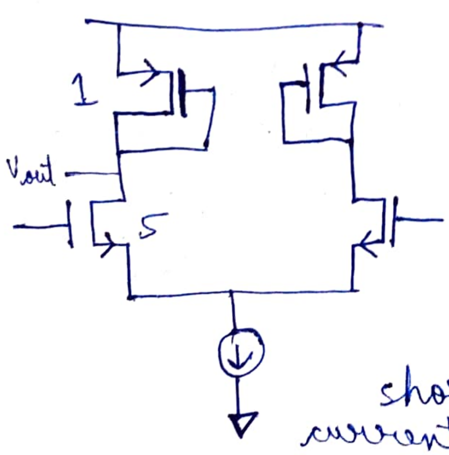
Saturation	weak inversion
Linear	strong inversion

$V_{ds} \geq V_{ds,sat}$

$\downarrow$

$\cancel{\beta}\cdot(V_{GS}-V_T)$

L-21



This ckt has low impedance at output but gain $\xi = 1$ so cant be used as amplifier

$Z_{out} = \frac{1}{g_m}$ & effective transconductance $= -g_m$ so $g = 1$

short ckt the output to ground & check current going into ground to get ~~Ae~~ g_m eff while applying input.

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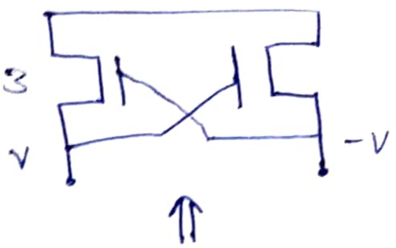
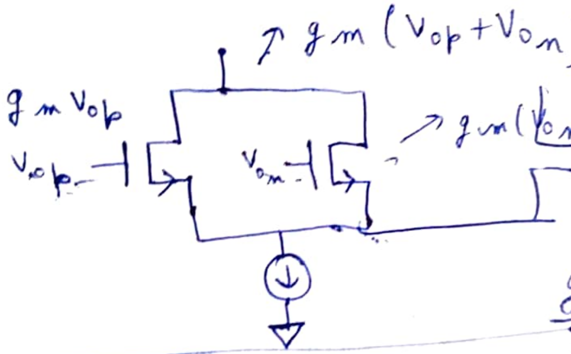


in differential picture $Z_{in} = -\frac{1}{g_m}$ & in CM picture $Z_{in} = \frac{1}{g_m}$

so on attaching this ckt at output of prev ckt we get low CM impedance so ~~b~~ stable output and a ~~high~~ high gain.

gain for combined ckt $= \Delta g_m (r_{o1} \| r_{o3} \| r_{o5})$



· ckt for Common mode sensing V_{ref} using current ~~so~~ source voltage ?

$\frac{g_m}{2}(V_{op} - V_x + V_{om} - V_x)$ —

L-(22)

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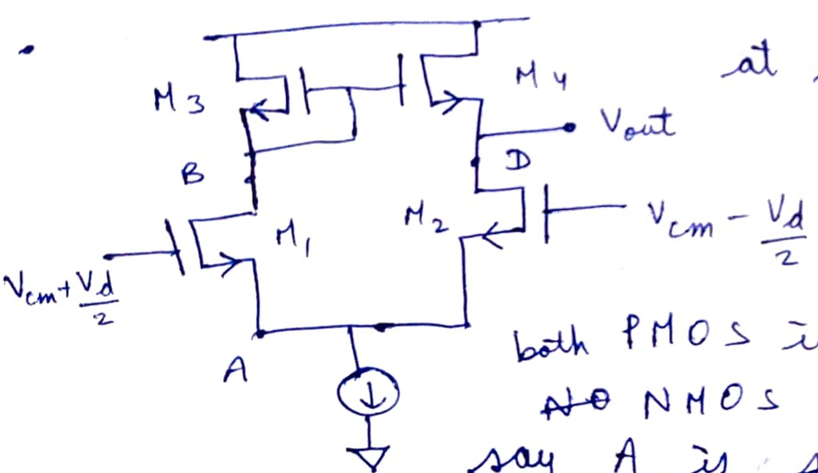


looking down impedance at output is r_{on} as at A & B it is $\frac{1}{g_m}$

If the dimension of both PMOS is similar & of both ~~NO~~ NMOS is same then we can say A is ~~short~~ grounded in ~~increment~~ incremental picture. As if ~~B~~ $V_B > V_D$ then current thru M_1 & M_4 is ↑ & thru M_2 & M_3 is ↓ which is not possible ~~#~~ so $V_B = V_D$ so ckt is again symmetric.

The effective g_m for this case is $\frac{+g_m V_d}{V_d} = g_m$

& ~~effe~~ $Z_{out} = r_{on} \| r_{op}$

~~Th~~ The ~~output~~ impedance at ~~B~~ B is low so ~~swing~~ swing is low so it can be incrementally considered ground.

p_2 $\qquad$ p_1 $\qquad$ z_1

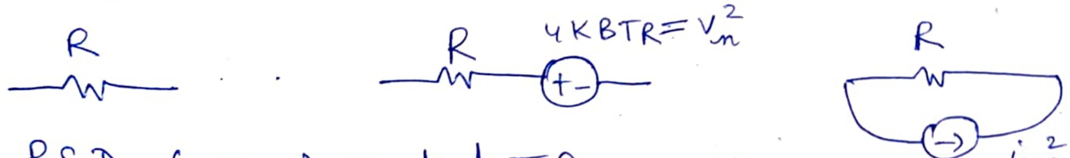
$$-\frac{G_L}{C_o} \qquad -\frac{g_{mp}}{C_M} \qquad -\frac{2g_{mp}}{C_M}$$

~~ever~~ presence of left half plane zero improves stability. Even after occurrence of 2 poles before UGB (unity gain pt.) we can have high ~~bandw~~ bandwidth

~~L-23~~ L-23

$V_n^2 = 4kBTR$, $i_n^2 = \frac{4kBT}{R}$ (~~Thermal~~ Thermal Noise)

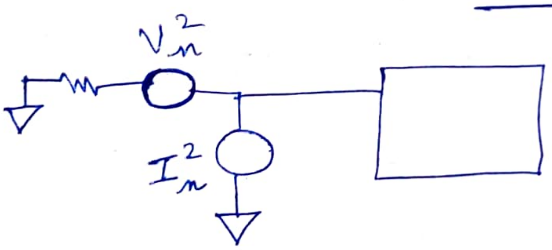
only real impedances have noise



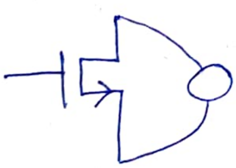
$i_n^2 = \frac{4KBT}{R}$

$$PSD\ (S_{v^2}) = 4kTR \rightarrow \frac{V^2}{Hz}$$

L-24



complete picture for noise consideration

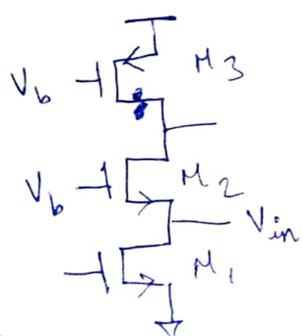


$S_i = 4kT\gamma g_m$ $\qquad$ γ is large for short channel device

$\gamma = \frac{2}{3}$ for long channel device

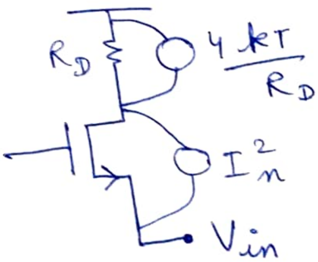
If resistors are connected in parallel noise reduces

Short ckt input to get noise due to I_n & open $\rightarrow V_n$



$$\frac{(4kT\gamma g_{m_3} + 4kT\gamma g_{m_2})(r_{o_2} \| r_{o_3})^2}{g_{m_2}^2 (r_{o_2} \| r_{o_3})^2} = V_{in}^2$$

L-25

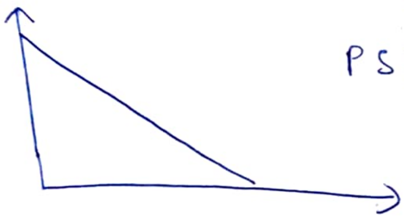


$$V_{in}^2 = \frac{\frac{4kT}{R_D} + 4kT\gamma g_{m_1}}{g_{m_1}^2}$$

$$I_{in}^2 = \frac{4kT}{R_D} \quad (\because \text{current gain is } 1)$$

~~Stat~~ Flicker noise – Not fully understood
↳ modelled at gate

PSD of flicker noise

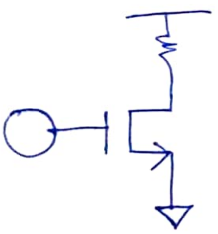


probability of e^- getting trapped is higher if observed for longer time

Noise bandwidth / corner frequency – freq. at which flicker noise becomes equal to thermal noise

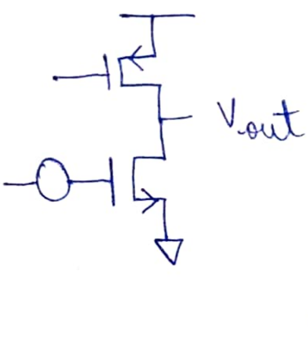
- As we move to smaller processes flicker noise dominates

$$V_n^2 = \frac{k}{WLC_{ox}} \frac{1}{f}$$ ✓ not for resistor



$$\frac{\frac{4kT}{R} + 4kT\gamma g_m}{g_m^2} + \frac{K}{WLC_{ox}} \cdot \frac{1}{f}$$

we could add both as they are uncorrelated

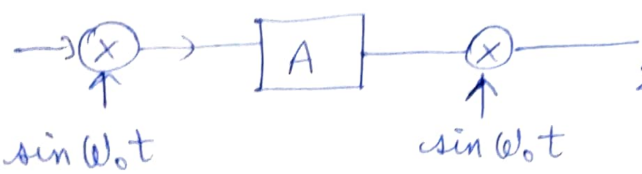


$$\frac{4kT\gamma(g_{mn} + g_{mp})}{g_{mn}^2} +$$

$$\frac{k_p}{(WL)_p C_{ox}} \frac{1}{f} \frac{g_{mp}^2}{g_{mn}^2} + \frac{k_n}{(WL)_n C_{ox}} \cdot \frac{1}{f}$$

Chopping for EEG signals →

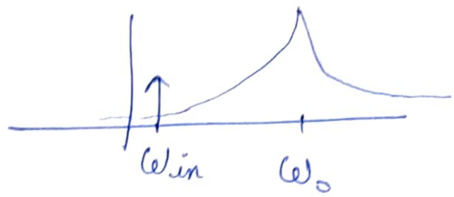
$\sin \omega_{in} t$ then pass thru LPF



$2\omega_0 \pm \omega_{in}$

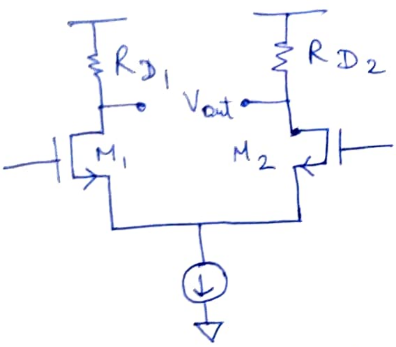
$\pm\, \omega_{in}$

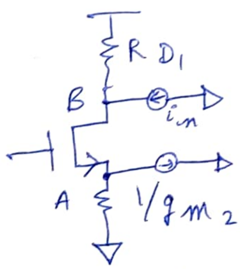
noise profile –



Noise analysis for differential amplifier

We do superposition of noise due to both NMOS





looking up impedance at A is same as ~~lookin~~ looking down $= 1/g_m$ so current gets equally distributed. Current $\frac{I_n}{2}$ moves upward in R_{D_1} & downward in R_{D_2} so

$$V_{out} = \frac{I_n}{2} R_{D_1} + \frac{I_n}{2} R_{D_2}$$

$$\text{so } V_n = I_n R_D \quad (\text{if } R_{D_1} = R_{D_2})$$

$$V_n^2 = I_{n_1}^2 R_D^2 + I_{n_2}^2 R_D^2 \longrightarrow \text{output referred voltage noise}$$

$$\text{Input referred noise} = \frac{(I_{n_1}^2 + I_{n_2}^2) R_D^2}{g_m^2 R_D^2} = \frac{8kT\gamma}{g_m}$$

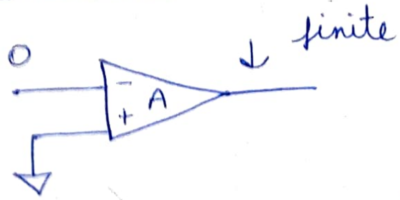
(thermal noise due to transistors)

$$+ \left(\frac{4kT}{R\, g_m^2}\right) \times 2$$

(due to R_D)

Lec - 26

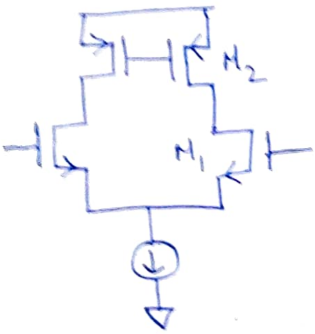
ideal opamp
A is infinite
so we get a
virtual ground



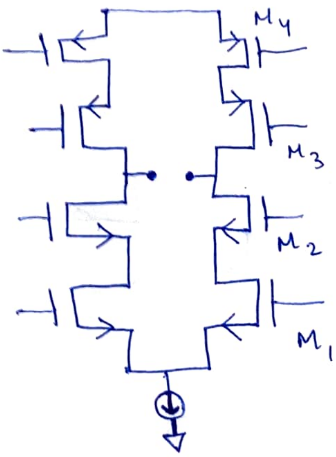
$Z_{in} = \infty$
& $Z_{out} = 0$
so VCVS
$V_o = A(V_A - V_B)$

operational transconductance amplifier (OTA) -
If output ~~im~~ impedance isn't low then Opamp becomes OTA

\# Cascoding done to increase gain

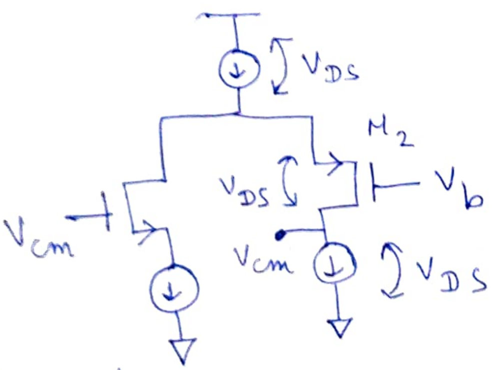


$g_{m_1}(r_{o1} \| r_{o2})$



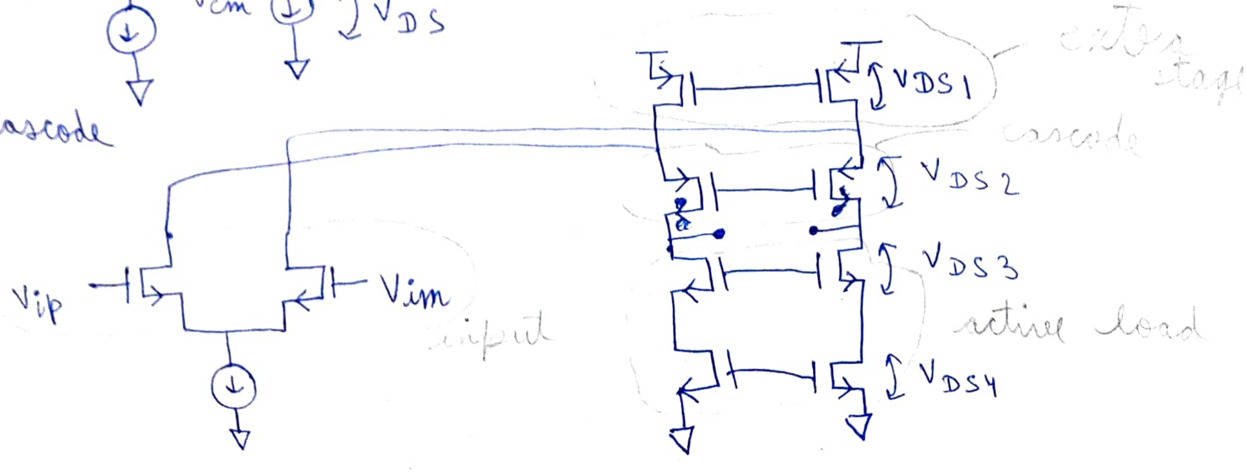
$g_{m_1}(r_{o1} g_{m_2} r_{o2} \| r_{o4} g_{m_3} r_{o3})$

folded cascode gives greater swing



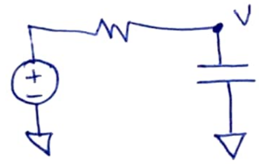
output & voltages ranges from
300 mV - 4.4 V
$V_{DS} - (V_{DD} - 2V_{DS})$

folded cascode
OTA



$V_{DS_3} + V_{DS4} < V_{out} < V_{DD} - V_{DS1} - V_{DS2}$

The extra stage causes noise so we get a higher ~~out~~ output swing at the cost of noise (from telescopic amp. to folded ~~caused~~ cascode OTA)

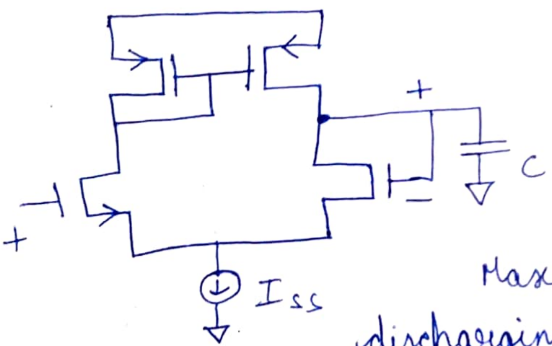


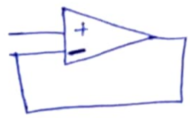
$$V_o = V(1 - e^{-t/RC})$$

$$C\frac{dV_o}{dt} = \frac{V}{R} \cdot e^{-t/RC}$$

if bias current for amplifier is less than what is needed to achieve $C\frac{dV_o}{dt}$ (for higher step input) then amplifier is said to ~~slew~~ slew and it leads to a slower response at output.

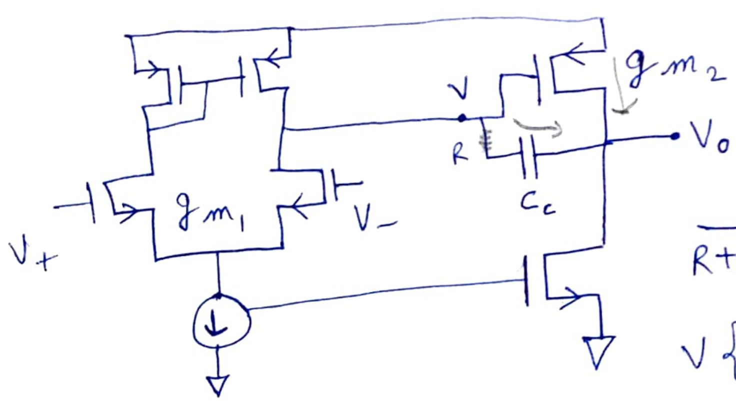
L-27





$\frac{I_{ss}}{C}$ is the slew rate in case of both +ve & -ve pulse applied

Maximum extent of charging & discharging current is the slew rate



zero location is found by making total current 0.

$$\frac{V}{R + \frac{1}{sC_c}} - g_m V$$

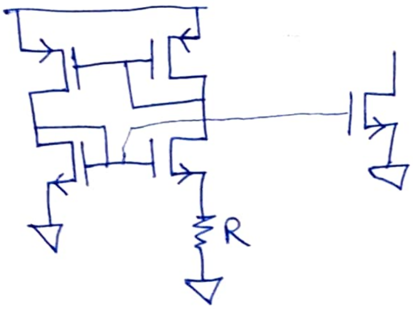
$$V\{sC_c - g_m - sRC_c g_m\} = 0$$

so $C_c - RC_c g_m = 0$ to eliminate zero

$$\Rightarrow R = \frac{1}{g_m}$$

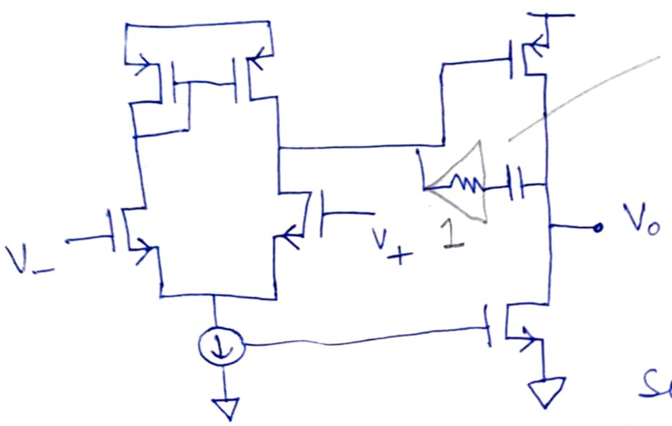
for $R = 0$ we have zero at $\frac{g_m}{C_c}$ in RHP then for $R = \frac{1}{g_m}$ we get zero at ∞. Now on increasing R we get a LHP zero which is actually good for stability.

ckt for g_m to ~~track~~ track $\frac{1}{R}$



g_m of this NMOS tracks $\frac{1}{R}$

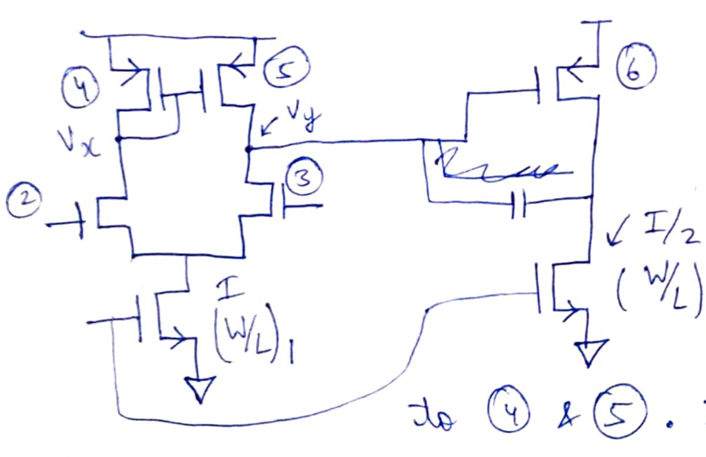
L-28



indirect compensation

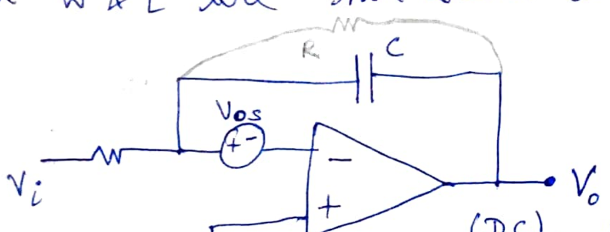
it causes miller distribution of the capacitor but doesn't lead to 2 paths from input to output. So the zero is eliminated (without the need of resistor by applying unity gain voltage buffer.)

could be made using common drain amp.



$\left(\frac{W}{L}\right)_7 \times 2 = \left(\frac{W}{L}\right)_1$

We know from earlier discussion that $V_x = V_y$ so 6 is also properly biased if 6 is identical to 4 & 5. If only W/L ratio is same but W & L are not same ~~&~~ it leads to higher order differences.



resistor is added to prevent saturation of output. At high freq. current passes thru C ~~R~~ & at low f thru R.

offset is caused due to mismatch in NMOS parameters like V_T

L-29

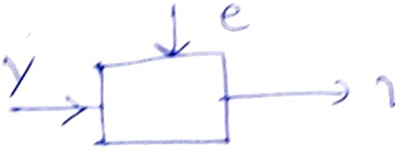
~~Ho~~ Nyquist sampling theorem → $f_s > 2f_m$

Analog	CA CT	CA discrete DT time signal
CT digital	DA CT	DA ↘ digital (square wave) DT

The reason for this pathway is because if we discretise first then the wave will ~~have~~ have higher order harmonics (square wave) so we will ~~have~~ have to sample at ∞ freq. to prevent data loss (acc. Nyquist)

digital signal

quantisation error



$v = y + e$

① Random

As we increase the no. of levels for quantisation the error signal becomes more random

L-30

Ideal LPF is not realisable as the function is non causal & we can design only causal systems.