ELL 304: Lab 2 Report
Single Device Amplifier

T Pratham: 2020EE10559

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1 Aim

To characterize single-MOSFET amplifiers.

1. Resistive biasing
2. Common source amplifier
3. Common gate amplifier
4. Common drain amplifier

2 Apparatus Required

- CD4007 IC
- Breadboard
- Oscilloscope
- DC Source Generator
- Function Generator
- Resistances
- Capacitors

3 Theory

- With proper biasing, the MOSFET will provide amplification for small signal inputs.
- We are only interested in the saturation region of the MOSFET operation. That is, we need to bias our MOSFET such that $V_{DS} > V_{GS} - V_{Th}$ for an nMOS.
- Our baising is such that we are providing V_G via a resistive divider. The value of V_G is given as: $V_G = \frac{R_{G2}}{R_{G1}+R_{G2}} V_{DD}$.

- The value of V_D is given as: $V_D = V_{DD} - I_D R_D$.
- The value of V_S is given as: $V_S = I_D R_S$.
- Since we an directly measure all the above three voltages, we can also calculate I_D using any of the previous two relations.
- **Common Source Amplifier:** In a common source amplifier, input is connected at the gate and output is taken at the drain of the MOSFET. A common source amplifier is an inverting amplifier where the output is phase shifted by 180°. The gain obtained is given as:

$$A_v = -\frac{\text{resistance at drain}}{\text{resistance at source}} = -\frac{g_m R_D}{1 + g_m R_S}$$

  Since $g_m R_S \gg 1$,

$$A_v \approx -\frac{R_D}{R_S}$$

- **Common Gate Amplifier:** In a common gate amplifier, input is connected at the source and output is taken at the drain of the MOSFET. A common gate amplifier is a non-inverting amplifier. It is also known as a current buffer since the input and output current is same. The voltage gain obtained is given as:

$$A_v = g_m R_D$$

- **Common Drain Amplifier:** In a common drain amplifier, input is connected at the gate and output is taken at the source of the MOSFET. A common drain amplifier is also known as a voltage buffer, since the input and output voltage is same. Thus, the gain obtained here is theoretically:

$$A_v \approx 1$$

4 Resistive Biasing

4.1 Procedure

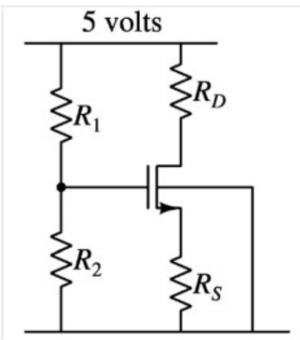

Figure 1: Circuit Diagram for part 1

- Circuit was connected as shown in circuit diagram.

- The value of resistors used was: R_s=**10k**Ω**,** R_{G1}=**100k**Ω **and** R_{G2}=**330k**Ω.
- Gate-source and drain-source voltage readings were taken for different values of R_D varying from 33kΩ to 0.

4.2 Readings

$V_{DD} = 5$ V

R_D (Ω)	V_G (V)	V_D (V)	V_S (V)	I_D(mA)	V_{DS}(V)	V_{GS} (V)
33000	3.76	1.49	1.35	0.135	0.14	2.41
10000	3.76	2.68	2.28	0.228	0.4	1.48
3300	3.76	4.16	2.32	0.232	1.84	1.44
1000	3.76	4.72	2.36	0.236	2.36	1.4
470	3.76	4.84	2.36	0.236	2.48	1.4
100	3.76	4.92	2.36	0.236	2.56	1.4
0	3.76	5	2.36	0.236	2.64	1.4

Table 1: Measurements of V_{GS} and V_{DS} and calculation of corresponding I_D

4.3 Circuit Snapshot

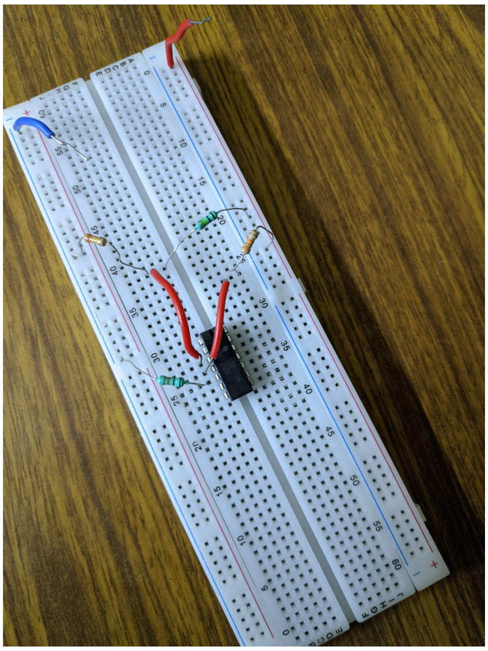

Figure 2: Connections snapshot for Part 1

4.4 Graphs

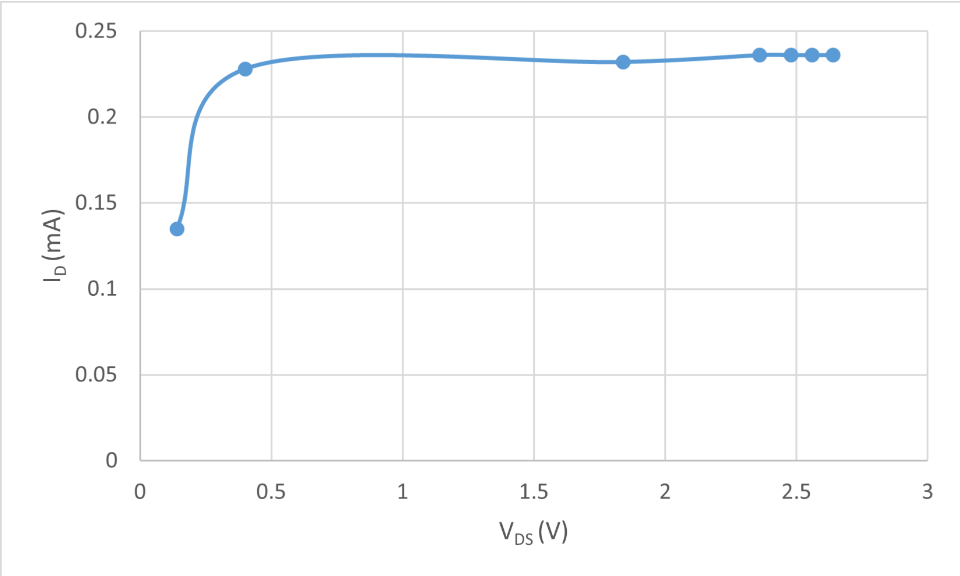

Figure 3: I_D vs V_{DS}

4.5 Observations

- We get some current with R_D=33kΩ. On decreasing this resistance R_D (thus increasing V_{DS}), the current increases.
- Below a certain R_D, the current saturates.
- The current was very low at R_D=33kΩ.
- When we make R_D=10kΩ, the current increases.
- When we make R_D=0 (short), the current is almost same as with R_D=10kΩ.
- The largest (available) R_D for which the current does not change is found to be 10kΩ.

5 Common Source Amplifier

5.1 Procedure

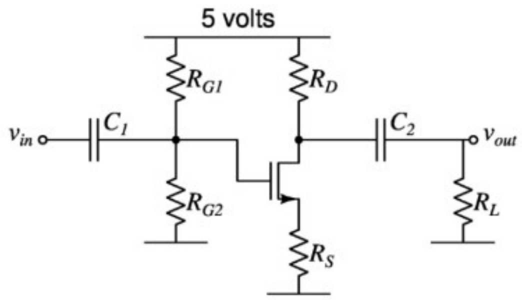

Figure 4: Circuit Diagram for common source amplifier.
R_D = 10kΩ, R_S = 10kΩ, R_{G1} = 330kΩ, R_{G2} = 100kΩ, R_L = 100kΩ, $C_1 = C_2 = 22\mu$F

- Connections were made as shown in circuit diagram.
- The resistance values used were R_D=10kΩ, R_S=10kΩ, R_{G1}=330kΩ, R_{G2}=100kΩ and R_L=100kΩ. The capacitance used were all 22 μF.
- A 100mV pk-pk 100Hz sine wave was injected at v_{in}. And voltage gain was measured from v_{out}/v_{in}.
- Source frequency was increased till 1MHz and the above measurement was repeated each time.

5.2 Readings

DC operating point : V_G = 3.76V, V_D = 3.54V, V_S = 1.72V

Therefore, V_{DS} = 1.82V and $V_{GS} - V_{Th}$ = 2.04V-0.9V = 1.14V. Hence, $V_{DS} > V_{GS} - V_{Th}$.

Small signal readings : v_{in} = 100mV pk-pk sine, V_{DD} = 5 V

Frequency (Hz)	v_{out} (mV)	$\lvert\text{Gain}\rvert = \lvert v_{out}/v_{in}\rvert$
100	68	0.68
200	68	0.68
400	68	0.68
600	68	0.68
800	68	0.68
1000	67	0.67
2000	68	0.68
4000	68	0.68
6000	68	0.68
8000	68	0.68
10000	68	0.68
20000	66	0.66
40000	70	0.7
60000	68	0.68
80000	68	0.68
100000	67	0.67
200000	66	0.66
400000	61	0.61
600000	56	0.56
800000	52	0.52
1000000	49	0.49
2000000	36	0.36
4000000	26	0.26

Table 2: Measurements of v_{out} and calculation of corresponding gain for Common Gate Amplifier

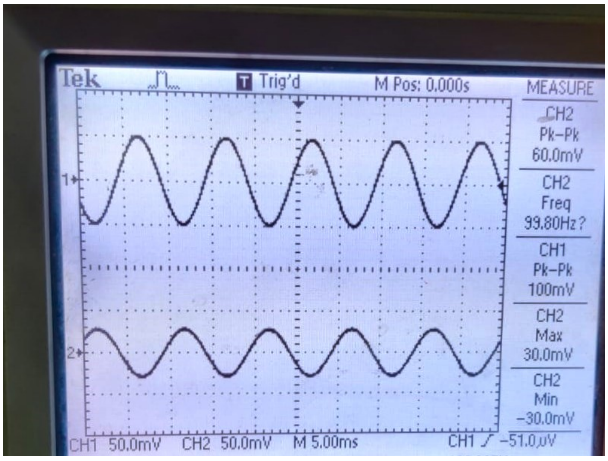

Figure 5: Common Source Amplifier Output at 100Hz

5.3 Circuit Snapshot

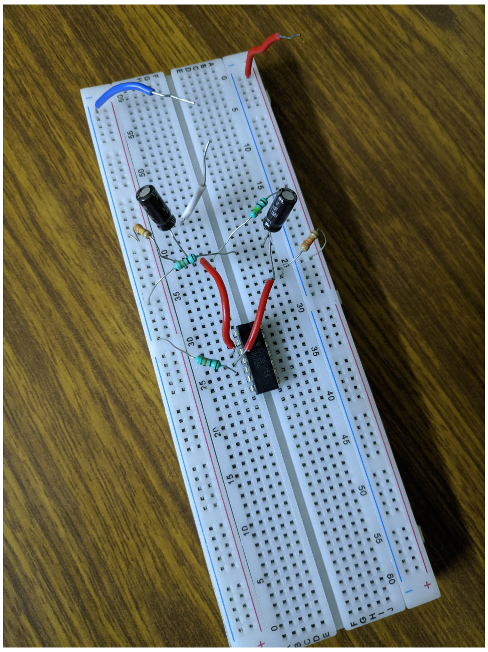

Figure 6: Connections snapshot for Part 2

5.4 Graphs

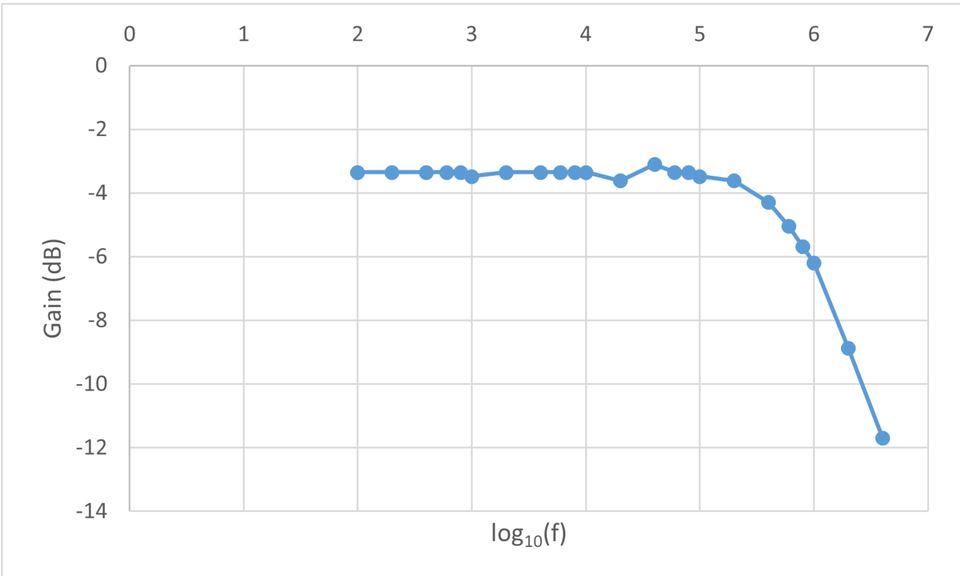

Figure 7: Gain (dB) vs log_{10}(frequency) plot

5.5 Observations

- We observe that we get a small signal gain of around ~ 0.68
- Initially, the gain is almost unchanging on changing frequency.

- We also observe that after around 400kHz, on increasing frequency, the gain decreases drastically.

6 Common Gate Amplifier

6.1 Procedure

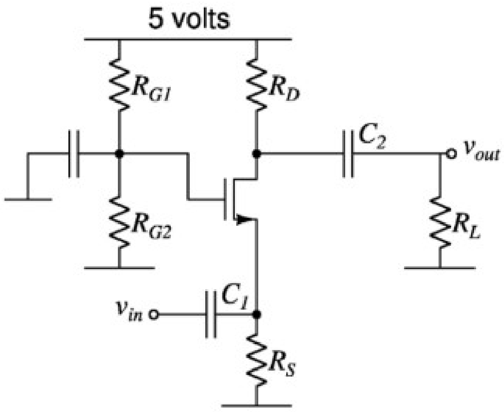

Figure 8: Circuit Diagram for common gate amplifier.
R_D = 10kΩ, R_S = 10kΩ, R_{G1} = 330kΩ, R_{G2} = 100kΩ, R_L = 100kΩ, $C_1 = C_2 = 22\mu$F

- Connections were made as shown in circuit diagram.
- The resistance values used were R_D=**10kΩ,** R_S=**10kΩ,** R_{G1}=**330kΩ,** R_{G2}=**100kΩ and** R_L=**100kΩ**. The capacitance used were all **22 μF**.
- A 100mV pk-pk 100Hz sine wave was injected at v_{in}. And voltage gain was measured from v_{out}/v_{in}.
- Source frequency was increased till 1MHz and the above measurement was repeated each time.

6.2 Readings

DC operating point : V_G = 3.76V, V_D = 3.31V, V_S = 1.72V
Therefore, V_{DS} = 1.59V and $V_{GS} - V_{Th}$ = 2.04V-0.9V = 1.14V. Hence, $V_{DS} > V_{GS} - V_{Th}$.

Small signal readings : v_{in} = 100mV pk-pk sine, V_{DD} = 5 V

Frequency (Hz)	v_{out} (mV)	$\lvert\text{Gain}\rvert = \lvert v_{out}/v_{in}\rvert$
100	644	6.44
200	636	6.36
400	636	6.36
600	636	6.36
800	636	6.36
1000	636	6.36
2000	636	6.36
4000	636	6.36
6000	640	6.4
8000	636	6.36
10000	632	6.32
20000	600	6
40000	508	5.08
60000	420	4.2
80000	352	3.52
100000	296	2.96
200000	166	1.66
400000	90	0.9
600000	62	0.62
800000	48	0.48
1000000	36	0.36

Table 3: Measurements of v_{out} and calculation of corresponding gain for Common Gate Amplifier

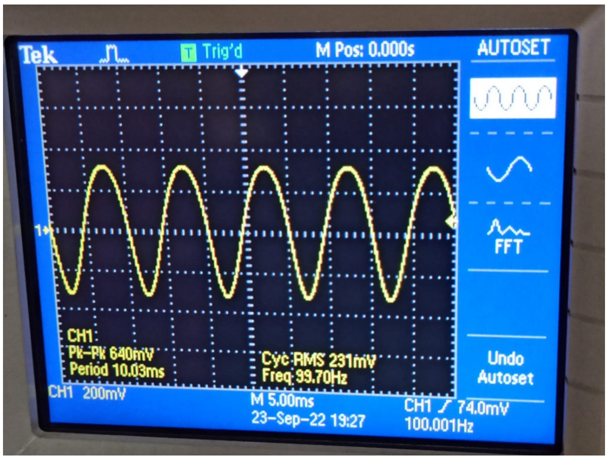

Figure 9: Common Gate Amplifier Output at 100Hz

6.3 Circuit Snapshot

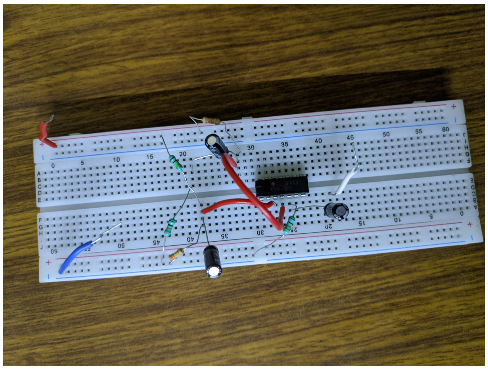

Figure 10: Connections snapshot for Part 3

6.4 Graphs

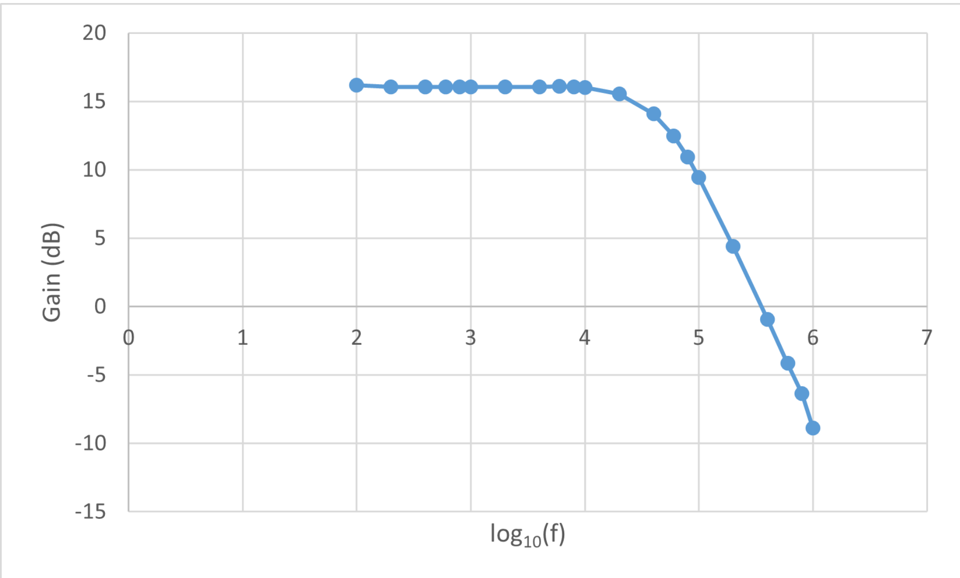

Figure 11: Gain (dB) vs log_{10}(frequency) plot

6.5 Observations

- We observe that we get a small signal gain of ˜6.
- Just like common source, here also the gain drops close to zero at very high frequencies. Here, above 600kHz, there is a significant drop in gain.

7 Common Drain Amplifier

7.1 Procedure

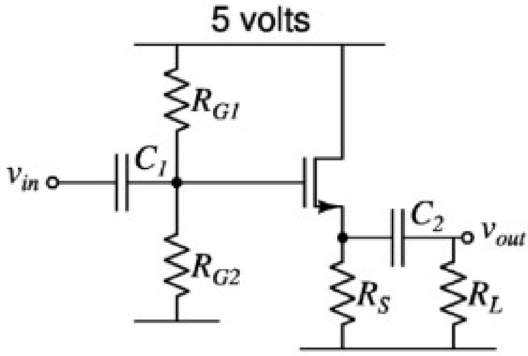

Figure 12: Circuit Diagram for common drain amplifier.
R_S = 10kΩ, R_{G1} = 330kΩ, R_{G2} = 100kΩ, R_L = 100kΩ, $C_1 = C_2$ = 22μF

- Connections were made as shown in circuit diagram.
- The resistance values used were R_S=10kΩ, R_{G1}=330kΩ, R_{G2}=100kΩ and R_L=100kΩ. The capacitance used were all 22 μF.
- A 100mV pk-pk 100Hz sine wave was injected at v_{in}. And voltage gain was measured from v_{out}/v_{in}.
- Source frequency was increased till 1MHz and the above measurement was repeated each time.

7.2 Readings

DC operating point : V_G = 3.76V, V_D = 5V, V_S = 1.82V
Therefore, V_{DS} = 3.18V and $V_{GS} - V_{Th}$ = 1.94V-0.9V = 1.04V. Hence, $V_{DS} > V_{GS} - V_{Th}$.

Small signal readings : v_{in} = 100mV pk-pk sine, V_{DD} = 5 V

Frequency (Hz)	v_{out} (mV)	$\|Gain\| = \|v_{out}/v_{in}\|$
100	85	0.85
250	86	0.86
500	82	0.82
750	82	0.82
1000	78.4	0.784
2500	62.8	0.628
5000	58.4	0.584
7500	62.8	0.628
10000	60.4	0.604
25000	64	0.64
50000	60	0.6
75000	60	0.6
100000	62	0.62
250000	62	0.62
500000	62	0.62
750000	7	0.07
1000000	3	0.03

Table 4: Measurements of v_{out} and calculation of corresponding gain for Common Drain Amplifier

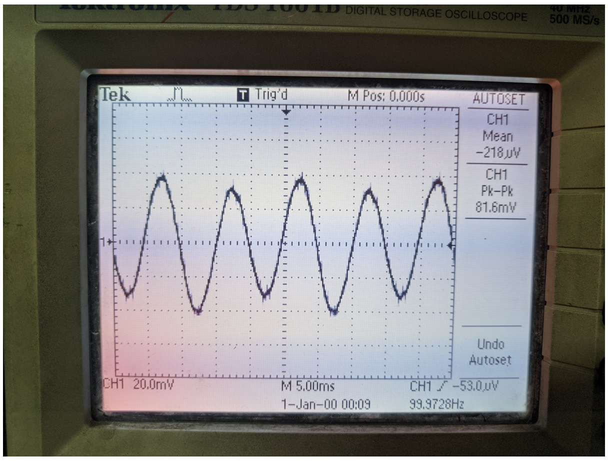

Figure 13: Common Drain Amplifier Output at 100Hz

7.3 Circuit Snapshot

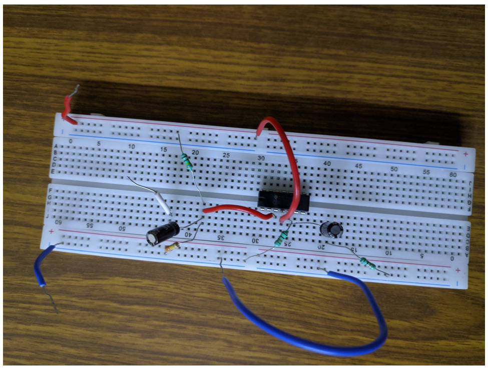

Figure 14: Connections snapshot for Part 4

7.4 Graphs

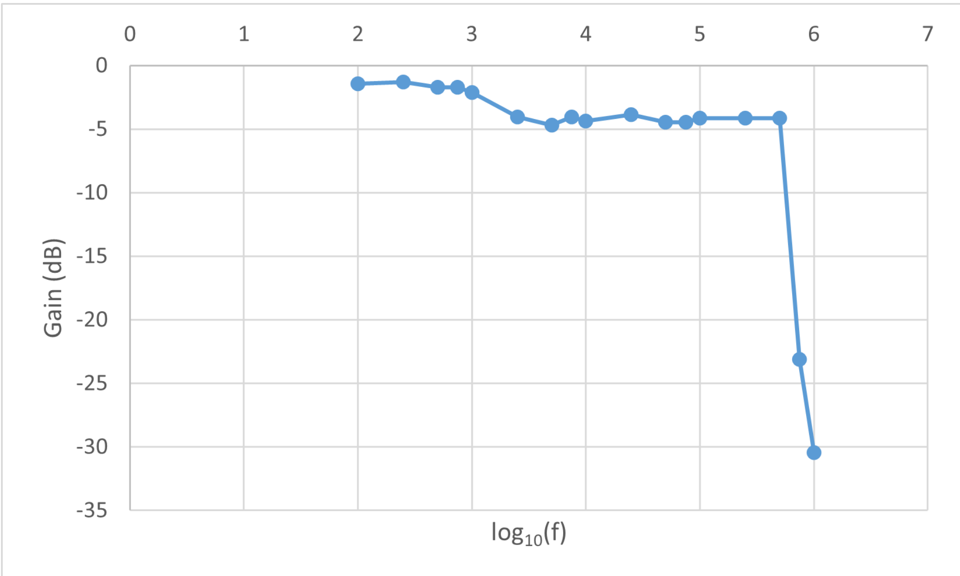

Figure 15: Gain (dB) vs log_{10}(frequency) plot

7.5 Observations

- We get a small signal gain of ˜0.8.
- Again, the gain drops significantly at higher frequencies after 500kHz.

8 Conclusion

- **Resistive Biasing**: When the drain voltage is above overdrive voltage in an nMOS, i.e., when the nMOS is in saturation, the device current remains constant.
- **Common Source Amplifier**: The gain obtained is ˜ 0.68, which is the expected gain from theory. Since we are using $R_D = R_S =$ 10kΩ, the approximate gain is

around 1. If we calculate the exact value without approximation using $\frac{g_m R_D}{1+g_m R_S}$ and using $g_m = \frac{2I_D}{V_{GS}-V_{Th}}$, we get a value smaller than 1 (around 80%). Due to practical limitations, we do not get an exact gain, and hence within the practical bounds, our observations match with theory. We also see that gain decreases by about 3dB at 1MHz.

- **Common Gate Amplifier**: The gain obtained is ~6.3, which is the expected gain from theory within practical bounds. Also, the gain decreases by 3dB at around 60kHz
- **Common Drain Amplifier**: The gain obtained is ~0.8 which is very close to the source follower property of common drain amplifier. Within practical bounds, the theoretical value matches the experimental value. Also, the gain decreases by 3dB at around 750kHz.
- We observed that the gain in all the three configurations is nearly constant in lower frequencies and then suddenly drops considerably when frequency is increased. We can see this in the graphs plotted which resemble a low pass filter. This can be explained by the parasitics. At higher frequencies, the parasitic capacitances start to show their effect. The impedances of parasitic capacitance of the MOSFET become comparable to the biasing impedances in the circuit. Hence, all the current now does not flow through the load resistors and hence the output voltage also decreases.