Transient and Frequency Analysis of various Analog, Op-Amp and Mixed Signal Circuits using LTSpice & Cadence Virtuoso-Spectre

Introduction: -

The project aims to simulate, analyse and understand the behaviour of various analog circuits by utilising transient and frequency analysis on LTSpice.

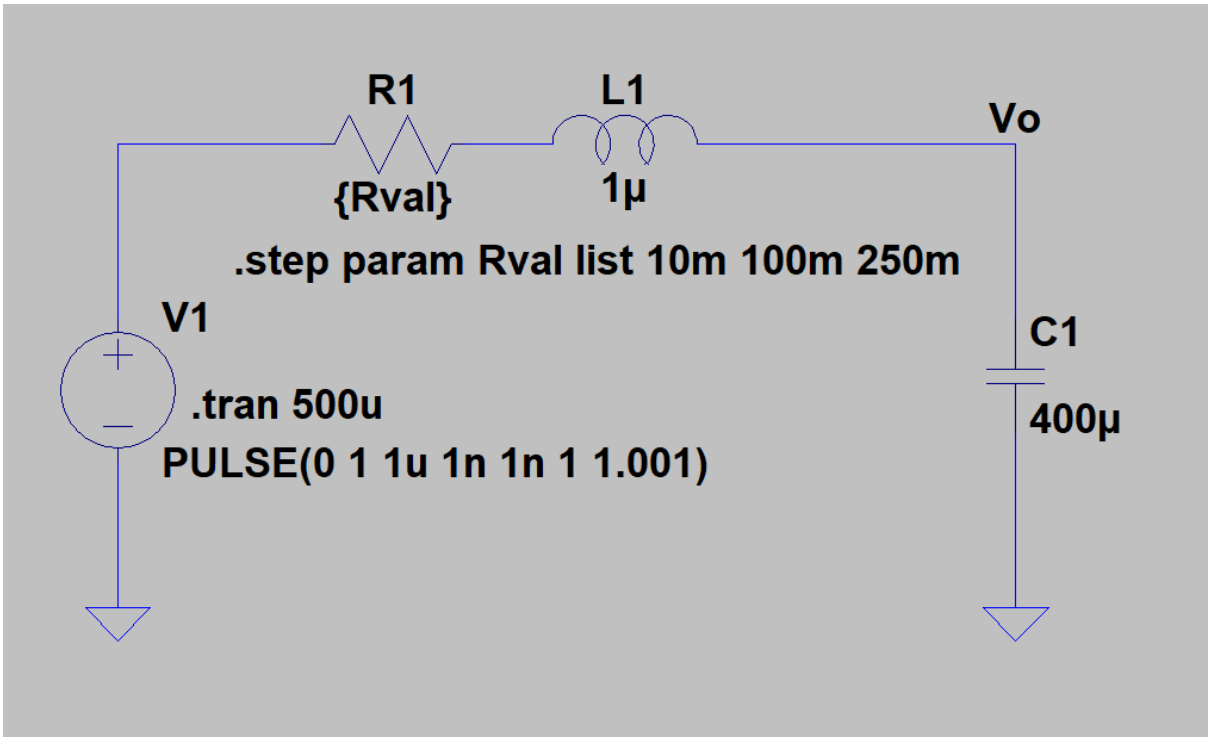
Following are a few circuit simulations.

Transient analysis of series RLC circuit: -

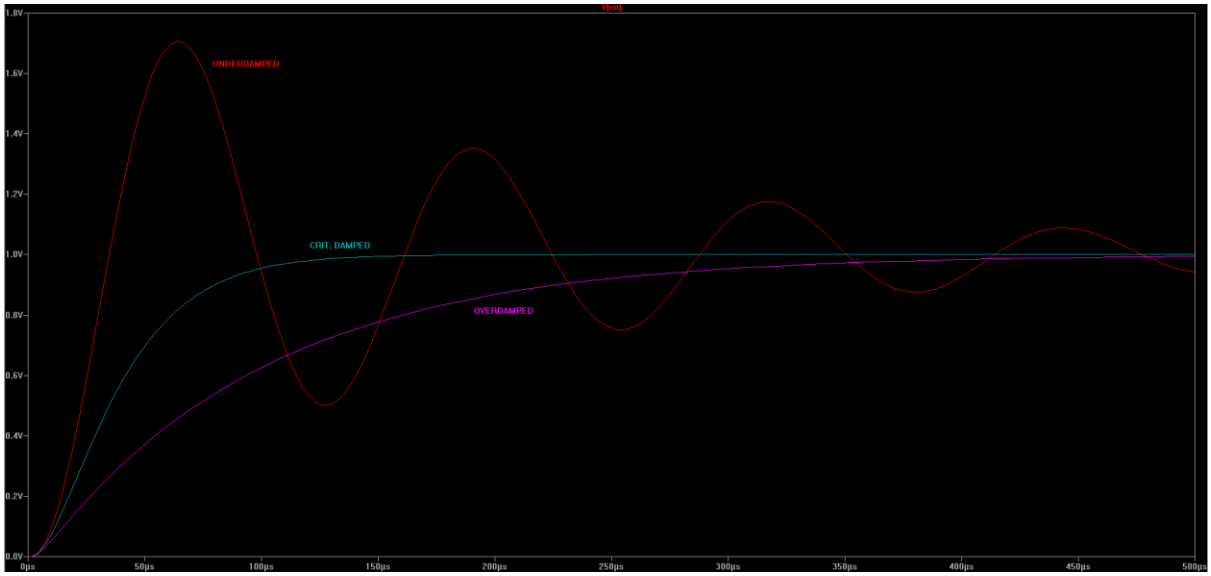
For **C = 400uF** and **L = 1uH**, we get the value of **R = 100 m-Ohm** to be the condition for critically damped (from $\mathbf{R^2 = 4(L/C)}$). Any value of R less than this would render the circuit to operate in an under-damped condition while the value of R greater than this would make it operate in an over-damped condition.

Attached are the circuit along with simulation parameters and the waveform.

LTSpice: -

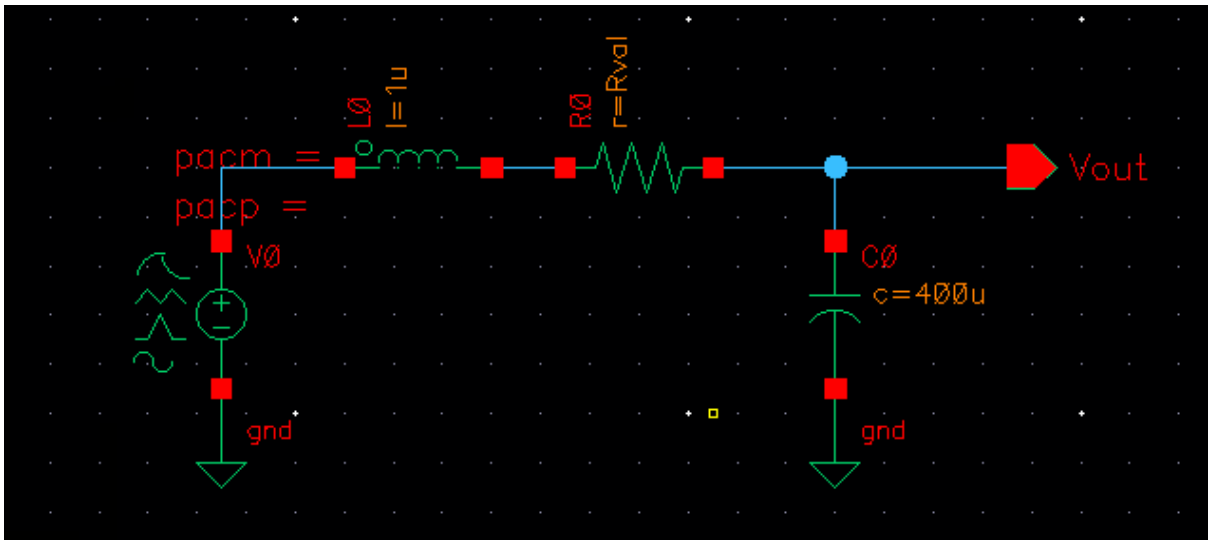


Schematic for transient analysis



Transient analysis plot

Virtuoso: -

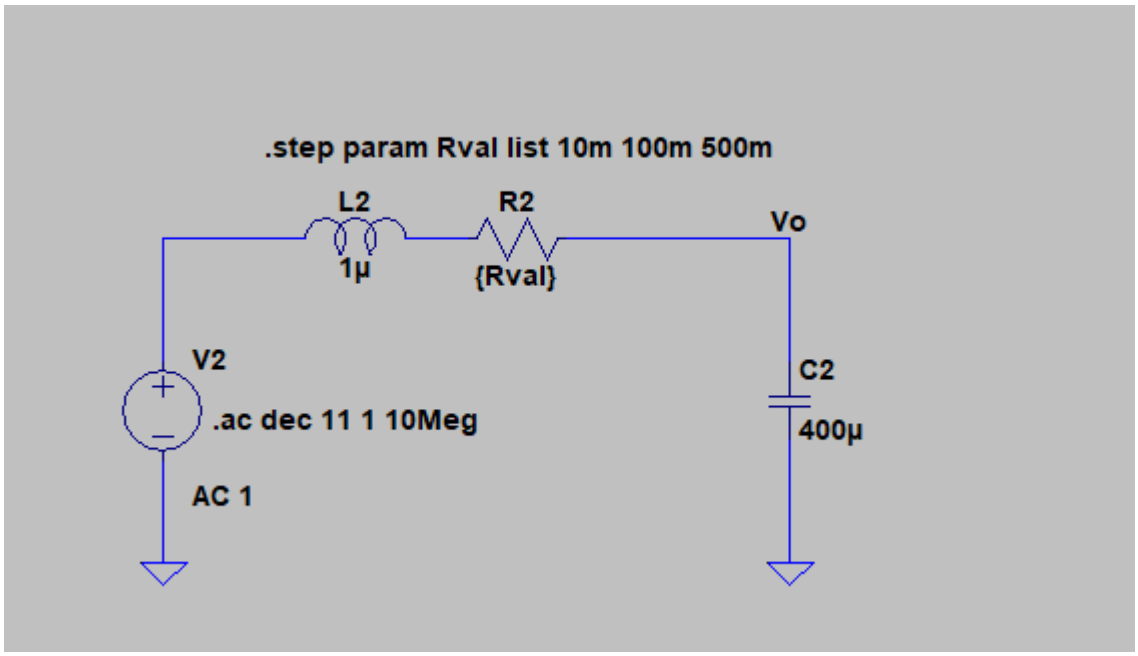


Schematic

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter	Filter
Parameters: Rval=10m						
1	mylib1_rlc1_1	/Vo				
Parameters: Rval=100m						
2	mylib1_rlc1_1	/Vo				
Parameters: Rval=250m						
3	mylib1_rlc1_1	/Vo				

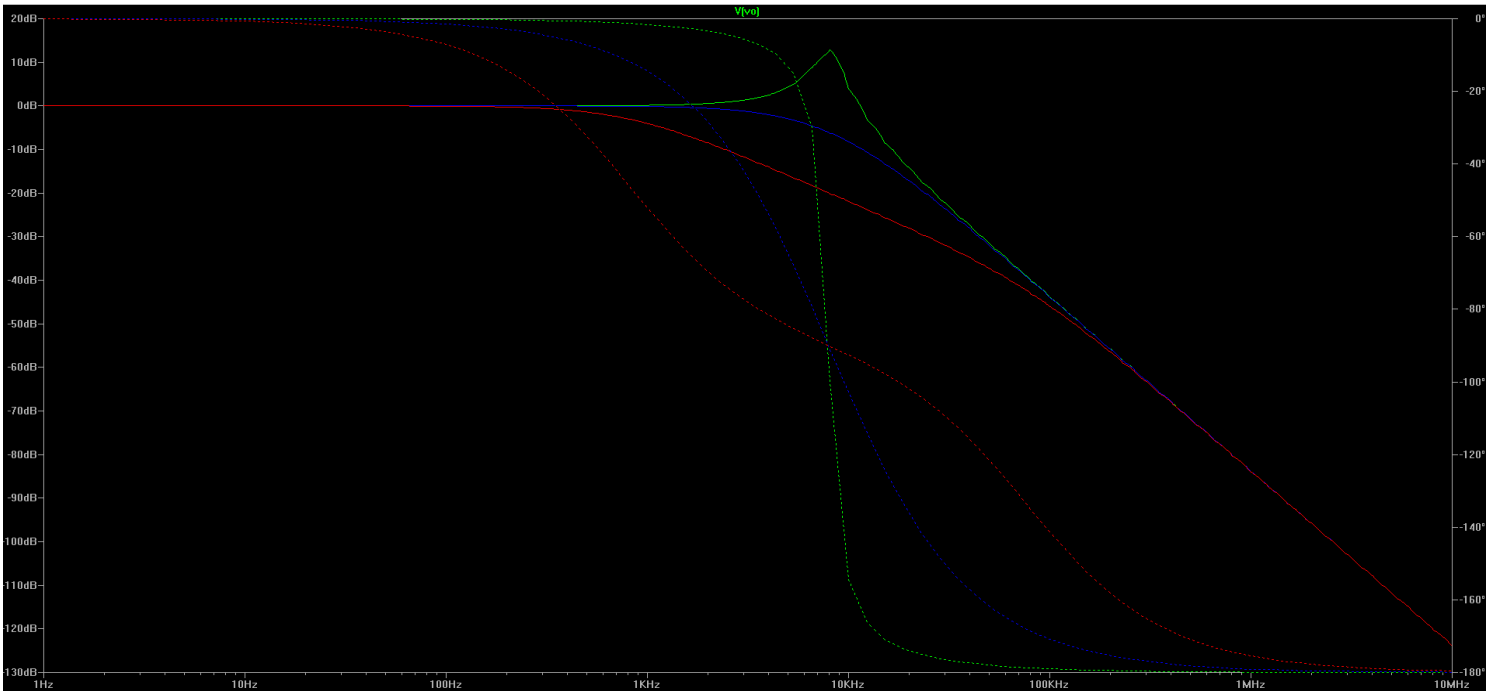
Setup of parameters

Frequency Analysis of Series LRC Circuit: -



Schematic for AC analysis

I have used a similar circuit (LRC instead of RLC), performed AC analysis using decade sweep from 1Hz to 10 MegHz, and parameter sweeps to represent 3 cases for showing bode plots of over, under and critically damped cases.

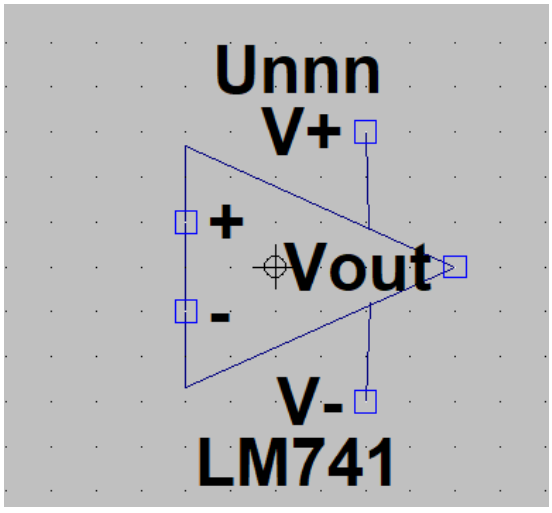


Bode plots

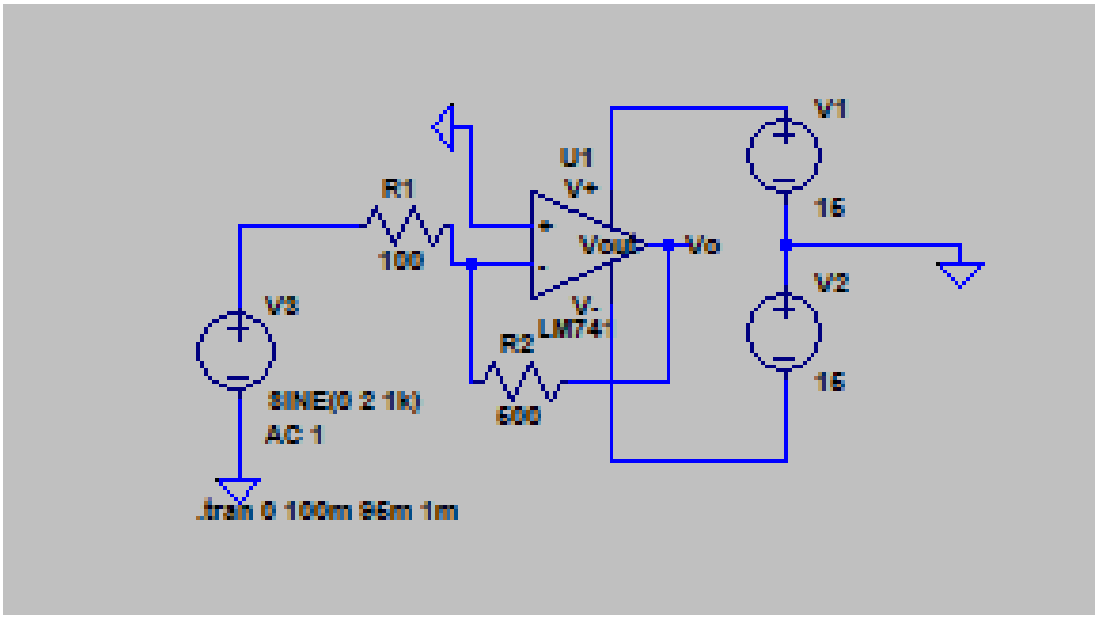
Inverting & Non-Inverting Op-Amp:-

I have utilised the LM741 Op-Amp here. Since it is not available in the standard LTSpice library I had to download its file from the TI website and restructure the schematic making it visually easier to understand.

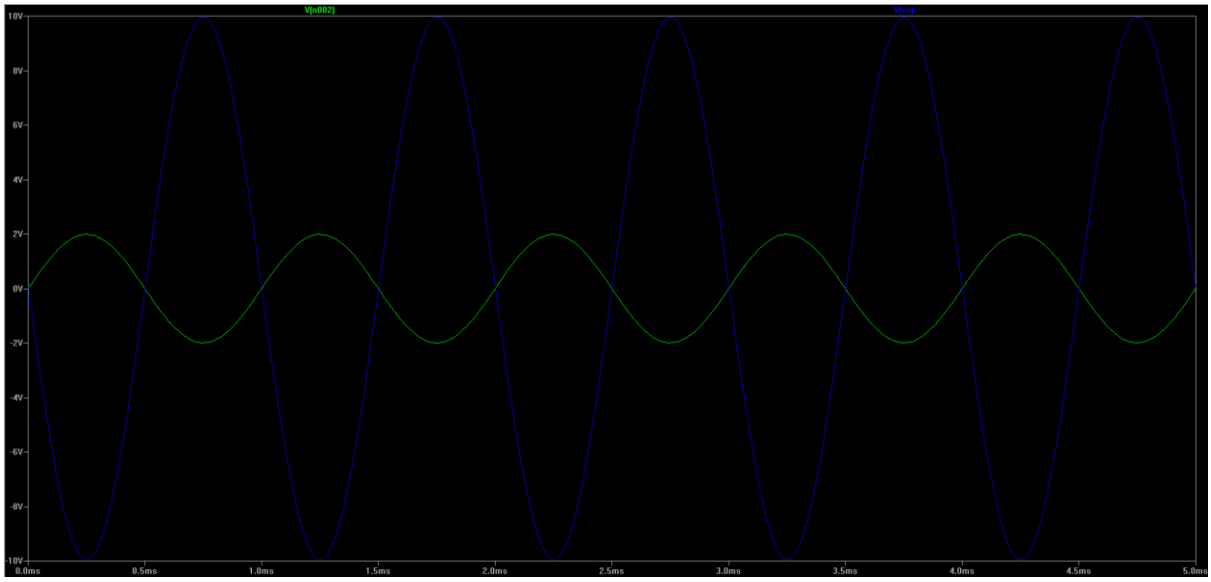
LTSpice:-



Created schematic for LM741



Schematic for inverting Op-Amp

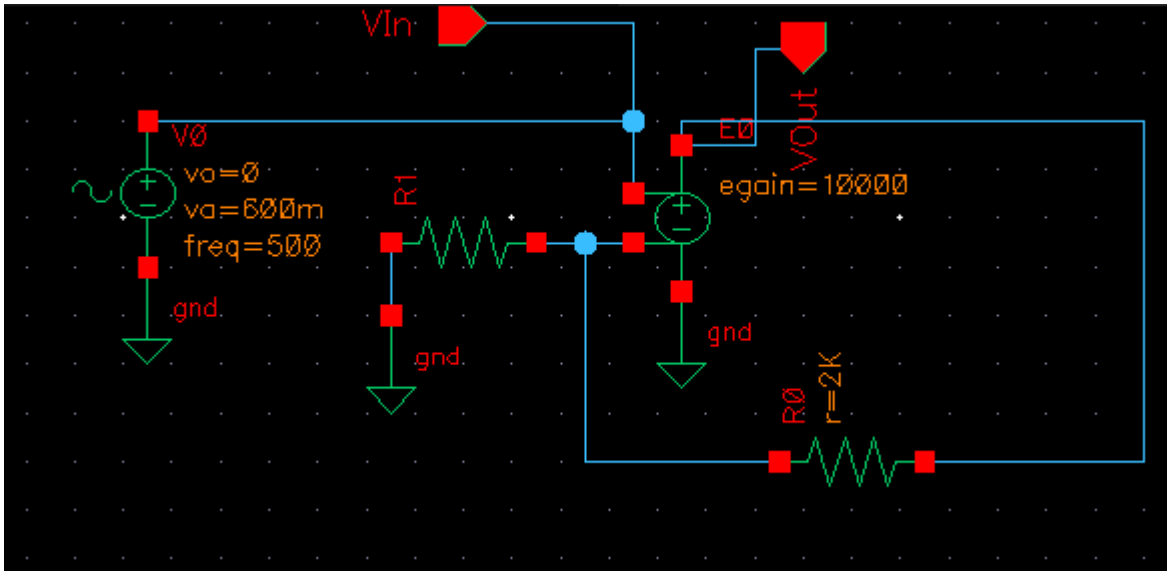


Waveform for inverting Op-Amp

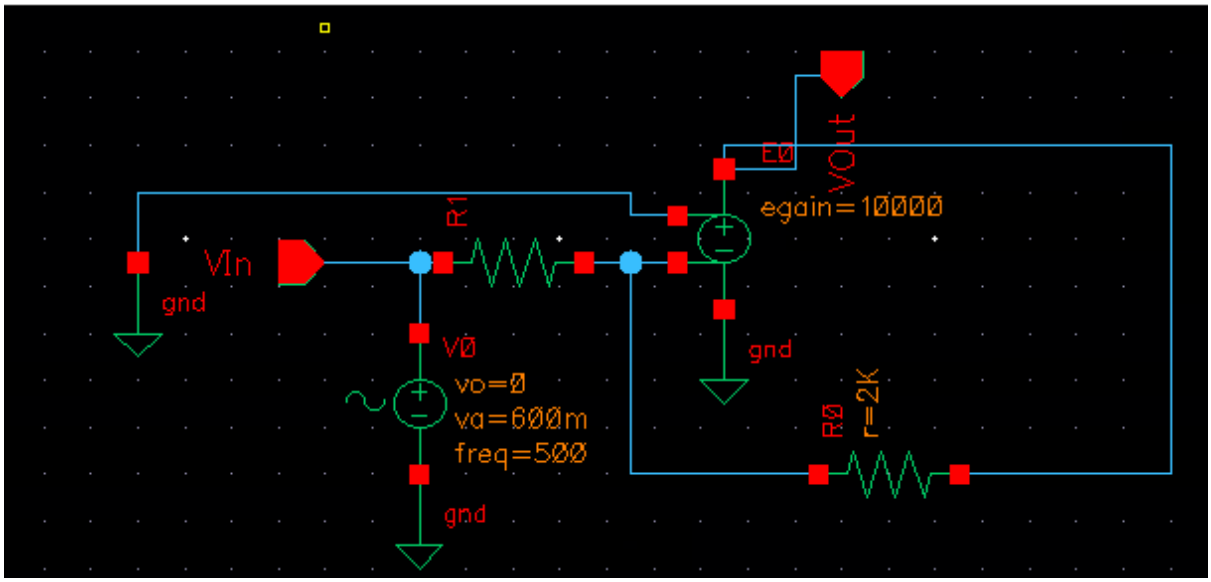
Virtuoso:-

For the implementation of the inverting and non-inverting op-amp, I have utilised a **VCVS** (**V**oltage **C**ontrolled **V**oltage **S**ource) as the main device for the construction of the circuit.

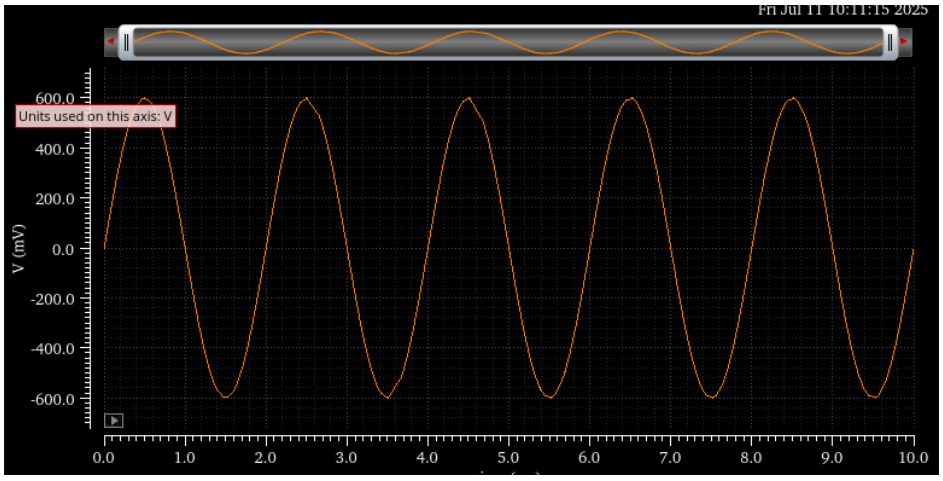
Following are the schematics and results for the above-mentioned circuits: -



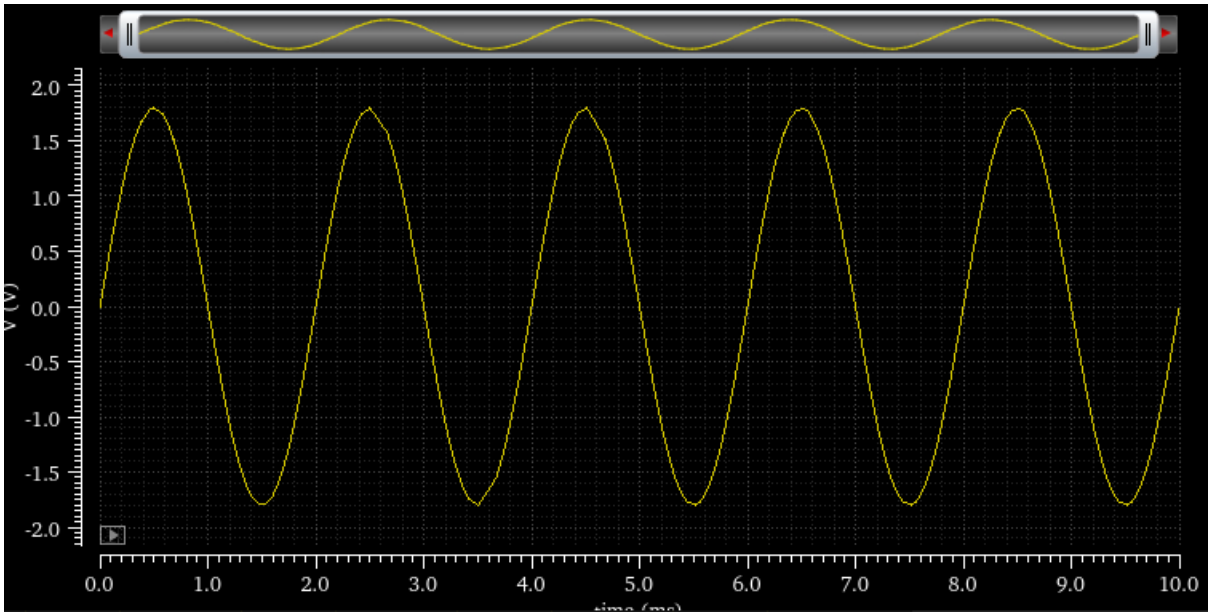
Non-inverting amplifier (schematic)



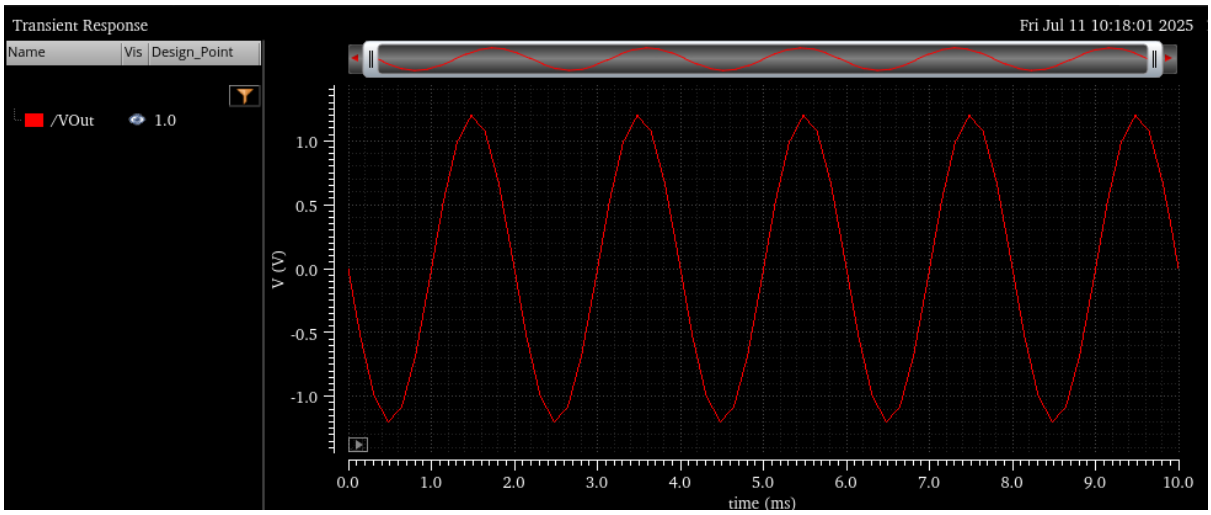
Inverting Amplifier (schematic)



Input wave



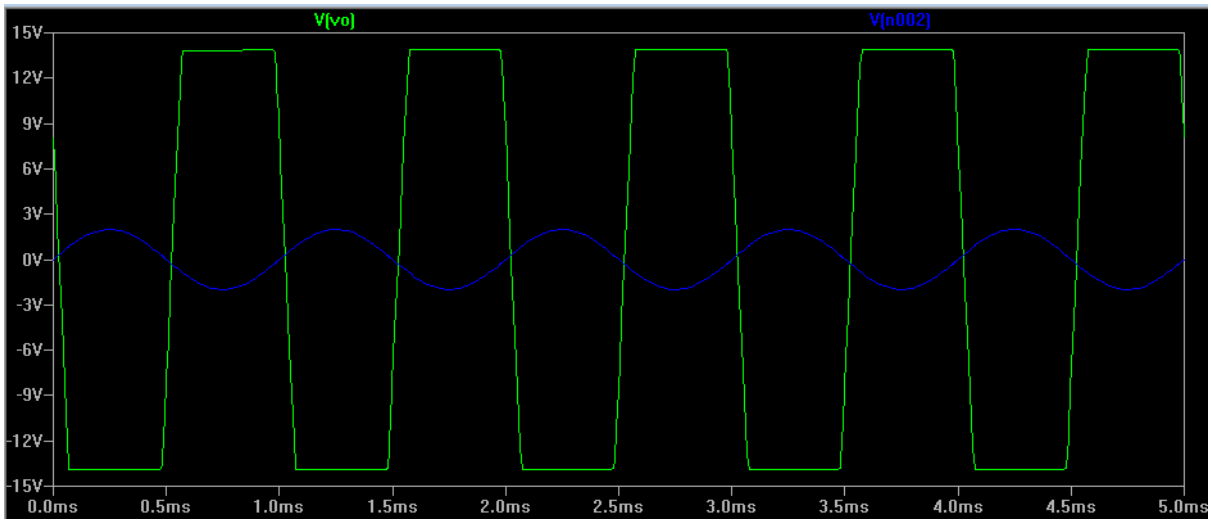
O/p for non-inverting amp



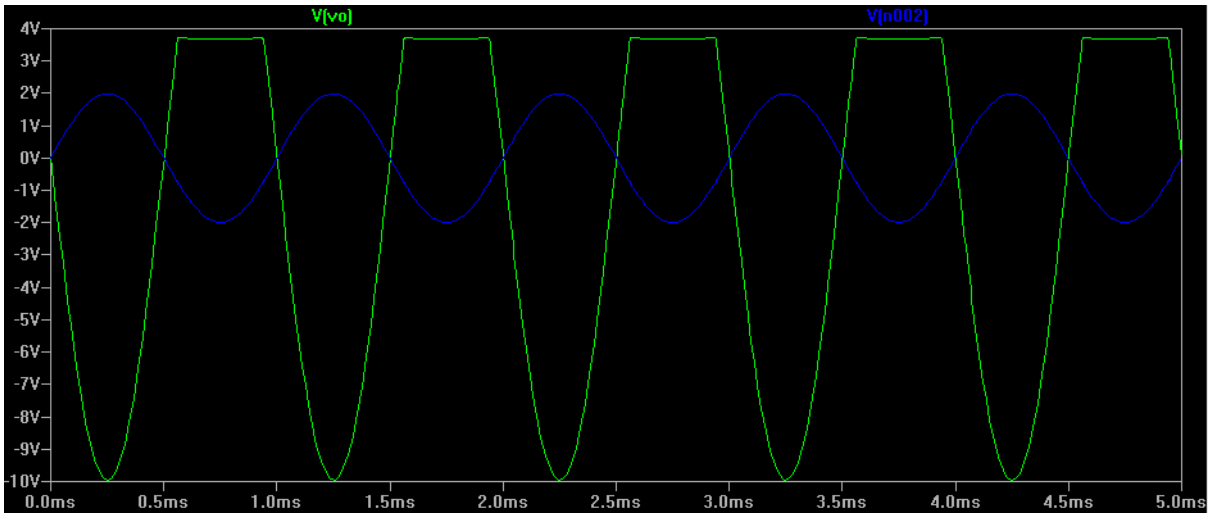
O/p for inverting amp

Clipping: -

The following are the graphs for clipping circuits, showing both positive and negative clipping as well as only positive clipping.

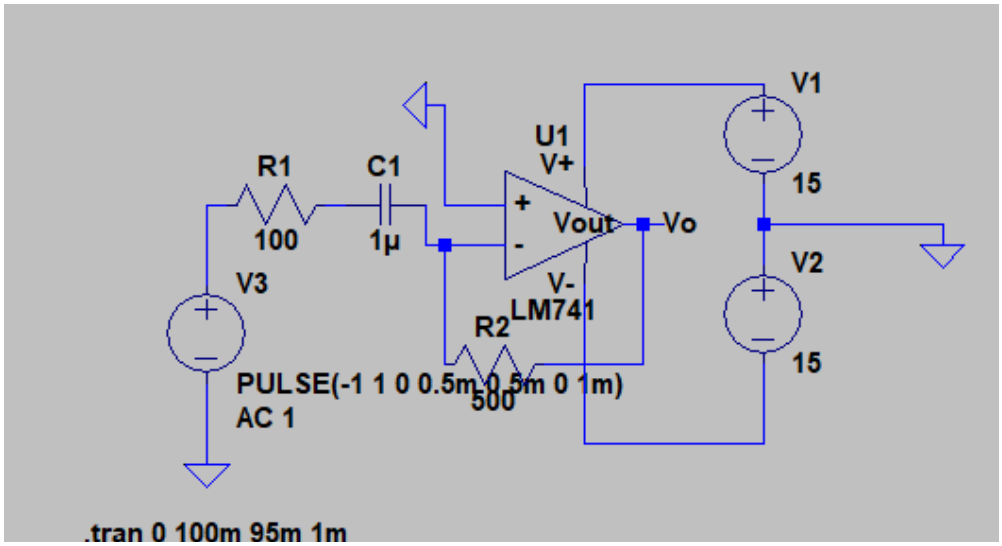


Clipping when gain is excess

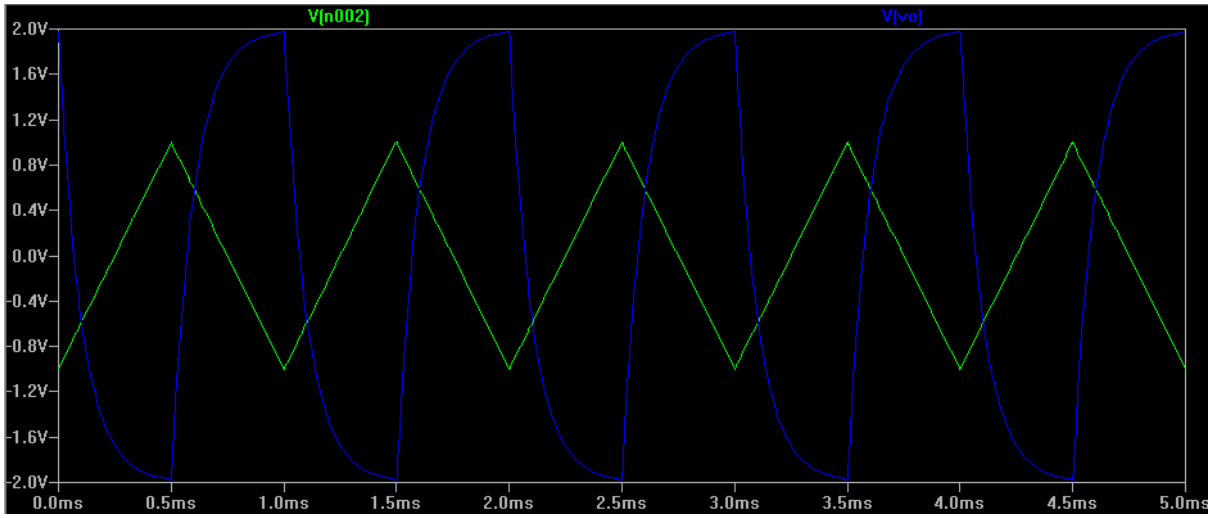


Positive clipping when Vcc+ is reduced

Differentiator Op-Amp: -



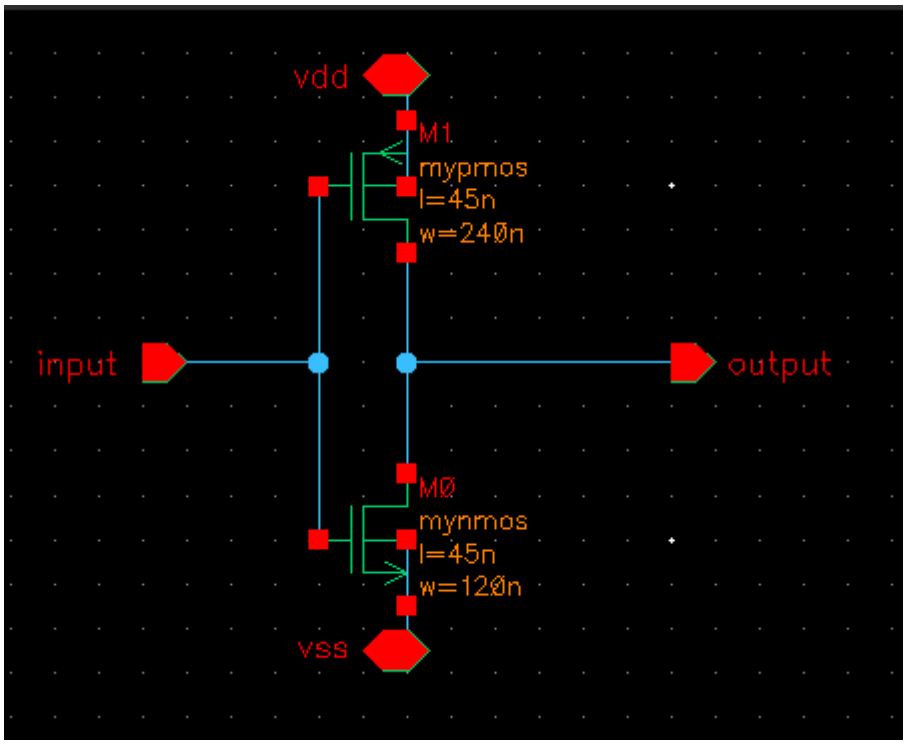
Differentiator Op-Amp Schematic



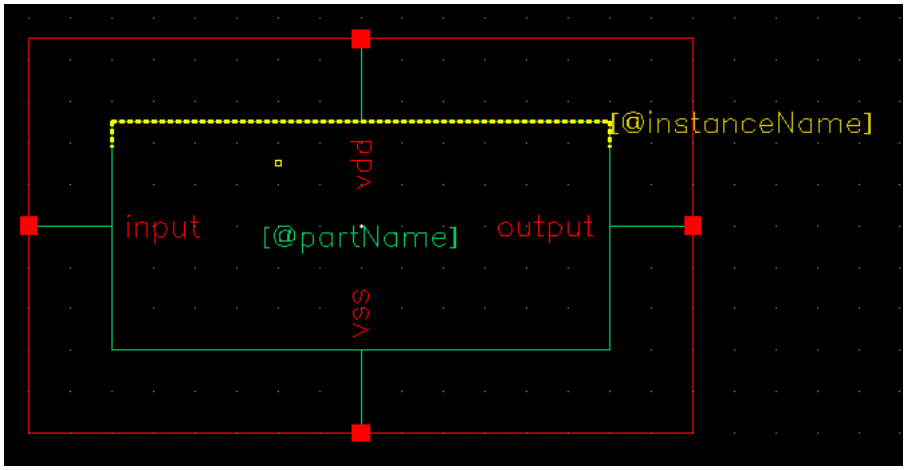
Waveform

CMOS Inverter: -

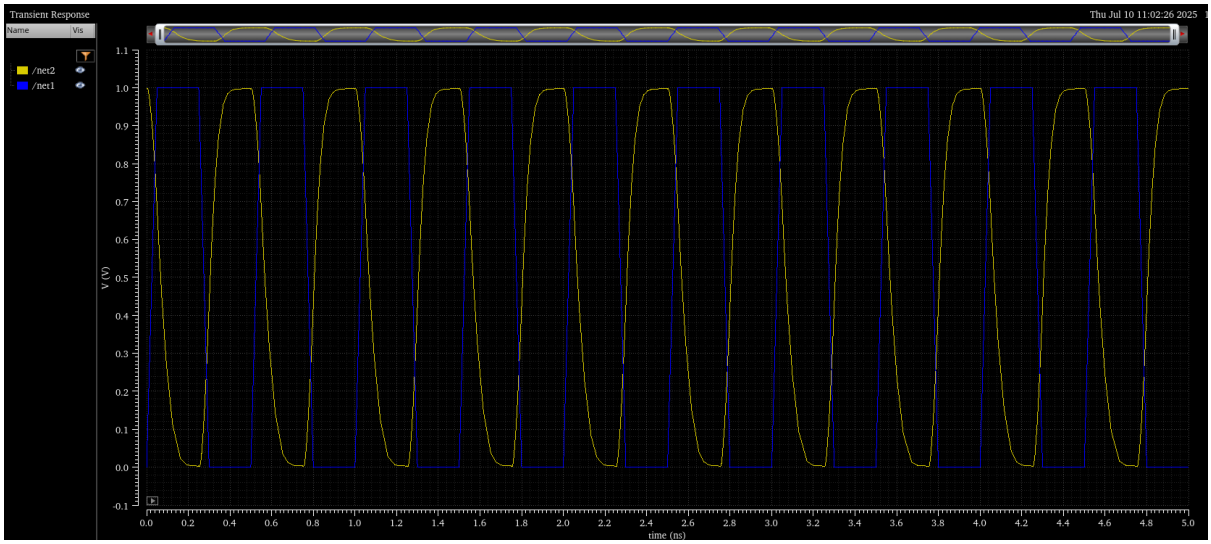
Schematic, symbol creation and choice of analyses shown for a cmos inverter.



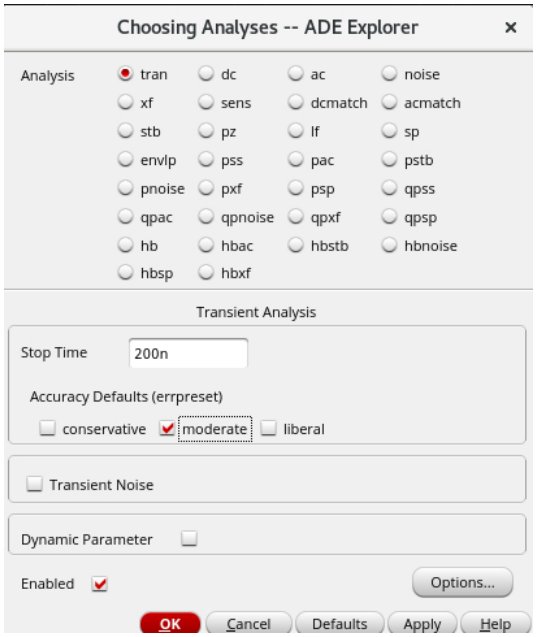
Schematic



Symbol created for the circuit using the pins marked

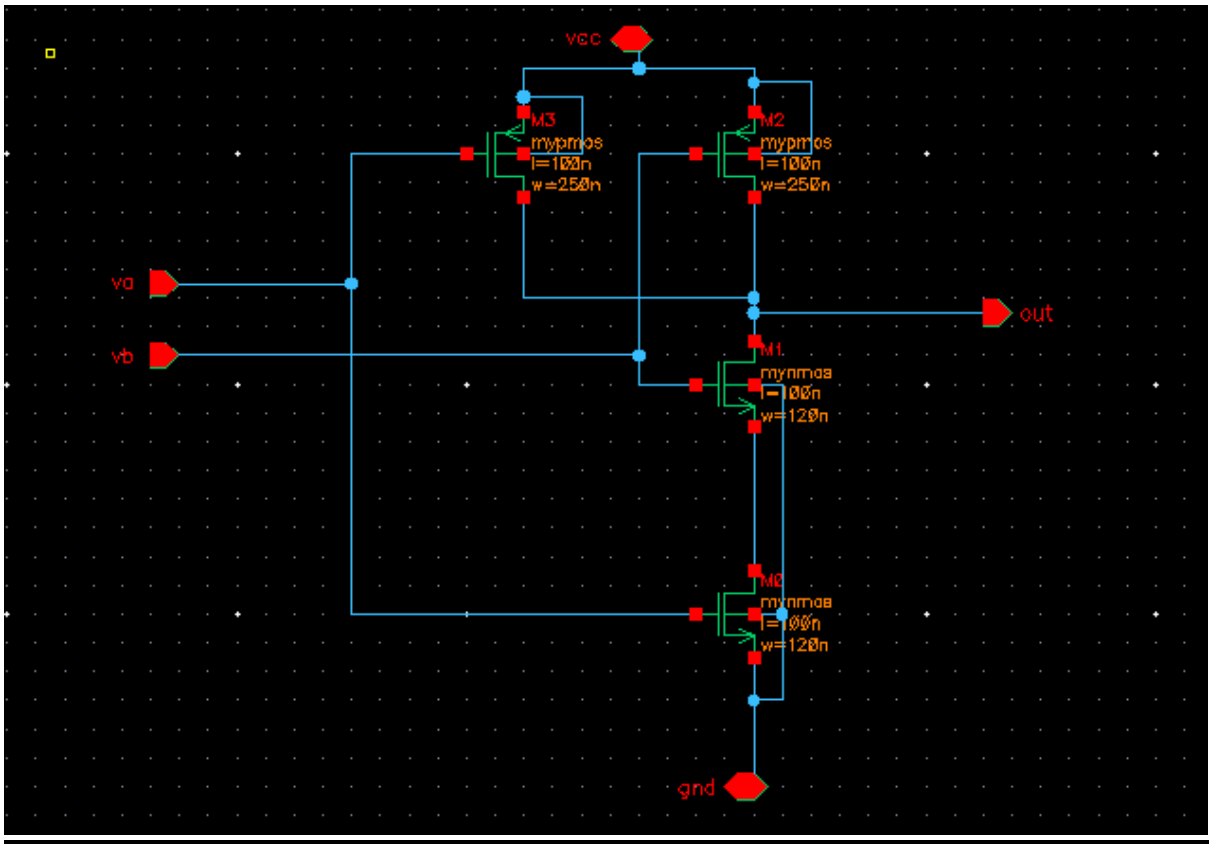


I/p vs O/p plot (transient response)

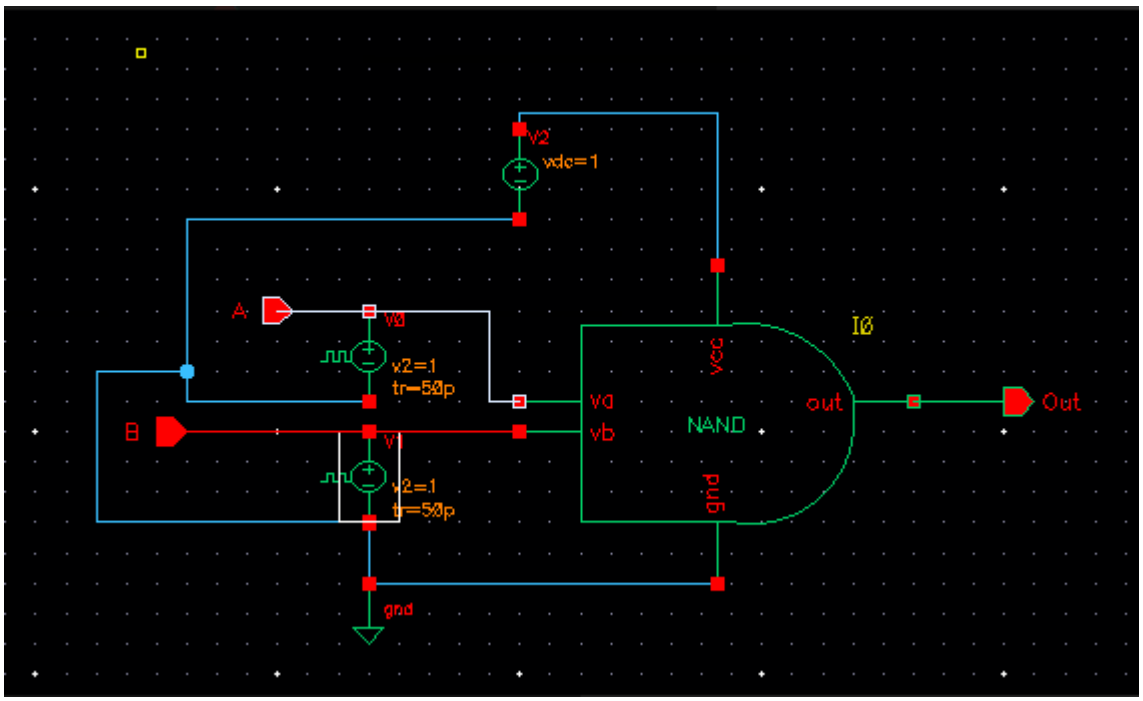


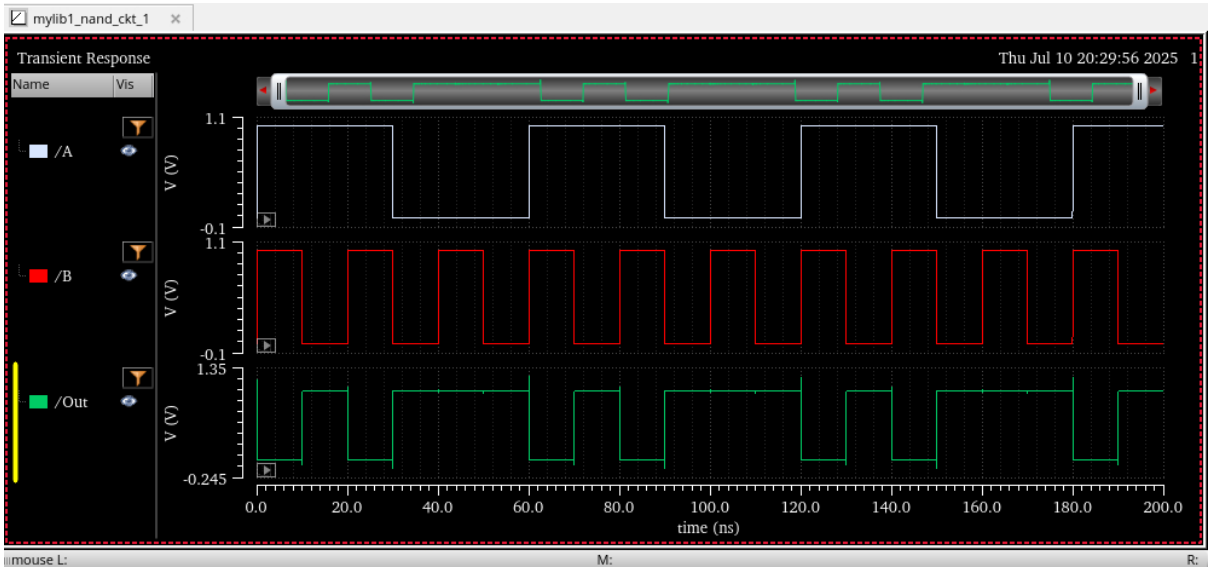
Analysis set-up

CMOS NAND Gate Implementation: -

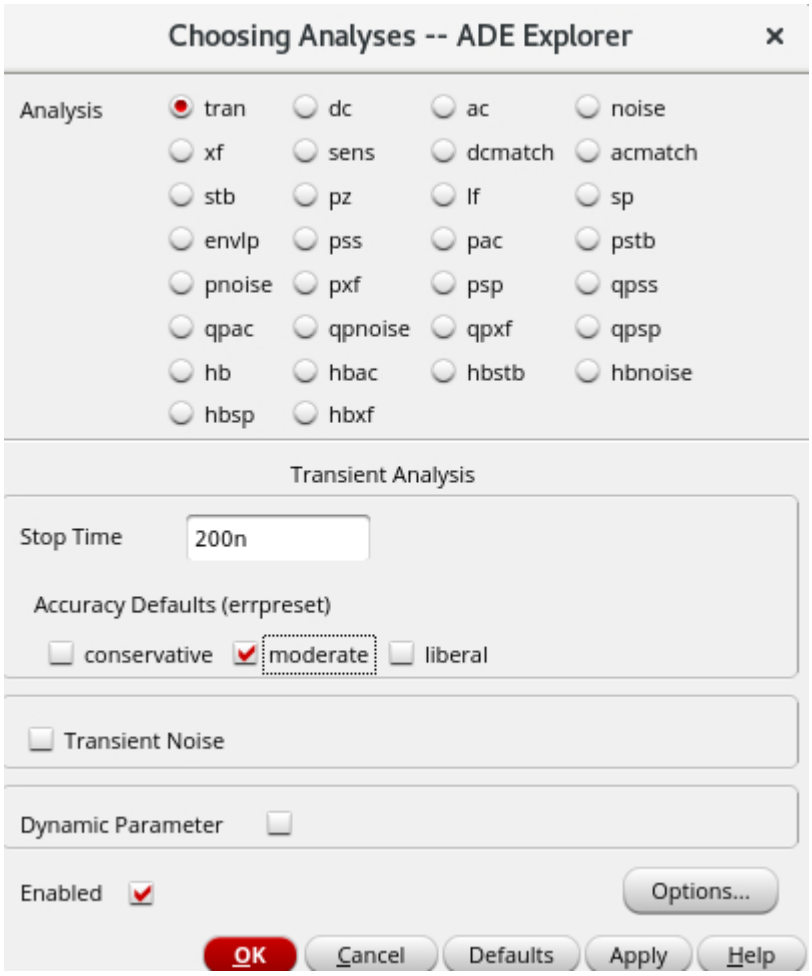


NAND Gate Schematic





Waveforms (top wave is o/p)



Analysis setup