List of Experiments

Digital Logic Design Laboratory

(Computer Engineering and Information Technology)

Experiment 1 : Study of digital kit and ICS

I. To familiarize digital IC trainer kit
II. To familiarize basic logic gates and universal gates ICs.

Experiment 2 : Boolean function using logic gates.

I. To study and verify the truth table of various logic gates (NOT, AND, OR, NAND, NOR, EX-OR, & EX-NOR).
II. To design circuit and verify truth table of Boolean function using gates.

Experiment 3 : Half Adder

I. To design and verify a half adder using S= (x+y)(x'+y') C= xy
II. To design and verify a half adder using S= xy'+x'y C= xy
III. To design and verify a half adder using S= (C+x'y')' C=xy
IV. To design and verify a half adder using S= (x+y)(x'+y') C= (x'+y')'
V. To design and verify a half adder using S = x EX-OR y C=xy

Experiment 4 : Full Adder

I. To design and verify a full adder using S = x'y'z+x'yz'+xy'z'+xyz C=xy+xz+yz
II. To design and verify a full adder using S = z X-OR(x EX-OR y) C=xy'z+x'yz+xy
III. To design and verify a full adder using full adder IC 7483.

Experiment 5 : Half Subtracter

I. To design and verify a half subtractor using D = x'y +xy' B=x'y.
II. To design and verify a half subtractor using D = x EX-OR y B=x'y.
III. To design and verify a full subtractor using D = x'y'z+x'yz'+xy'z'+xyz B=x'y+x'z+yz
IV. To design and verify a full subtractor using IC 7483.

Experiment 6 : Combinational Circiut, BCD, Number Converter etc.

I. Design a BCD to Excess 3 code converter using combinational circuits.
II. Design a BCD to decimal converter using combinational circuits.
III. Design a 3 bit binary to gray code converter using combinational circuits.
IV. Design a combinational circuit whose output is the 2's complement of the input number.

Experiment 7 : Multiplexer

I. To design and implement a 4:1 multiplexer.
II. To design and implement a 8:1 multiplexer
III. To design and implement a 16:1 multiplexer
IV. To design a multiplexer tree to implement 32:1 multiplexer using two 16:1 multiplexer.

Experiment 8 : Demultiplexer

I. To design and implement a 1:4 demultiplexer.
II. To design and implement a 1:8 demultiplexer.
III. To design and implement a 1:16 demultiplexer.
IV. To design and implement a 1:16 demultiplexer using two 1:8 demultiplexer.

Experiment 9 : Decoder

I. To design and verify a 2:4 decoder.
II. To design and verify a 3:8 decoder.
III. To design a BCD to decimal decoder.
IV. To design and verify a 4:16 decoder.
V. Implement a full adder circuit with a decoder

Experiment 10 : Encoder

I. To design and implement a 4:2 encoder.
II. To design and implement a 8:3 encoder.
III. To design and implement a decimal to BCD encoder.
IV. To design and implement a octal to binary encoder.

Experiment 11 : Flip-Flops

I. To design and verify the operation of RS flip-flops using logic gates.
II. To design and verify the operation of T flip-flops using logic gates
III. To design and verify the operation of D flip-flops using logic gates.
IV. To design and verify the operation of JK flip-flops using logic gates.

V. Experiment 12 : Counter

I. To verify the operation of asynchronous counter.
II. To verify the operation of a synchronous counter
III. To verify the operation of a decade counter.
IV. To design and implement the operation of a Mod-16 counter using JK flip-flops
V. To design and implement a Mod-10 counter using JK flip flops and logic gates.
VI. To verify the operation of a ring counter.
VII. Sequence generator.

Experiment 13 : Shift Register

I. To design and verify the operation of a 4-bit shift left register using D flip-flops.
II. To design and verify the operation of a 4-bit shift right register using D flip-flops.