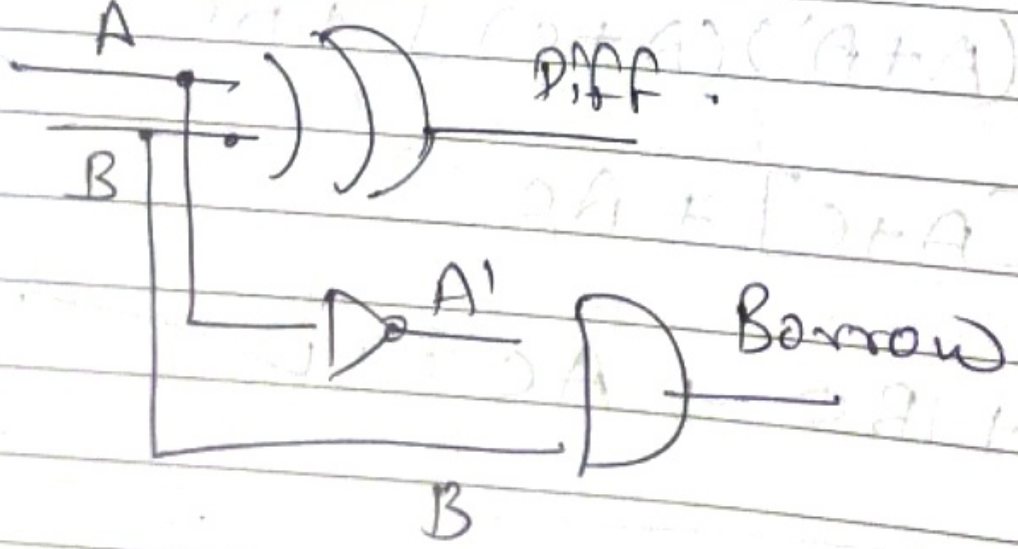
Half Subtractor.

A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$Diff = AB' + A'B$.

$Borrow = A'B$.



full Subtractor.

Date: YOUVA

A	B	C	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

C → Borrow from next stage.

Borrow

⇒ $0-0 = 0-0 = 0$

$0-0 = 0-1 = 1$ 1

$0-1 = 1-0 = 1$ 1

$0-1 = 1-1 = 0$ 1

$1-0 = \phi-0 = 1$ 0

$1-0 = 1-1 = 0$ 0

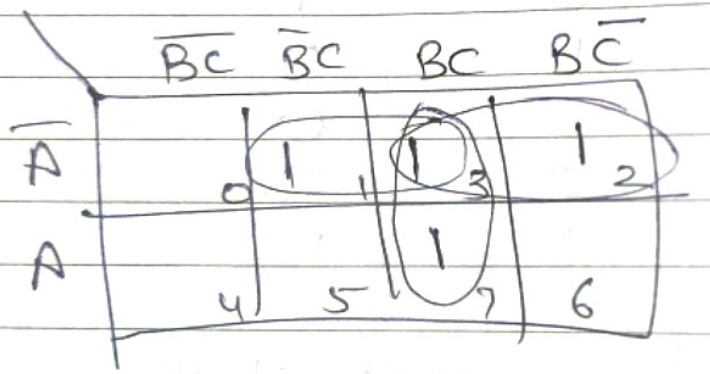
$1-1 = 0-0 = 0$ 0

$1-1 = 0-1 = 1$ 1

Diff = $\Sigma(1, 2, 4, 7)$

= Same as full Adder

Borrow = $\Sigma(1, 2, 3, 7)$



Borrow = $BC + \bar{A}C + \bar{A}B$.

* In full subtractor, in Borrow only one input A is inverted.

* All are same as full Adder.

Borrow = BC + A'C + A'B

* In full subtractor, in Borrow only one input A is inverted.

* All are same as full Adder.

$$\text{Borrow} = C[A \odot B) + A'B$$

$$= C[AB + A'B'] + A'B$$

$$= ABC + A'B'C + A'B$$

$$= A'[B'C + B] + ABC$$

$$A'[(B+B')(B+C)] + ABC$$

$= A'[B+C] + ABC$

$= A'B + A'C + ABC$

$= A'B + C[A' + AB]$

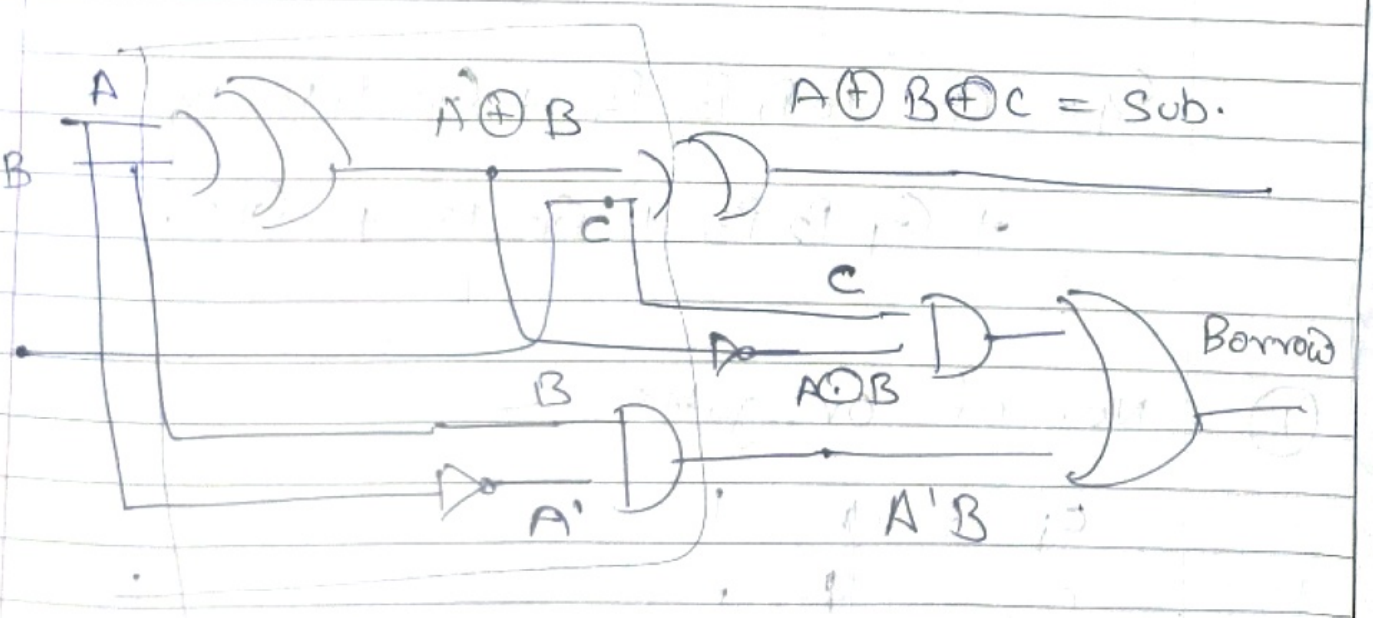
$= A'B + C[(A+A')(A'+B)]$

$= A'B + C[A'+B]$

$= A'B + A'C + BC$

$\Rightarrow$ Borrow $= A'B + A'C + BC = C[A \odot B] + A'B$

$= C[A \oplus B]' + A'B$



Q.1. Time complexity of n bit Adder (look ahead) is 3.

Assuming (n+1) input or and gates are available.

Ans. No. of stages = 4.

for Carry there are 3 stages.

4th stage only for Sum.

Ans. Time Comx = O(1).

$A_{n-1} \cdots A_2\ A_1\ A_0$

$B_{n-1} \quad B_2\ B_1\ B_0$

$S_{n-1} \cdots S_2\ S_1\ S_0$

. . . . 4 stage 4 stag 4 stages

$\Rightarrow$ O(1) — constant.

Q. Amount of time needed to generate sum & carry of look ahead carry adder if delay xor And OR

50 10 20 nsec.

regardless of no. of i/p to these gates.

Ans. n bit look ahead adder →

C_n → (n+1) input ~~OR~~ & gate

(n+1) input or gate.

for S_n → C_n → (n+1) input And gate.

~~—11—~~ ~~or gate~~

S_1 → xor, And. } To generate G_i^0 P_i^0

50

S_2 → And } 10 → 50+10 = 60

S_3 → or } 20 → 80 sec.

Total time for Carry = 80 nsec.

M T W T F S S

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Date:

Time to generate sum → 80 + 50

= 130 nsec.

S_1 → xor 50 } — 50nsec.
And 10 }

S_2 → And → 10 nsec.

S_3 → 20 / OR gate → 20nsec.

---

for Carry = 80 nsec.

for sum ⇒ 4 stages

= 80 sec. + 50 sec.
xor

= 130 nsec.

A 4 bit Carry Look Ahead (CLA) adder can be constructed with the help of following steps (Assuming T as the delay of a single 2-Input gate):

1. Generate All P and G internal signals. These can be generated simultaneously as C0 and all inputs are available.
2. Generate all carry output signals (C1, C2, C3, C4). These will be valid after 3T time
3. Generate Sum signals S = P xor C. It will be valid after 4T time.

Thus, Sum signals will be valid after a delay of 4T. On the other hand, delay expression in case of ripple carry adder = (2n+2)T. Thus, for n =4, i.e. for 4 bit ripple carry adder, delay will be 10T.

Q. Amount of time to generate Sum, Carry by 4 bit Carry look ahead

Xor And OR

$5n$ $2n$ n

$n \rightarrow$ no of inputs.

5 input And

Ans. $C_4 = C_0 P_0 P_1 P_2 P_3 + G_0 P_1 P_2 P_3 + G_1 P_2 P_3 + G_2 P_3 + G_3$

Max. 5 input And gate.

~~Max. or gate → 4 input~~

3 stages for Carry →

S_1 → Xor $5n \rightarrow 5 \times 2 = 10$

And $2n$

S_2 → 5 input And gate = $2 \times 5 = 10$

$C_0 P_0 P_1 P_2 P_3$.

S_3 → or gate → 5 input. = 5

Total = 25.

for Carry.