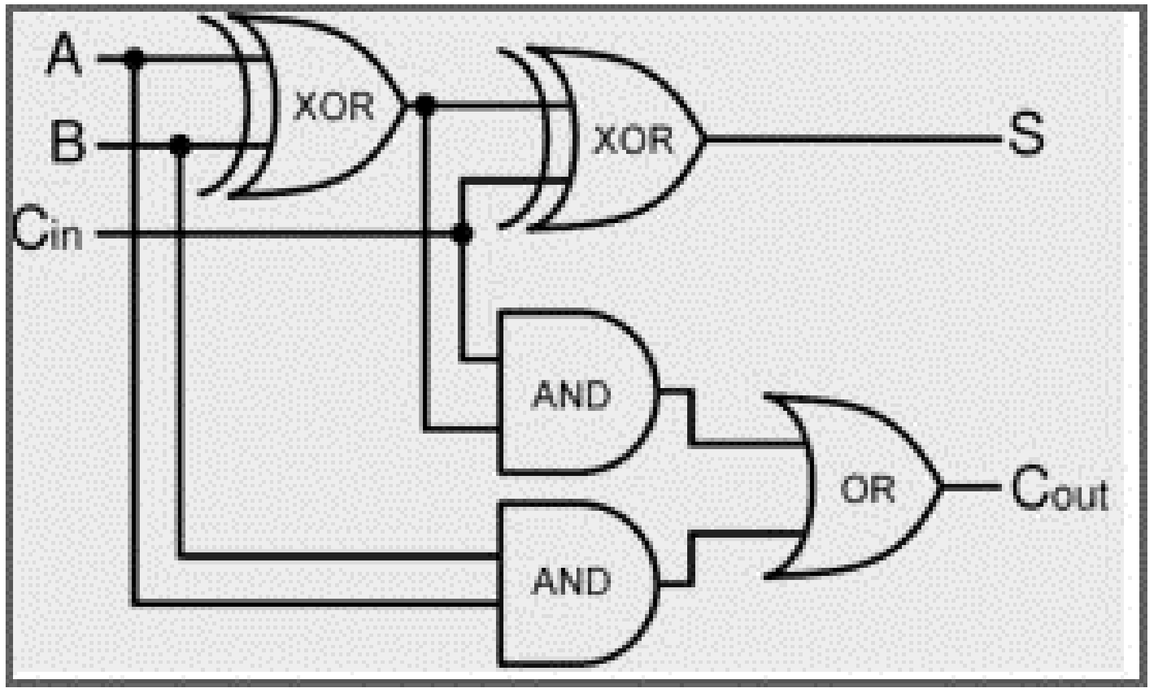
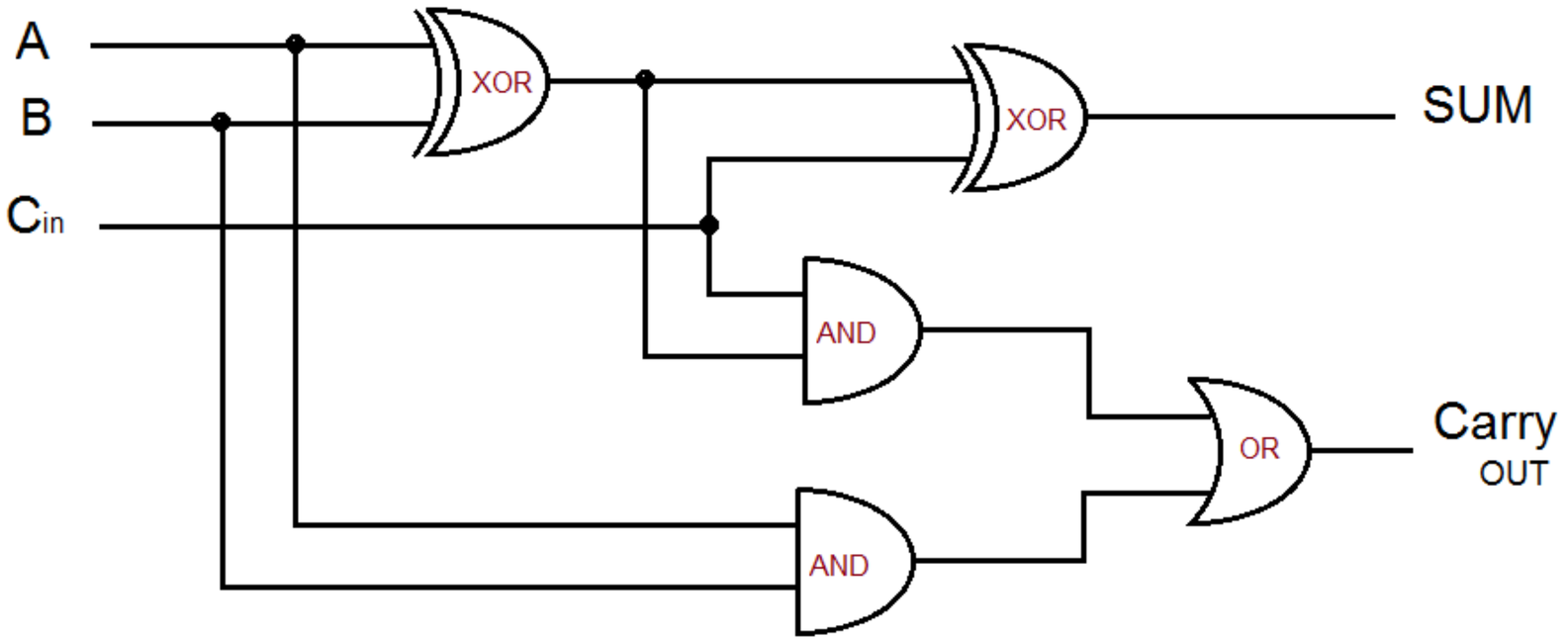
FULL ADDER . WAY 1



sum = A XOR B XOR Cin

carry out = AB +BC+CA

FULL ADDER : WAY 2



S = a ⊕ b⊕Cin.

Cout = (a*b) + (Cin*(a⊕b)).

NOTE : IF X OR GATE IS IMPLEMENTED USING NAND GATE .
4 NAND GATES ARE USED

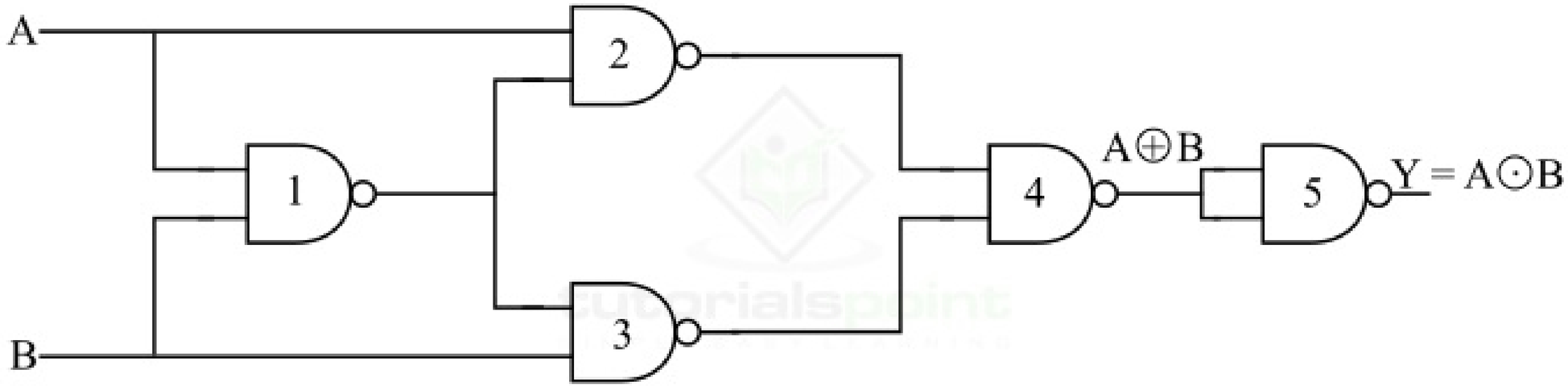
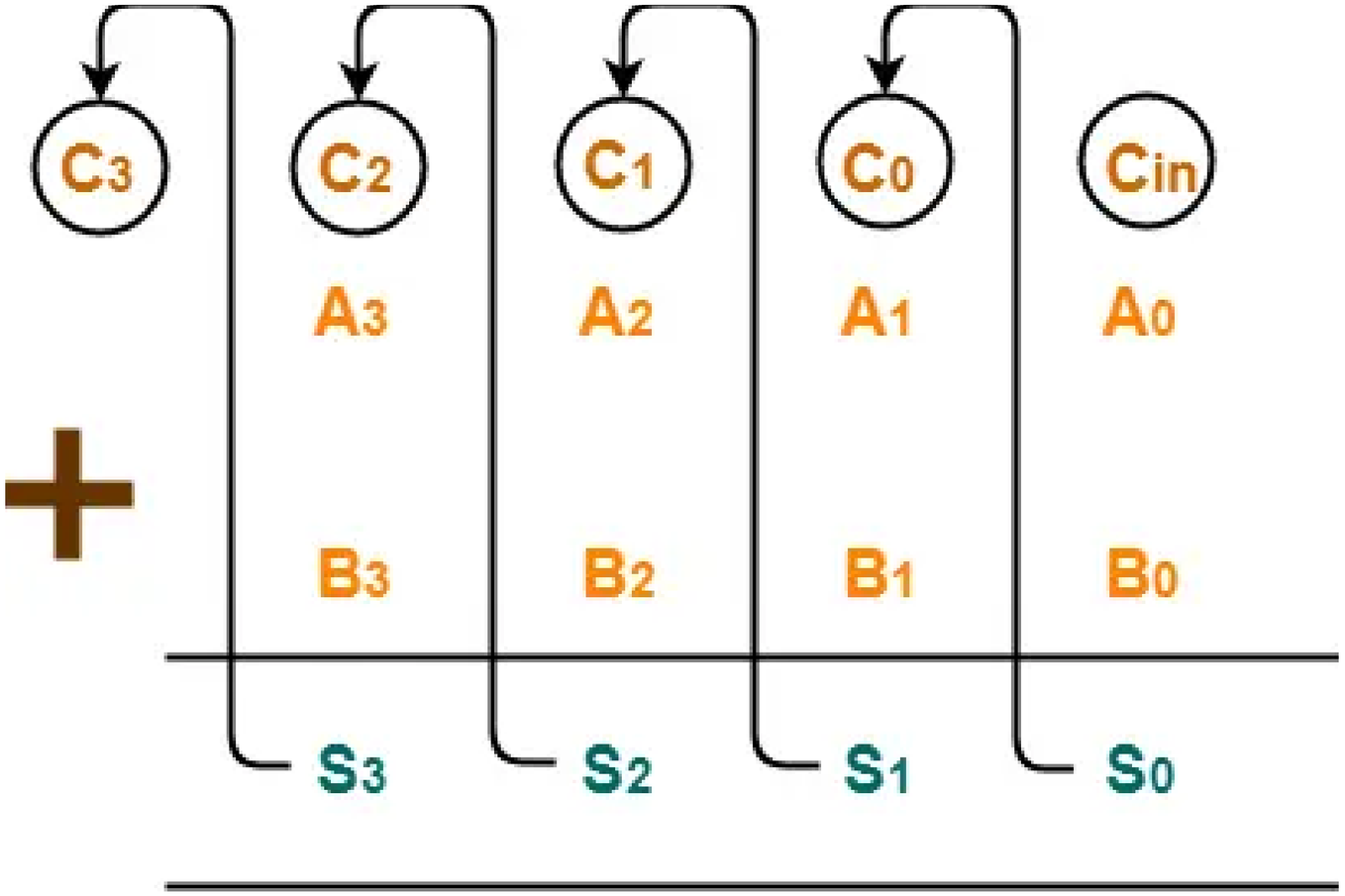
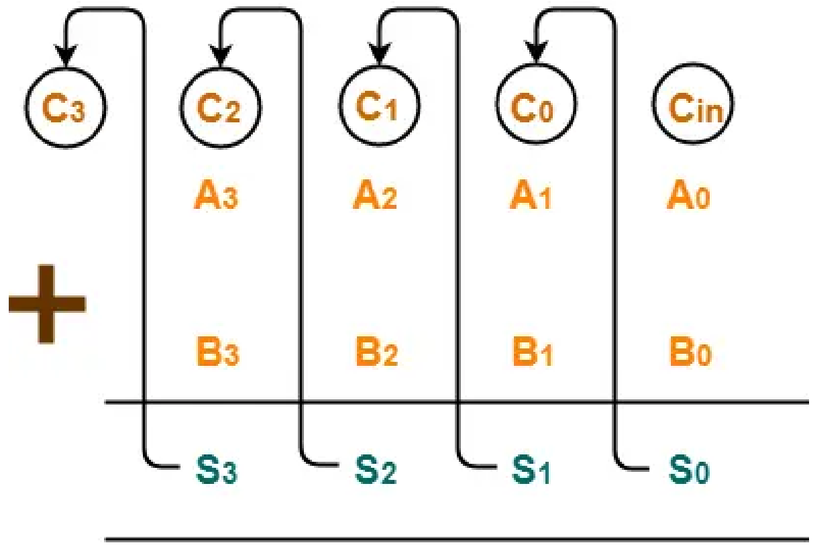


Figure 3 - XNOR Gate using NAND Gates

PARALLEL ADDER/ RIPPLE CARRY ADDER



Adding two 4-bit Numbers



Adding two 4-bit Numbers

S1 = A XOR B1 XOR C0

S2= A2 XOR B2 XOR C1

S3 = A3 XOR B3 XOR C2

S4= A4 XOR B4 XOR C3

C0 = INITIAL CARRY

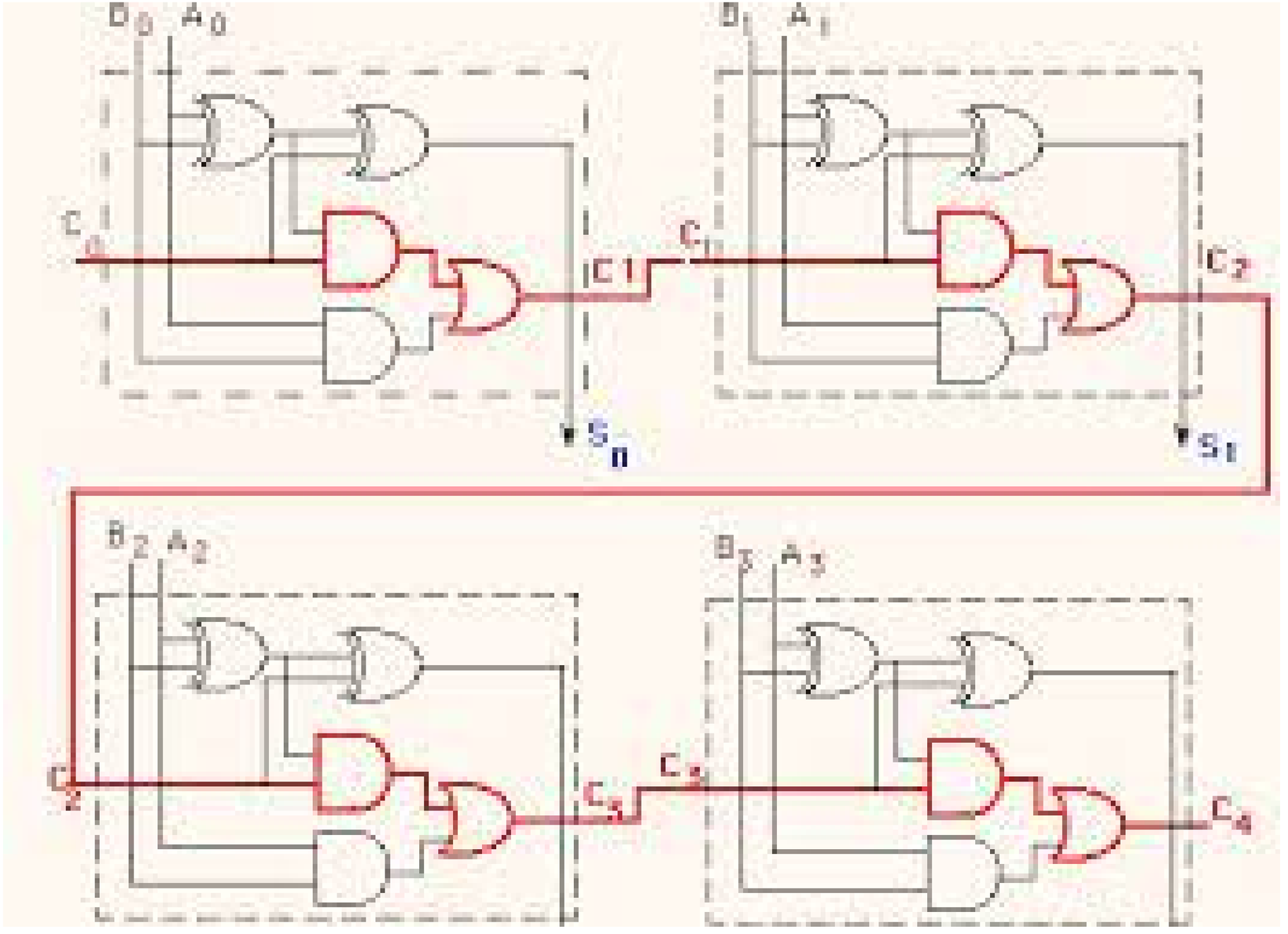
C1= A1 XOR B1)C0+ A1B1

C2 = A2 XOR B2) C1 + A2B2

C3 = A3 XOR B3) C2 + A3B3

SUM AT ONE STAGE DEPENDS ON CARRY OF PREVIOUS STAGE

CARRY AT ONE STAGE DEPENDS ON CARRY OF PREVIOUS STAGE


B0
A0
C0
C1
S0
B1
A1
C2
S1
B2
A2
C3
B3
A3
C4

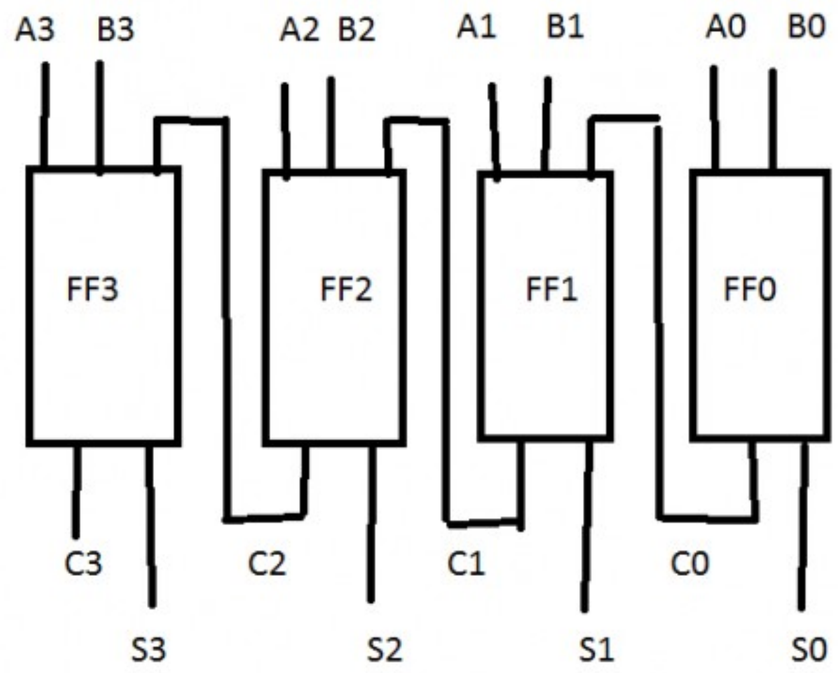
Half Adder is implemented with XOR and AND gate. A. FA is implemented with 2 HA and 1 OR gate The propagation delay of XOR -gate is twice that of AND / OR gate. Propagation delay of AND/OR is 1.2 ms. A 4-bit ripple carry binary adder is implemented using 4 full adder. the total propagation time of this 4 bit binary adder in micro second is _____?

CARRY TIME = 2.4 +1.2+1.2 = 4.8

CARRY TIME FOR 4 FULL ADDER = 4.8*4= 19.2

SUM TIME FOR 4TH ADDER = 3 * CARRY TIME FOR ADDER + SUM TIME AT 4TH TIME =4.8)*3 + 4.8=19.2

A one bit full adder takes 75 nsec to produce sum and 50 nsec to produce carry.A 4 bit parallel adder is designed using this type of full adder. The maximum rate of additions per second can be provided by 4 bit parallel adder.....?



Time (ns) Action Performed
0 ff0 start working
50 ff0 generate carry for ff1, thus ff1 start working
100 ff1 generate carry for ff2, thus ff2 start working
150 ff2 generate carry for ff3, thus ff3 start working
225 ff3 generate the final result.

Calculation Part:-

1 addition ---- 225ns

1/(225 * 10^-9) -------- 1 second

4.44 * 10 ^6 addition ------- 1 second

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit-ripple-carry binary adder is implemented by using four full adders. The total propagation time of this 4 -bit binary adder in microseconds is _____.

- In Ripple carry adder, a stage doesn't wait for the "full output" of previous stage. It only waits for the previous stage's carry to reach to itself. Now, carry generated by our current stage can be written in 2 ways:-

- 1. CARRY = AB+BC+CA ..... 3 AND in parallel + 1 or gate = 1.2+1.2 =2.4
- 2. CARRY+1 = (A XOR B)Ci + AB ..... 2.4 +1.2 + 1.2 = 4.8

  - Using 2nd way, delay in carry generation would be 4.8 nsec and by using 1st way, delay in carry generation would be 2.4nsec

So, answer should be according to 2.4 delay(better than 4.8 delay).

total delay = (4-1) 2.4 + 4.8 = 12 nsec

CARRY LOOK AHEAD

P = A XOR B

G = AB

Ci+1 = Gi+PiCi

SUM i = Pi XOR Ci

STAGE 1 _: PI AND GI CALCULATIONS
IN PARALLEL

STAGE 2 : carry generation using AND OR GATE

1. AND GATE
2. OR GATE

STAGE 3 “ SUM GENERATION USING X OR GATE

$$C1 = G0 + P0 \cdot C0$$

(1 AND GATE , 1 OR GATE WITH 2 INPUT)

$$C2 = G1 + P1 \cdot C1 = \quad G1 + P1 \cdot G0 + P1 \cdot P0 \cdot C0$$

(2 AND GATE , 1 OR GATE WITH 3 INPUT)

$$C3 = G2 + P2 \cdot C2 = \quad G2 + P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot P0 \cdot C0$$

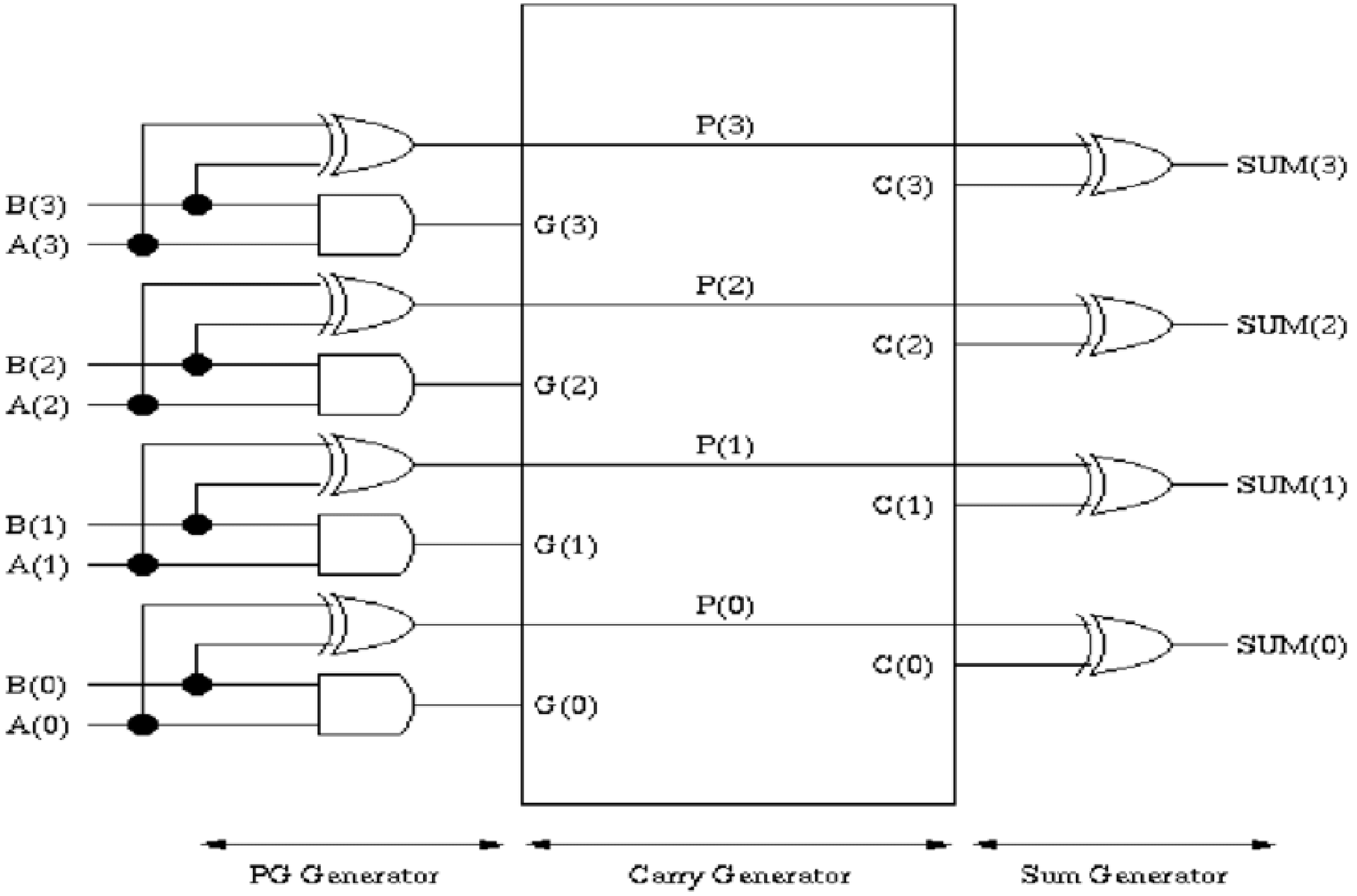
(3 AND GATE , 1 OR GATE WITH 4 INPUT)

$$C4 = G3 + P3 \cdot C3 = G3 + P3 \cdot G2 + P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0 + P3 \cdot P2 \cdot P1 \cdot P0 \cdot C0$$

(4 AND GATE , 1 OR GATE WITH 5 INPUT)

TOTAL And gates = N(N+1)/2

TOTAL OR GATES = N


B(3)
A(3)
B(2)
A(2)
B(1)
A(1)
B(0)
A(0)
P(3)
G(3)
P(2)
G(2)
P(1)
G(1)
P(0)
G(0)
C(3)
C(2)
C(1)
C(0)
SUM(3)
SUM(2)
SUM(1)
SUM(0)
PG Generator
Carry Generator
Sum Generator

A 4-bit carry look ahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the delay of each gate is one time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.

4 time units
6 time units
10 time units
12 time units

answer : 6 time units

In a 4 bit carry look ahead adder, the propagation delay of EX-OR gate is 20 NSEC, AND and OR gates is 10nsec. The sum and carry output of full adder takes 20nsec and 10nsec respectively. The total propagation delay of the above adder in is ?

solution : 20ns (External Ex-OR GATE) + 10ns (Internal AND GATE) + 10ns (Next level OR GATE + 20ns (External Ex_OR GATE)

Total : 20ns + 10ns + 10ns + 20ns = 60ns

4 stages ;

1 STAGE : Gi = AiBi, Pi = Ai xor Bi.... gi and pi in parallel ... 20 NSEC

2 AND 3RD STAGE : c4 generate using OR AND GATE .....10+10 NSEC..

STAGE 4 : SUM GENERATE: Pi xor Ci ....20 nsec