

Sky130 Day-1

to 5

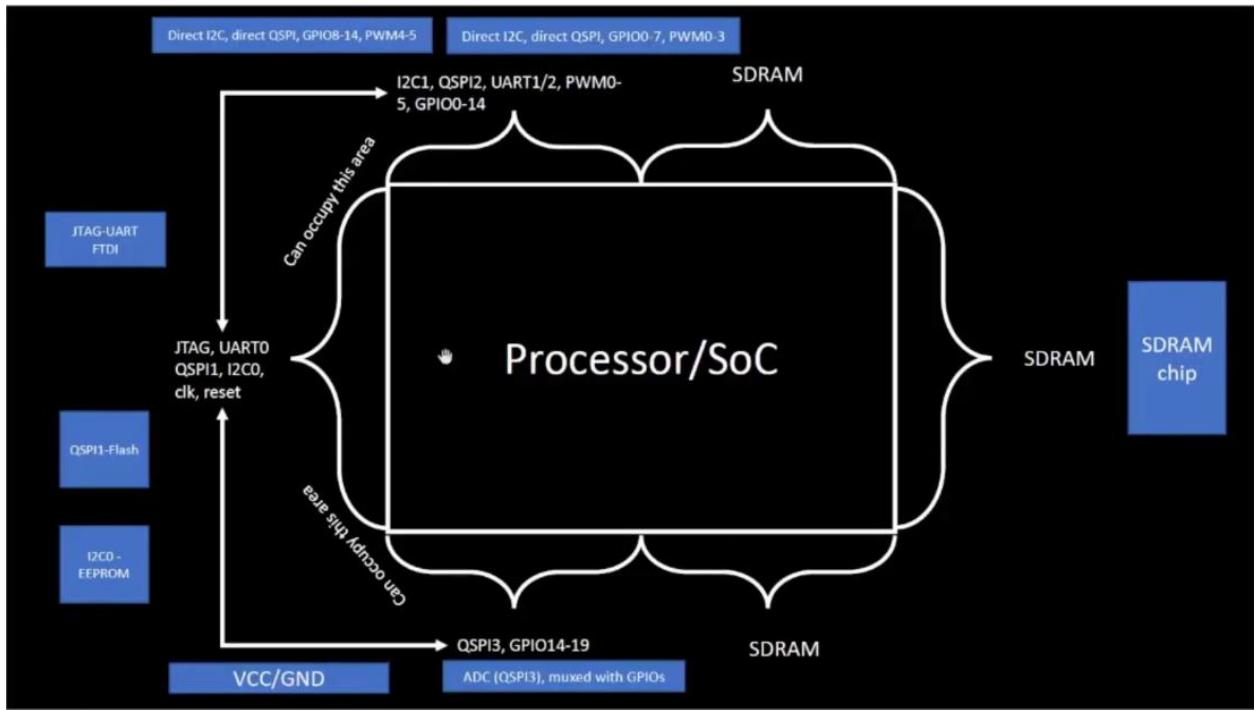
Inception of open-
source EDA, OpenLANE
and Sky130 PDK

Brief Introduction:-



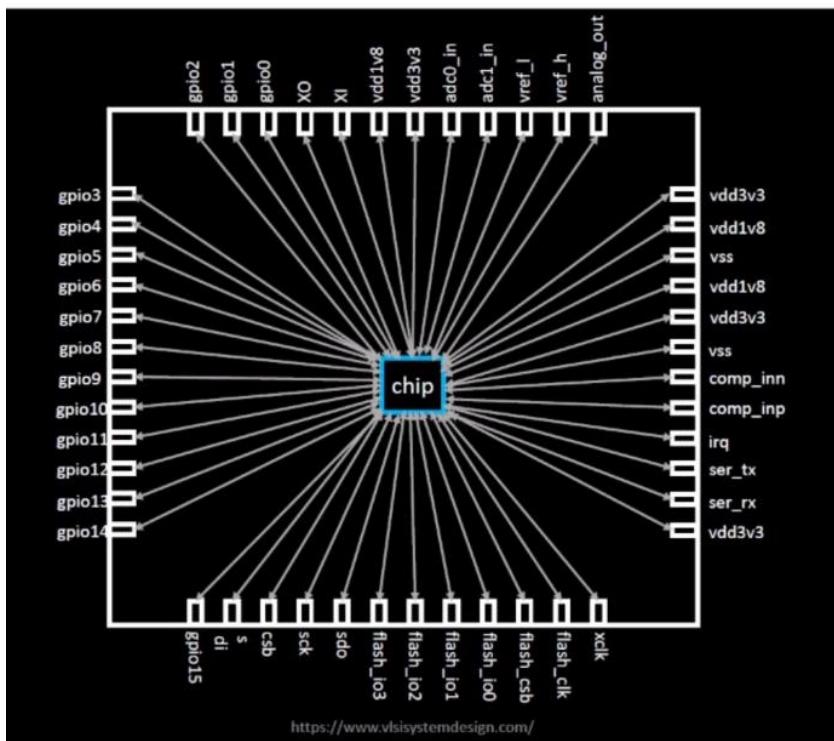
(Image credits:- VSDIAT)

This is an Arduino Board which is a type of "Leonardo". We are mentioning this to you because we will work on a similar project. The industry lying inside the encircled area is the "Chip". Our main focus is to develop a Chip in this Advanced Physical Designing Program (level-3).



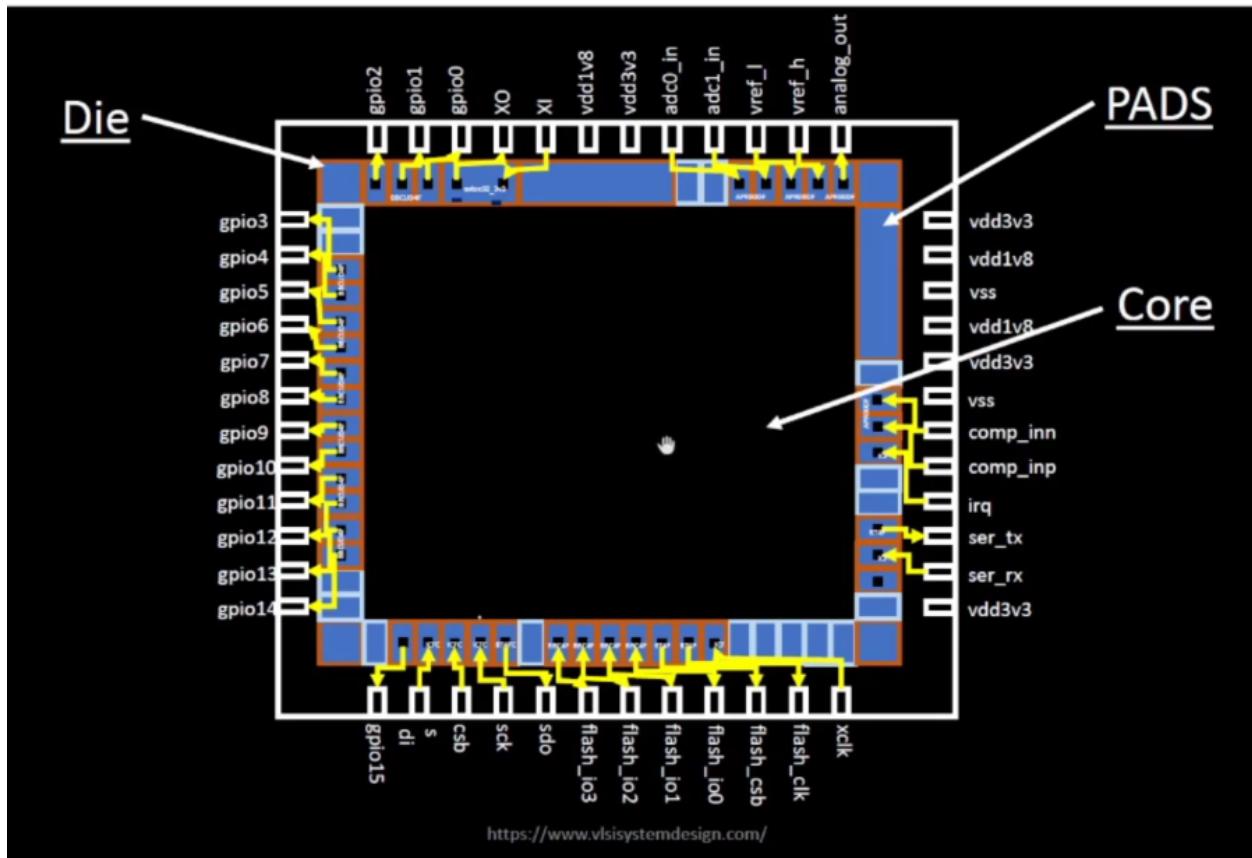
(Image credits:- VSDIAT)

A Block diagram of a processor.



(Image credits:- VSDIAT)

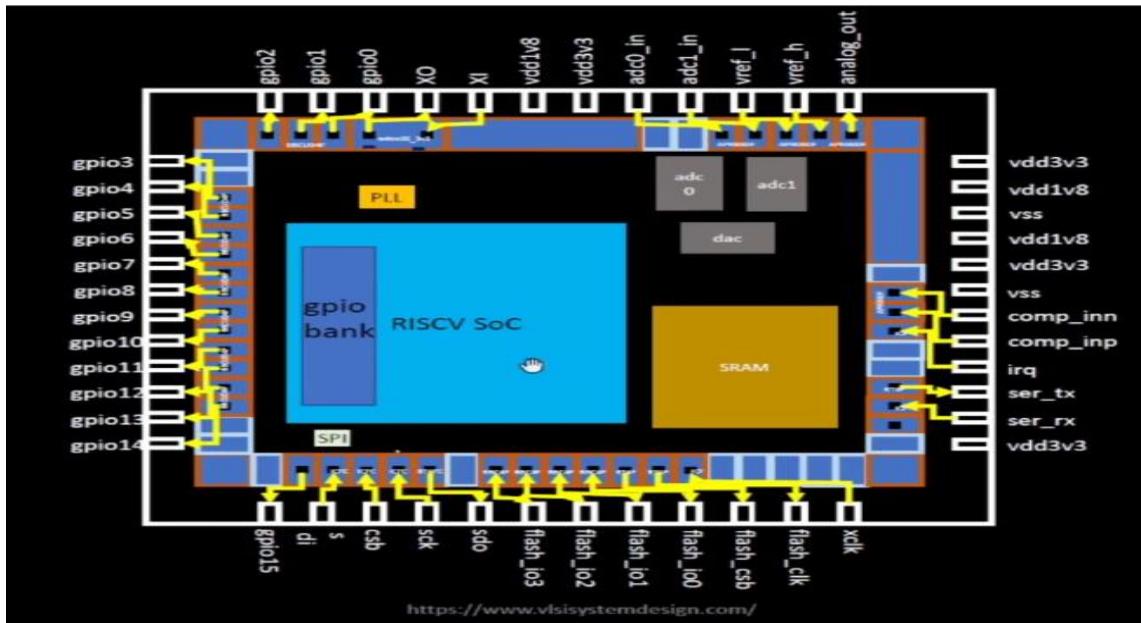
Chip inside the Package known as “QFN-48” with
connected to pins through wire bonds.



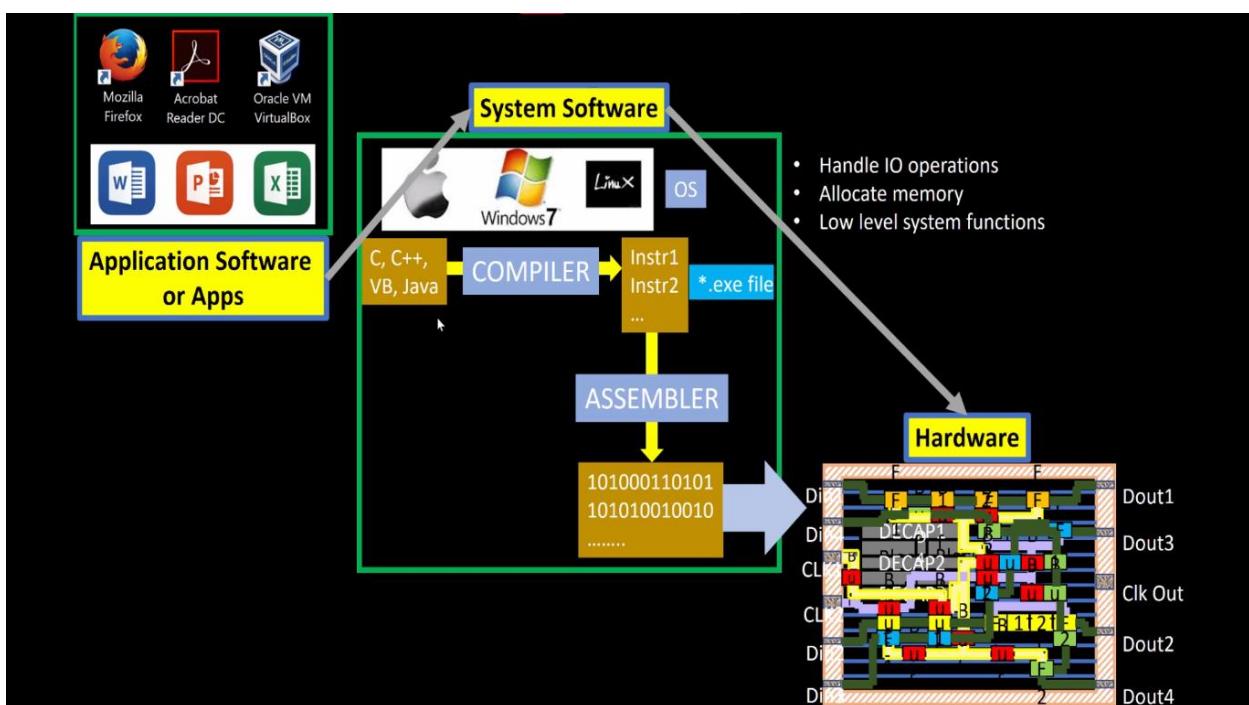
(Image credits:- VSDIAT)

Structure and components of a Chip. “Pads” are like doors of the Chip which allows or disallows signals to go inside or outside the Chip. “Core” is the main part of the Chip where all the logic gates and instructions are kept. Processing is done in the Core. “Die” is the Area or

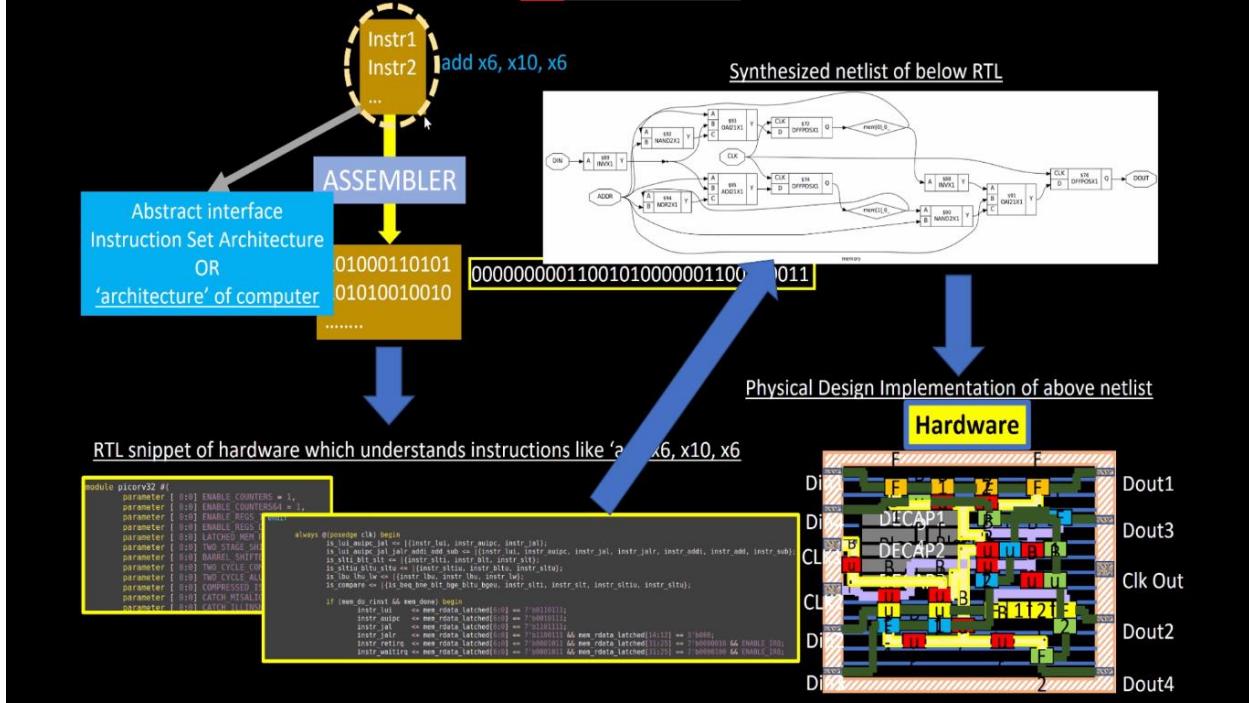
Boundary of the Chip. Basically, Die is the group of Pads and thus form an Area.



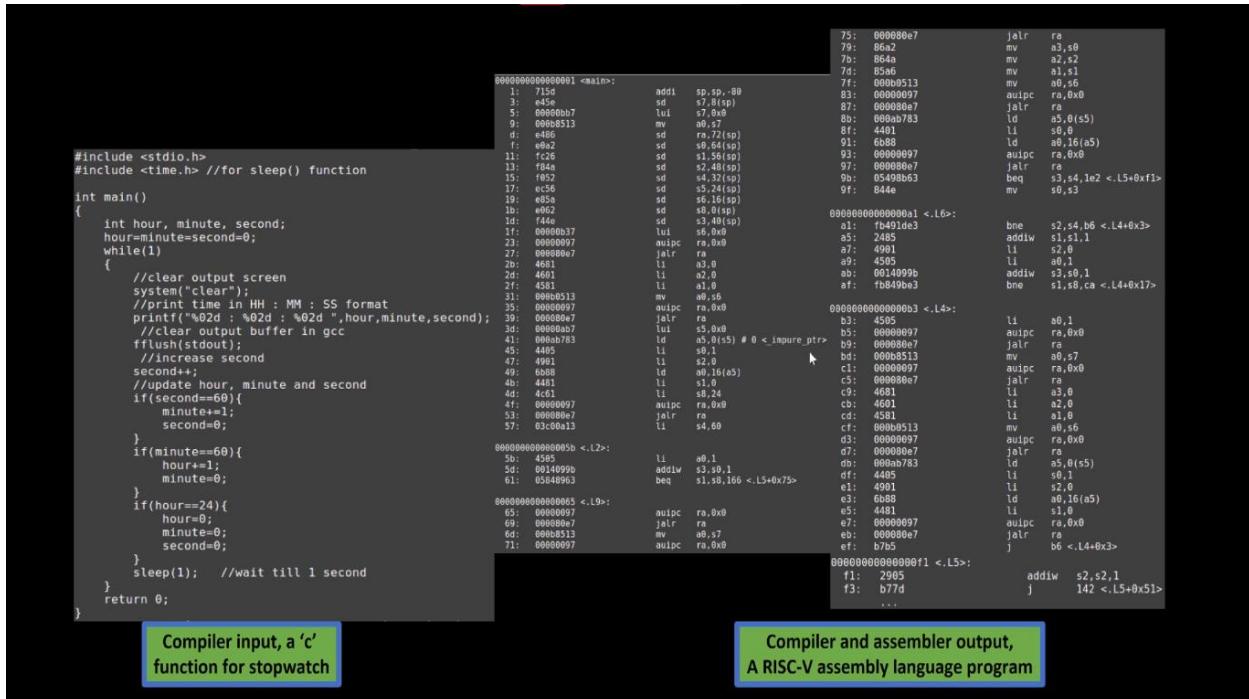
(Image credits:- VSDIAT)



(Image credits:- VSDIAT)



(Image credits:- VSDIAT)



(Image credits:- VSDIAT)

```

kunal@kunal-VirtualBox ~$ cd Desktop/tools/riscv_sim/riscv-tools
kunal@kunal-VirtualBox ~$ cat swap.c
#include <stdio.h>
swap (size_t my[], size_t s)
{
    size_t temp;
    temp = my[s];
    my[s] = my[s+1];
    my[s+1] = temp;
}

kunal@kunal-VirtualBox ~$ riscv64-unknown-elf-objdump -d swap.o
swap.o: file format elf64-littleriscv

Disassembly of section .text:
0000000000000000 <swap>:
 1: 7170      addi    sp,sp,-48
 3: f422      sd      $0,40(sp)
 5: 1800      addi    $0,sp,48
 7: f424      addi    $0,-48($0)
 9: fd43c23   sd      $1,-48($0)
10: fd43c23   sd      $1,-48($0)
11: fd043703   ld      $5,-48($0)
13: 078e      slli    $5,$5,6x3
15: fd043703   addi    $4,-40($0)
19: 078d      addi    $5,$5,4
1b: 639c      ld      $5,0($5)
1d: fd43c23   sd      $5,-24($0)
21: fd043703   ld      $5,-48($0)
25: 0785      addi    $5,$5,1
27: 078d      slli    $5,$5,6x3
29: fd043703   ld      $4,-40($0)
2a: 077a      addi    $4,$4,x5

```

RISC-V Architecture

Implementation (picorv32 cpu core)

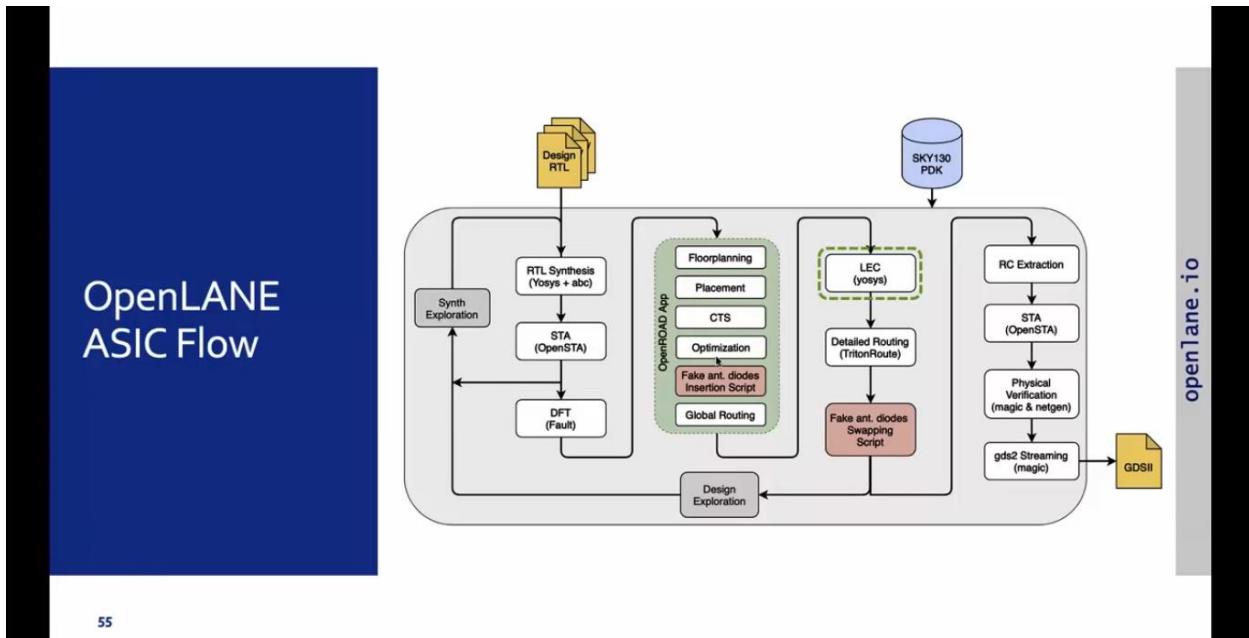
```

module picorv32 #(
  parameter [ 0:0] ENABLE_COUNTERS = 1,
  parameter [ 0:0] ENABLE_COUNTERS64 = 1,
  parameter [ 0:0] ENABLE_REGS = 1,
  parameter [ 0:0] LATCHED_MEM_R = 1,
  parameter [ 0:0] TWO_STAGE_SH = 1,
  parameter [ 0:0] BARREL_SHIFTER = 1,
  parameter [ 0:0] TWO_CYCLE_COP = 1,
  parameter [ 0:0] TWO_CYCLE_ALU = 1,
  parameter [ 0:0] COMPRESSED_IS = 1,
  parameter [ 0:0] CATCH_MISALIG = 1,
  parameter [ 0:0] CATCH_TIL_ITNS = 1
);
  ...
  always @ (posedge clk) begin
    is_lui_auipc_jal <= |(instr_lui, instr_auipc, instr_jal);
    is_lui_auipc_jal_jalr_addi_sub <= |(instr_lui, instr_auipc, instr_jalr, instr_addi, instr_sub);
    is_stl_blt_stt <= |(instr_stl, instr_blt, instr_stt);
    is_sttu_bitu_sttu <= |(instr_sttu, instr_bitu, instr_sttu);
    is_lbu_lhu_lw <= |(instr_lbu, instr_lhu, instr_lw);
    is_compare <= |(is_beq_bne_bit_bge_bitu, instr_stlti, instr_stlt, instr_stltiu, instr_stltu);

    if (mem_do_rinst && mem_done) begin
      instr_rdata <- mem_rdata_latched[6:0] == 7'b0110111;
      instr_auipc <- mem_rdata_latched[6:0] == 7'b1101111;
      instr_jal <- mem_rdata_latched[6:0] == 7'b1100111;
      instr_jalr <- mem_rdata_latched[6:0] == 7'b1100111 && mem_rdata_latched[14:12] == 3'b000;
      instr_retiq <- mem_rdata_latched[6:0] == 7'b0001011 && mem_rdata_latched[31:25] == 7'b0000010 && ENABLE_IRO;
      instr_waitirq <- mem_rdata_latched[6:0] == 7'b0001011 && mem_rdata_latched[31:25] == 7'b0000100 && ENABLE_IRO;
    end
  end
endmodule

```

(Image credits:- VSDIAT)



(Image credits:- VSDIAT)



(Image credits:- AUTHOR)

```
vsduser@vsdsquadron:~$ cd Desktop
vsduser@vsdsquadron:~/Desktop$ cd work/tools
vsduser@vsdsquadron:~/Desktop/work/tools$ ls -ltr
total 8
drwxrwxr-x 7 vsduser docker 4096 Jun 28 2021 vsdflow
drwxrwxrwx 5 vsduser docker 4096 Jun 29 2021 openlane_working_dir
vsduser@vsdsquadron:~/Desktop/work/tools$ cd openlane_working_dir
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ ls -ltr
total 12
drwxr-xr-x 5 vsduser docker 4096 Jun 28 2021 pdks
drwxr-xr-x 10 vsduser docker 4096 Jun 29 2021 openlane_old
drwxr-xr-x 10 vsduser docker 4096 May 20 2023 openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ cd pdks
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks$ ls -ltr
total 12
drwxr-xr-x 9 vsduser docker 4096 Jun 28 2021 skywater-pdk
drwxr-xr-x 8 vsduser docker 4096 Jun 28 2021 open_pdk
drwxr-xr-x 5 vsduser docker 4096 Jun 28 2021 sky130A
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks$ cd sky130A
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A$ ls -ltr
total 12
drwxr-xr-x 11 vsduser docker 4096 Jun 28 2021 libs.tech
drwxr-xr-x 14 vsduser docker 4096 Jun 28 2021 libs.ref
-rw xr-xr-x 1 vsduser docker 170 Jun 28 2021 SOURCES
```

(Image credits:- AUTHOR)

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdkssky130A/libs.ref$ cd sky130_fd_sc_hd
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdkssky130A/libs.ref/sky130_fd_sc_hd$ ls -ltr
total 88
drwxr-xr-x 2 vsduser docker 4096 Jun 28 2021 verilog
drwxr-xr-x 2 vsduser docker 4096 Jun 28 2021 techlef
drwxr-xr-x 2 vsduser docker 4096 Jun 28 2021 spice
drwxr-xr-x 2 vsduser docker 28672 Jun 28 2021 maglef
drwxr-xr-x 2 vsduser docker 28672 Jun 28 2021 mag
drwxr-xr-x 2 vsduser docker 4096 Jun 28 2021 lib
drwxr-xr-x 2 vsduser docker 4096 Jun 28 2021 lef
drwxr-xr-x 2 vsduser docker 4096 Jun 28 2021 gds
drwxr-xr-x 2 vsduser docker 4096 Jun 28 2021 doc
drwxr-xr-x 2 vsduser docker 4096 Jun 28 2021 cdl
```

(Image credits:- AUTHOR)

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdkssky130A/libs.ref/sky130_fd_sc_hd$ cd ../../../../
bash: cd../../../../: No such file or directory
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdkssky130A/libs.ref/sky130_fd_sc_hd$ cd ../../../../
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ ls -ltr
ls:ltr: command not found
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ ls -ltr
total 12
drwxr-xr-x 5 vsduser docker 4096 Jun 28 2021 pdkss
drwxr-xr-x 10 vsduser docker 4096 Jun 29 2021 openlane_old
drwxr-xr-x 10 vsduser docker 4096 May 20 2023 openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ cd openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ ls -ltr
total 136
drwxr-xr-x 15 vsduser docker 4096 Jun 29 2021 scripts
-rw-r--r-- 1 vsduser docker 20787 Jun 29 2021 run_designs.py
-rw-r--r-- 1 vsduser docker 7898 Jun 29 2021 report_generation_wrapper.py
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 regression_results
-rw-r--r-- 1 vsduser docker 25509 Jun 29 2021 README.md
-rw-r--r-- 1 vsduser docker 7273 Jun 29 2021 Makefile
-rw-r--r-- 1 vsduser docker 11350 Jun 29 2021 LICENSE
-rwrf-xr-x 1 vsduser docker 6519 Jun 29 2021 flow.tcl
drwxr-xr-x 5 vsduser docker 4096 Jun 29 2021 docs
drwxr-xr-x 5 vsduser docker 4096 Jun 29 2021 docker_build
drwxr-xr-x 44 vsduser docker 4096 Jun 29 2021 designs
-rw-r--r-- 1 vsduser docker 1285 Jun 29 2021 CONTRIBUTING.md
```

(Image credits:- AUTHOR)

```
-rw-r--r-- 1 vsduser docker      5514 Jun 29  2021 conf.py
drwxr-xr-x 2 vsduser docker     4096 Jun 29  2021 configuration
-rw-r--r-- 1 vsduser docker      966 Jun 29  2021 clean_runs.tcl
-rw-r--r-- 1 vsduser docker     709 Jun 29  2021 AUTHORS.md
-rw-r--r-- 1 vsduser vsduser    963 May 20  2023 default.cvcrc
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ ls -lrth
total 136K
drwxr-xr-x 15 1000  997 4.0K Jun 29  2021 scripts
-rw-r--r--  1 1000  997  21K Jun 29  2021 run_designs.py
-rw-r--r--  1 1000  997  7.8K Jun 29  2021 report_generation_wrapper.py
drwxr-xr-x  3 1000  997 4.0K Jun 29  2021 regression_results
-rwxr-xr-x  1 1000  997  6.4K Jun 29  2021 flow.tcl
drwxr-xr-x  5 1000  997 4.0K Jun 29  2021 docs
drwxr-xr-x  5 1000  997 4.0K Jun 29  2021 docker_build
drwxr-xr-x 44 1000  997 4.0K Jun 29  2021 designs
drwxr-xr-x  2 1000  997 4.0K Jun 29  2021 configuration
-rw-r--r--  1 1000  997  5.4K Jun 29  2021 conf.py
-rwrxr-xr-x  1 1000  997  966 Jun 29  2021 clean_runs.tcl
-rw-r--r--  1 1000  997  25K Jun 29  2021 README.md
-rw-r--r--  1 1000  997  7.2K Jun 29  2021 Makefile
-rw-r--r--  1 1000  997  12K Jun 29  2021 LICENSE
-rw-r--r--  1 1000  997  1.3K Jun 29  2021 CONTRIBUTING.md
-rw-r--r--  1 1000  997  709 Jun 29  2021 AUTHORS.md
-rw-r--r--  1 1000 1000  963 May 19  2023 default.cvcrc
bash-4.2$ ./flow.tcl -interactive
```

(Image credits:- AUTHOR)

[INFO]:

```
[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
0.9
```

(Image credits:- AUTHOR)

```
% prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/30-01_13-38
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l11 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROS matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROS matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: MACROS matched found: 1
mergeLef.py : Merging LEFs complete
```

(Image credits:- AUTHOR)

```
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% ┌─[
```

(Image credits:- AUTHOR)

```
vsduser@vsdsquadron:~$ cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ ls -ltr
total 32
drwxr-xr-x 2 vsduser docker 4096 Jun 29 2021 src
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_ms_config.tcl
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_ls_config.tcl
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_hs_config.tcl
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_hd_ll_config.tcl
-rwxr-xr-x 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_hd_config.tcl
-rwxr-xr-x 1 vsduser docker 444 Jun 29 2021 config.tcl
drwxr-xr-x 3 vsduser vsduser 4096 Jan 30 19:08 runs
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ d
```

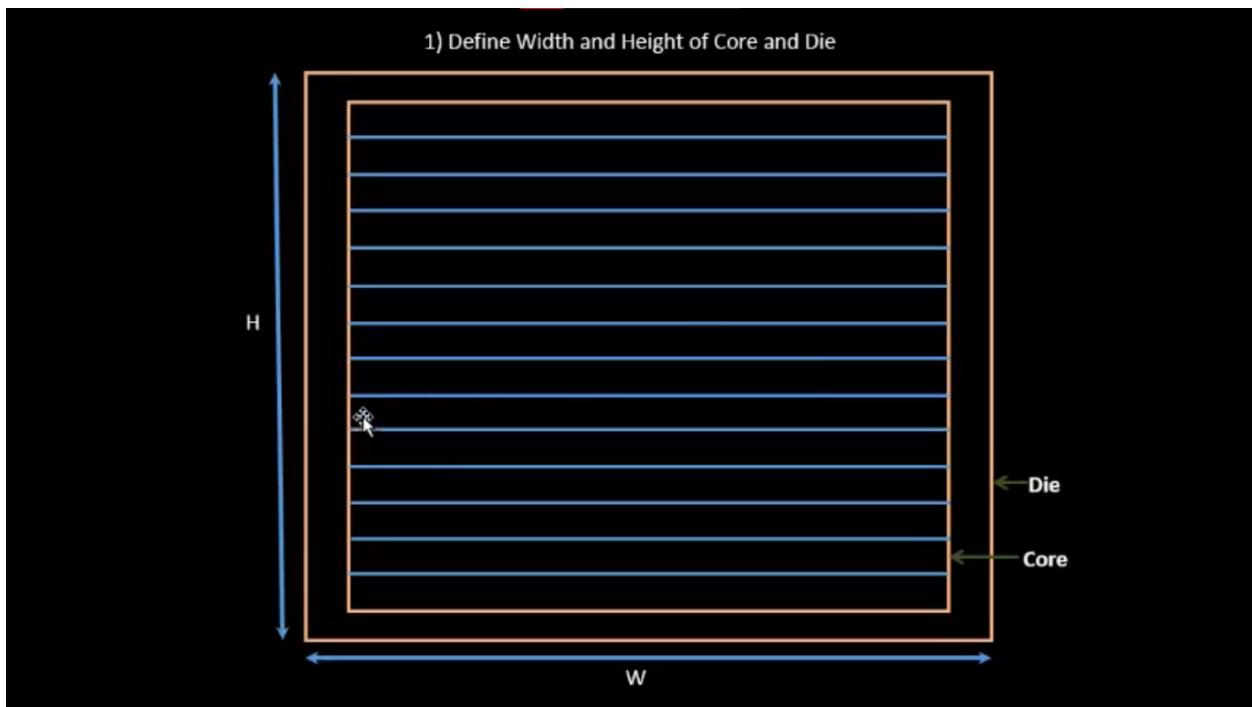
(Image credits:- AUTHOR)

Good Floorplan vs Bad

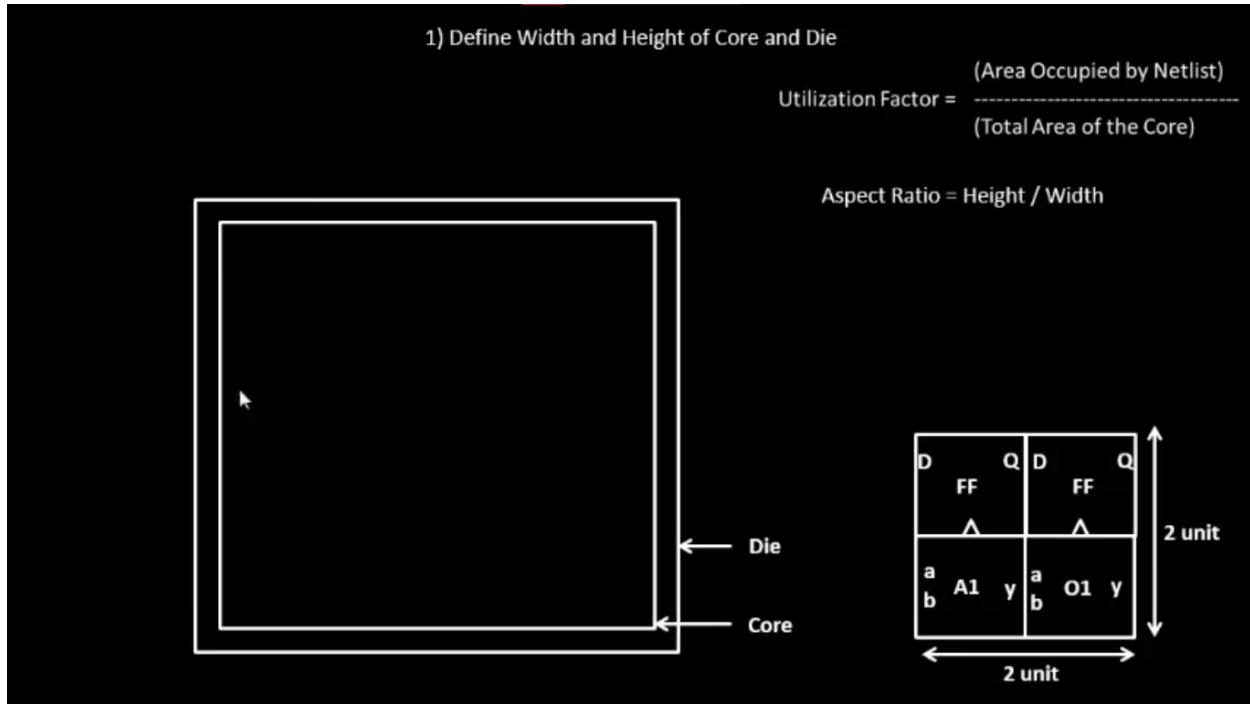
Floorplan and

Introduction to Library

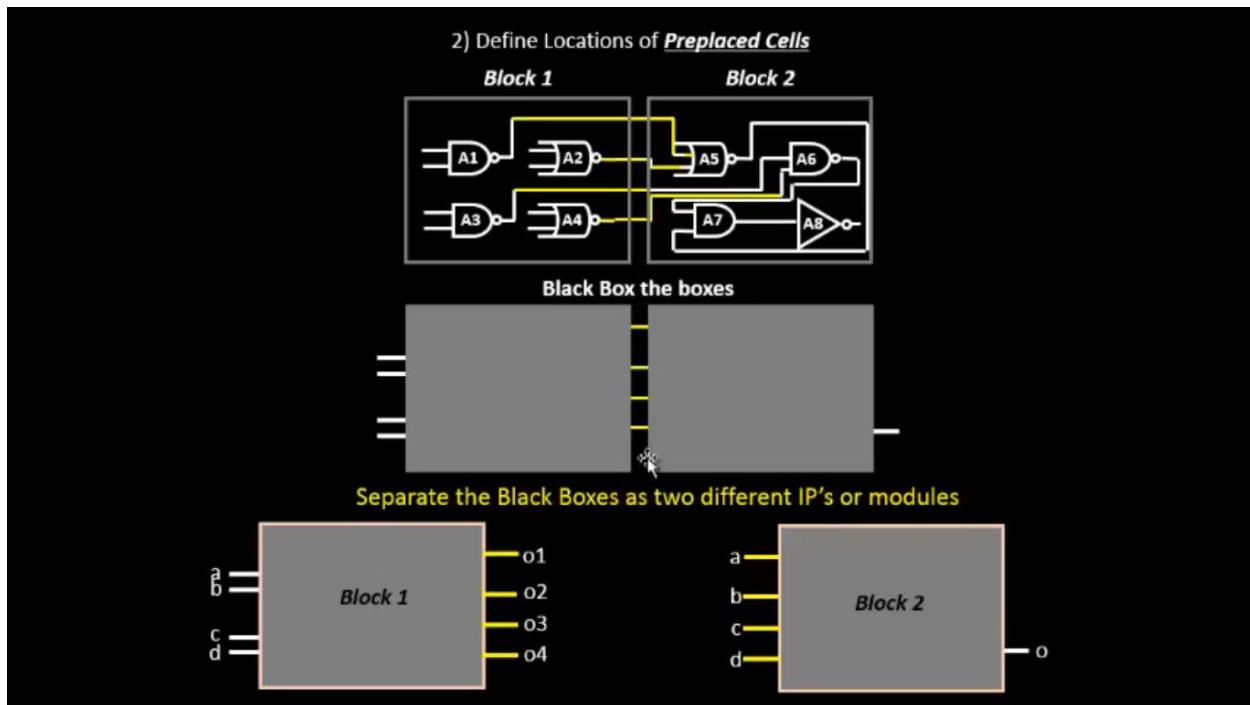
Cells



(Image credits:- VSDIAT)

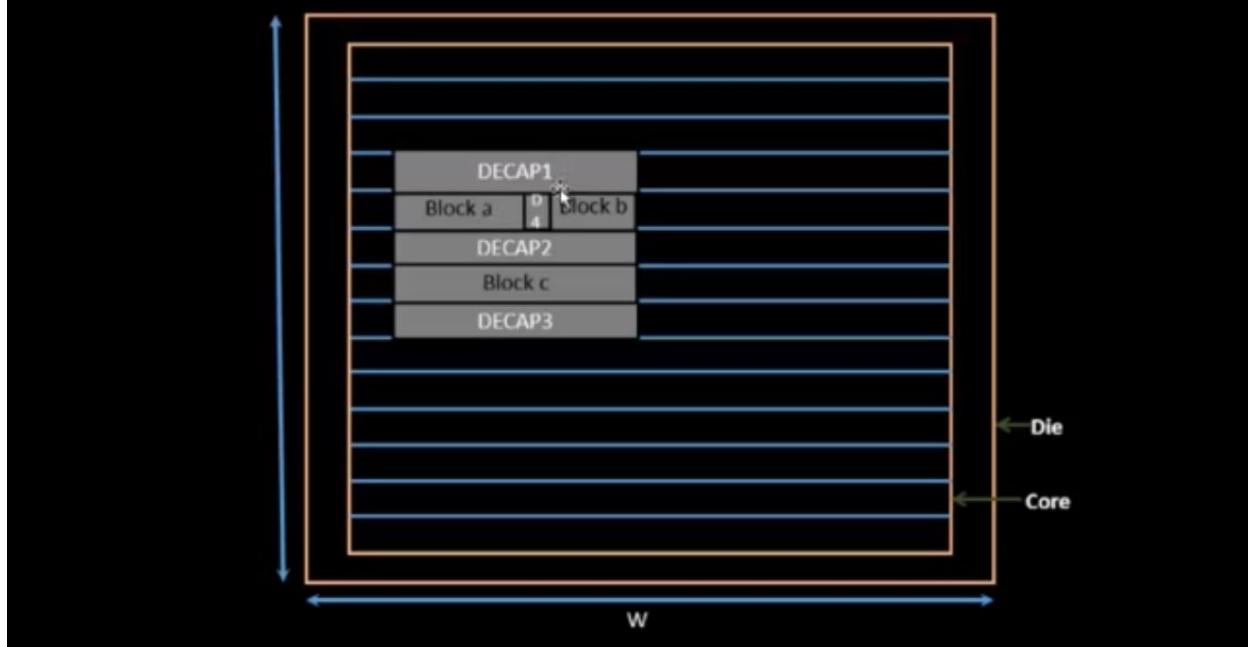


(Image credits:- VSDIAT)



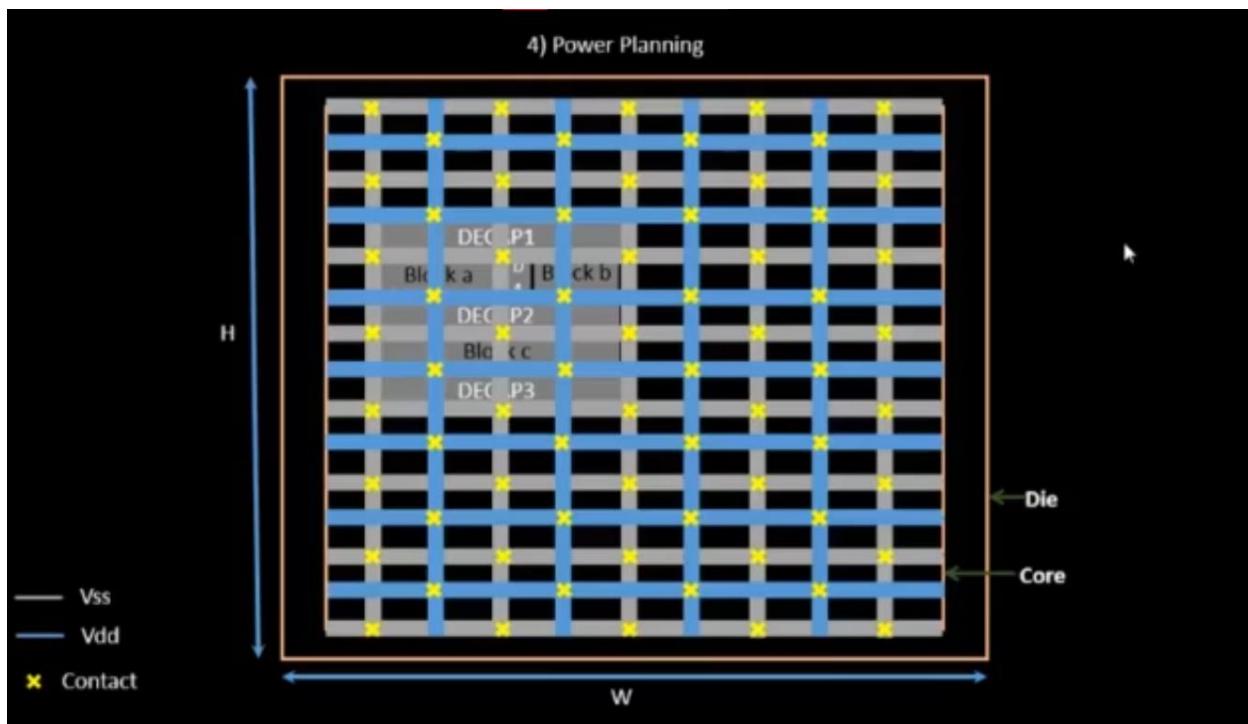
(Image credits:- VSDIAT)

3) Surround pre-placed cells with Decoupling Capacitors

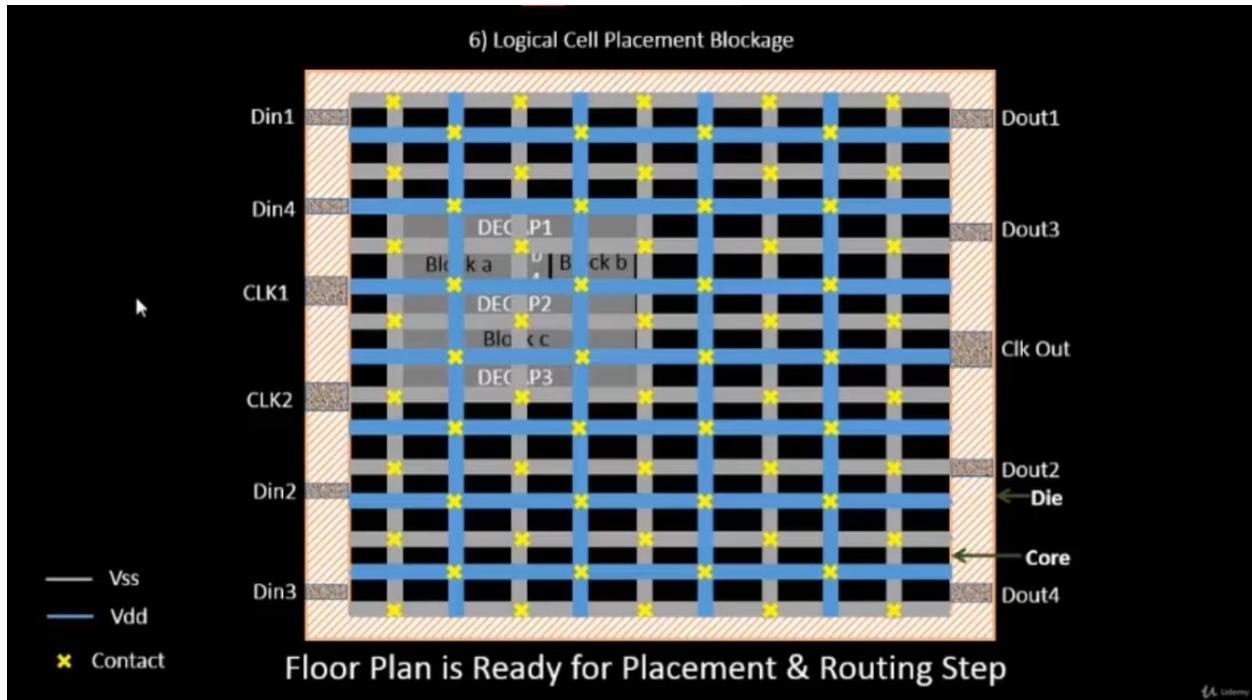


(Image credits:- VSDIAT)

4) Power Planning



(Image credits:- VSDIAT)



(Image credits:- VSDIAT)

```

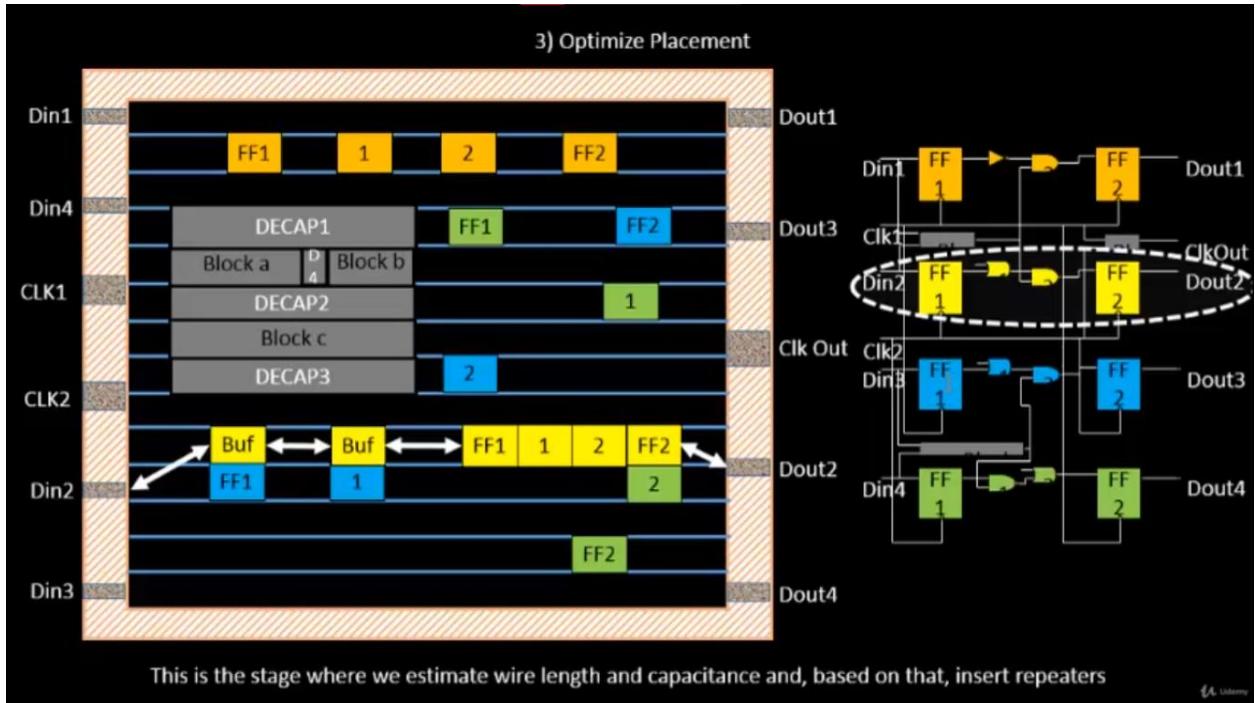
tms -759.40
wns -24.89
[INFO]: Synthesis was successful
% run_floorplan
[INFO]: Running Floorplanning...
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 3
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Warning: /home/vsdiat/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd_tt_025C_1v80 not found.
b line 31, default_operating_condition tt_025C_1v80 not found.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/01-02_05-36/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 440 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/01-02_05-36/tmp/merged_unpadded.lef
[INFO] IFP-0001] Added 238 rows of 1412 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 660.685 671.405 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/01-02_05-36/floorplan/3-verilog2def.die_area.rpt.

```

(Image credits:- AUTHOR)



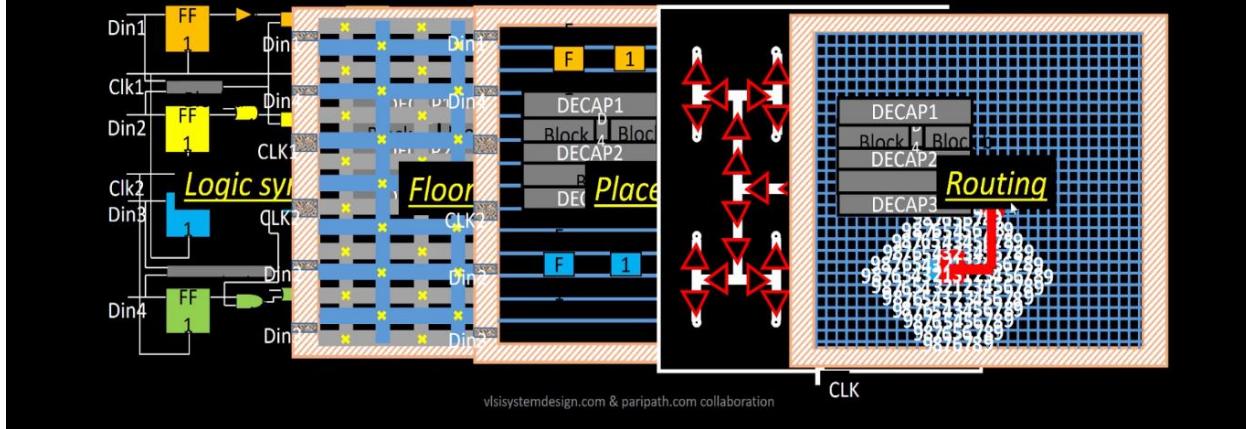
(Image credits:- AUTHOR)



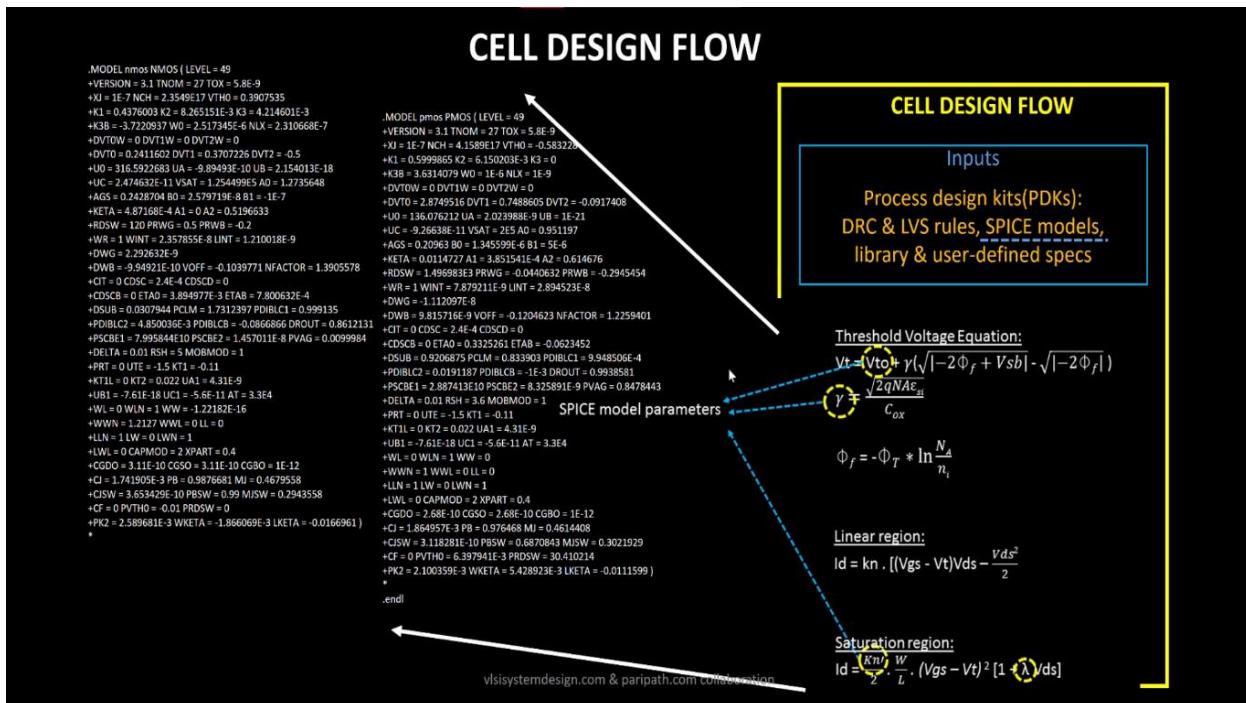
(Image credits:- VSDIAT)

Library characterization and modelling

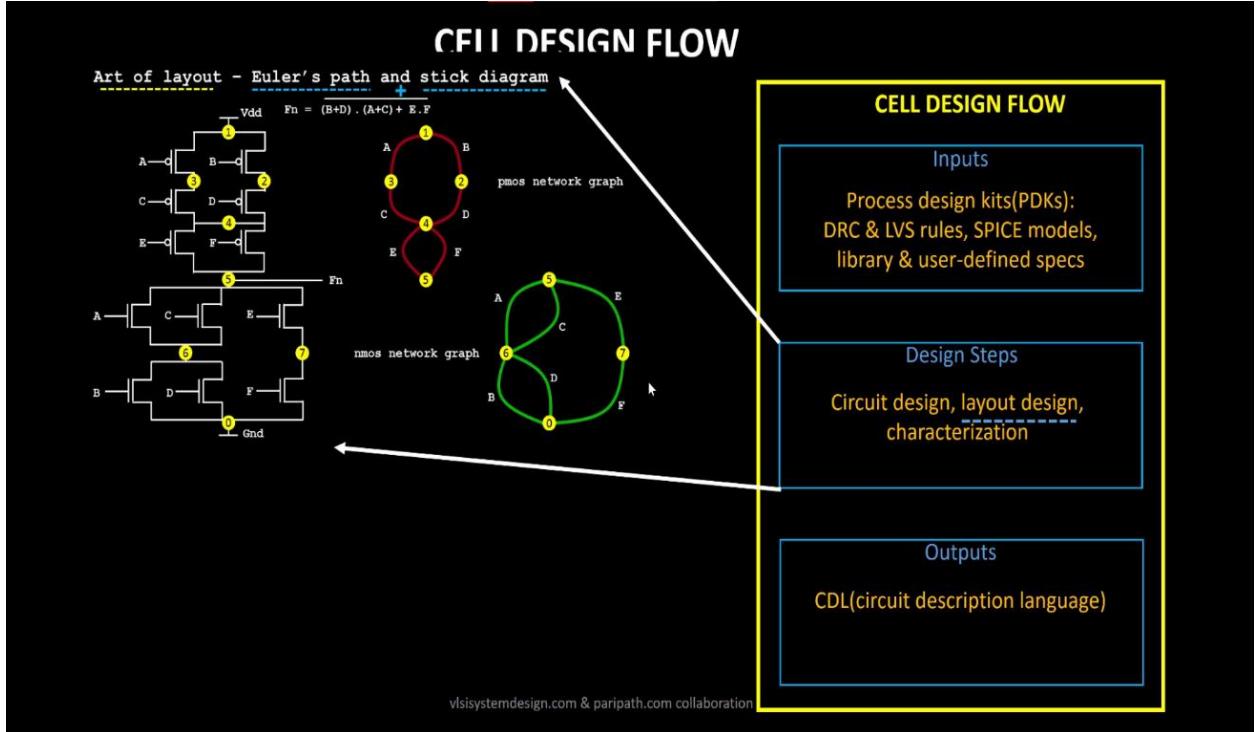
Part 1 – Concepts and Theory – NLDM, CCS timing, power and noise characterization



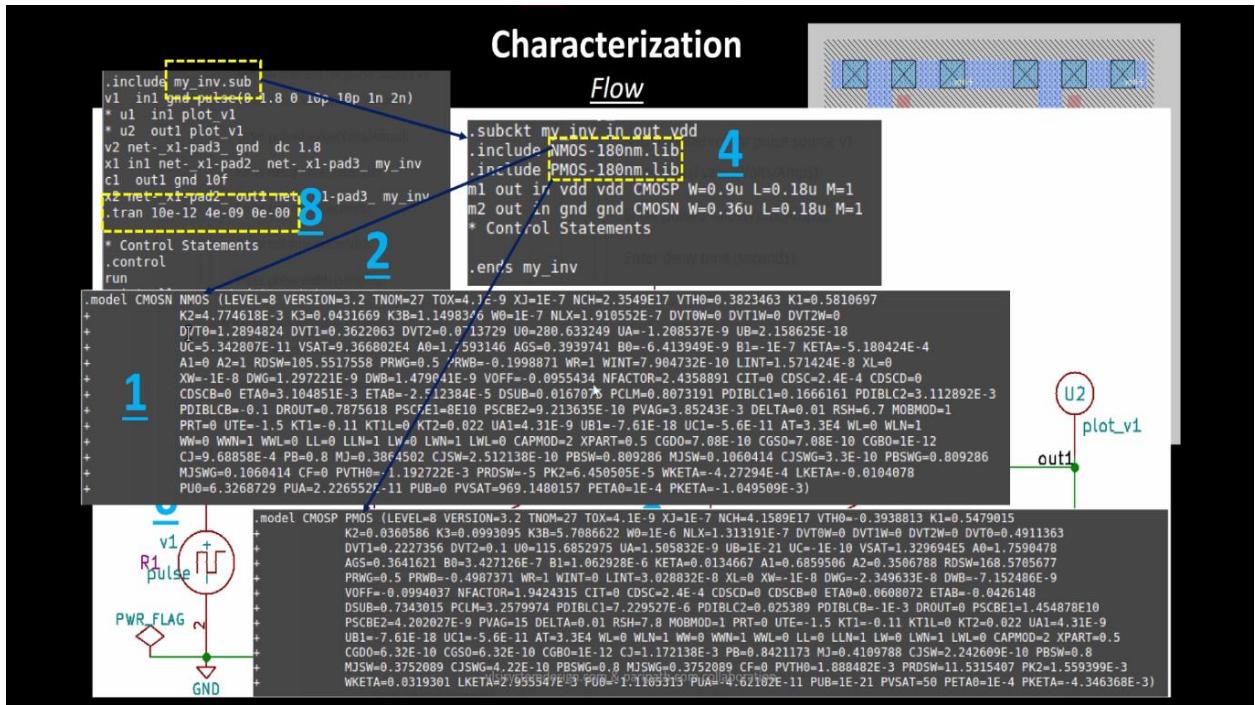
(Image credits:- VSDIAT)



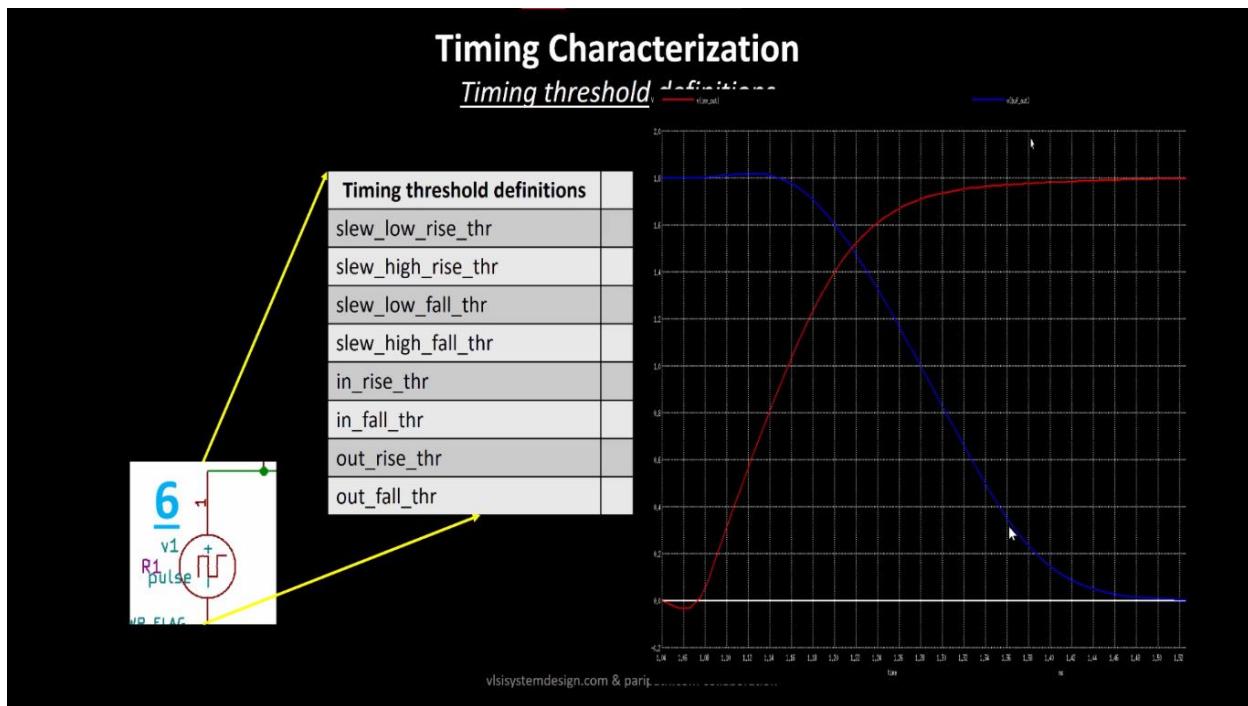
(Image credits:- VSDIAT)



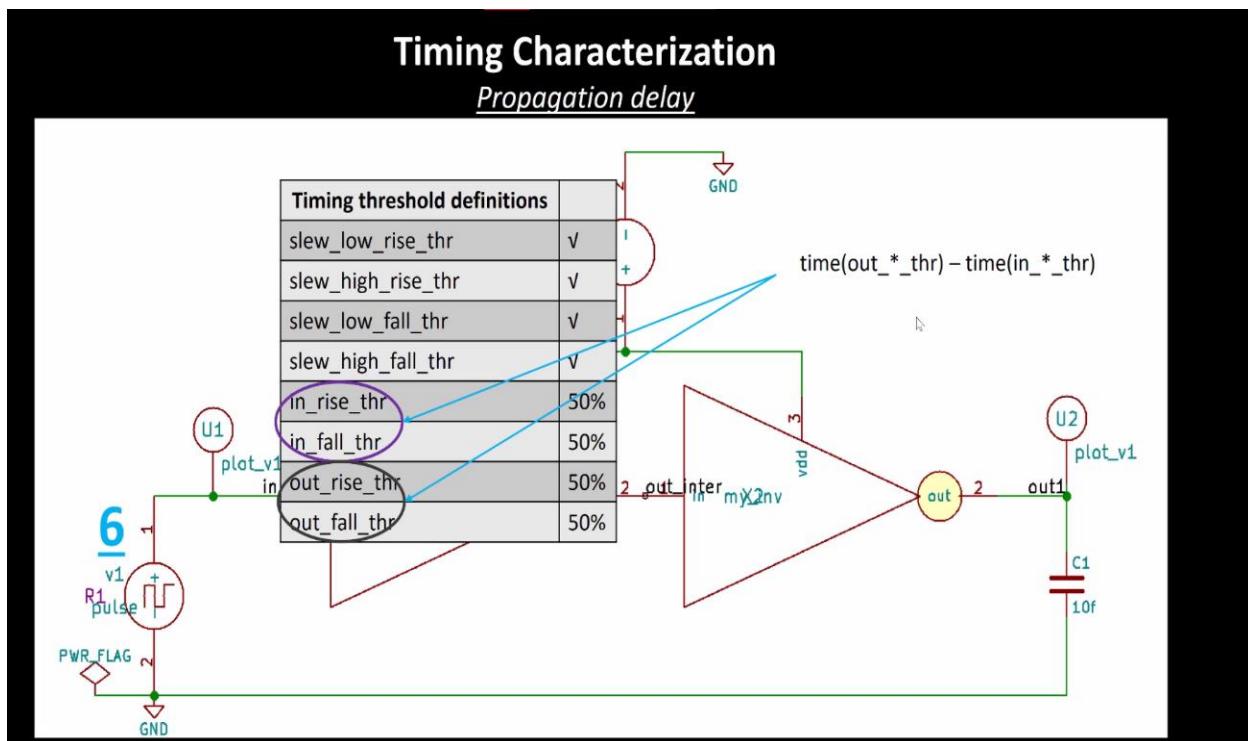
(Image credits:- VSDIAT)



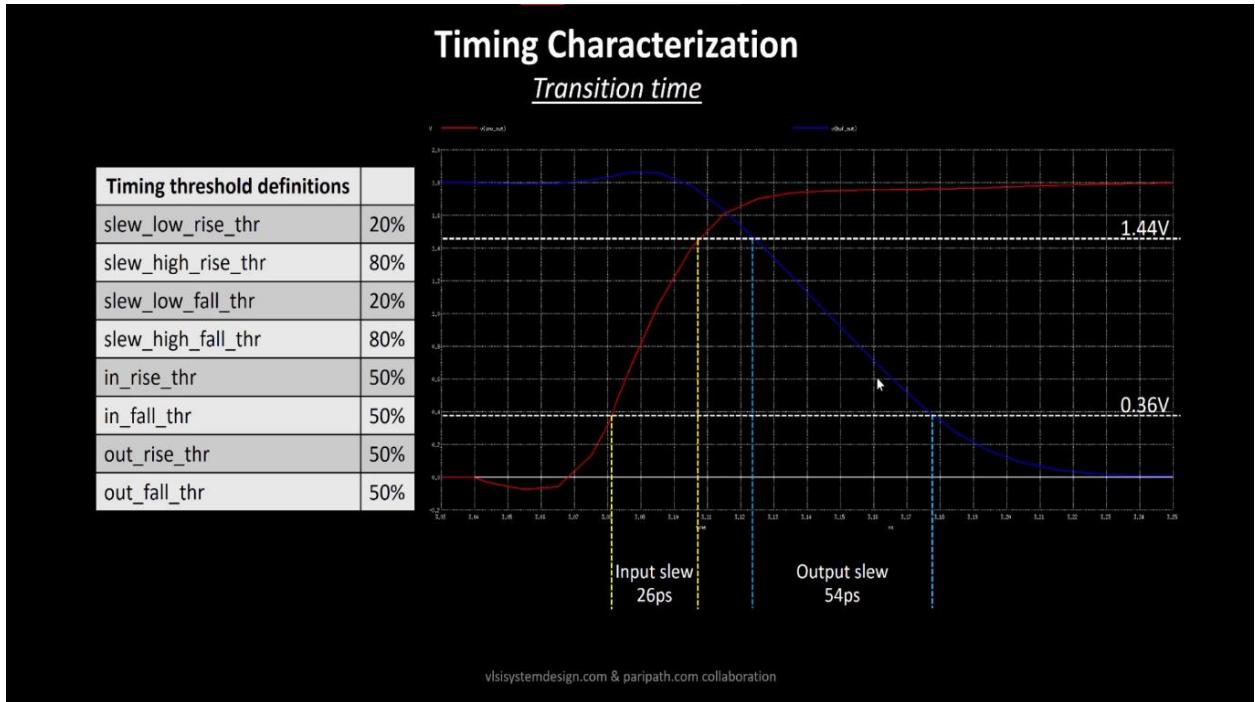
(Image credits:- VSDIAT)



(Image credits:- VSDIAT)

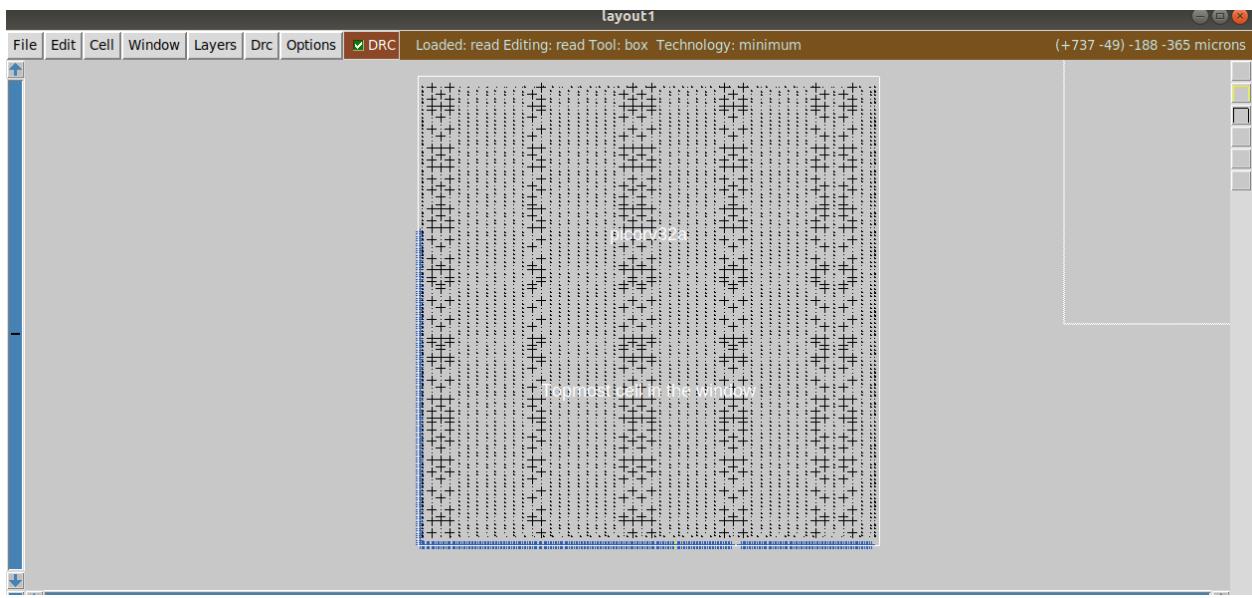


(Image credits:- VSDIAT)



(Image credits:- VSDIAT)

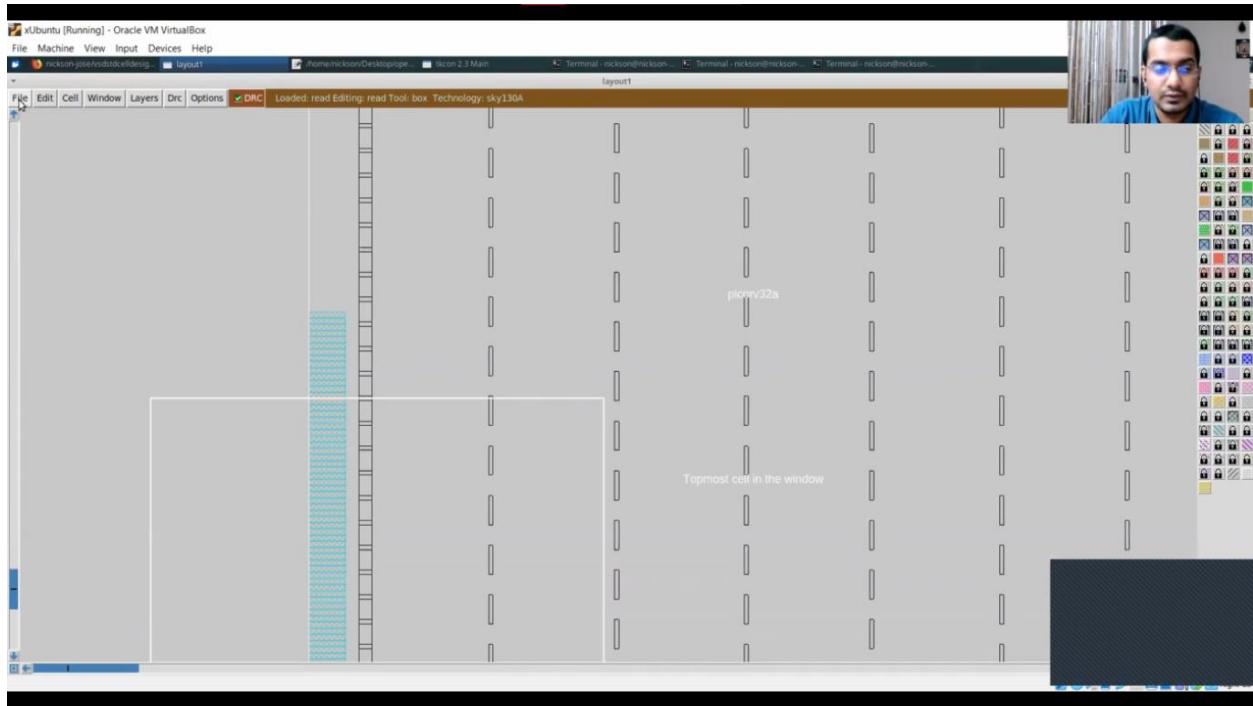
Design Library Cell using Magic Layout and ngspice characterization



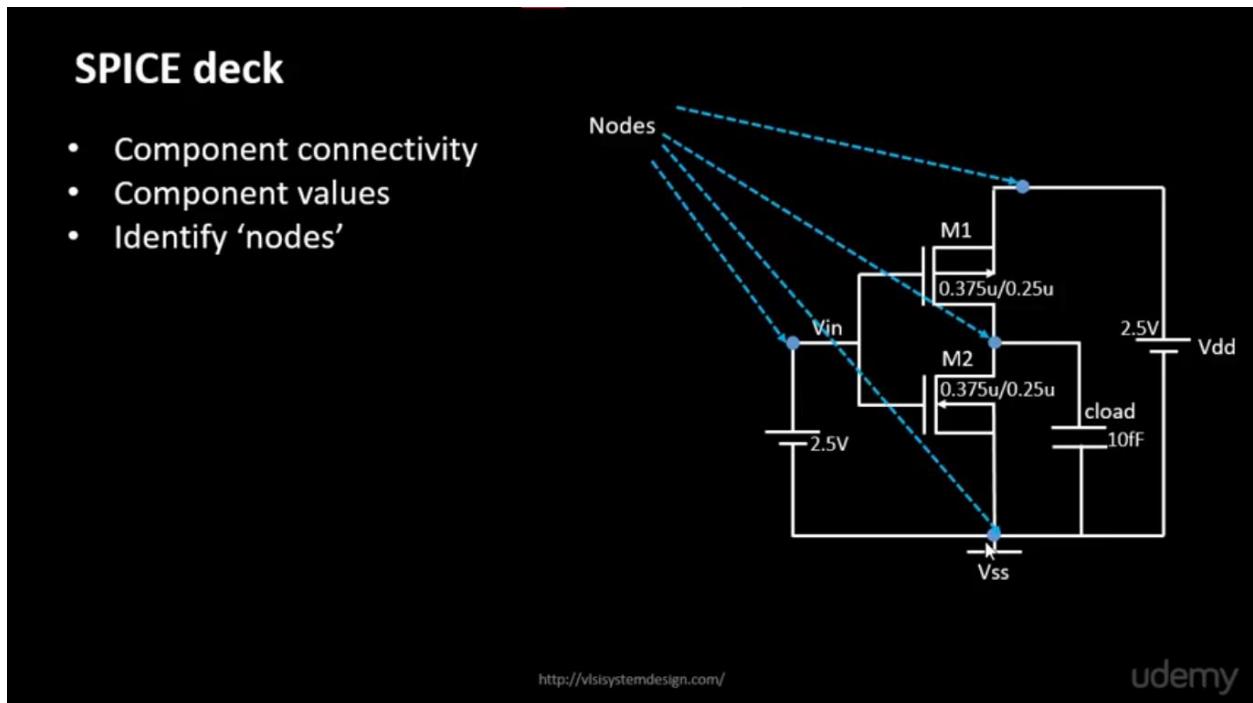
(Image credits:- AUTHOR)

```
% set ::env(FP_IO_MODE) 2
2
% run_floorplan
[INFO]: Running Floorplanning...
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 8
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Warning: /home/vsuser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd_tt_025C_1v80.lib line 31, default_operating_condition tt_025C_1v80 not found.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/01-02_08-02/tmp/merged_unpadded.lef
```

(Image credits:- AUTHOR)



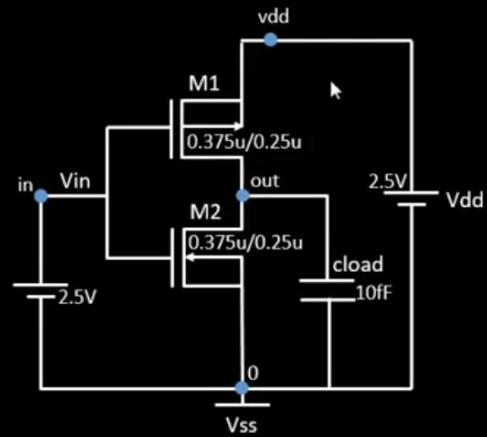
(Image credits:- VSDIAT)



(Image credits:- VSDIAT)

SPICE deck

- Component connectivity
- Component values
- Identify 'nodes'
- Name 'nodes'



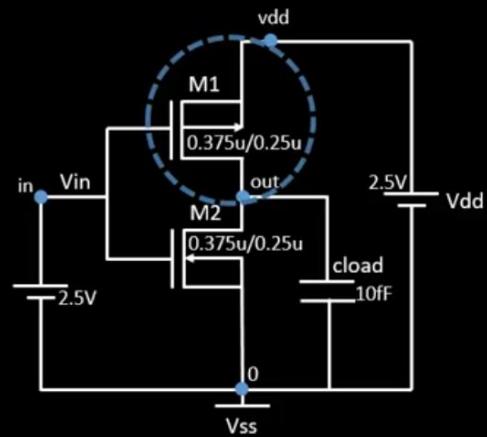
<http://vlisystemdesign.com/>

udemy

(Image credits:- VSDIAT)

SPICE deck

```
*** MODEL Descriptions ***
*** NETLIST Description ***
M1 out in vdd vdd pmos W=0.375u L=0.25u
M2 out in 0 0 nmos W=0.375u L=0.25u
```



<http://vlisystemdesign.com/>

udemy

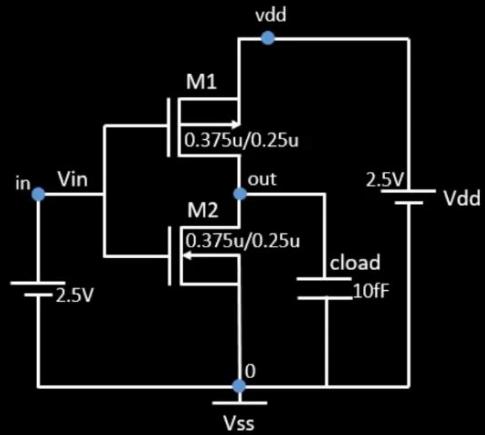
(Image credits:- VSDIAT)

SPICE deck

```
*** MODEL Descriptions ***
*** NETLIST Description ***
M1 out in vdd vdd pmos W=0.375u L=0.25u
M2 out in 0 0 nmos W=0.375u L=0.25u

cload out 0 10f

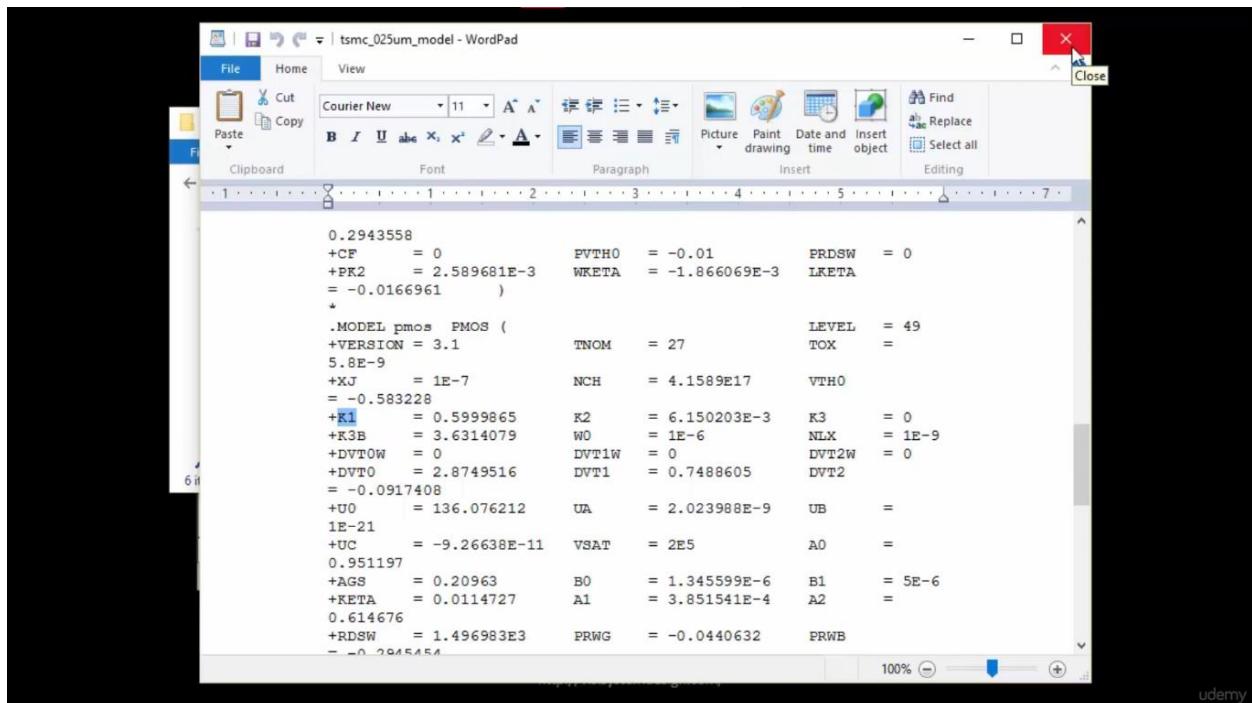
Vdd vdd 0 2.5
Vin in 0 2.5
*** SIMULATION Commands ***
.op
.dc Vin 0 2.5 0.05
*** .include tsmc_025um_model.mod ***
.LIB "tsmc_025um_model.mod" CMOS_MODELS
.end
```



<http://vlssystemdesign.com/>

udemy

(Image credits:- VSDIAT)



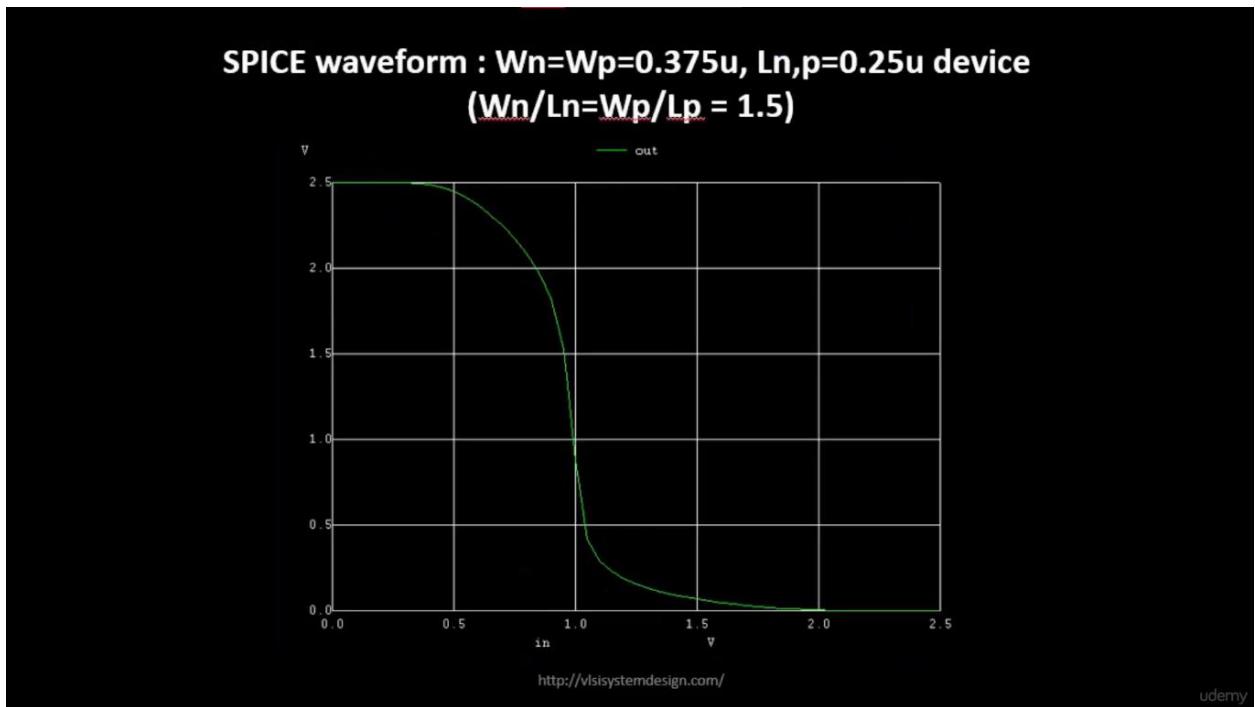
(Image credits:- VSDIAT)

The screenshot shows a Microsoft WordPad window titled "cmosVTC_PMOSwidth_NMOSwidth - WordPad". The document contains a SPICE netlist:

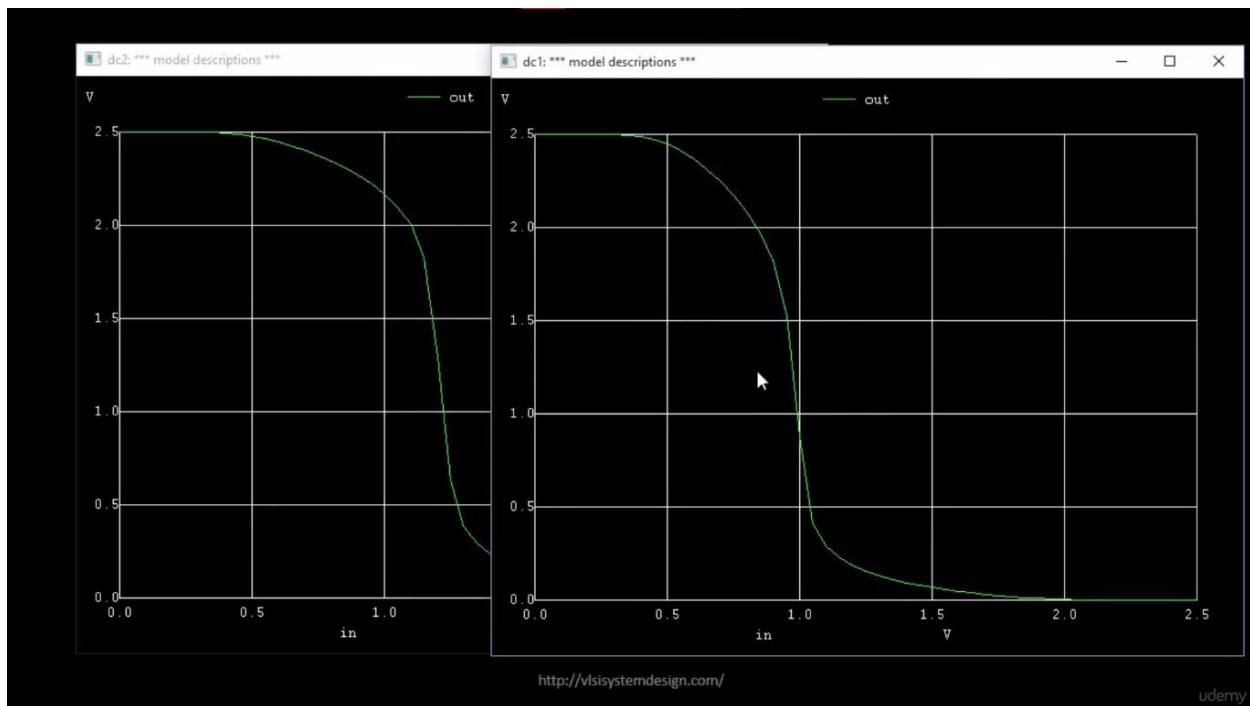
```
*** MODEL Descriptions ***
*** NETLIST Description ***
M1 out in vdd vdd pmos W=0.375u L=0.25u
M2 out in 0 0 nmos W=0.375u L=0.25u

cload out 0 10f
|
Vdd vdd 0 2.5
Vin in 0 2.5
*** SIMULATION Commands ***
.op
.dc Vin 0 2.5 0.05
*** .include tsmc_025um_model.mod ***
.LIB "tsmc_025um_model.mod" CMOS_MODELS
.end
```

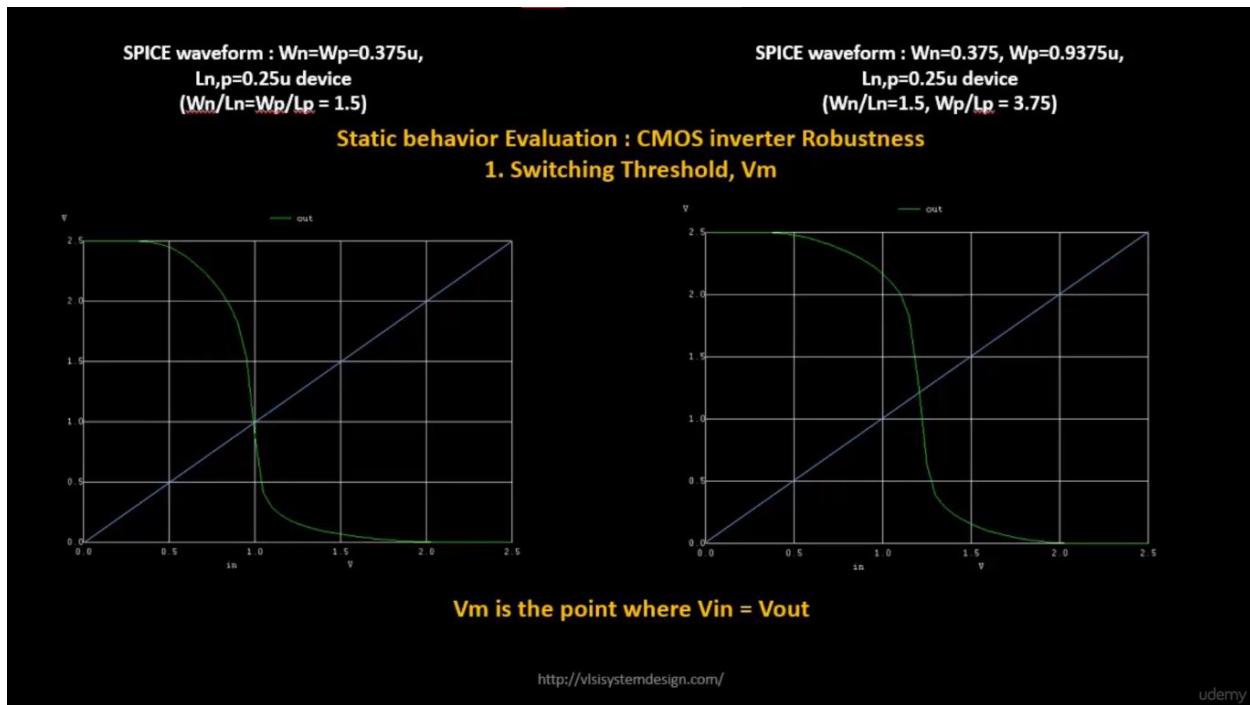
(Image credits:- VSDIAT)



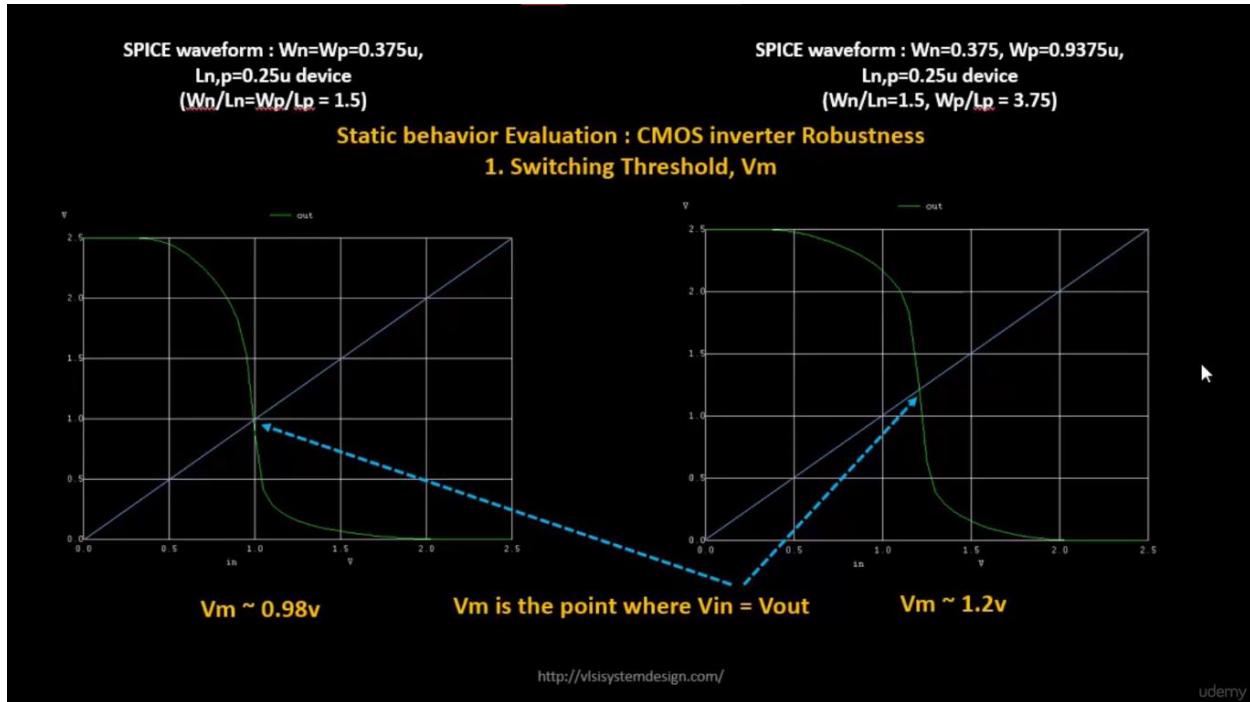
(Image credits:- VSDIAT)



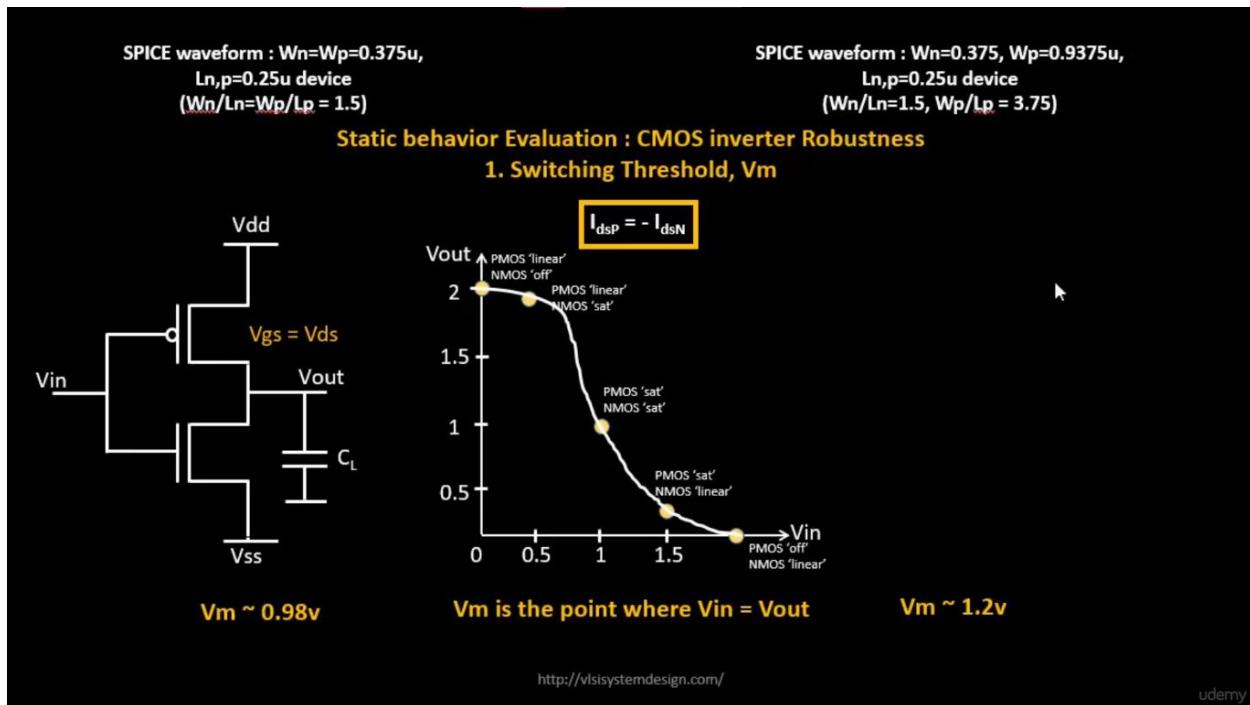
(Image credits:- VSDIAT)



(Image credits:- VSDIAT)



(Image credits:- VSDIAT)



(Image credits:- VSDIAT)

SPICE waveform : $W_n = W_p = 0.375\mu$,
 $L_n, p = 0.25\mu$ device
 $(W_n/L_n = W_p/L_p = 1.5)$

SPICE waveform : $W_n = 0.375, W_p = 0.9375\mu$,
 $L_n, p = 0.25\mu$ device
 $(W_n/L_n = 1.5, W_p/L_p = 3.75)$

Static behavior Evaluation : CMOS inverter Robustness

1. Switching Threshold, V_m

$$V_m = R \cdot V_{dd} / (1+R)$$

$$\text{Where } R = \frac{K_p \cdot V_{dsatp}}{K_n \cdot V_{dsatn}} = \frac{\left(\frac{W_p}{L_p}\right) K_p \cdot V_{dsatp}}{\left(\frac{W_n}{L_n}\right) K_n \cdot V_{dsatn}}$$

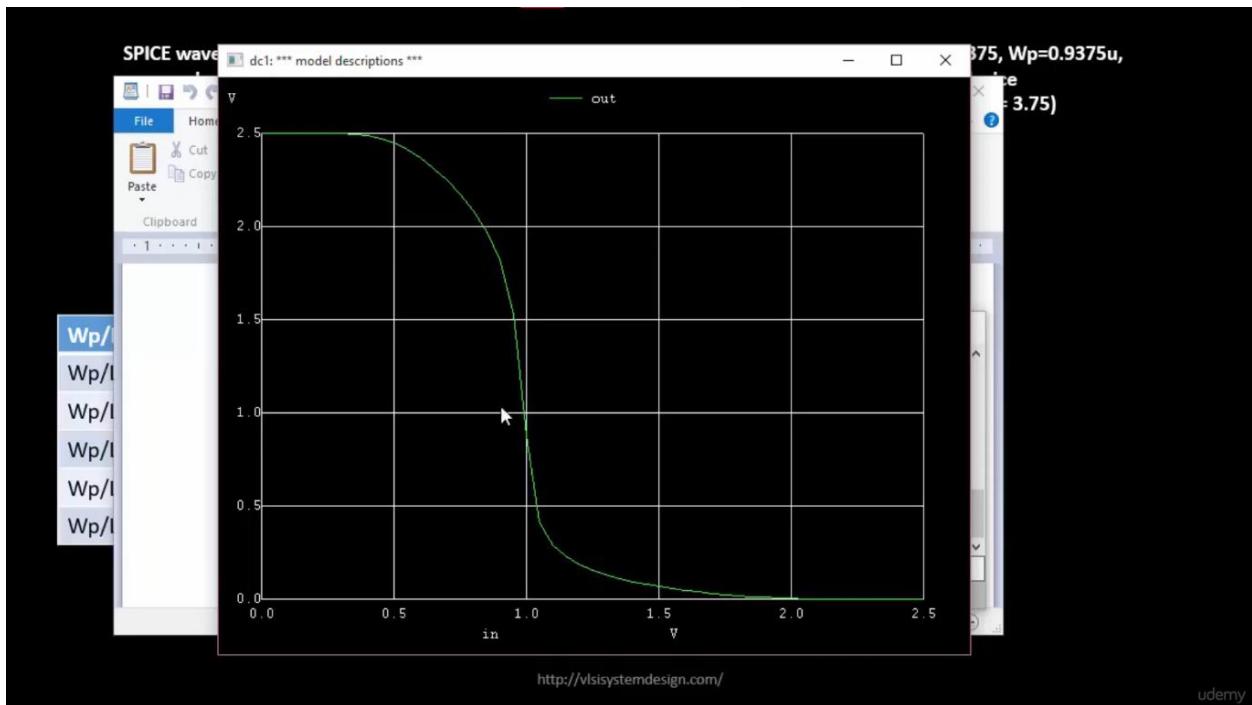
$$\frac{\left(\frac{W_p}{L_p}\right)}{\left(\frac{W_n}{L_n}\right)} = \frac{K_n \cdot V_{dsatn}([V_m - V_t]) - \frac{V_{dsatn}}{2}}{K_p \cdot V_{dsatp}([-V_m + V_{dd} + V_t]) + \frac{V_{dsatp}}{2}}$$

V_m is the point where $V_{in} = V_{out}$

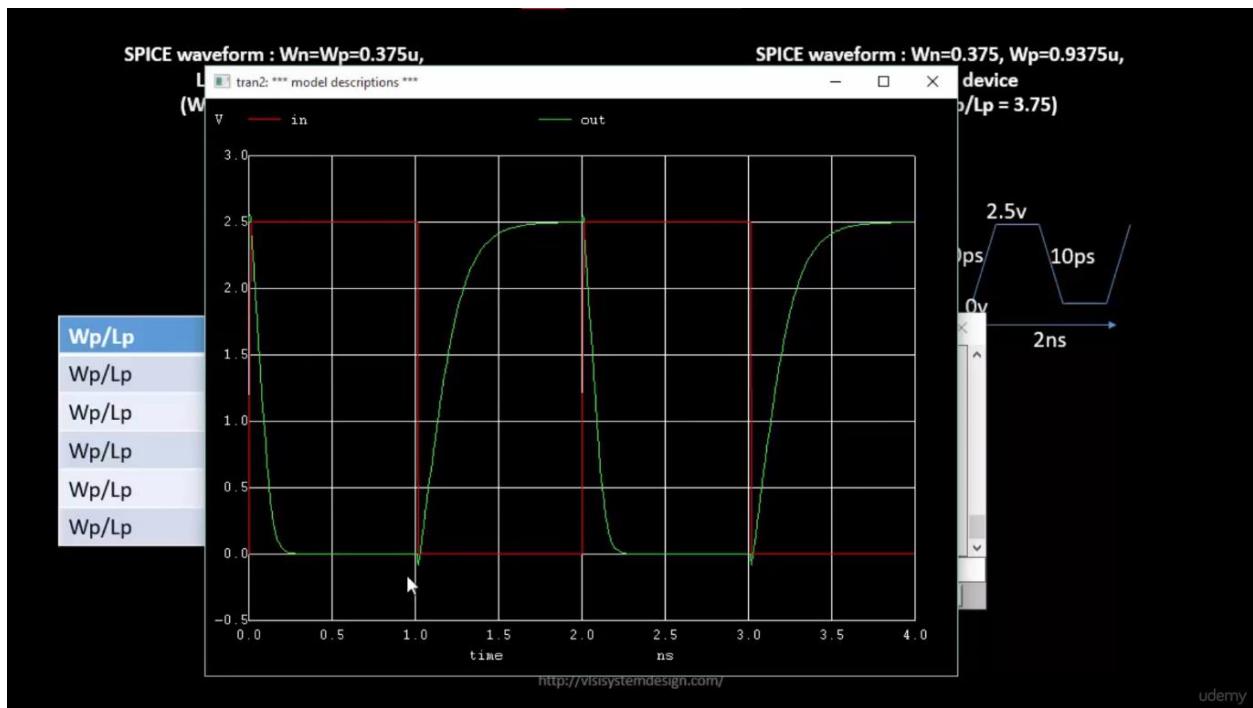
<http://vlsisystemdesign.com/>

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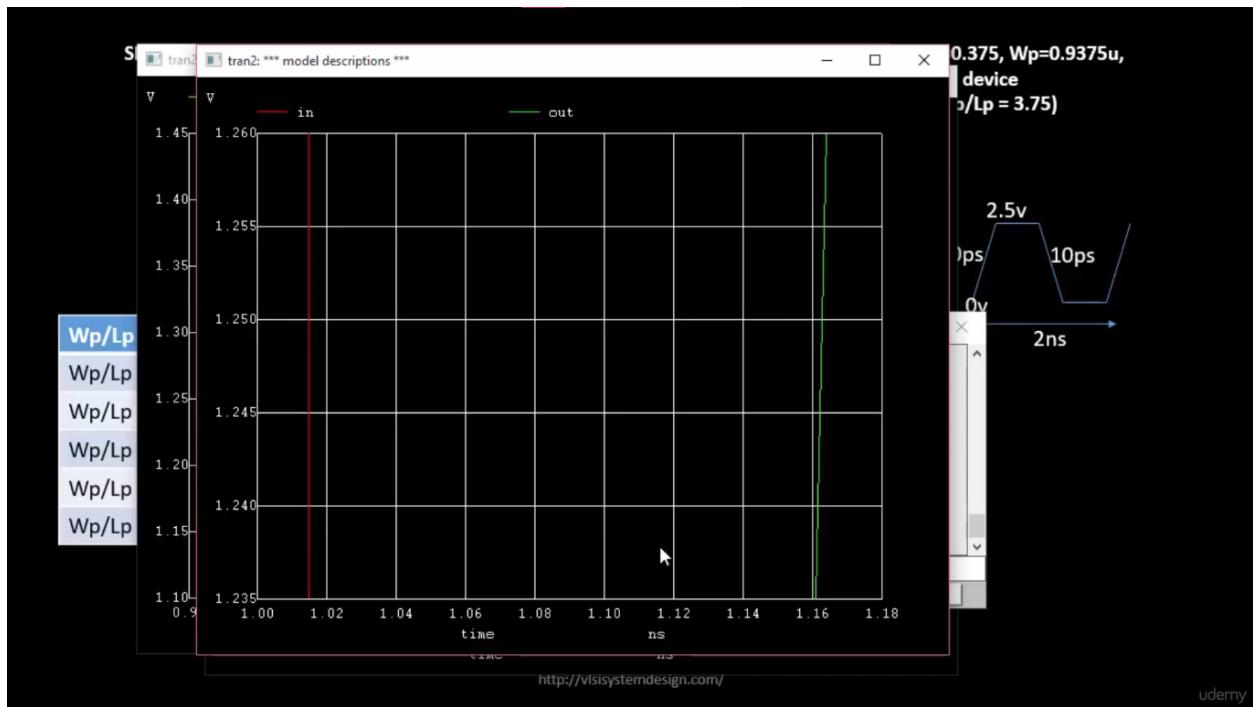
(Image credits:- VSDIAT)



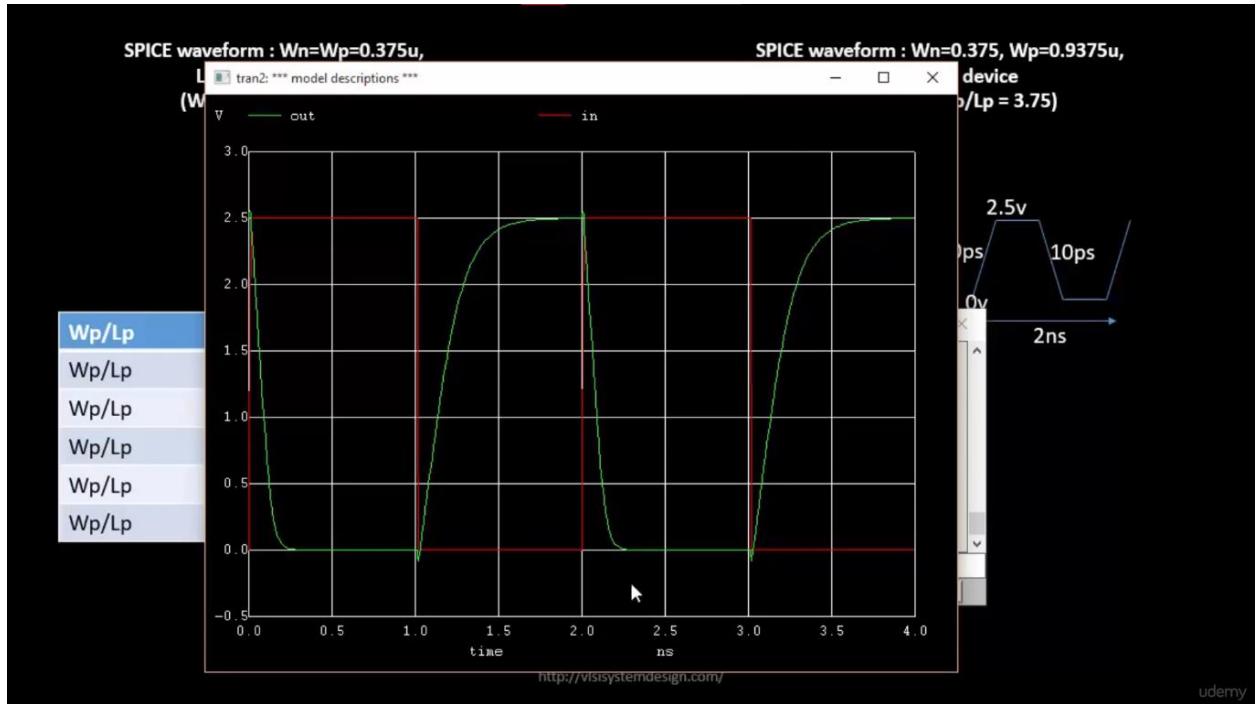
(Image credits:- VSDIAT)



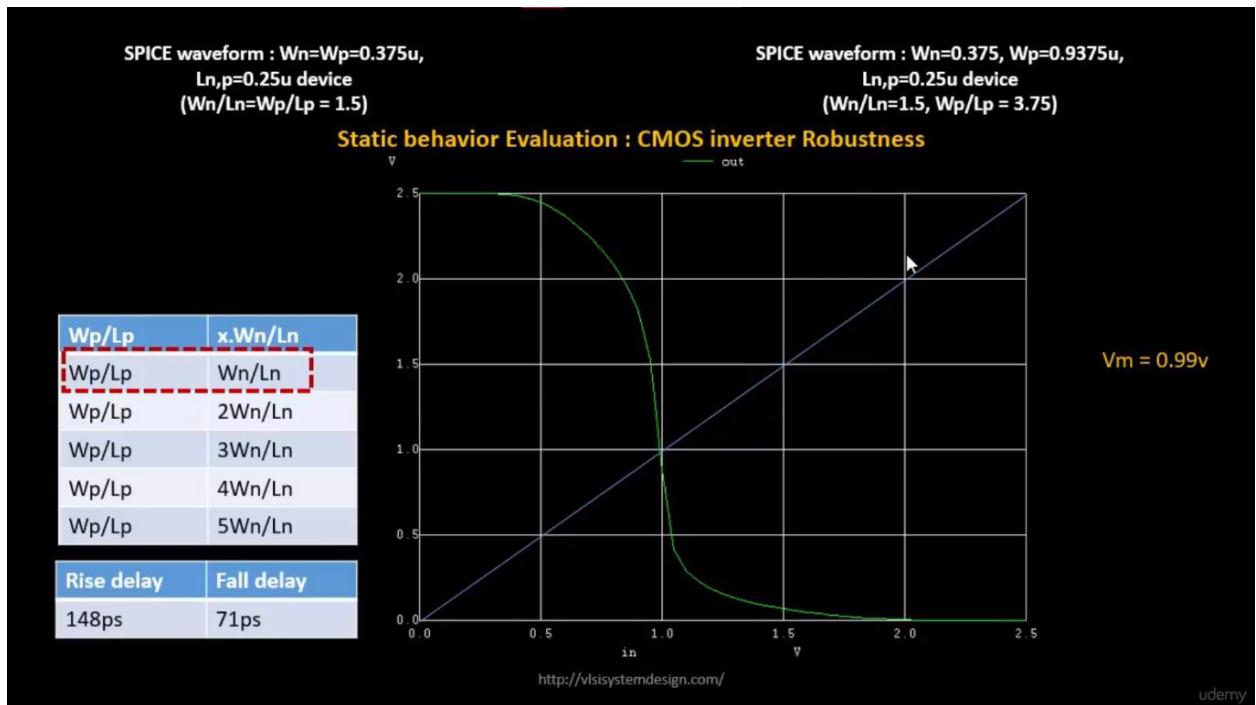
(Image credits:- VSDIAT)



(Image credits:- VSDIAT)



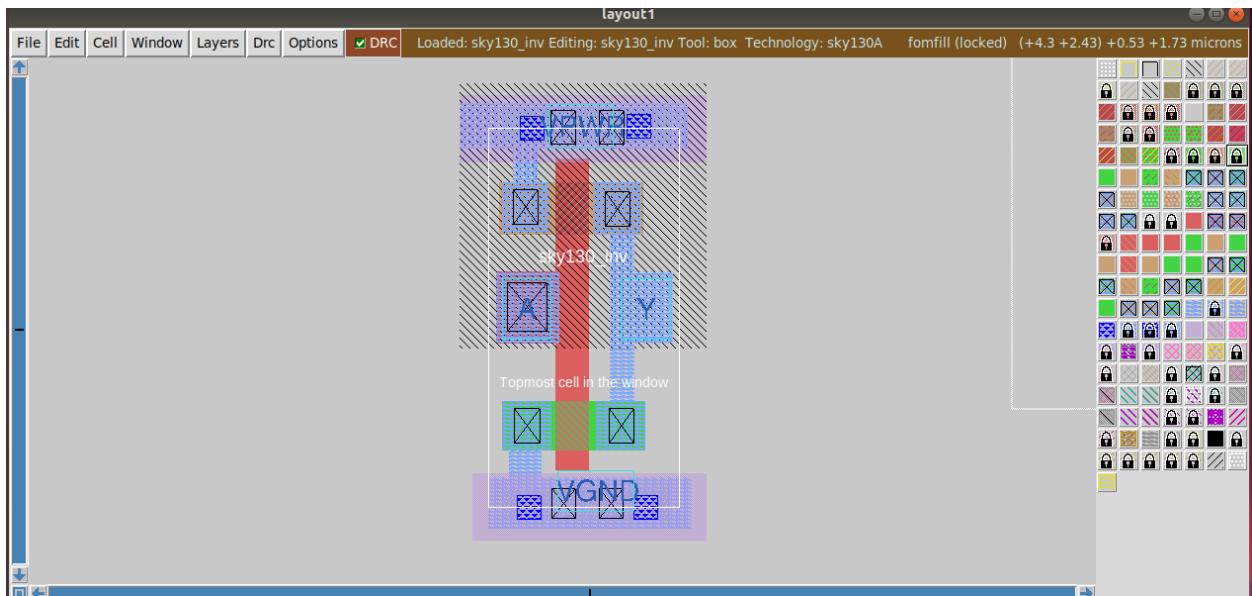
(Image credits:- VSDIAT)



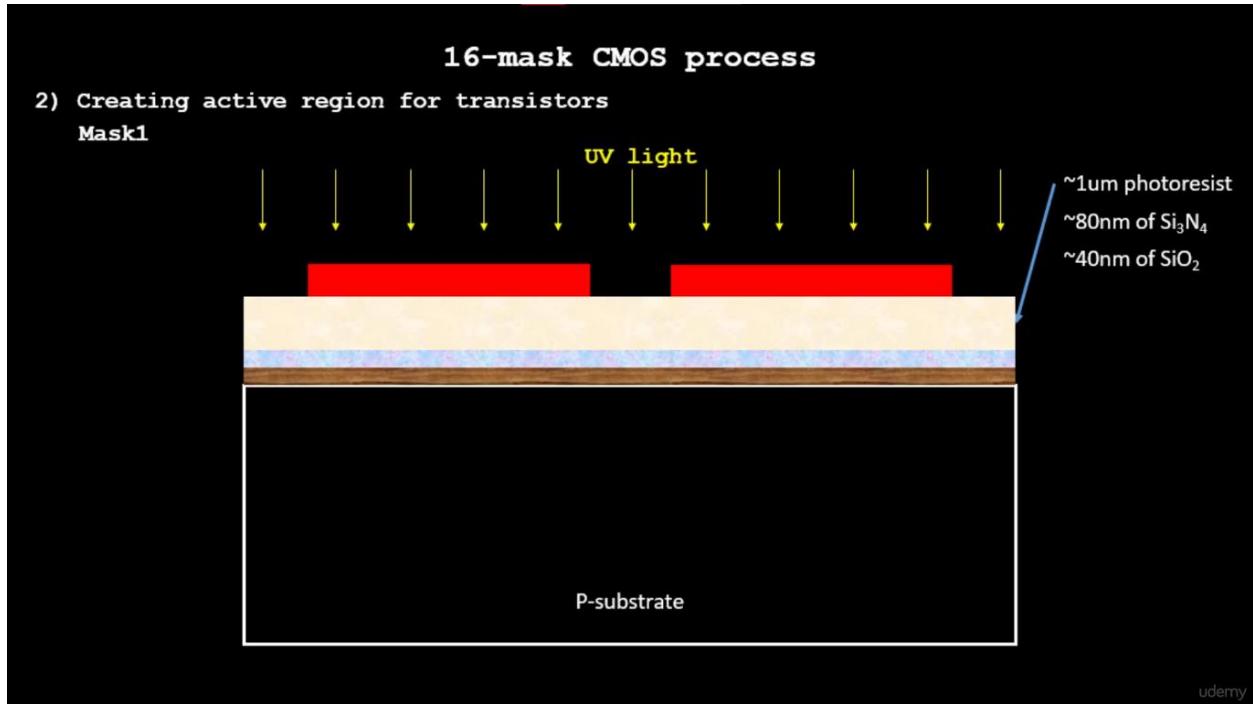
(Image credits:- VSDIAT)

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ magic -T sky130A.tech sky130_inv.mag &
[1] 6771
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

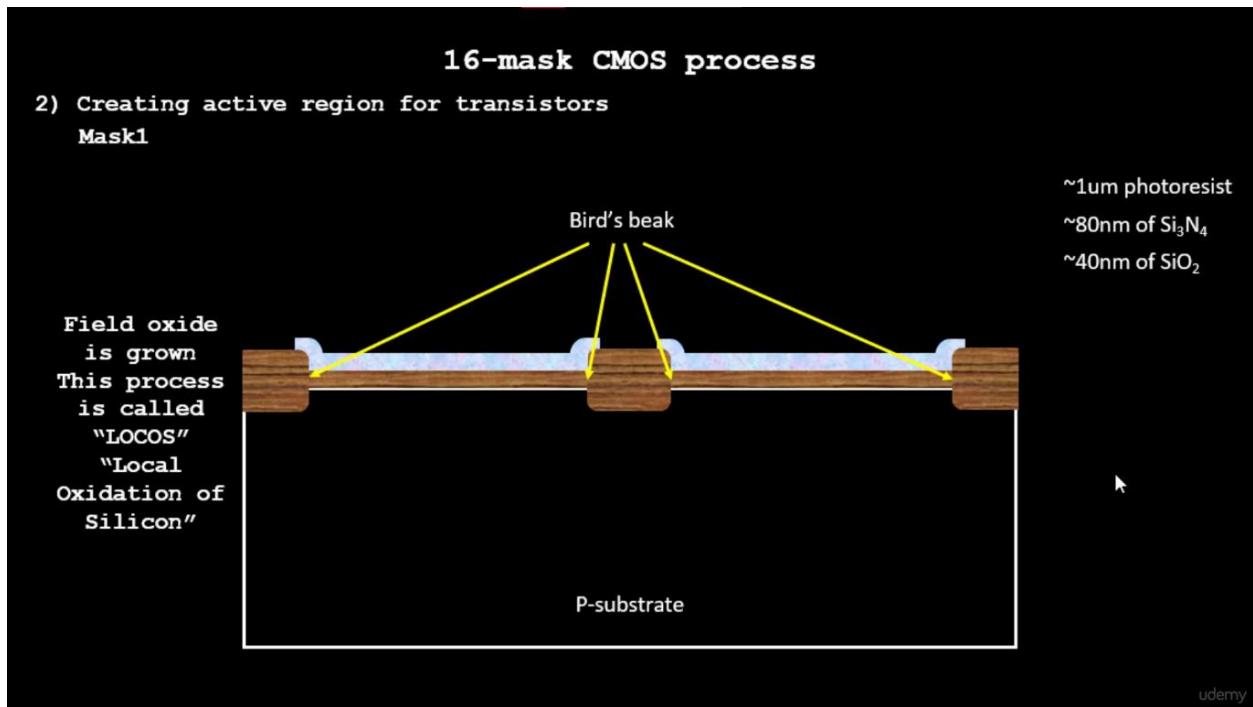
(Image credits:- AUTHOR)



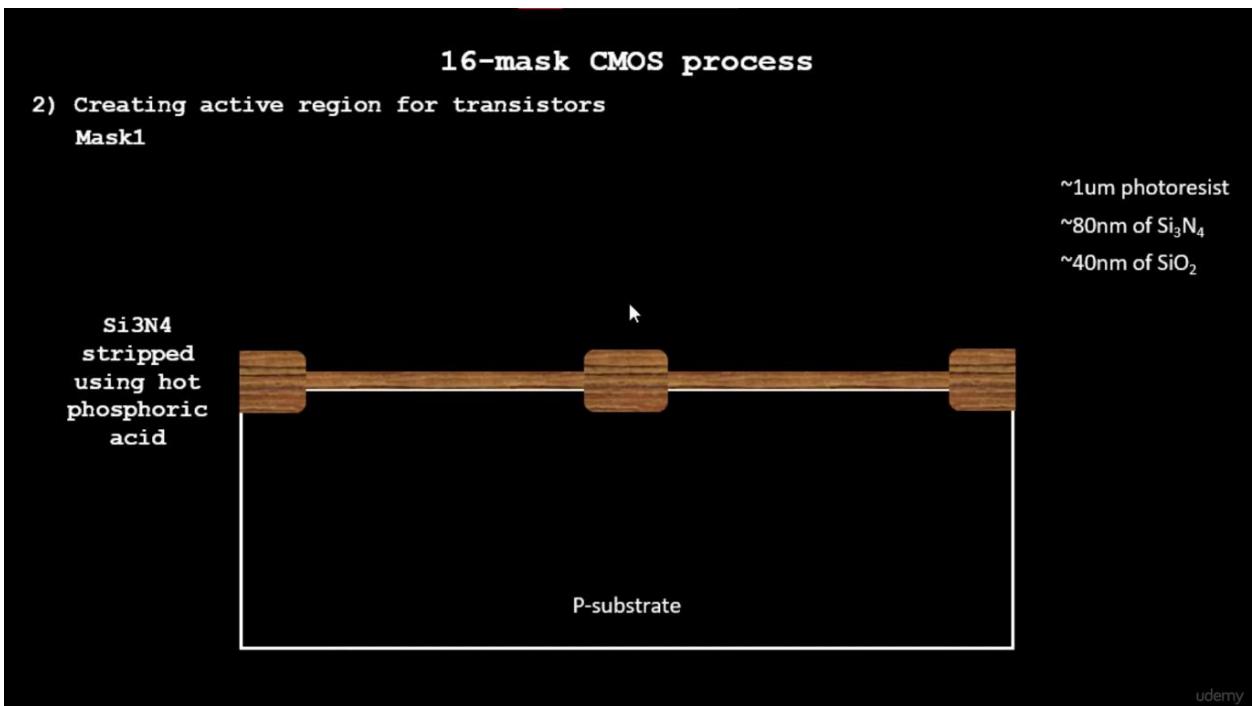
(Image credits:- AUTHOR)



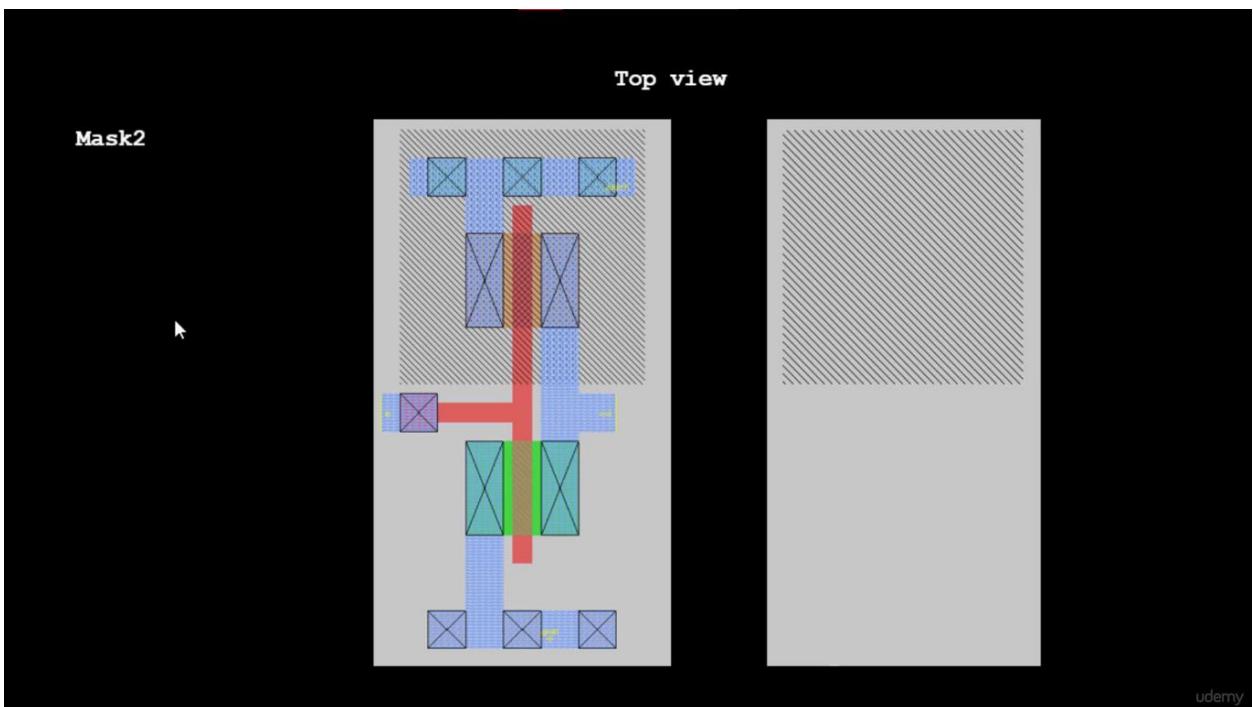
(Image credits:- VSDIAT)



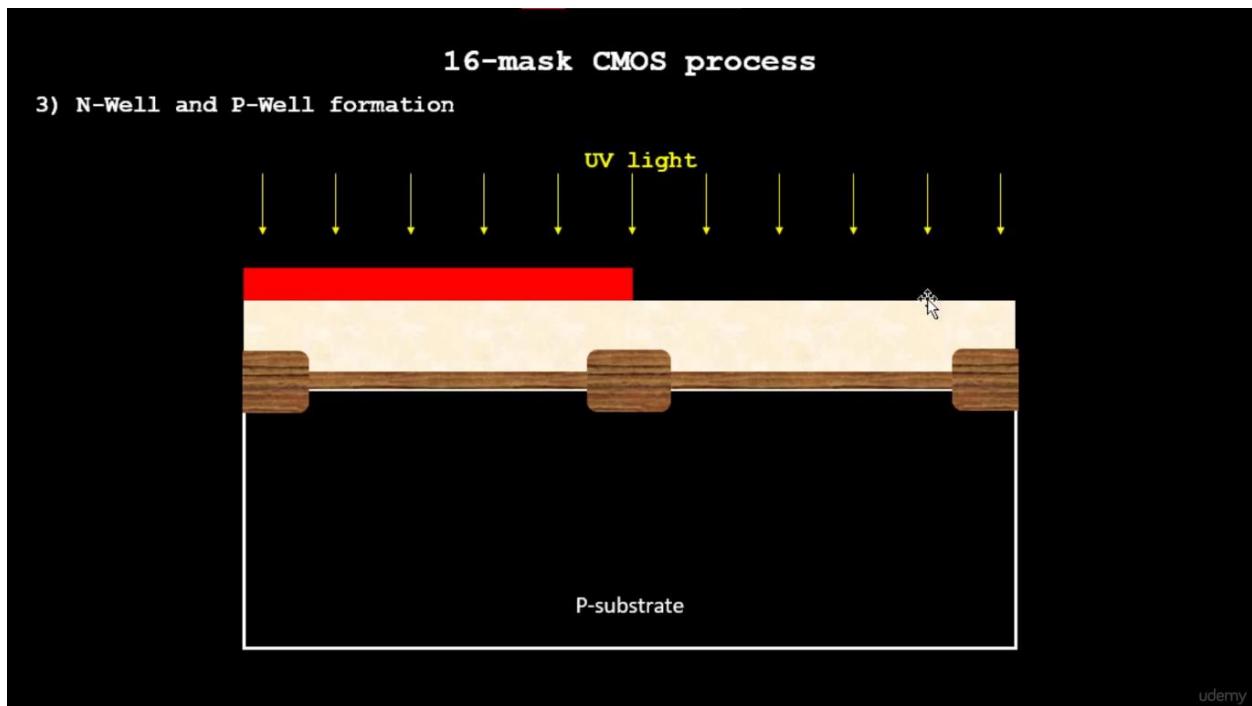
(Image credits:- VSDIAT)



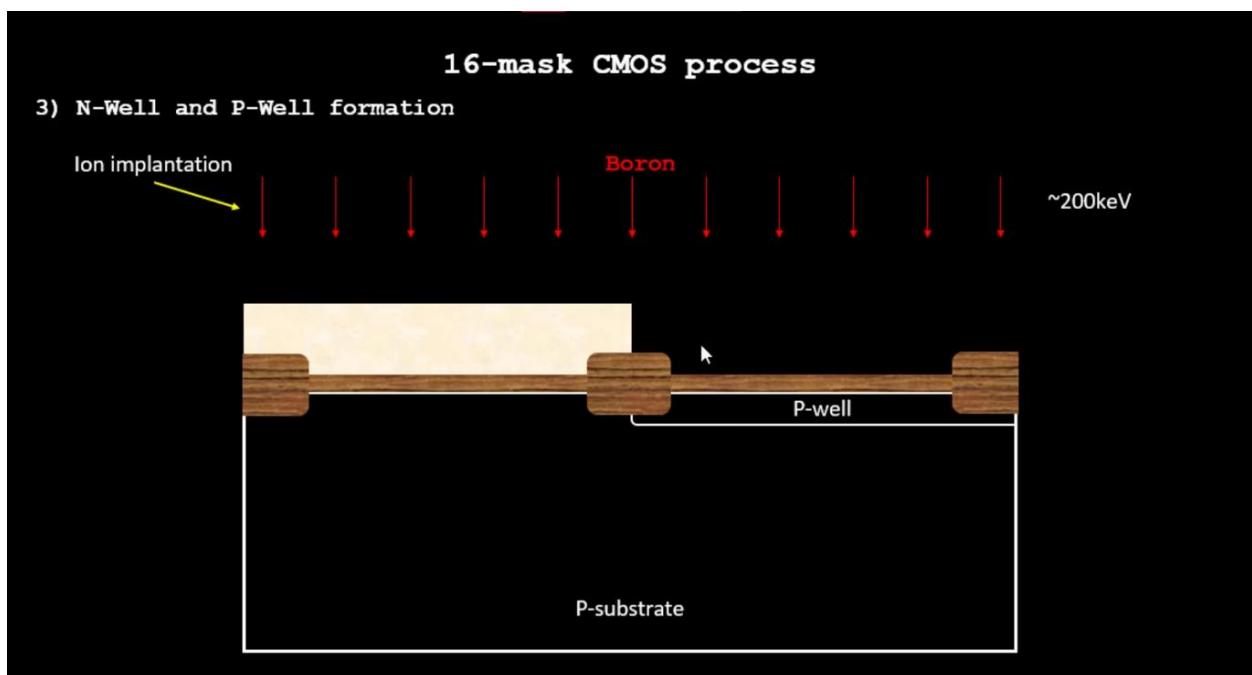
(Image credits:- VSDIAT)



(Image credits:- VSDIAT)



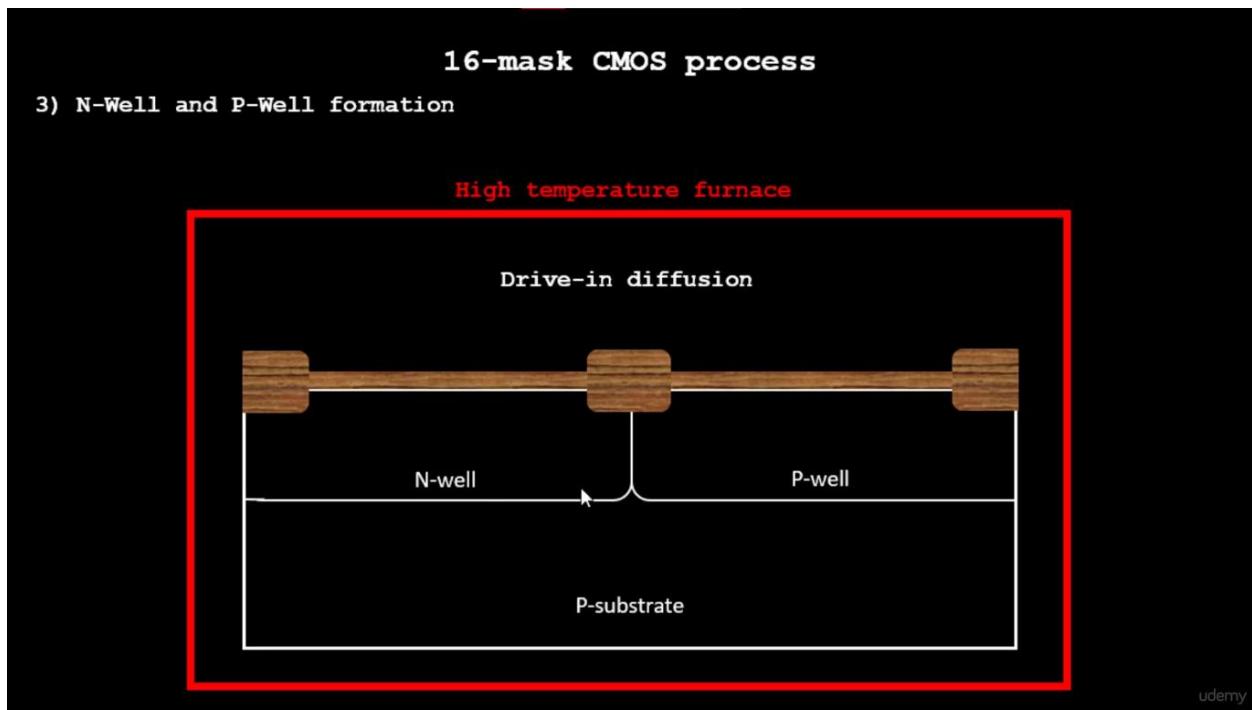
(Image credits:- VSDIAT)



(Image credits:- VSDIAT)

16-mask CMOS process

3) N-Well and P-Well formation



udemy

(Image credits:- VSDIAT)

Threshold Voltage Equation:

$$V_t = V_{to} + \gamma(\sqrt{|-2\Phi_f + V_{sb}|} - \sqrt{|-2\Phi_f|})$$

Where

V_{to} = Threshold voltage at $V_{sb} = 0$, and is a function of manufacturing process

γ = body effect coefficient, expresses the impact of changes in body bias V_{sb} (Unit is $V^{0.5}$)

Φ_f = Fermi Potential

$$\gamma = \frac{\sqrt{2qNA\epsilon_{si}}}{C_{ox}}$$

ϵ_{si} = relative permittivity of silicon = 11.7

N_A = doping concentration

q = charge of the electron

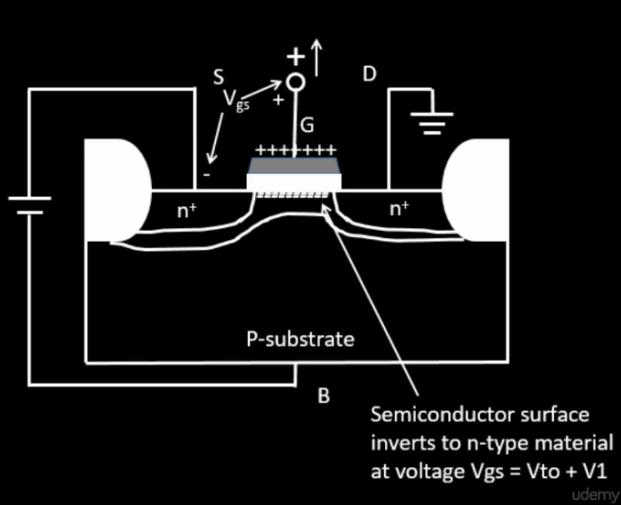
C_{ox} = oxide capacitance

$$\Phi_f = -\Phi_T * \ln \frac{N_A}{n_i}$$

n_i = intrinsic doping parameter for the substrate

Snippet from "Circuit design and SPICE simulation" course

$V_{sb} = +ve$ value



udemy

(Image credits:- VSDIAT)

Threshold Voltage Equation:

Snippet from "Circuit design and SPICE simulation" course

$$V_t = V_{to} + \gamma(\sqrt{|-2\Phi_f + V_{sb}|} - \sqrt{|-2\Phi_f|})$$

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2 important terms for gate formation, as they control V_t

ϵ_{si} = relative permittivity of silicon = 11.7

N_A = doping concentration

q = charge of the electron

C_{ox} = oxide capacitance

$$\Phi_f = -\Phi_T * \ln \frac{N_A}{n_i}$$

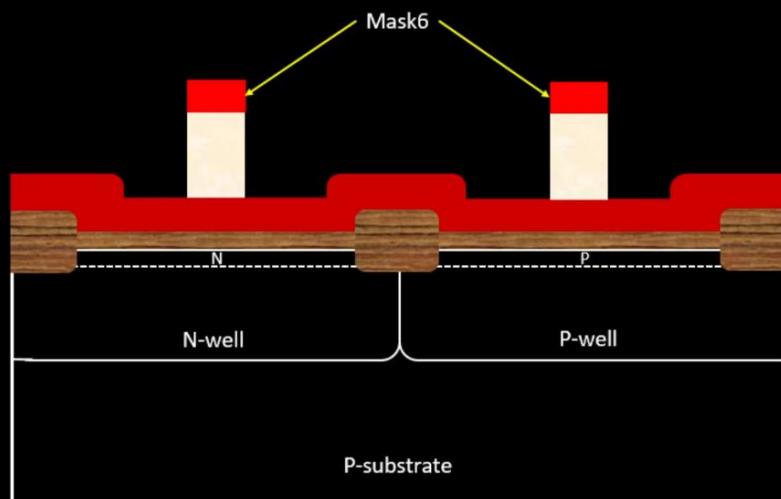
n_i = intrinsic doping parameter for the substrate

udemy

(Image credits:- VSDIAT)

16-mask CMOS process

4) Formation of 'gate'

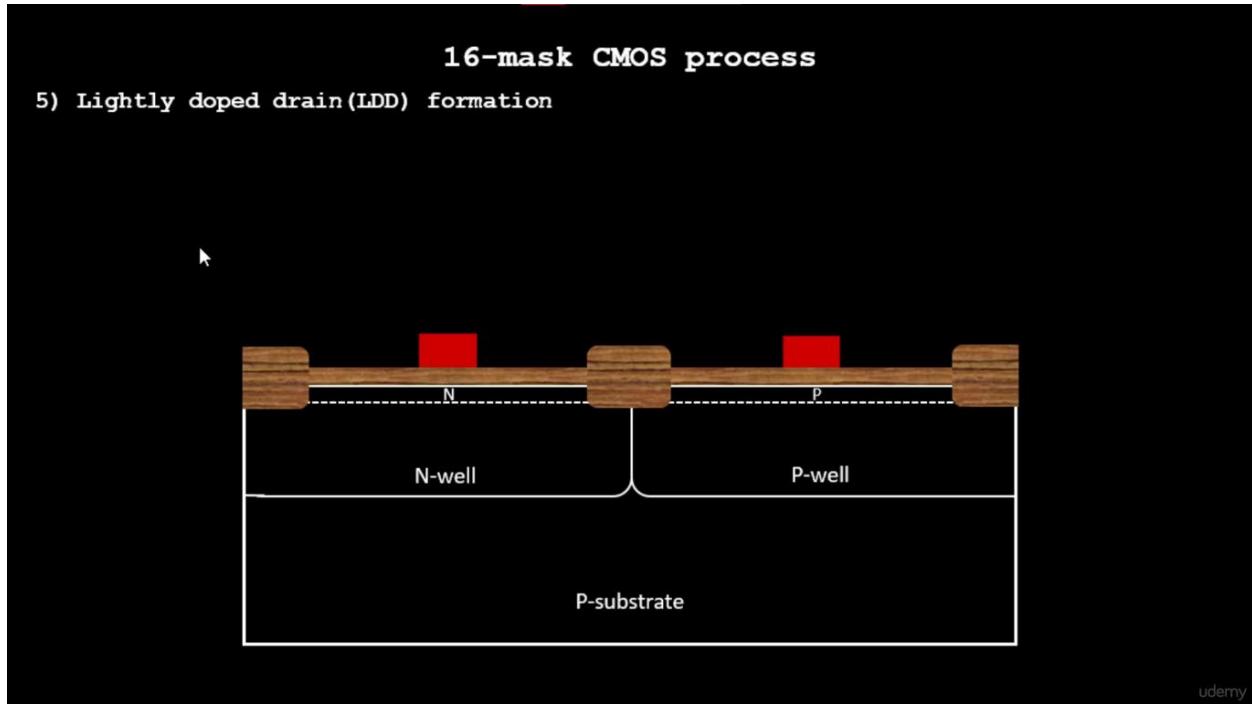


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(Image credits:- VSDIAT)

16-mask CMOS process

5) Lightly doped drain(LDD) formation



udemy

(Image credits:- VSDIAT)

Threshold Voltage Equation:

Snippet from "Circuit design and SPICE simulation" course

$$V_t = V_{to} + \gamma(\sqrt{|-2\Phi_f + V_{sb}|} - \sqrt{|-2\Phi_f|})$$

Where

V_{to} = Threshold voltage at $V_{sb} = 0$, and is a function of manufacturing process

V_{sb} = +ve value

γ = body effect coefficient, expresses the impact of changes in body bias V_{sb} (Unit is $V^{0.5}$)

Φ_f = Fermi Potential

$$\gamma = \frac{\sqrt{2qNA\epsilon_{si}}}{C_{ox}}$$

ϵ_{si} = relative permittivity of silicon = 11.7

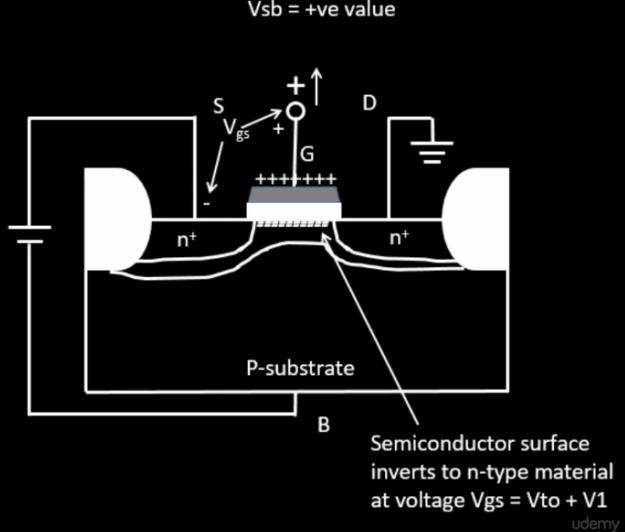
N_A = doping concentration

q = charge of the electron

C_{ox} = oxide capacitance

$$\Phi_f = -\Phi_T * \ln \frac{N_A}{n_i}$$

n_i = intrinsic doping parameter for the substrate



Semiconductor surface
inverts to n-type material
at voltage $V_{gs} = V_{to} + V_1$

udemy

(Image credits:- VSDIAT)

Threshold Voltage Equation:

Snippet from "Circuit design and SPICE simulation" course

$$V_t = V_{to} + \gamma(\sqrt{|-2\Phi_f + V_{sb}|} - \sqrt{|-2\Phi_f|})$$

Where

V_{to} = Threshold voltage at $V_{sb} = 0$, and is a function of manufacturing process

γ = body effect coefficient, expresses the impact of changes in body bias V_{sb} (Unit is $V^{0.5}$)

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$$\gamma = \frac{\sqrt{2qNA\epsilon_{si}}}{C_{ox}}$$



2 important terms for gate formation, as they control V_t

ϵ_{si} = relative permittivity of silicon = 11.7

N_A = doping concentration

q = charge of the electron

C_{ox} = oxide capacitance

$$\Phi_f = -\Phi_T * \ln \frac{N_A}{n_i}$$

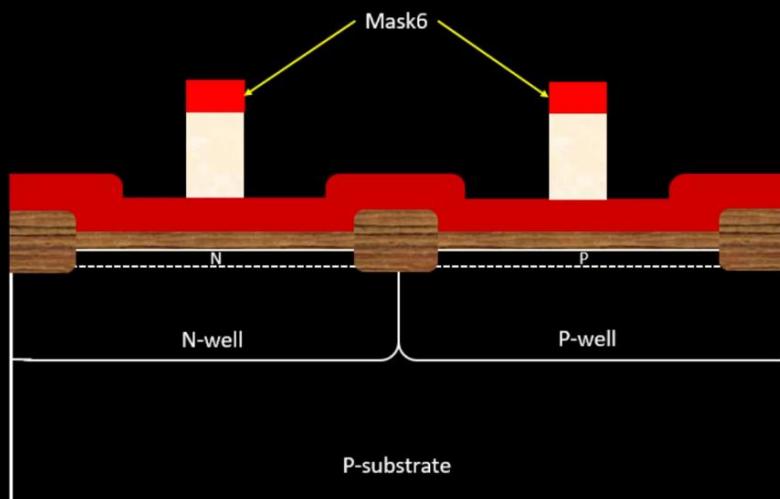
n_i = intrinsic doping parameter for the substrate

udemy

(Image credits:- VSDIAT)

16-mask CMOS process

4) Formation of 'gate'

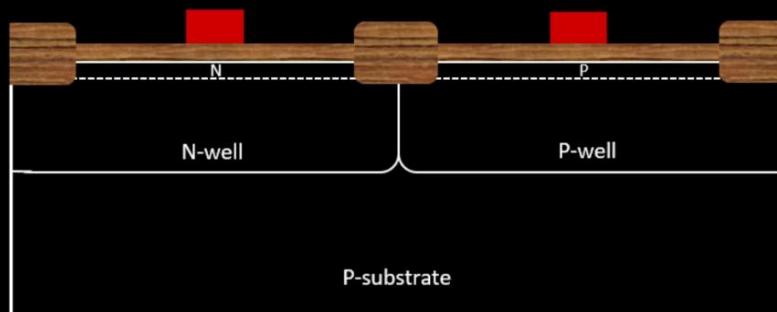


udemy

(Image credits:- VSDIAT)

16-mask CMOS process

5) Lightly doped drain(LDD) formation

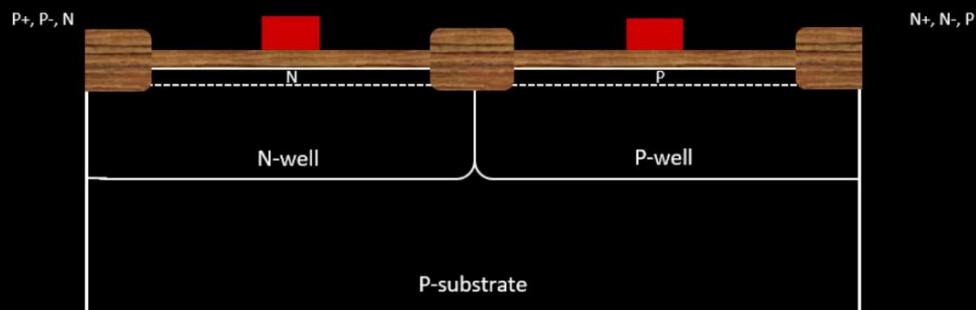


udemy

(Image credits:- VSDIAT)

16-mask CMOS process

5) Lightly doped drain(LDD) formation



udemy

(Image credits:- VSDIAT)

16-mask CMOS process

5) Lightly doped drain(LDD) formation

2 reasons for this

- Hot electron effect
- Short channel effect

Electric field $E=V/d$

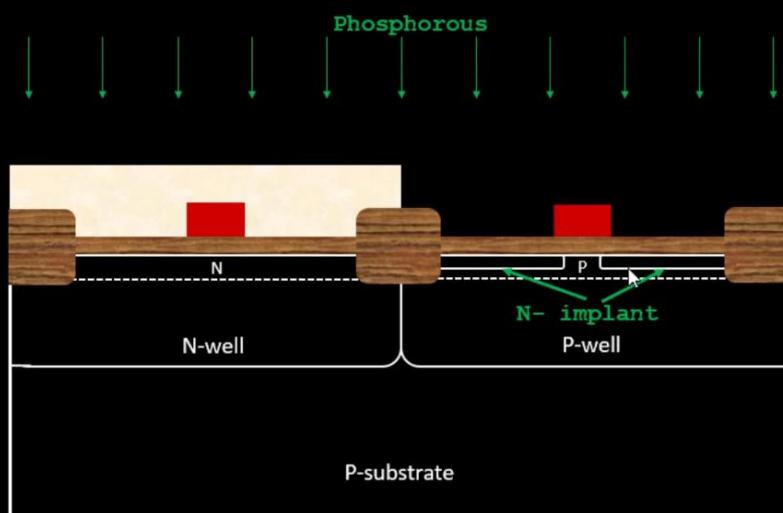
High energy carriers break Si-Si bonds
3.2eV barrier b/w Si conduction band
SiO₂ conduction band

udemy

(Image credits:- VSDIAT)

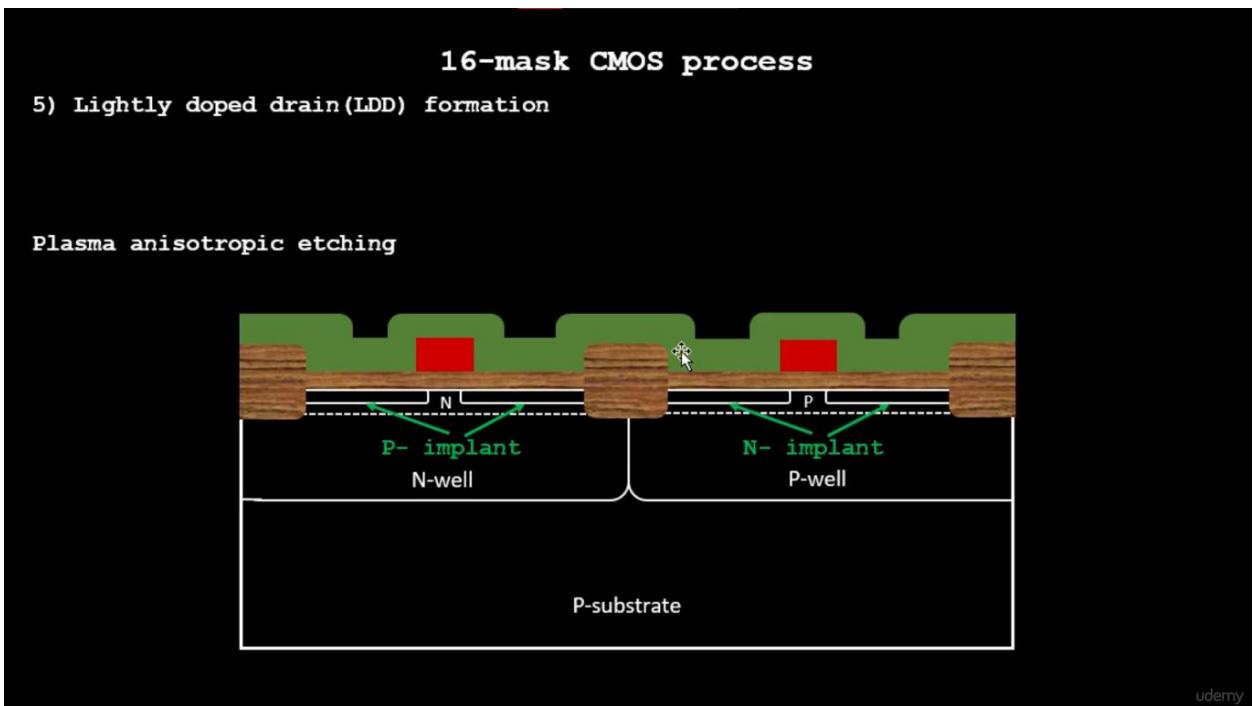
16-mask CMOS process

5) Lightly doped drain(LDD) formation

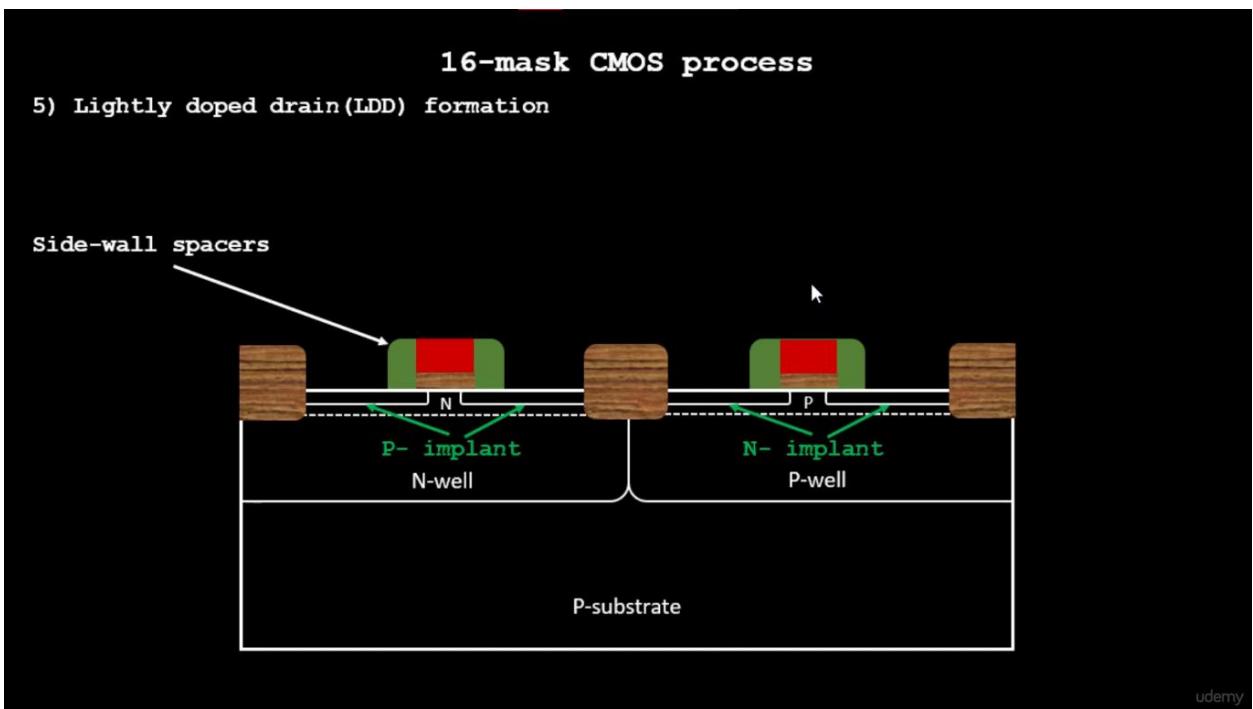


udemy

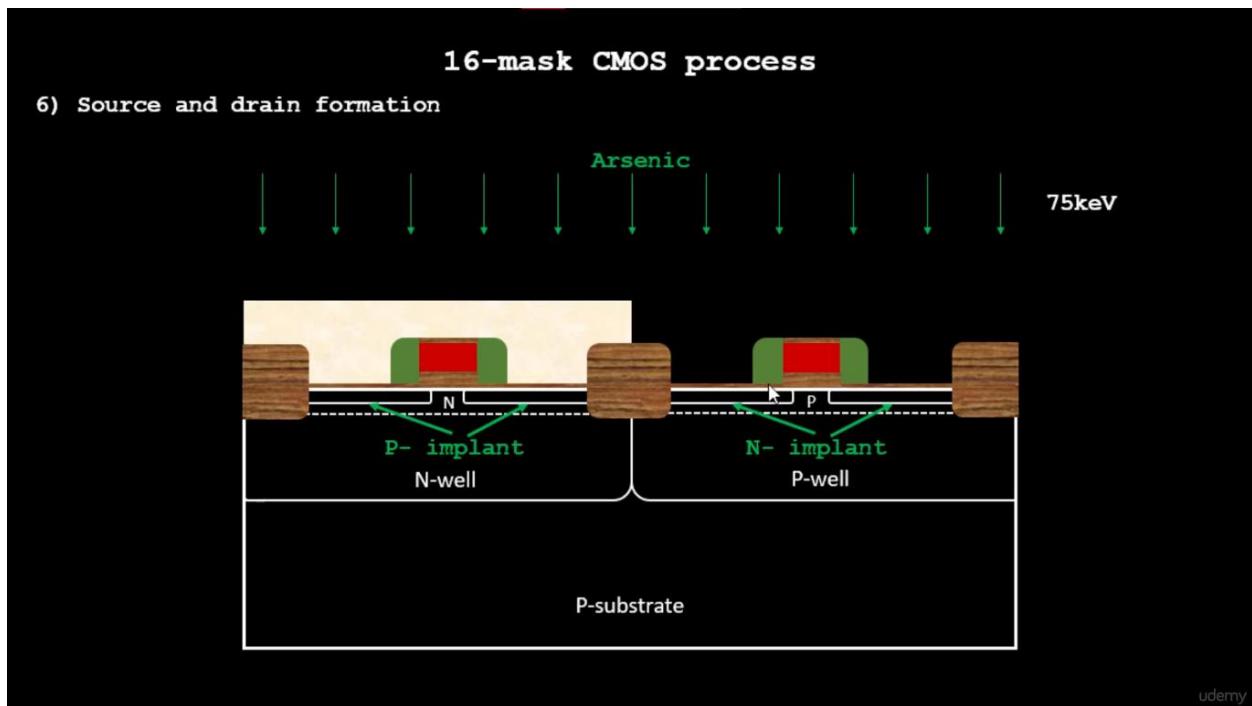
(Image credits:- VSDIAT)



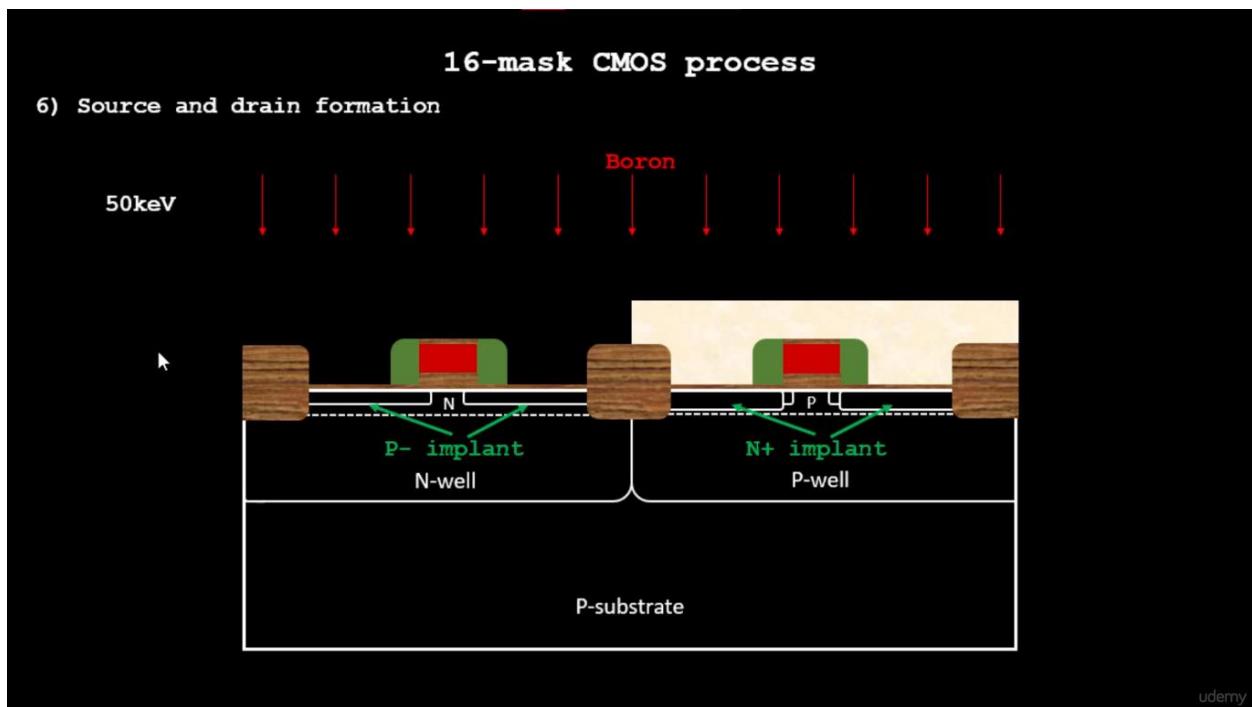
(Image credits:- VSDIAT)



(Image credits:- VSDIAT)



(Image credits:- VSDIAT)

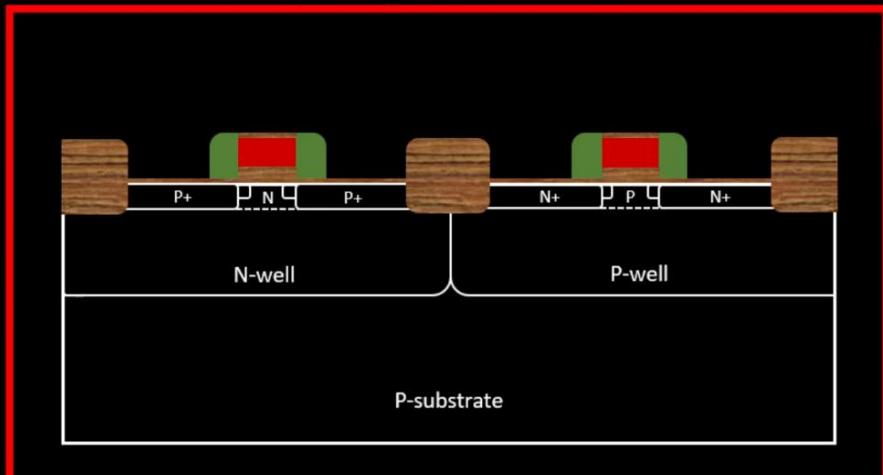


(Image credits:- VSDIAT)

16-mask CMOS process

6) Source and drain formation

High temperature annealing High temperature furnace

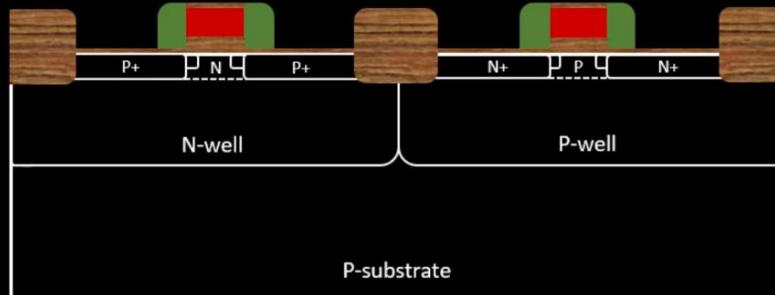


udemy

(Image credits:- VSDIAT)

16-mask CMOS process

7) Steps to form contacts and interconnects (local)



udemy

(Image credits:- VSDIAT)

16-mask CMOS process

7) Steps to form contacts and interconnects (local)

deposit titanium on wafer surface, using sputtering

substrate

Argon (Ar^+) gas

↑
↑
↑

Ti

udemy

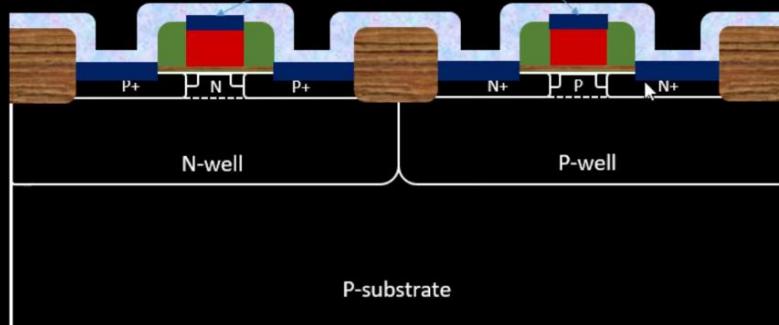
(Image credits:- VSDIAT)

16-mask CMOS process

7) Steps to form contacts and interconnects (local)

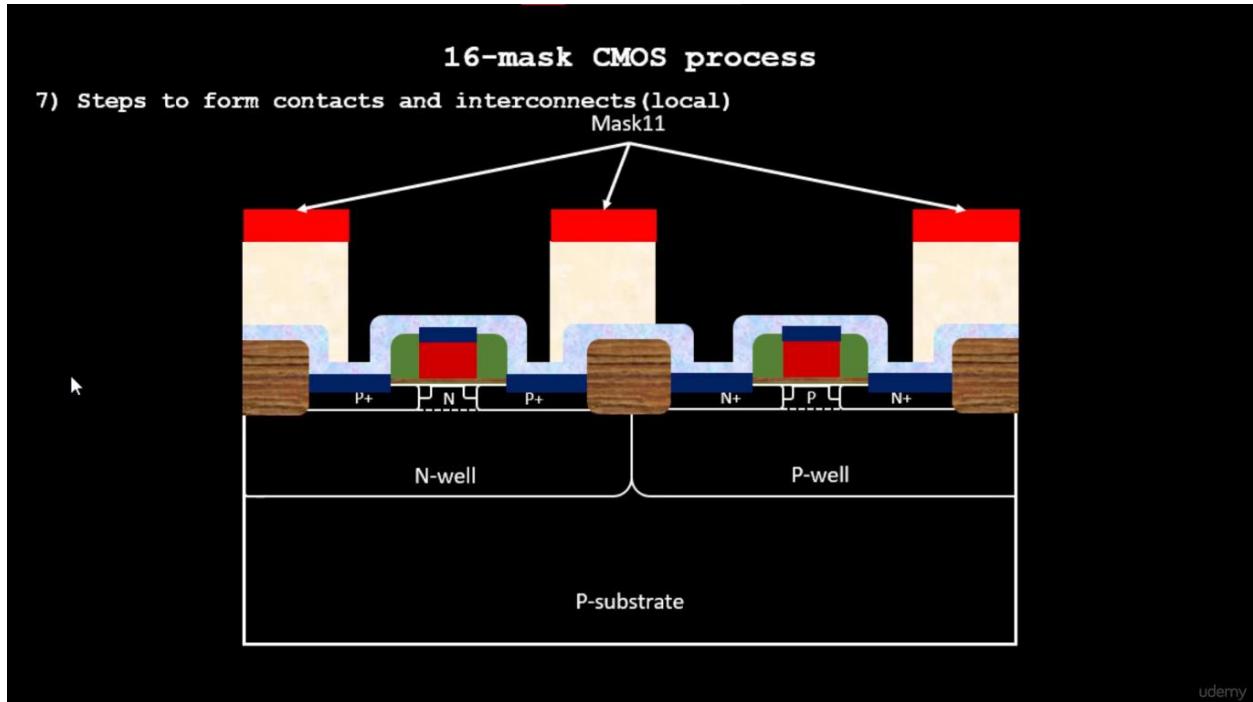
Wafer heated at about $650-700^\circ\text{C}$ in N_2 ambient for 60sec

Result = low resistant TiSi_2

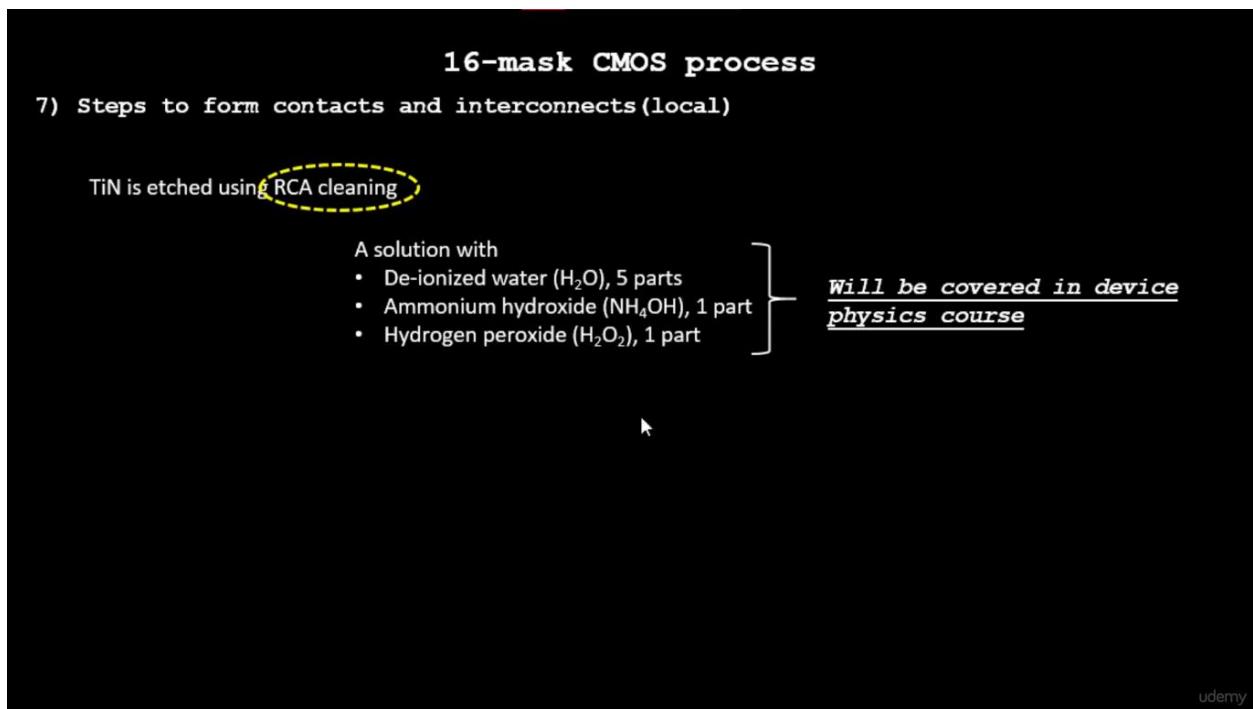


udemy

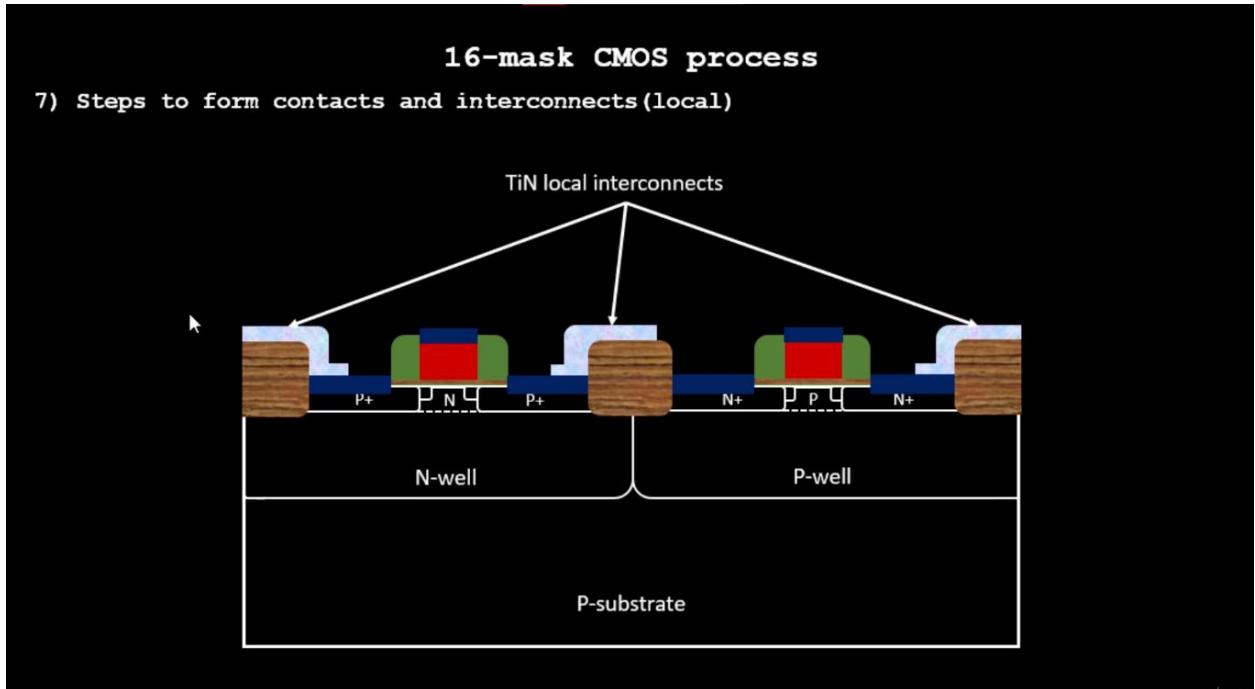
(Image credits:- VSDIAT)



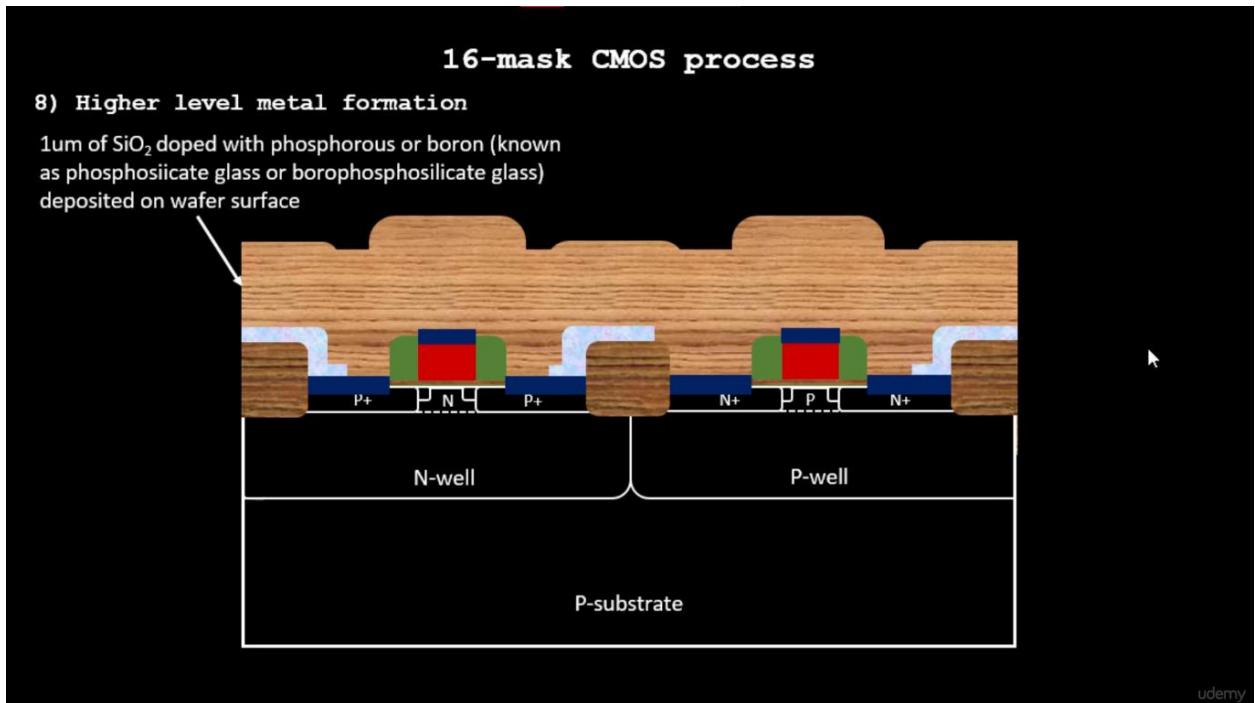
(Image credits:- VSDIAT)



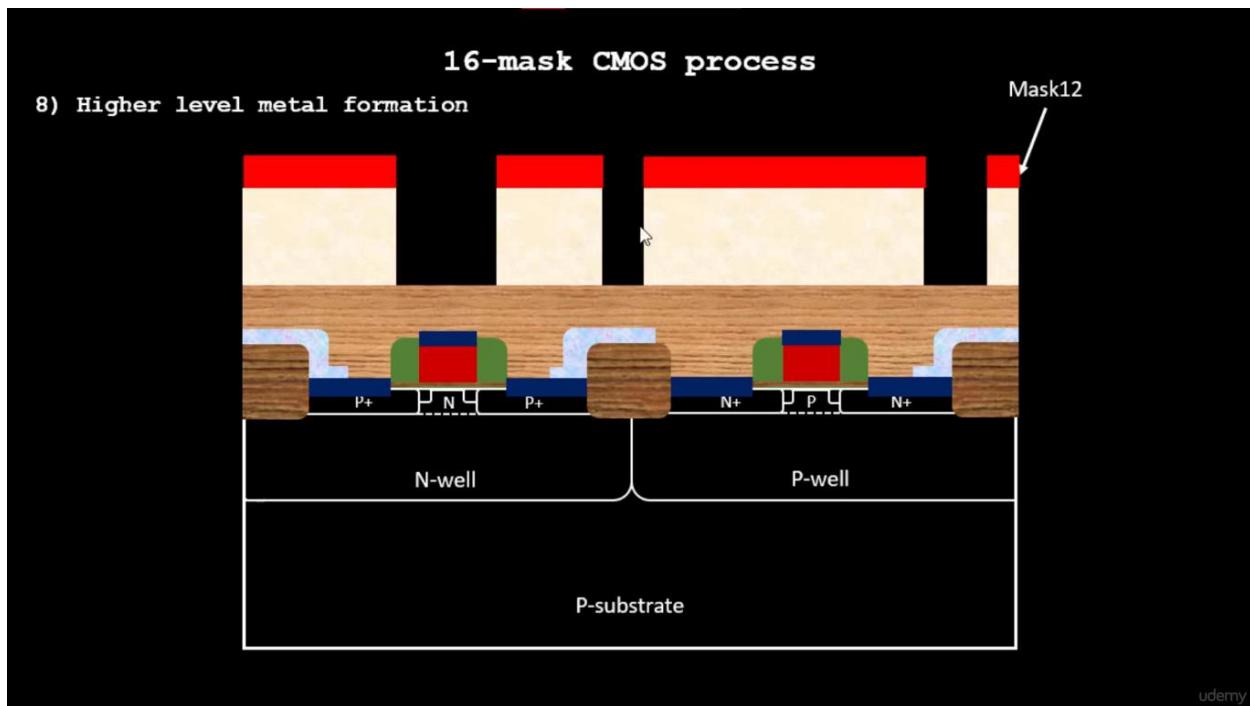
(Image credits:- VSDIAT)



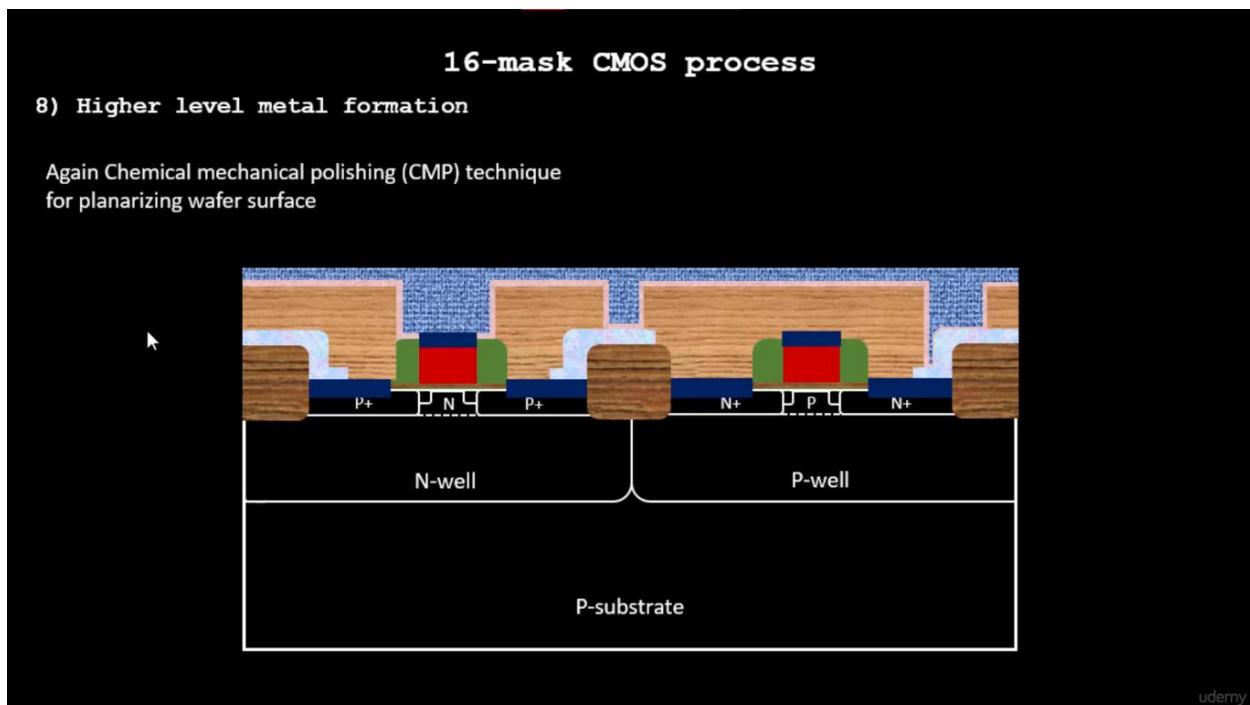
(Image credits:- VSDIAT)



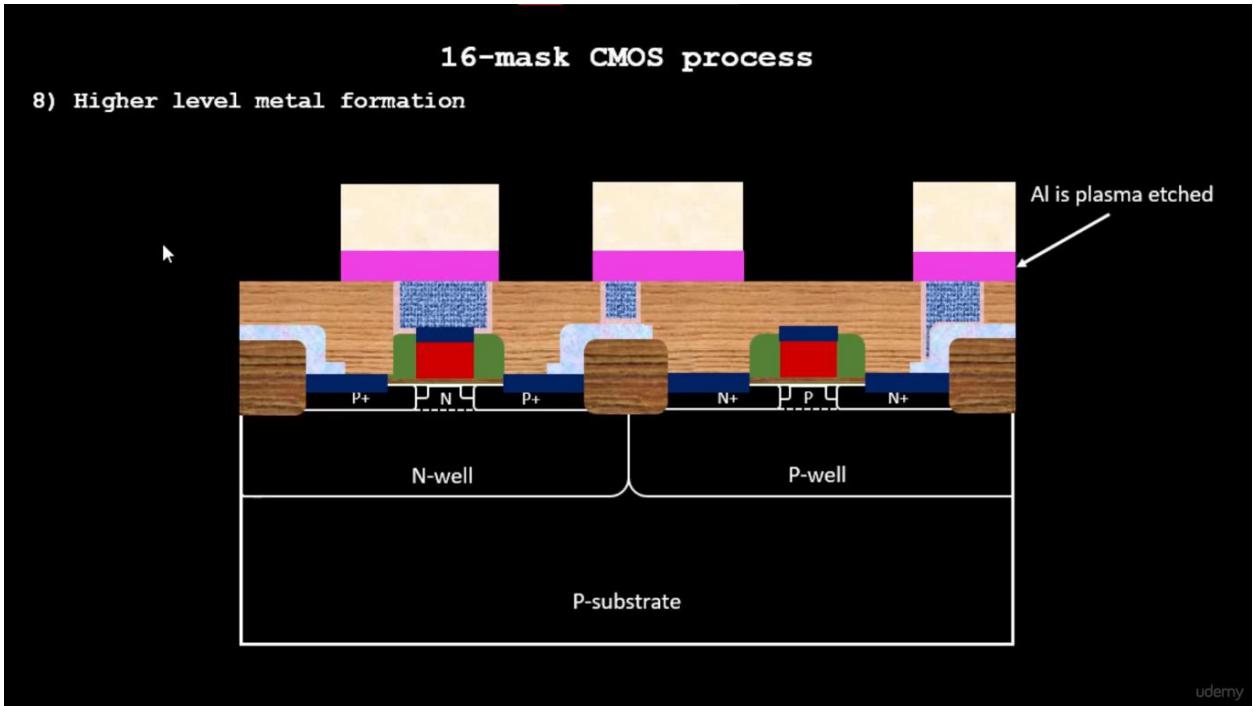
(Image credits:- VSDIAT)



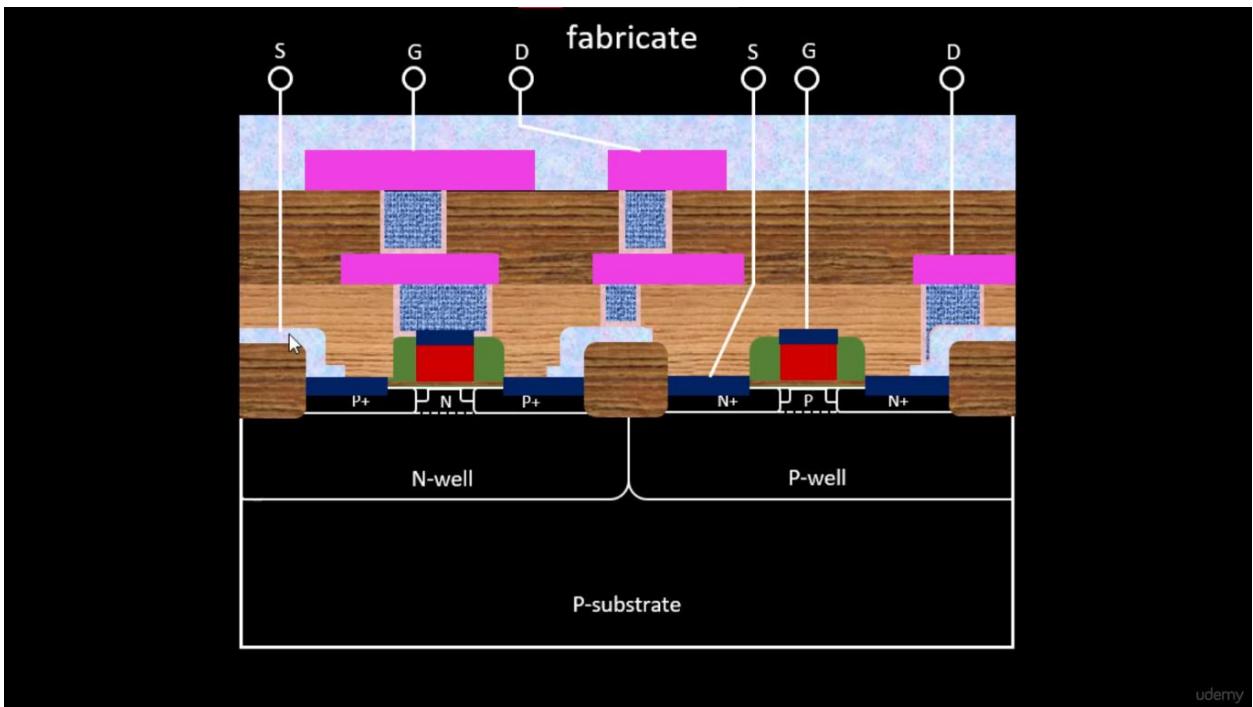
(Image credits:- VSDIAT)



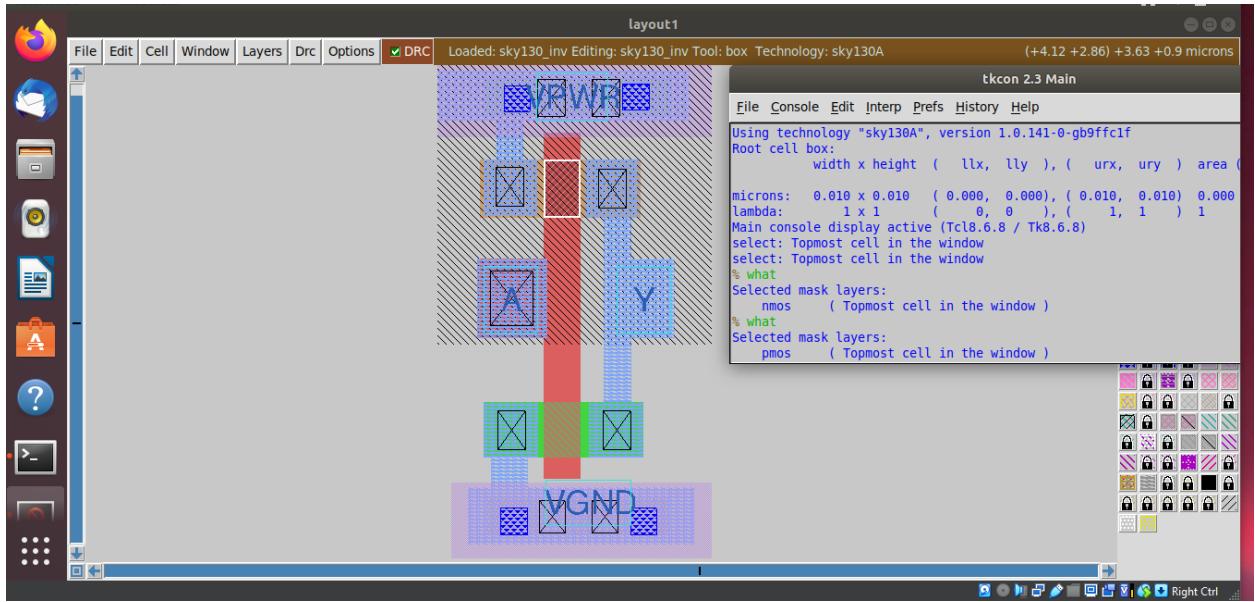
(Image credits:- VSDIAT)



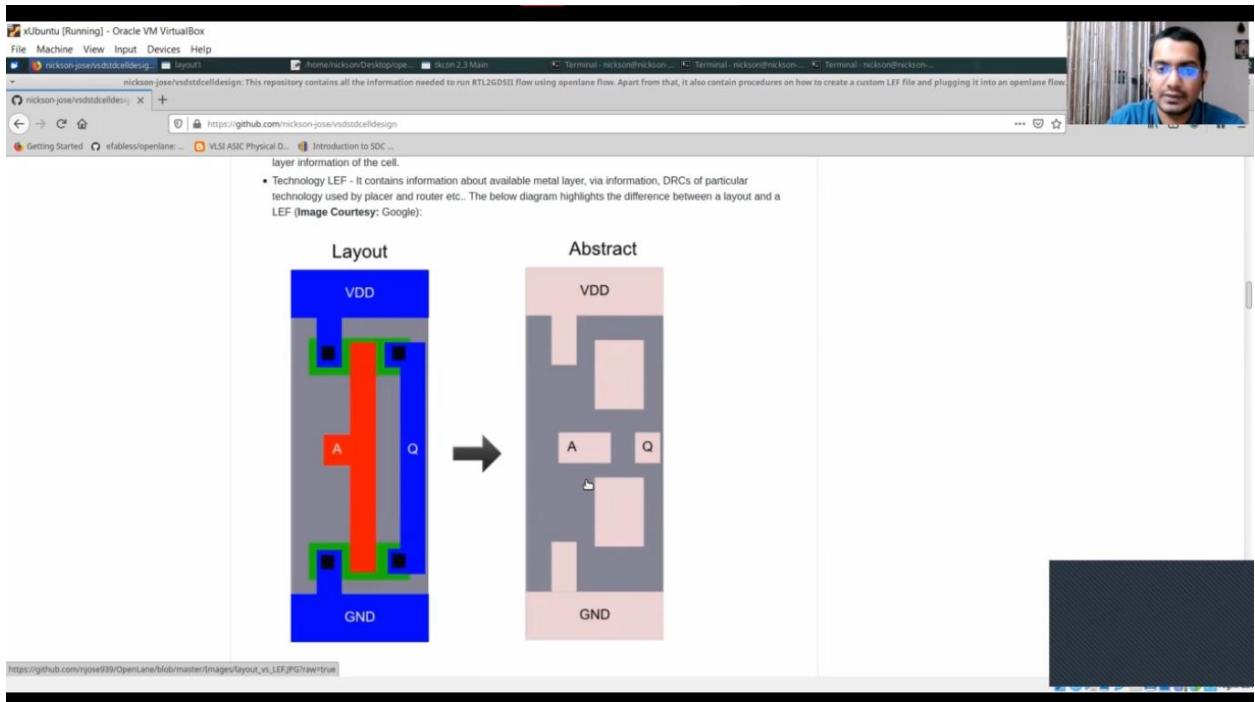
(Image credits:- VSDIAT)



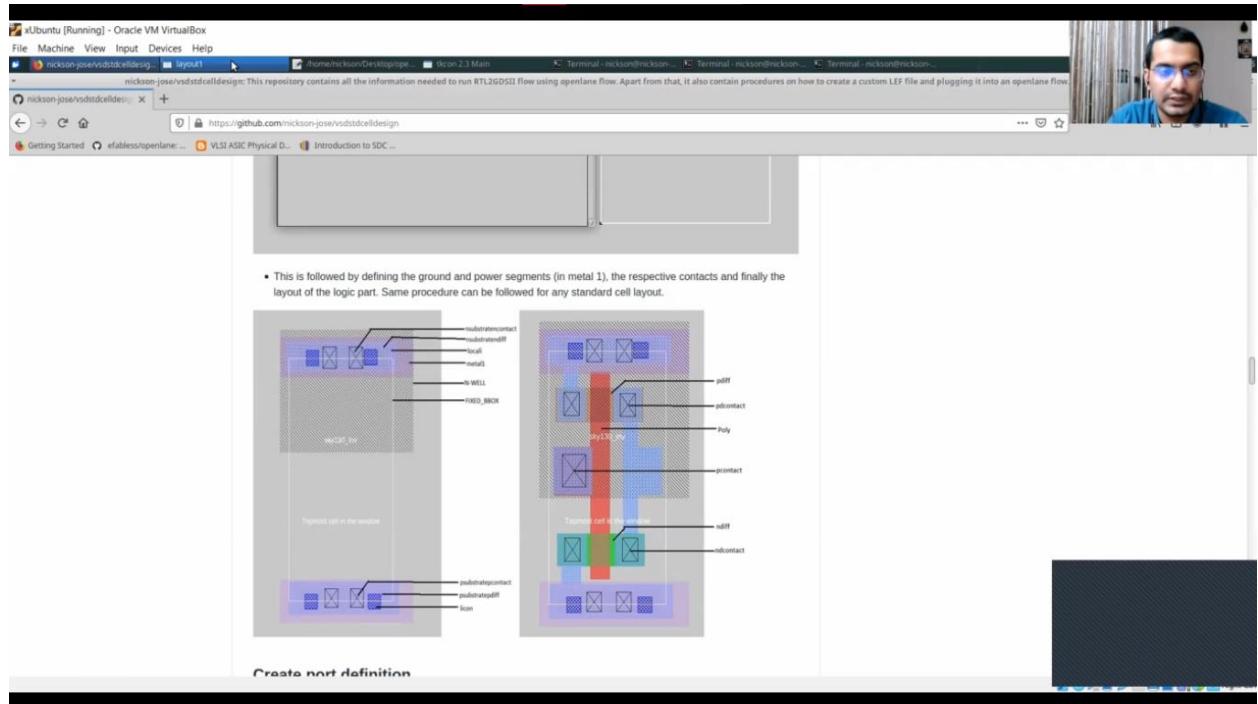
(Image credits:- VSDIAT)



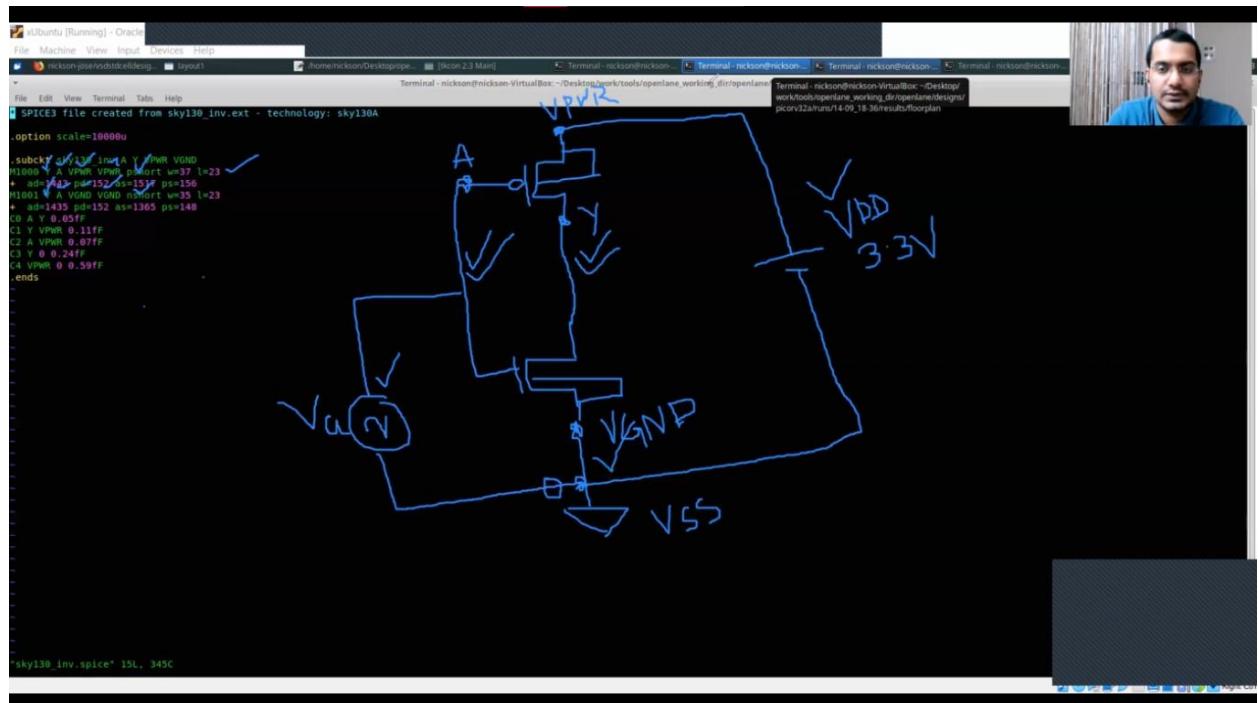
(Image credits:- AUTHOR)



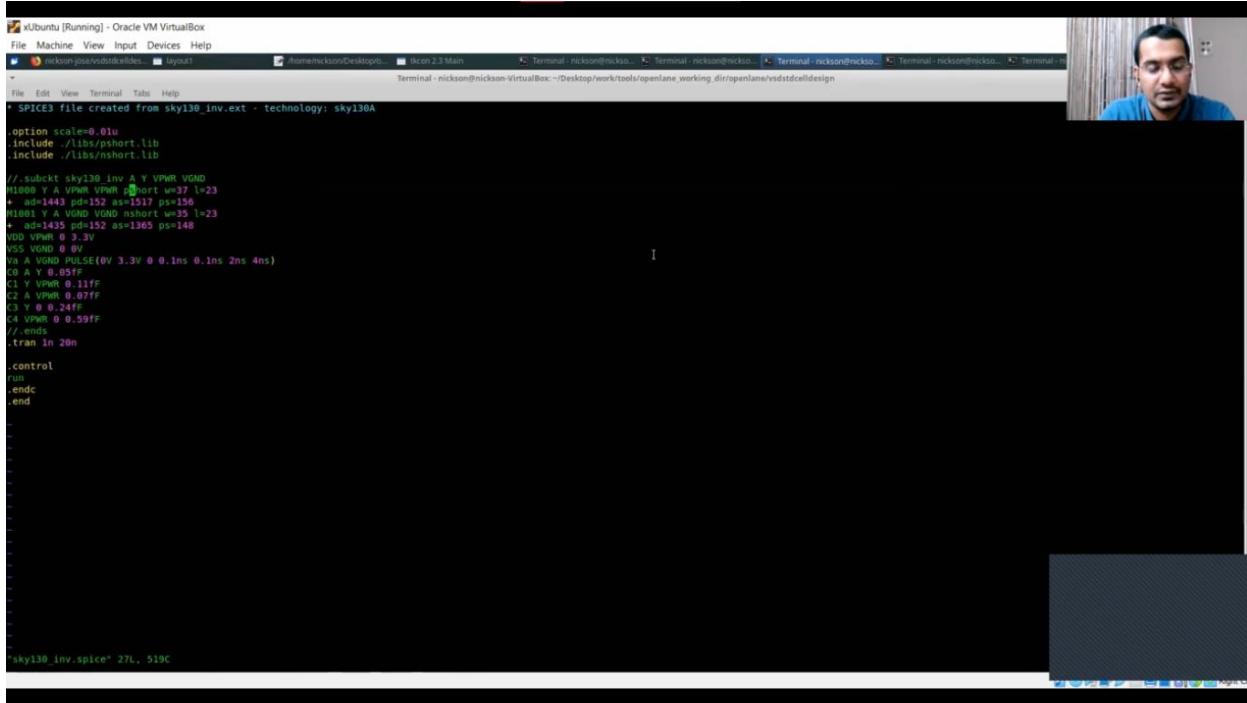
(Image credits:- VSBIAT)



(Image credits:- VSDIAT)



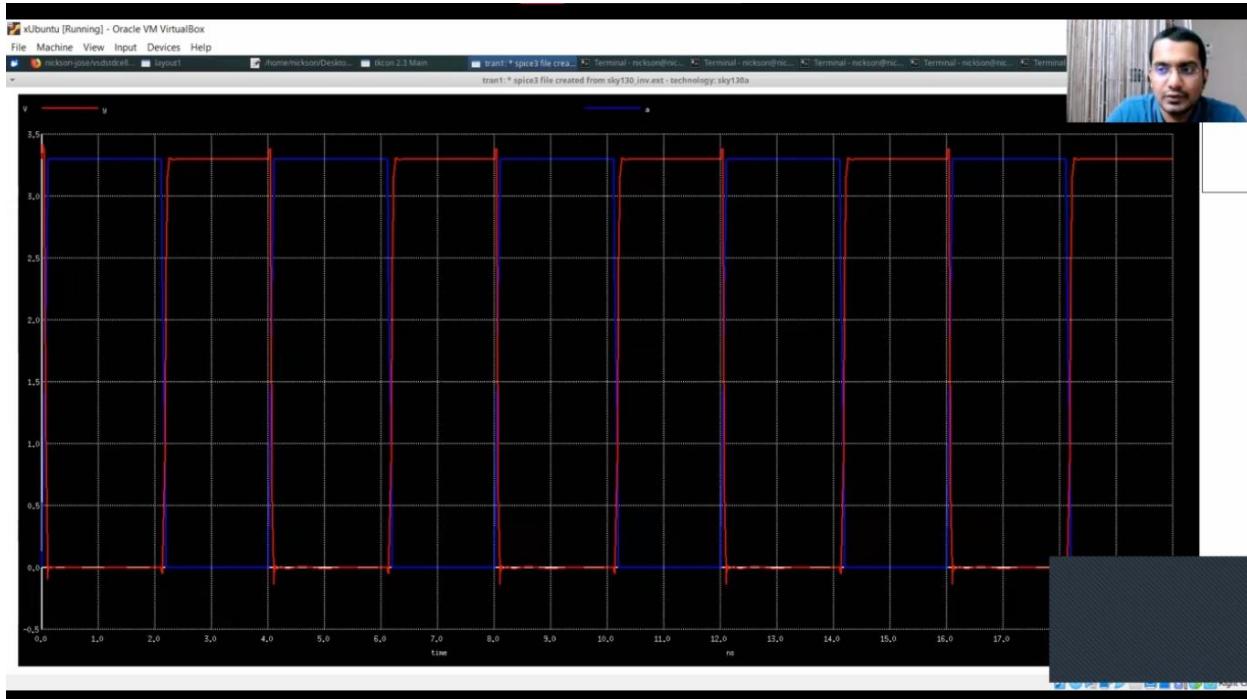
(Image credits:- VSDIAT)



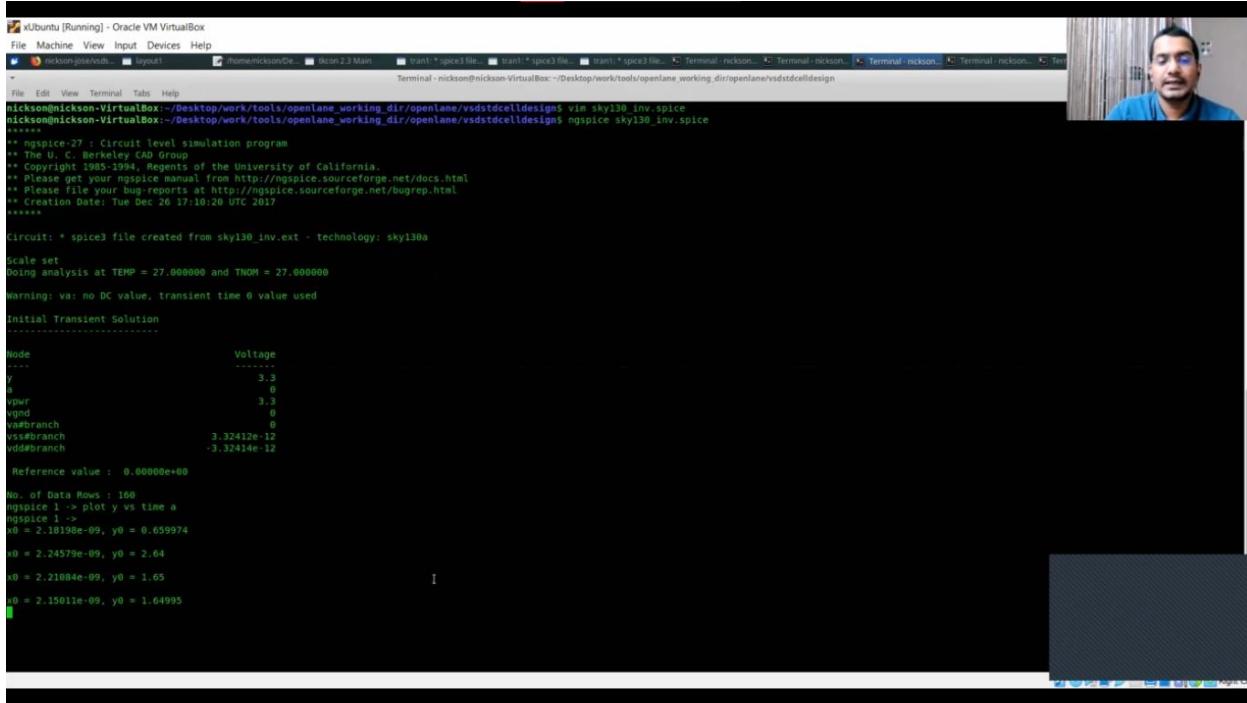
```
xUbuntu [Running] - Oracle VM VirtualBox
File Machine View Input Devices Help
File nickson@nickson-VirtualBox... layout /home/nickson/Desktop... icon 2.3 Main Terminal - nickson@nickson... Terminal - nickson@nickson... Terminal - nickson@nickson... Terminal - nickson@nickson... Terminal - nickson@nickson...
File Edit View Terminal Tabs Help
* SPICE3 file created from sky130_inv.ext - technology: sky130a
.option scale=0.1m
.include ./libs/pshort.lib
.include ./libs/nshort.lib
// Subckt sky130_inv A Y VDD VSSD VGND
M1000 Y A VPMR VPMR pshort w=37 l=23
+ ad=1443 pd=152 as=1517 ps=156
M1001 Y A VGND VGND nshort w=35 l=23
+ ad=1435 pd=152 as=1365 ps=148
VDD VPMR 0 3.3V
VSS VGND 0 0V
V1000 VPMR VPMR DC 3.3V 0 0.1ns 0.1ns 2ns 4ns
C0 A Y 0.05FF
C1 Y VPMR 0.11FF
C2 A VPMR 0.07FF
C3 Y 0 0.24FF
C4 VPMR 0 0.59FF
// Transistor models
.tran 1n 20n
.control
run
.endc
.end

"sky130_inv.spice" 27L, 519C
```

(Image credits:- VSDIAT)



(Image credits:- VSDIAT)

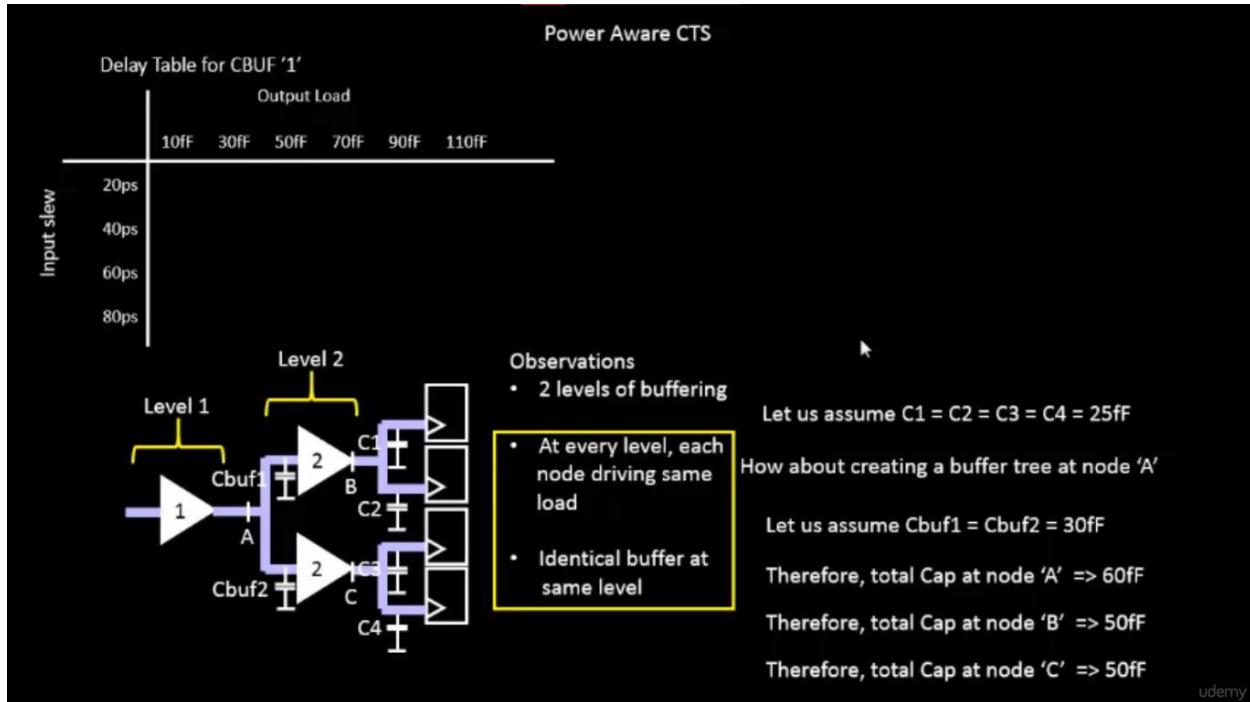


```
xUbuntu [Running] - Oracle VM VirtualBox
File Machine View Input Devices Help
File Edit View Terminal Tabs Help
nickson@nickson-VirtualBox:~/Desktop/work/tools/openlane_working_dir/openlane/vsstdcelldesign$ vim sky130_inv.spice
nickson@nickson-VirtualBox:~/Desktop/work/tools/openlane_working_dir/openlane/vsstdcelldesign$ ngspice sky130_inv.spice
*** ngspice-27.1 Circuit level simulation program
*** The U. C. Berkeley CAD Group
*** Copyright 1985-1994, Regents of the University of California.
*** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
*** Please file your bug reports at http://ngspice.sourceforge.net/bugrep.html
*** Creation Date: Tue Dec 26 17:18:29 UTC 2017
****

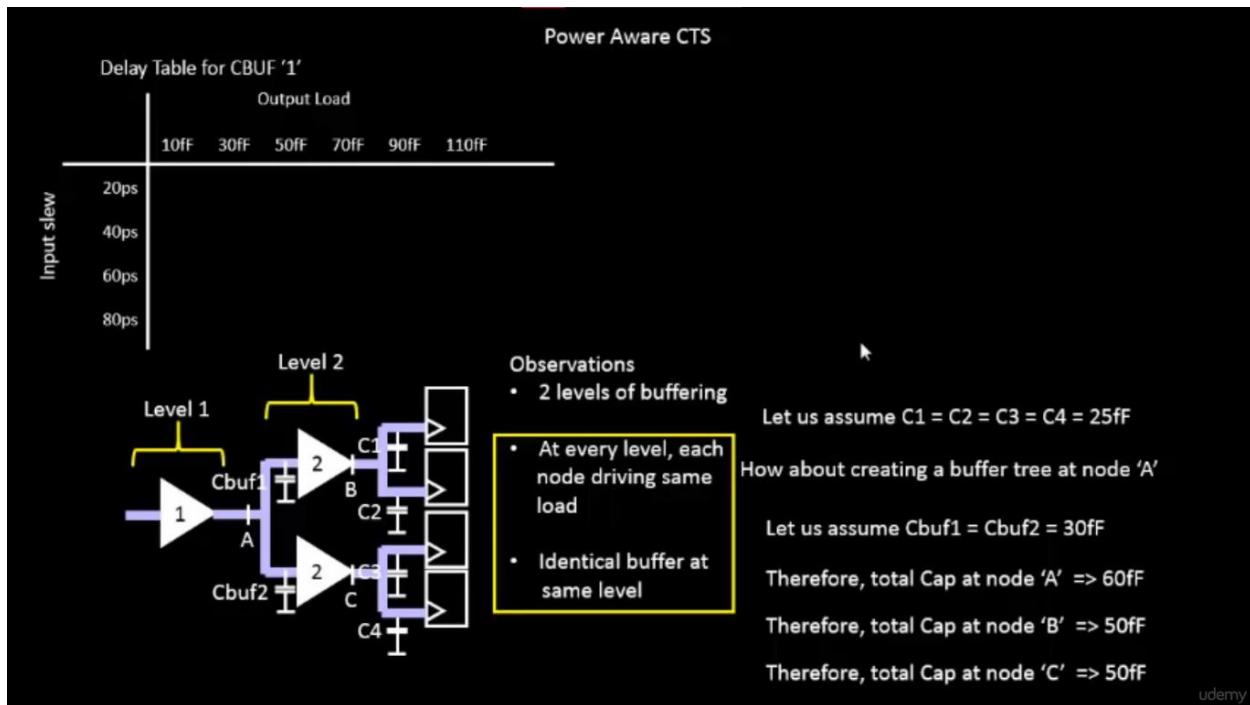
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vppur        3.3
vqnd         0
vddbranch    0
vss#branch   3.32412e-12
vddatbranch -3.32414e-12
Reference value :  0.00000e+00
No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18198e-09, y0 = 0.659974
x0 = 2.24579e-09, y0 = 2.64
x0 = 2.21684e-09, y0 = 1.65
x0 = 2.15611e-09, y0 = 1.64995
```

(Image credits:- VSDIAT)

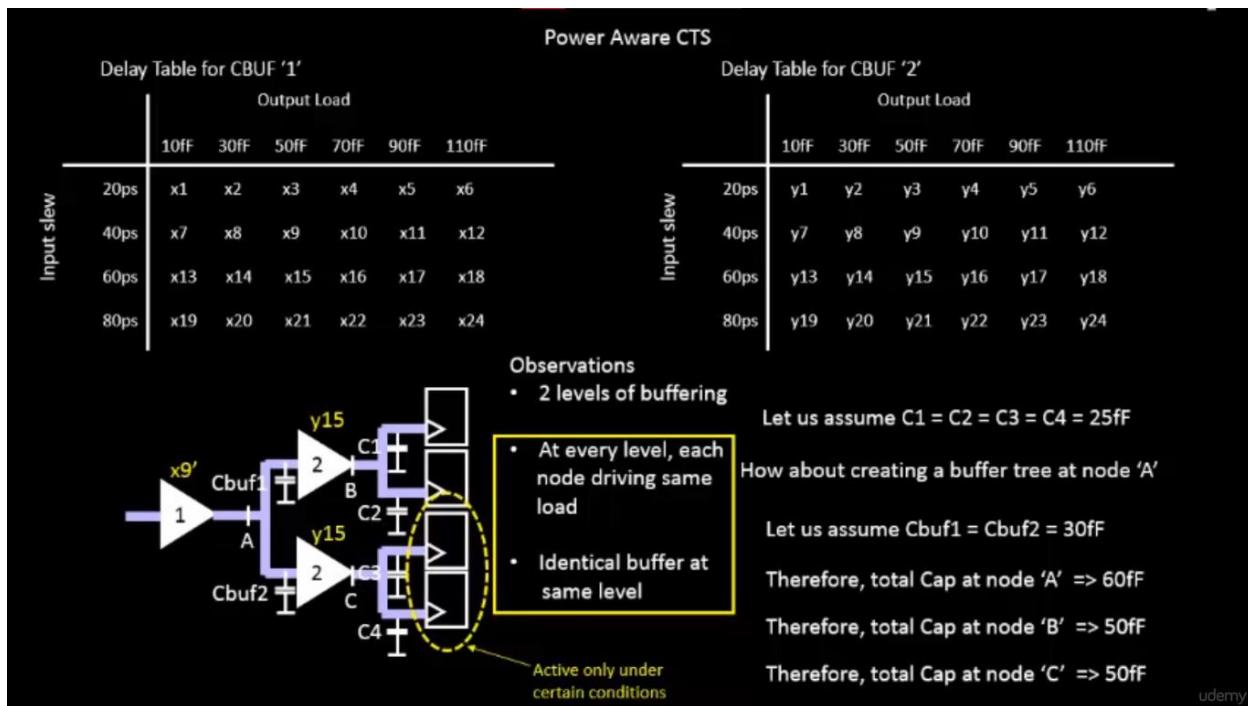
Pre-layout timing analysis and importance of good clock tree



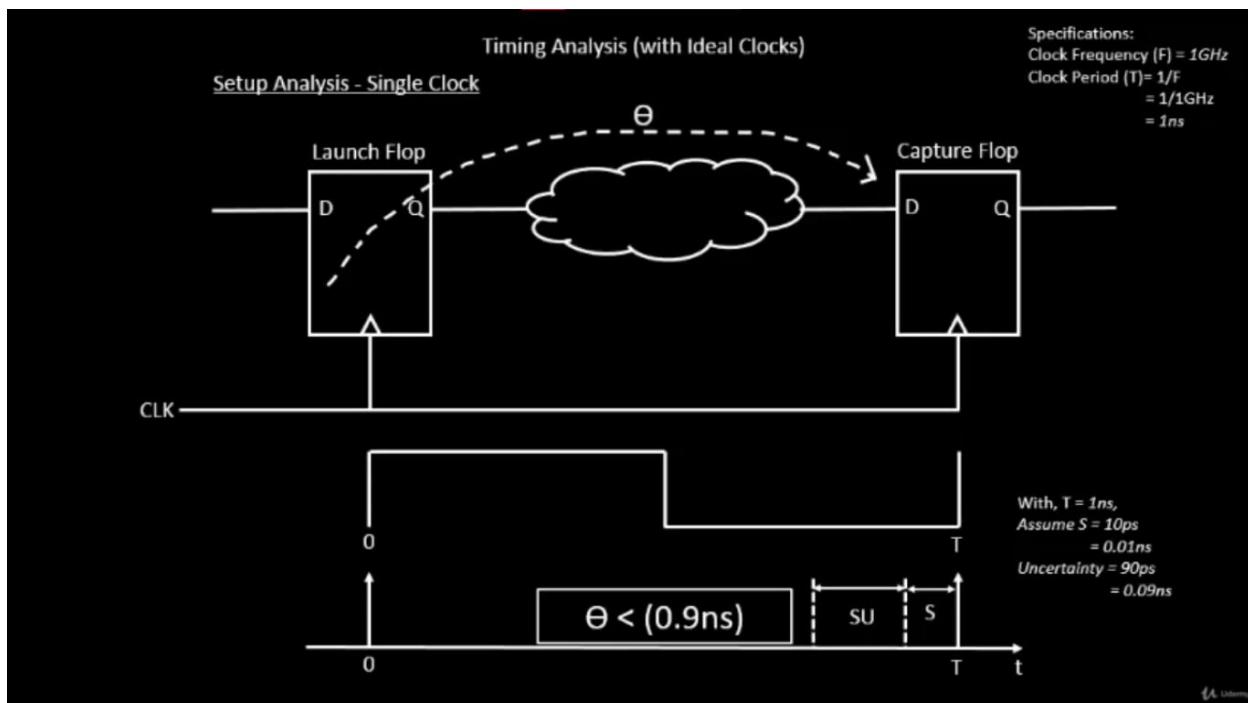
(Image credits:- VSDIAT)



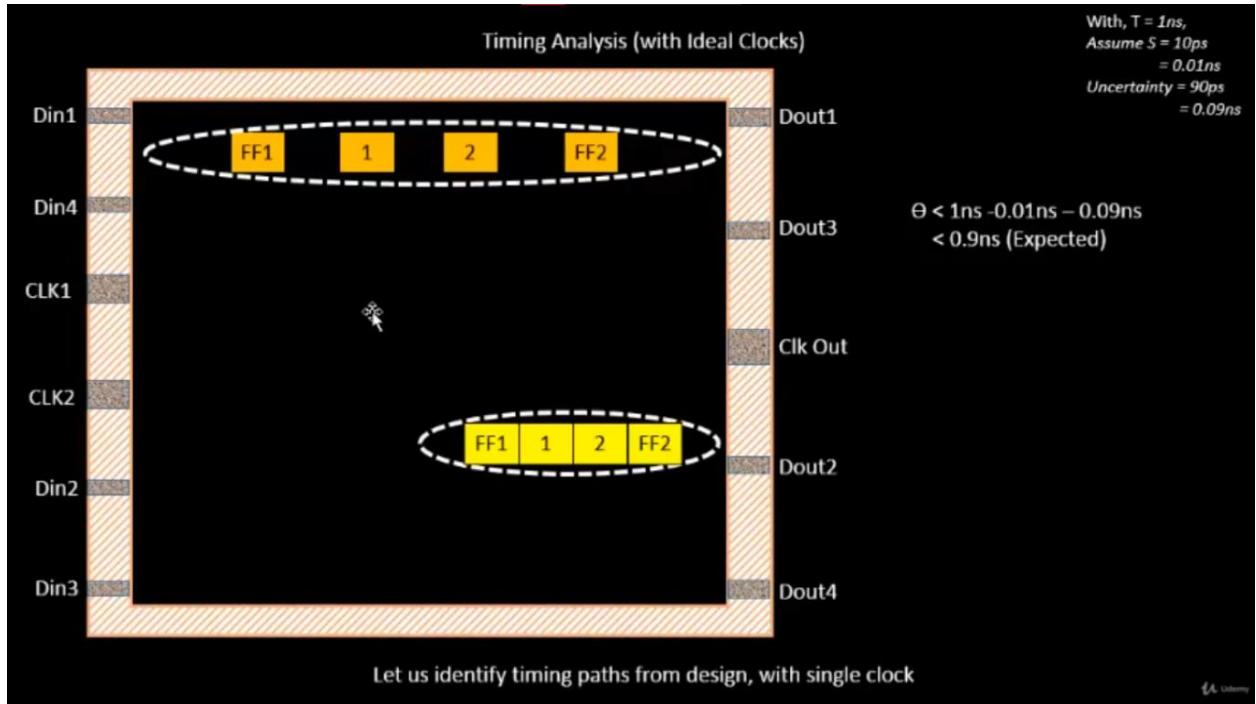
(Image credits:- VSDIAT)



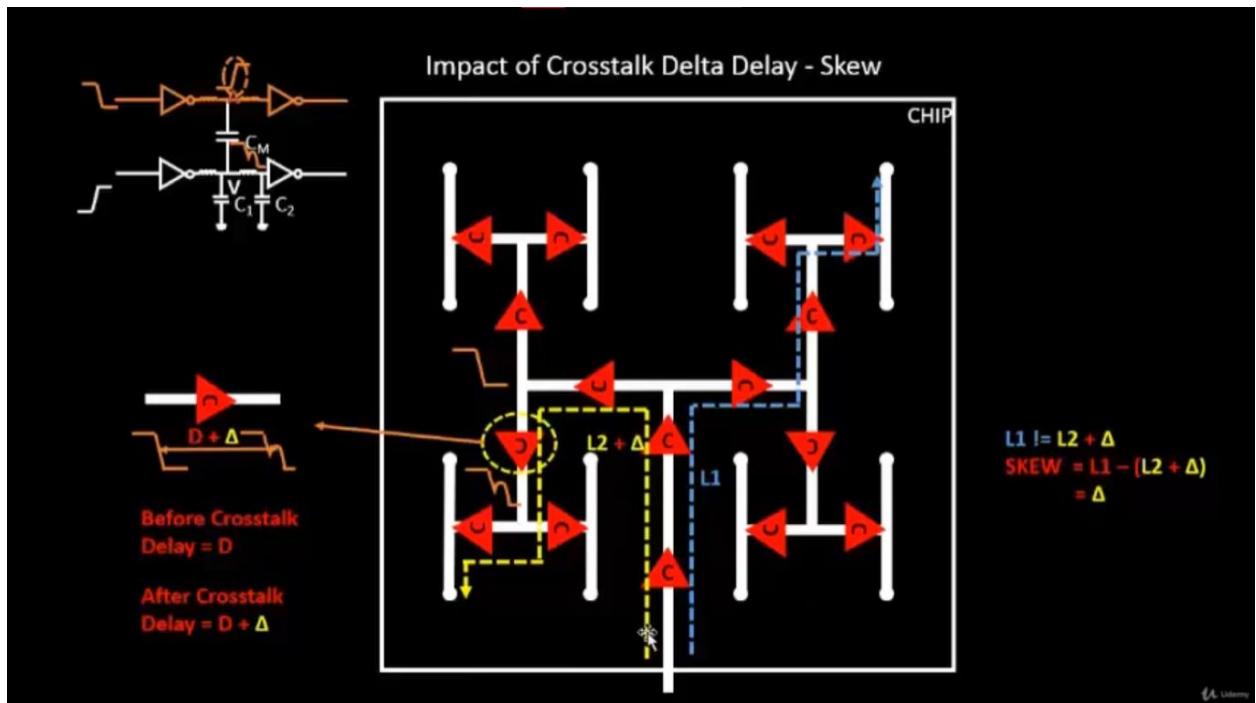
(Image credits:- VSDIAT)



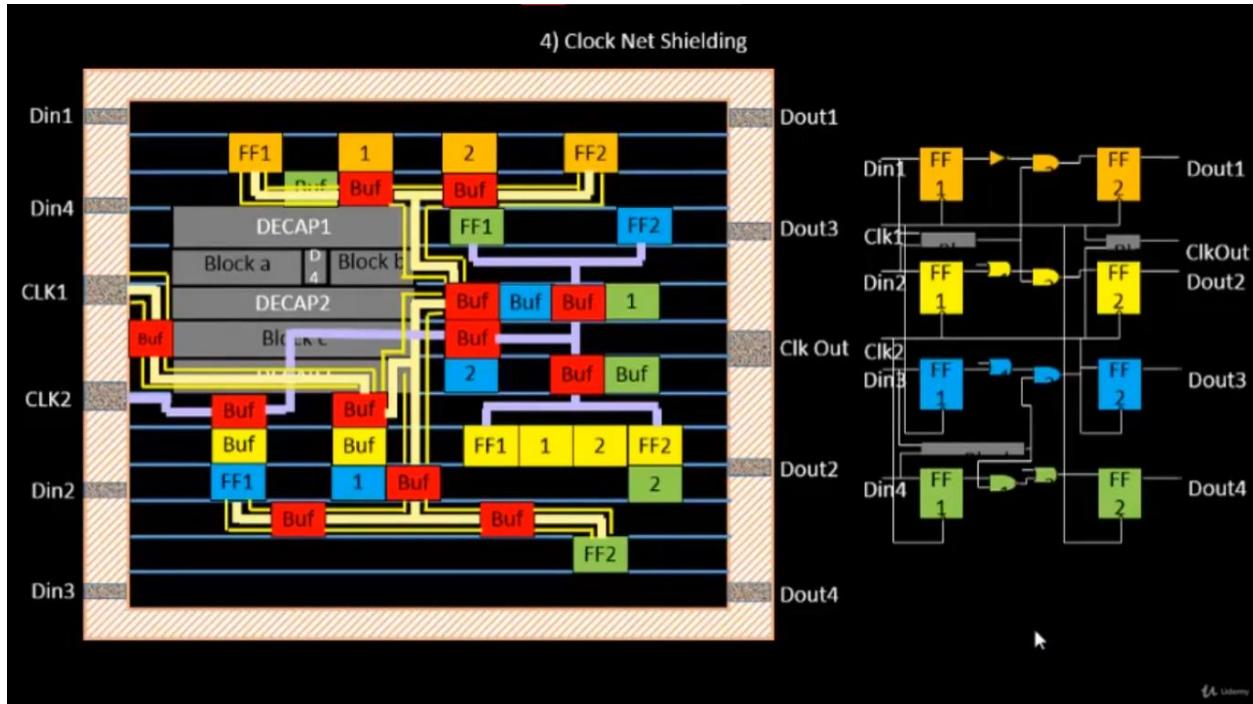
(Image credits:- VSDIAT)



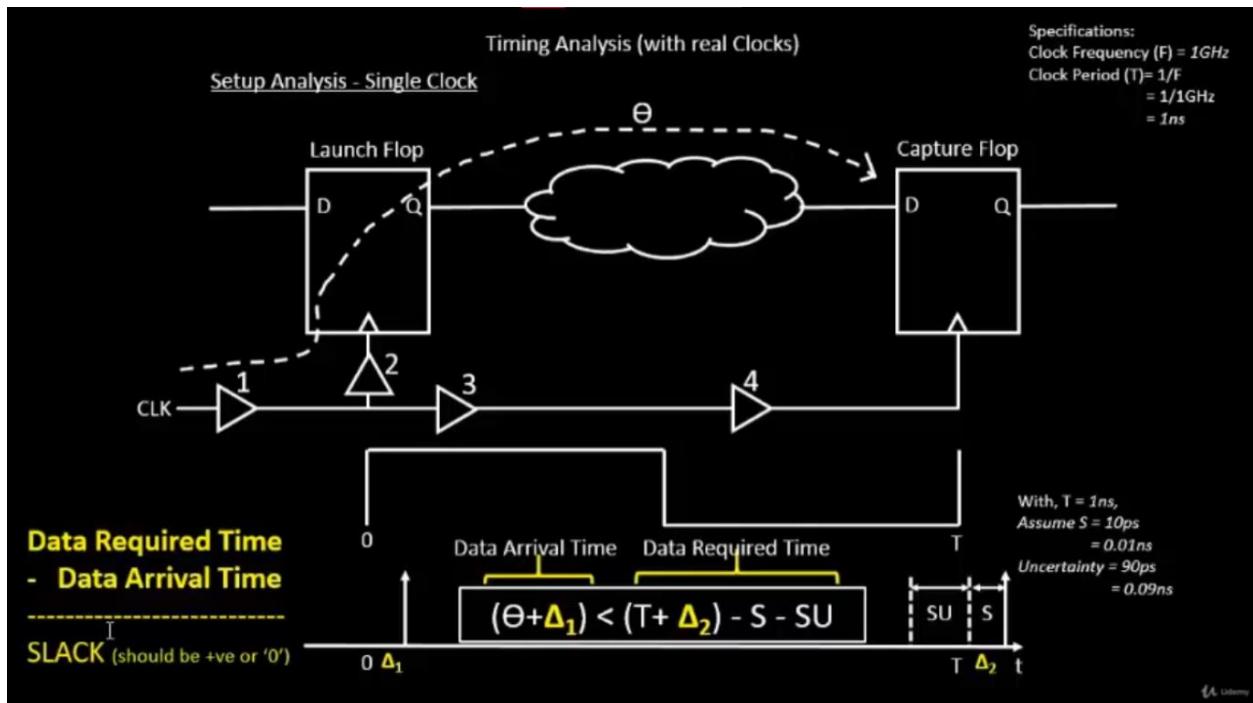
(Image credits:- VSDIAT)



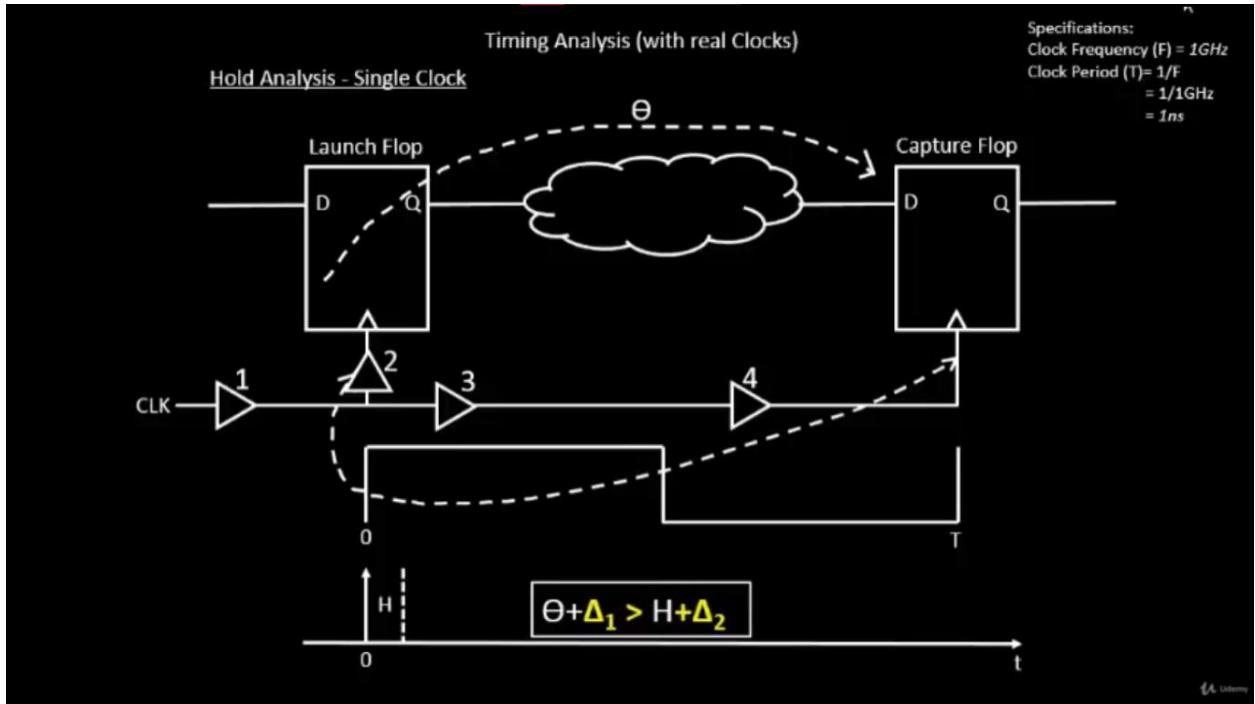
(Image credits:- VSDIAT)



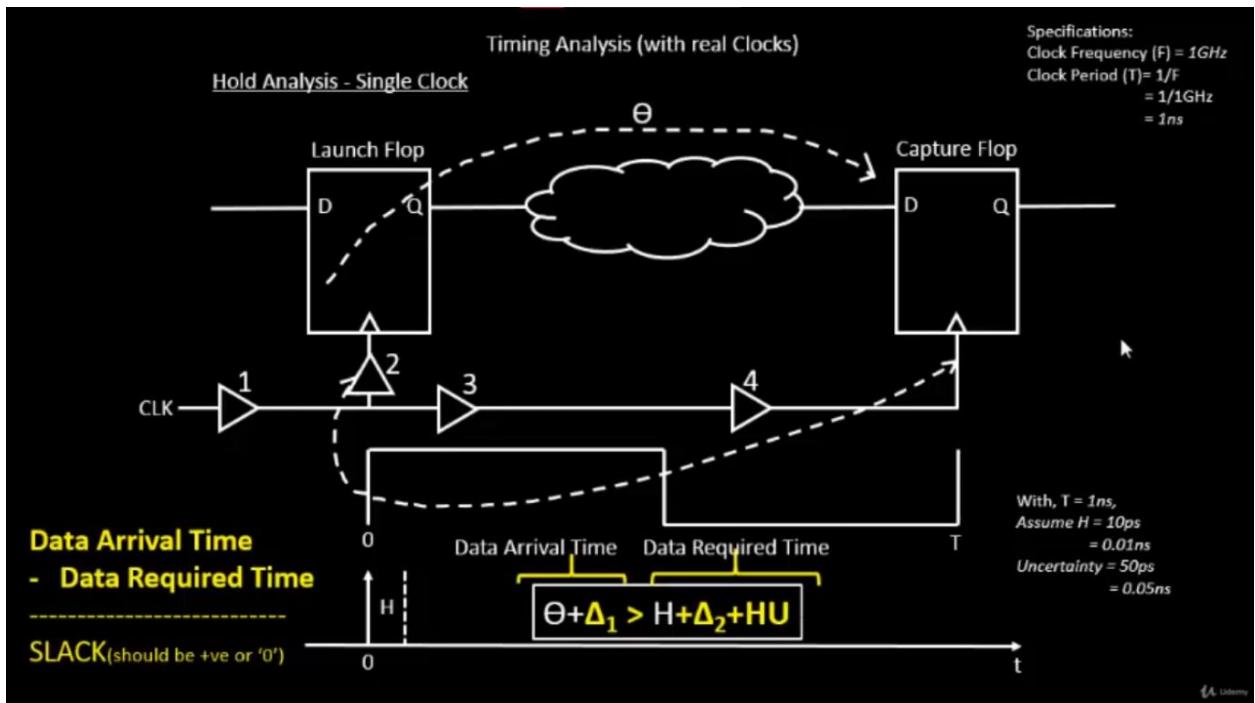
(Image credits:- VSDIAT)



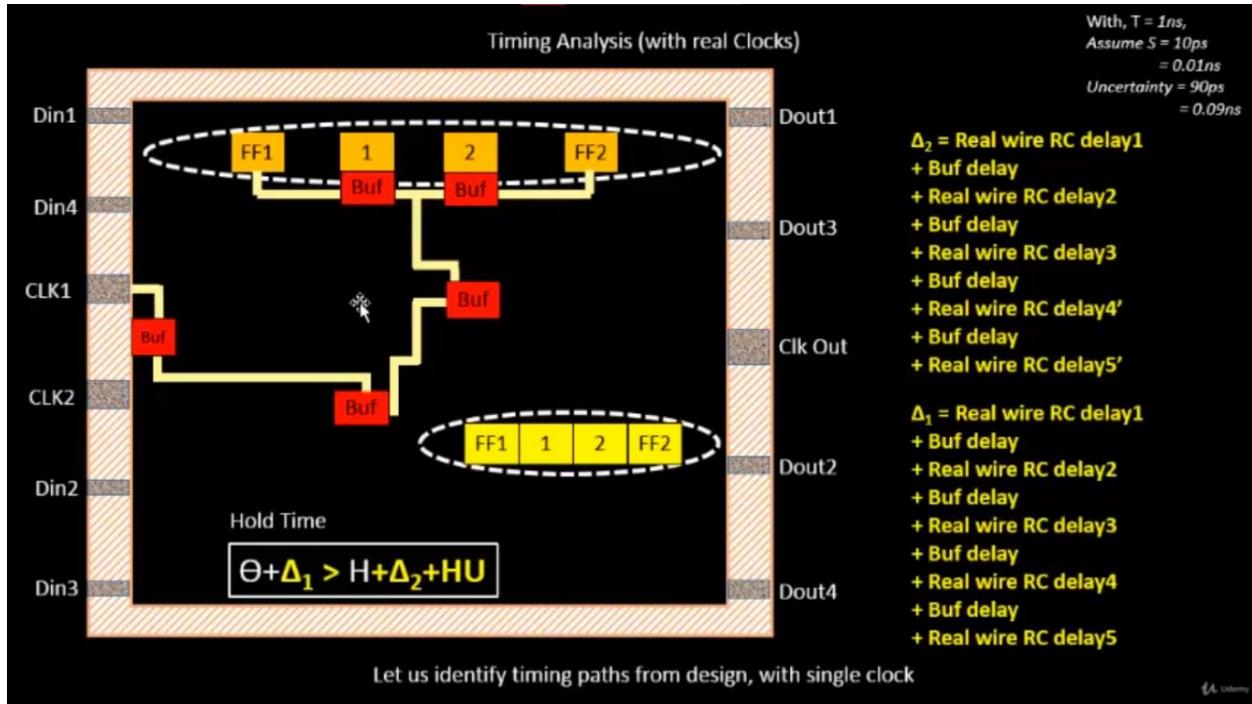
(Image credits:- VSDIAT)



(Image credits:- VSDIAT)



(Image credits:- VSDIAT)

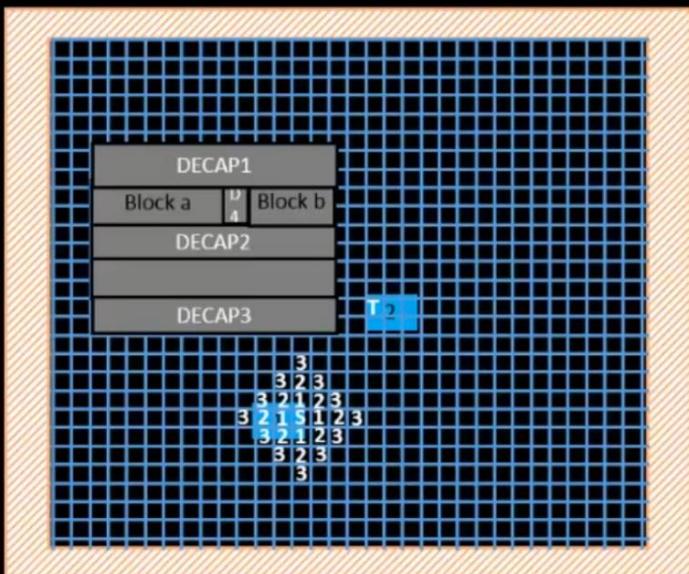


(Image credits:- VSDIAT)

Final steps for RTL2GDS using tritonRoute and openSTA

5) Route

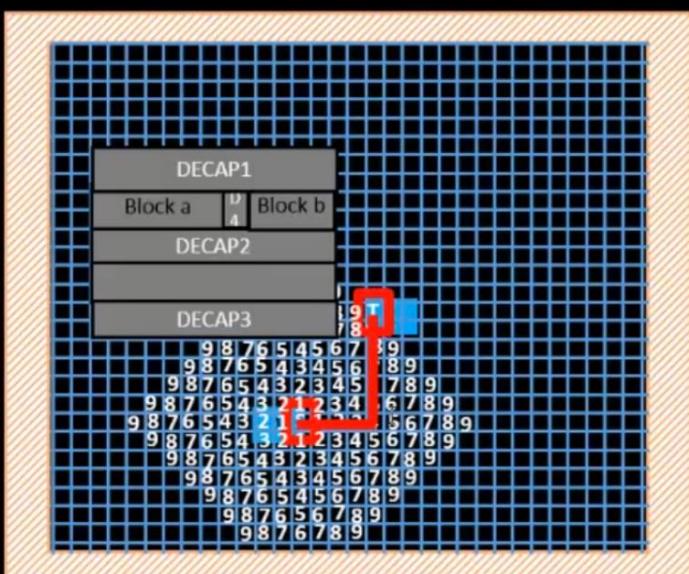
Maze Routing – Lee's Algorithm [Lee 1961]



(Image credits:- VSDIAT)

5) Route

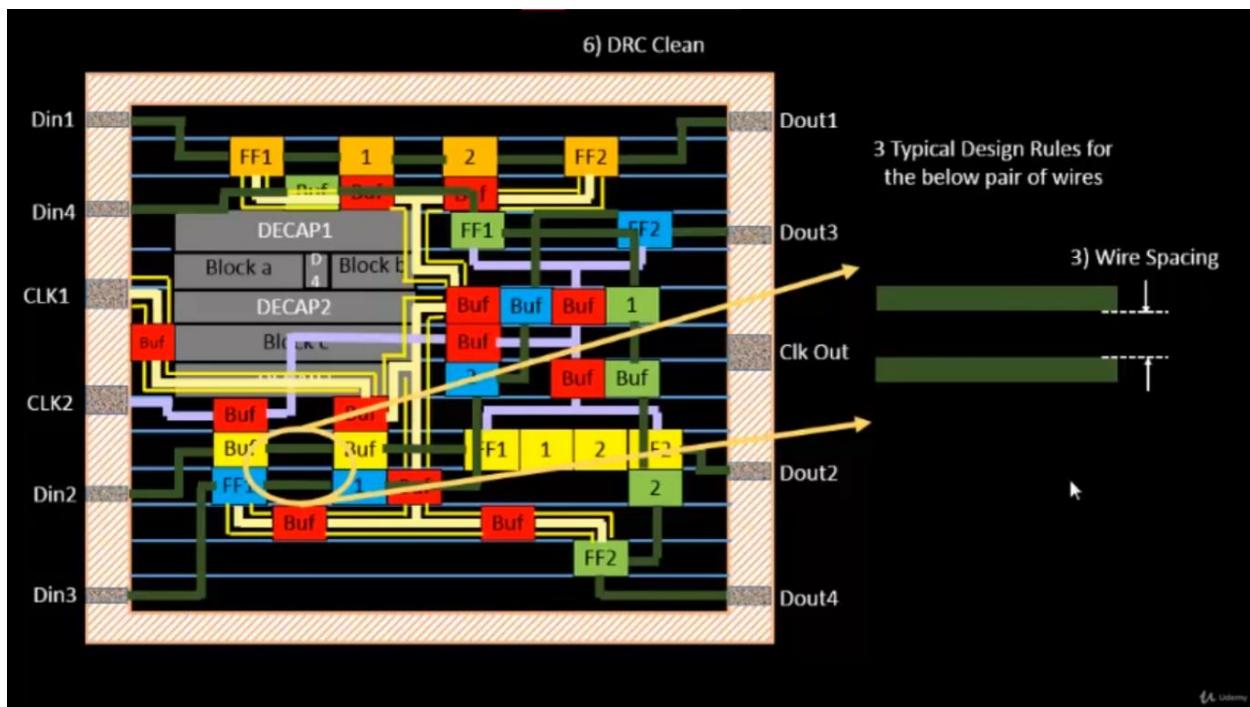
Maze Routing – Lee's Algorithm [Lee 1961]



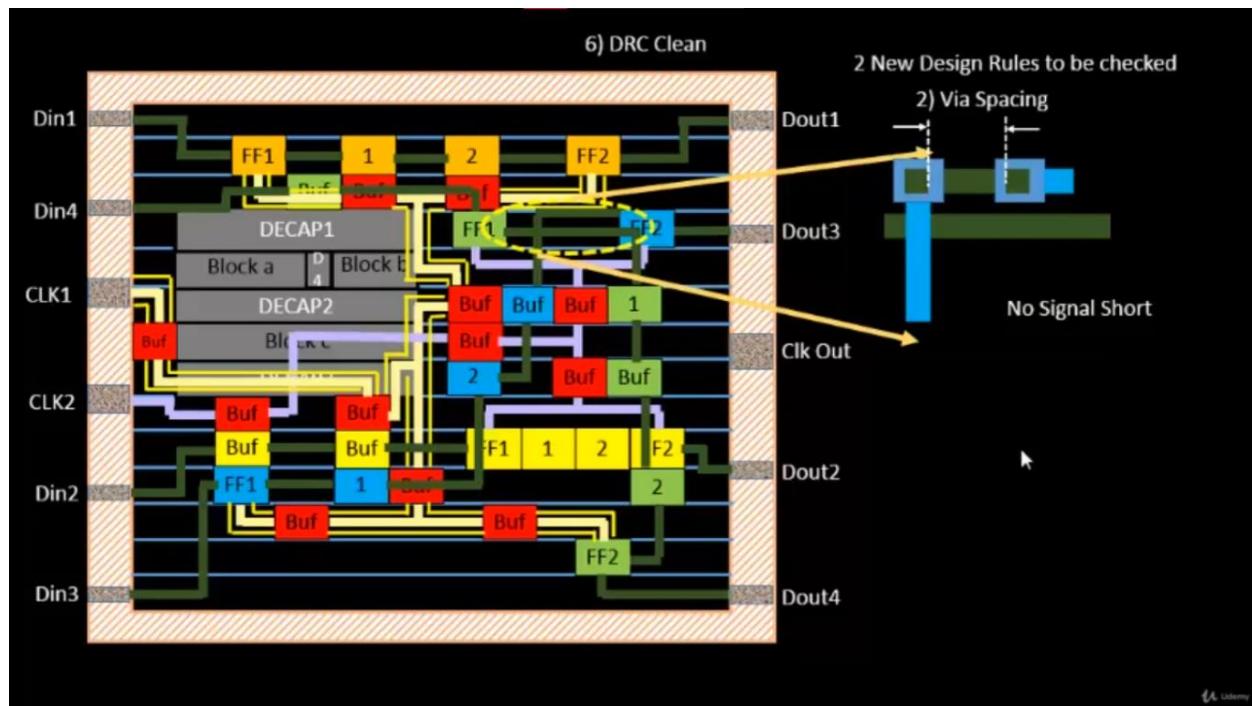
(Image credits:- VSDIAT)



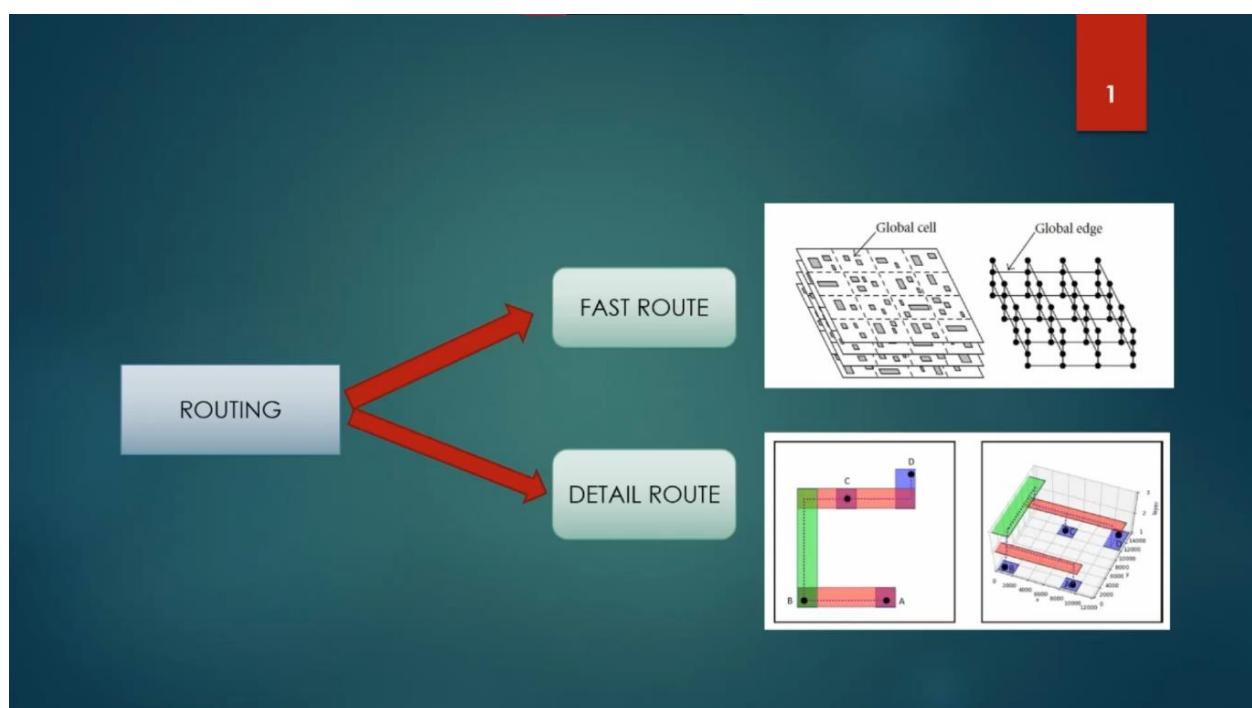
(Image credits:- VSDIAT)



(Image credits:- VSDIAT)



(Image credits:- VSDIAT)



(Image credits:- VSDIAT)

TritonRoute

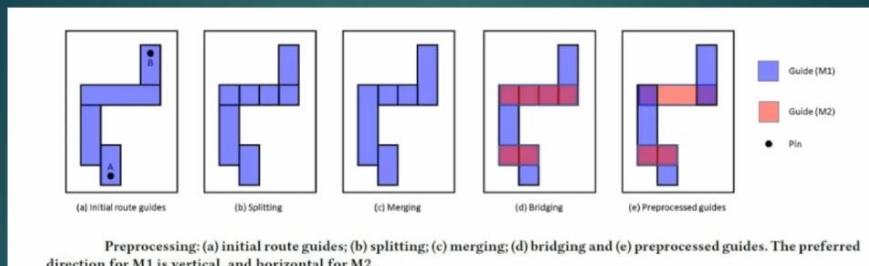
2

- ▶ Performs initial detail route.
- ▶ Honors the **preprocessed route guides** (obtained after fast route) ,i.e. , attempts as much as possible to route within route guides.
- ▶ Assumes route guides for each net satisfy **inter-guide connectivity**.
- ▶ Works on proposed MILP-based **panel routing** scheme with **intra-layer parallel** and **inter-layer sequential** routing framework.

(Image credits:- VSDIAT)

Preprocessed route guides

3



REQUIREMENTS OF PREPROCESSED GUIDES:

- Should have unit width.
- Should be in the preferred direction.

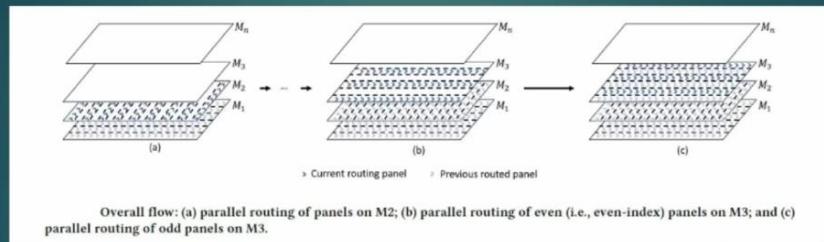
(Image credits:- VSDIAT)

Inter-guide connectivity

- ▶ Two guides are connected if:
 - ▶ they are on the same metal layer with touching edges, or
 - ▶ they are on neighboring metal layers with a nonzero vertically overlapped area.
- ▶ Each unconnected terminal (i.e., pin of a standard-cell instance) should have its pin shape overlapped by a route guide.

(Image credits:- VSDIAT)

Intra-layer parallel & Inter-layer sequential panel routing



(Image credits:- VSDIAT)

TritonRoute

6

► Problem Statement:

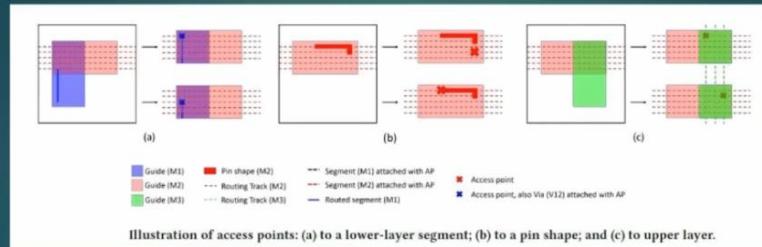
- **INPUTS:** LEF, DEF, Preprocessed route guides
- **OUTPUT:** Detailed routing solution with optimized wire-length and via count
- **CONSTRAINTS:** Route guide honoring, connectivity constraints and design rules

(Image credits:- VSDIAT)

TritonRoute

7

► Handling Connectivity



- **Access Point (AP):** An on-grid point on the metal layer of the route guide, and is used to connect to lower-layer segments, upper-layer segments, pins or IO ports.
- **Access Point Cluster (APC):** A union of all Ap's derived from same lower-layer segment, upper-layer guide, a pin or an IO port.

(Image credits:- VSDIAT)

Routing Topology Algorithm

Algorithm 1 Optimization of Routing Topology

```
1: for all  $i = 1$  to  $n - 1$  do
2:   for all  $j = i + 1$  to  $n$  do
3:      $cost_{i,j} \leftarrow dist(APC_i, APC_j)$ 
4:   end for
5: end for
6:  $T \leftarrow MST(APCs, COSTs)$ 
7: Return  $e_{i,j} \in T$ 
```

(Image credits:- VSDIAT)

