BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI (RAJ)

MEL G626 VLSI Architecture (Sem -2: AY 2024-25)

Lab-5

Objectives:

To develop a behavioral Verilog module named “cordic” for simulation (only simulation and not synthesis) of CORDIC algorithm for computing Sine and Cosine functions for a given angle (in radians) in the range: - Pi/2 to + Pi/2 for highest performance e.g. requiring minimum number of clock cycles.

Specifications:

You may use 16-bit signed representation of numerical values in 2.14 signed binary format (two bits to the left of binary point and 14 bits to the right of binary point).

Your module should have a 16-bit signed input port named “argument” through which the argument value in signed 2.14 binary format is supplied to the module and is kept applied throughout the computation until the Sine and Cosine values get computed and stored in 16-bit signed registers associated with signed output ports of the module named “sine_val” and “cos_val” respectively and another 1-bit output register associated with output port named “done” gets set.

Your module should also have an input port named “clock” for receiving a clock signal and an input port named “reset” which is synchronous high-active reset signal.

The use protocol for the module:

Apply and maintain the value of input argument at the input port named “argument” while the reset signal applied to the input port named “reset” is active (high) and a running clock signal is applied to the input port named “clock”. The output port named “done” should show low value and the output ports named “sine_val” and “cosine_val” should each show zero values.

Upon deactivation of reset signal (low value) CORDIC computation should start for the argument value that is being maintained at the signed input port “argument” and on completion of the computation the output port named “done” should show and maintain a high value and the signed output ports named sine_val and cosine_val should show and maintain the values of the computed Sine and Cosine functions respectively.

Design Verification:

Validate the functional correctness of your developed module “cordic” by writing a test bench where you instantiate the developed module “cordic” and successively compute Sine and Cosine values corresponding to each of the following angles: zero degree, thirty degree, forty five degree and sixty degree by generating and applying test inputs as per the use protocol of the module.

You should generate and apply a clock with a period of 100 time units.

You should also monitor/strobe/display the values of Sine and Cosine functions after every iteration step of CORDIC algorithm, so that successive improvements in the accuracy of Sine and Cosine values being computed can be seen for the applied argument value after each iteration step.