VLSI Architectures (Sem -2: AY 2024-25)

Lab-2

Objective:

To design, simulate, synthesize and characterize following types of adders by creating Verilog models (of indicated types) that use only logical operators (and not any arithmetic operators):

(1) 16-bit, 32-bit and 64-bit Unsigned Ripple Carry Adders that can also detect and signal arithmetic overflow caused by addition (behavioral Verilog module)

(2) 16-bit, 32-bit and 64-bit Signed Ripple Carry Adders that can also detect and signal arithmetic overflow caused by addition (behavioral Verilog module)

(3) A structural Verilog module for 32-bit Signed Redundant Carry Adder by defining and instantiating a behavioral module for 8-bit ripple carry adder, 8:1 multiplexor and 2:1 multiplexor. The adder should be able to detect and signal whenever the result of addition is zero

(4) Study the behavioral Verilog code for a 64-bit Hierarchical Carry Look-Ahead Adder being provided to you. Check out this code for its logical correctness and syntactical correctness. Make corrections in the code as necessary and document the same.

(5) Verify all the above designs through simulations. Synthesize all the above designs and tabulate your synthesis results: LUT count, delay and power