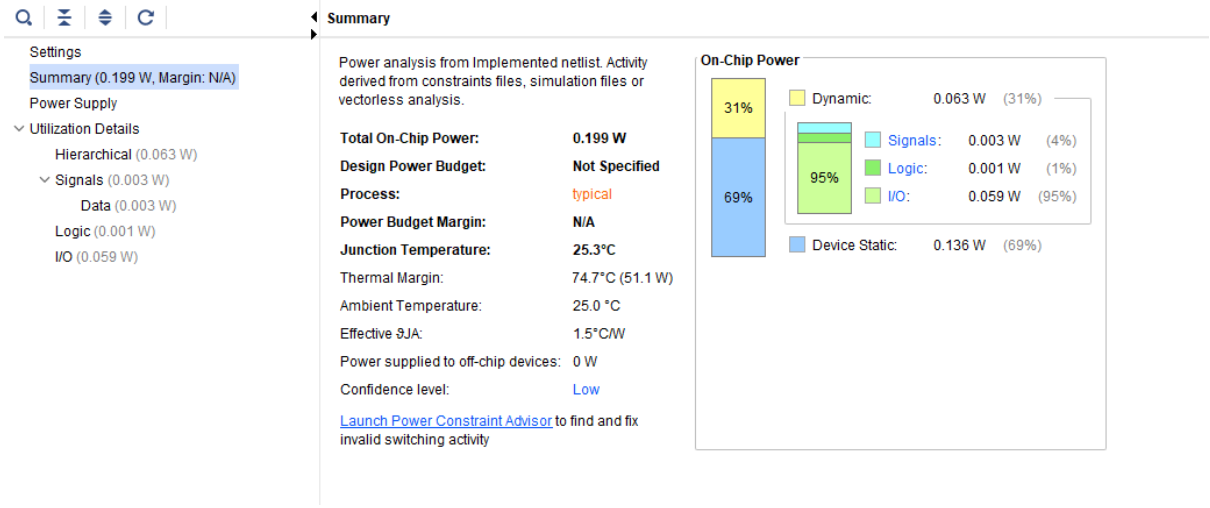
VLSI Arch – Lab 8

RISC V Execution Unit Synthesis

Note: xc7z020clg484-1 board has only 200 available I/O ports. But the EU needs 242 ports, so, xc7a200tffv1156-1 board is used since it has 500 I/O ports.

Synthesis and Implementation Summary: 403 LUTs

Power-



Maximum Delay Path:

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack:                   inf
  Source:                rs2i_d[1]
                           (input port)
  Destination:           res_d_op[0]
                           (output port)
  Path Group:            (none)
  Path Type:             Max at Slow Process Corner
  Data Path Delay:       28.469ns  (logic 7.481ns (26.279%)  route 20.988ns (73.721%))
  Logic Levels:          15  (CARRY4=9 IBUF=1 LUT2=1 LUT5=1 LUT6=2 OBUF=1)
```