BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI (RAJ)

MEL G626 VLSI Architecture (Sem -2: AY 2024-25)

Lab-3

Objective:

To understand, simulate, synthesize and characterize a behavioral model of the general purpose combinatorial shifter which can perform logical/arithmetic, left/right shift operation on a 32-bit operand by a specified number of bits in the range 0-31.

A behavioral Verilog module for the shifter is being provided to you.

(1) Check out this module for its logical correctness and syntactical correctness. Make corrections in the module as necessary and document the same.

(2) Then verify the design through simulation. Synthesize the design and tabulate your synthesis results: LUT count, delay and power