BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI (RAJ)

MEL G626 VLSI Architecture (Sem -2: AY 2024-25)

Lab-4

Ojectives:

1. Learning to design a Moore FSM from by transcribing its specification in natural language (English) into a Venn diagram
2. Learning to convert the Venn diagram into behavioral Verilog module
3. Learning to verify the Verilog design through simulation
4. Learning to synthesize the design for an FPGA and characterize the design for performance, gate complexity and power

Design a Moore FSM controller to control the appliances for room comfort as per specifications given below:

1. It turns on a heater when the room temperature drops below 15 degrees Celsius.
2. Once the room heater is turned on, it is turned off only when the room temperature exceeds 18 degrees Celsius. Once turned off, the heater is turned on again only when the temperature drops below 15 degrees Celsius.

3. If the room temperature exceeds 23 degrees Celsius, then the fan is switched on.
4. Once the fan is switched on, it is switched off only when the temperature drops below 22 degrees Celsius. Once switched off, it is switched on again only when the temperature exceeds 23 degrees Celsius

5. If the temperature exceeds 27 degrees Celsius then the Air Conditioner (AC) is turned on.
6. If the temperature drops below 23 degrees Celsius, then the AC is switched off. Once the AC is switched off, it is switched on again only when the temperature exceeds 27 degrees Celsius.

Assume that you have following six synchronized one-bit external inputs available to indicate different room temperature conditions:

Tgt18 : “1” value indicates that temperature is > 18C
Tlt15 : “1” value indicates that temperature is < 15C
Tgt23 : “1” value indicates that temperature is > 23C
Tlt22 : “1” value indicates that temperature is < 22C
Tgt27 : “1” value indicates that temperature is > 27C
Tlt23 : “1” value indicates that temperature is < 23C

(a) Draw Venn diagram for the controller

(b) Develop a Verilog behavioral module for the controller
(c) Verify your design through simulation
(d) Synthesize your design for a Xilinx FPGA (XC7Z020 CLG484-1) and characterize the synthesized design for performance, gate/LUT complexity and power consumption